74HC574
Octal D-Type Positive Edge-Triggered Flip-Flop with 3-State Outputs

GENERAL DESCRIPTION

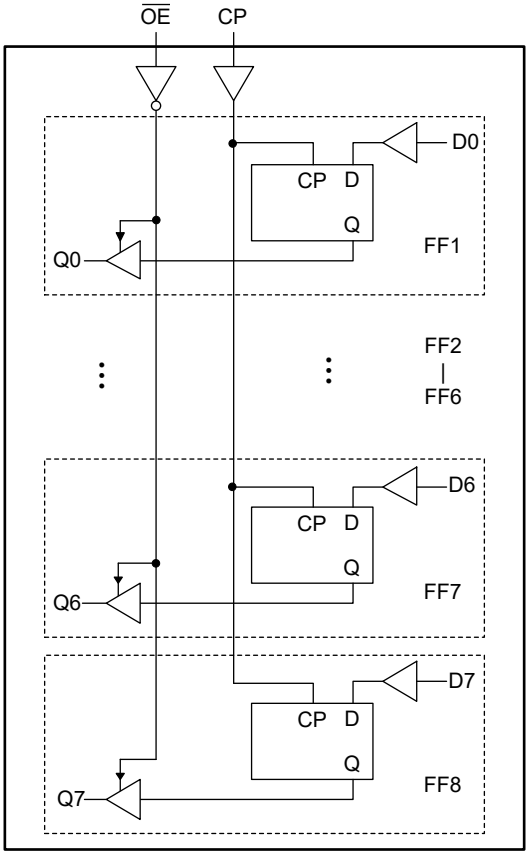
The 74HC574 is an octal D-Type positive edge-triggered flip-flop with 3-state outputs. The device can accept a wide supply voltage range from 2.0V to 5.5V.

$\overline{OE}$ is output enable input and CP is clock input. When $\overline{OE}$ sets high, the outputs are in a high-impedance state. $\overline{OE}$ does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

FEATURES

- **Wide Supply Voltage Range: 2.0V to 5.5V**
- **+7.8mA/-7.8mA Output Current**
- **8-Bit Positive Edge-Triggered Register**
- **3-State Non-Inverting Outputs Suitable for Bus-Oriented Applications**
- **CMOS Low Power Consumption**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-20 and SOIC-20 Packages**

LOGIC DIAGRAM



FUNCTION TABLE

INPUT			INTERNAL FLIP-FLOP	OUTPUT
$\overline{OE}$	CP	Dn		Qn
L	↑	l	L	L
L	↑	h	H	H
H	↑	l	L	Z
H	↑	h	H	Z

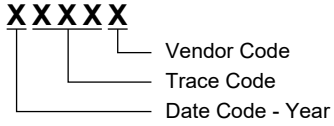
H = High voltage level.
h = High voltage level one set-up time before clock rising edge ↑.
L = Low voltage level.
l = Low voltage level one set-up time before clock rising edge ↑.
Z = High-impedance state.
↑ = Low-to-high clock transition.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74HC574	TSSOP-20	-40℃ to +125℃	74HC574XTS20G/TR	06GXTS20 XXXXX	Tape and Reel, 4000
	SOIC-20	-40℃ to +125℃	74HC574XS20G/TR	74HC574XS20 XXXXX	Tape and Reel, 1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 7.0V
Input Voltage Range, V_I (2) ... -0.5V to MIN (7.0V, V_{CC} + 0.5V)
Output Voltage Range, V_O (2) -0.5V to MIN (7.0V, V_{CC} + 0.5V)
Input Clamping Current, I_{IK} (V_I < 0V or V_I > V_{CC}) ..... ±20mA
Output Clamping Current, I_{OK} (V_O < 0V or V_O > V_{CC}) .. ±20mA
Output Current, I_O (V_O = 0V to V_{CC}) ..... ±35mA
Continuous Current (V_{CC} or GND) ..... ±70mA
Junction Temperature (3) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} ..... 2.0V to 5.5V
Input Voltage, V_I ..... 0V to V_{CC}
Output Voltage, V_O ..... 0V to V_{CC}
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 2.0V ..... 1000ns/V (MAX)
V_{CC} = 4.5V ..... 500ns/V (MAX)
V_{CC} = 5.5V ..... 400ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

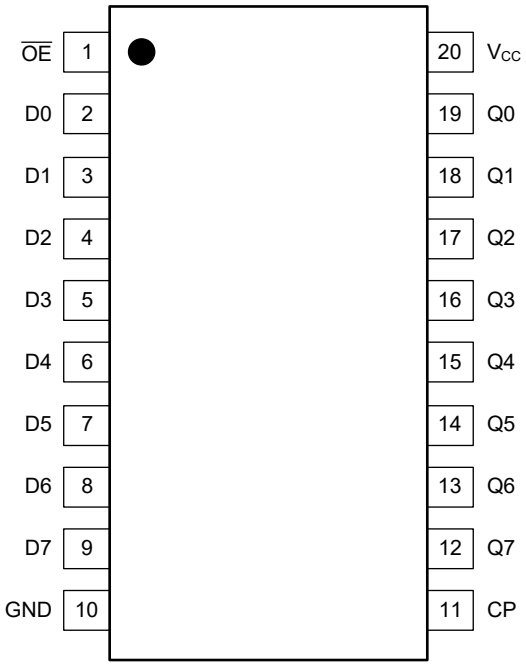
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

TOP VIEW



TSSOP-20/SOIC-20

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{OE}$	Output Enable Input (Active Low).
2, 3, 4, 5, 6, 7, 8, 9	D0, D1, D2, D3, D4, D5, D6, D7	Data Inputs.
10	GND	Ground.
11	CP	Clock Input (Low-to-High Clock Transition, Edge-Triggered).
12, 13, 14, 15, 16, 17, 18, 19	Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Outputs.
20	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V		Full	1.50			V
		V_{CC} = 4.5V		Full	3.15			
		V_{CC} = 5.5V		Full	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V		Full			0.50	V
		V_{CC} = 4.5V		Full			1.35	
		V_{CC} = 5.5V		Full			1.65	
High-Level Output Voltage	V_{OH}	$V_I = V_{IH}$	V_{CC} = 2.0V, I_O = -20μA	Full	1.95	1.995		V
			V_{CC} = 4.5V, I_O = -20μA	Full	4.45	4.495		
			V_{CC} = 5.5V, I_O = -20μA	Full	5.45	5.495		
			V_{CC} = 4.5V, I_O = -6.0mA	Full	4.00	4.290		
			V_{CC} = 5.5V, I_O = -7.8mA	Full	4.95	5.260		
Low-Level Output Voltage	V_{OL}	$V_I = V_{IL}$	V_{CC} = 2.0V, I_O = 20μA	Full		0.005	0.05	V
			V_{CC} = 4.5V, I_O = 20μA	Full		0.005	0.05	
			V_{CC} = 5.5V, I_O = 20μA	Full		0.005	0.05	
			V_{CC} = 4.5V, I_O = 6.0mA	Full		0.170	0.40	
			V_{CC} = 5.5V, I_O = 7.8mA	Full		0.210	0.40	
Input Leakage Current	I_I	V_{CC} = 5.5V, V_I = V_{CC} or GND		Full		±0.1	±1	μA
Off-State Output Current	I_{OZ}	V_{CC} = 5.5V, V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND		Full		±0.1	±2	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A		Full		0.1	10	μA
Input Capacitance	C_I			+25℃		4		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, C_L = 50pF, all typical values are measured at and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	CP to Qn	V_{CC} = 2.0V	Full		39	100	ns
			V_{CC} = 4.5V	Full		13	35	
			V_{CC} = 5.5V	Full		11	30	
Enable Time (2)	t_{EN}	$\overline{OE}$ to Qn	V_{CC} = 2.0V	Full		38	100	ns
			V_{CC} = 4.5V	Full		13	35	
			V_{CC} = 5.5V	Full		11	28	
Disable Time (2)	t_{DIS}	$\overline{OE}$ to Qn	V_{CC} = 2.0V	Full		16	40	ns
			V_{CC} = 4.5V	Full		12	20	
			V_{CC} = 5.5V	Full		12	20	
Transition Time (2)	t_T	Qn	V_{CC} = 2.0V	Full		27	80	ns
			V_{CC} = 4.5V	Full		9	20	
			V_{CC} = 5.5V	Full		7	18	
Pulse Width	t_W	CP high or low	V_{CC} = 2.0V	Full	80			ns
			V_{CC} = 4.5V	Full	24			
			V_{CC} = 5.5V	Full	20			
Set-Up Time	t_{SU}	Dn to CP	V_{CC} = 2.0V	Full	50			ns
			V_{CC} = 4.5V	Full	18			
			V_{CC} = 5.5V	Full	18			
Hold Time	t_H	Dn to CP	V_{CC} = 2.0V	Full	5			ns
			V_{CC} = 4.5V	Full	5			
			V_{CC} = 5.5V	Full	5			
Maximum Frequency	f_{MAX}	CP	V_{CC} = 2.0V	Full	4			MHz
			V_{CC} = 4.5V	Full	20			
			V_{CC} = 5.5V	Full	24			
Power Dissipation Capacitance (3)	C_{PD}	C_L = 50pF, f = 1MHz, V_I = GND to V_{CC}		+25℃		7		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}. t_{EN} is the same as t_{PZL} and t_{PZH}. t_T is the same as t_{THL} and t_{TLH}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

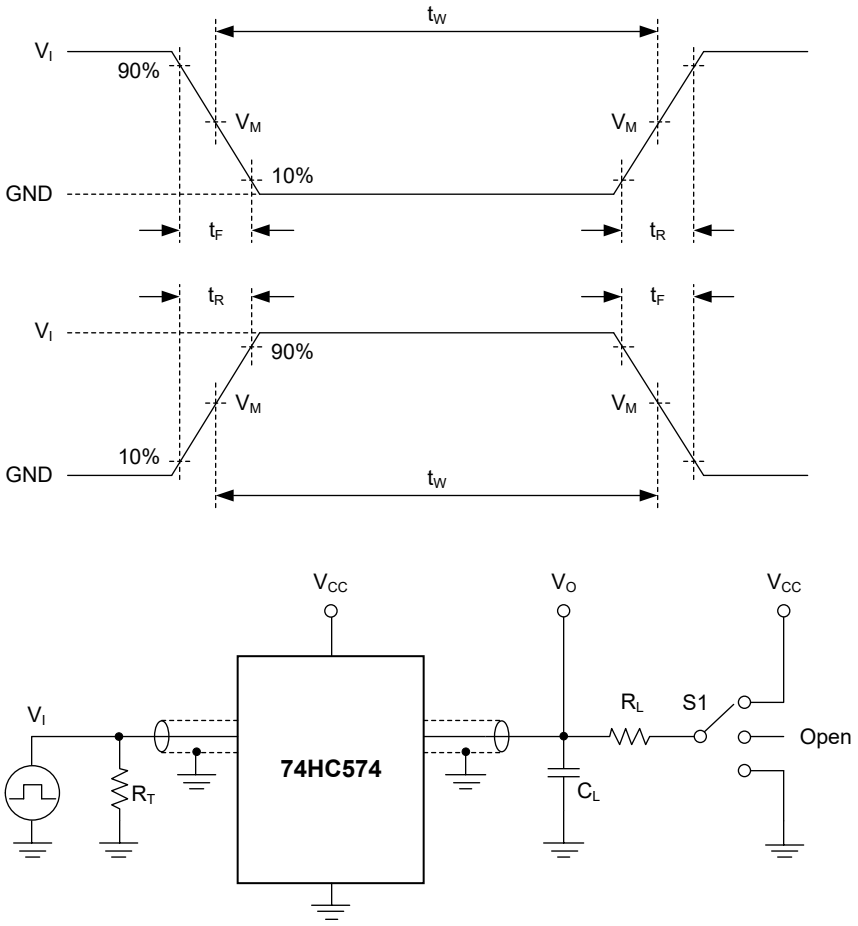
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

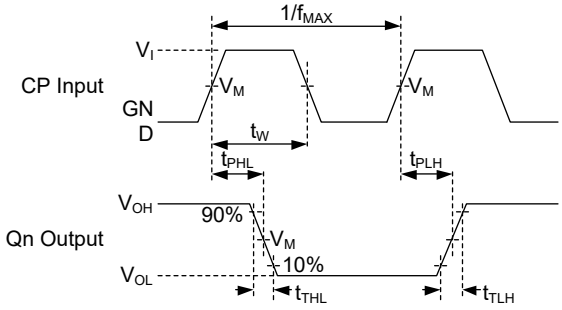
S1: Test selection switch.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		S1 POSITION		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.0V to 5.5V	V_{CC}	≤ 6.0ns	50pF	1kΩ	Open	V_{CC}	GND

WAVEFORMS

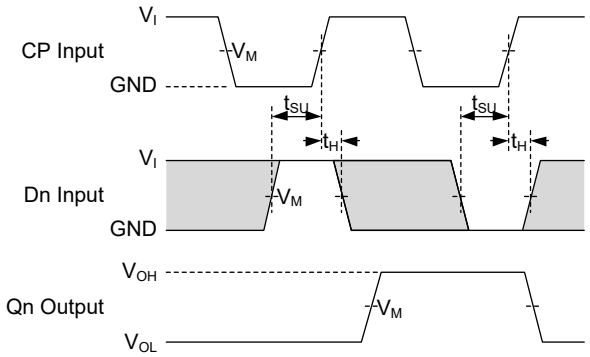


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Clock Input to Output Propagation Delays, Pulse Width, Transition Times and Maximum Clock Frequency



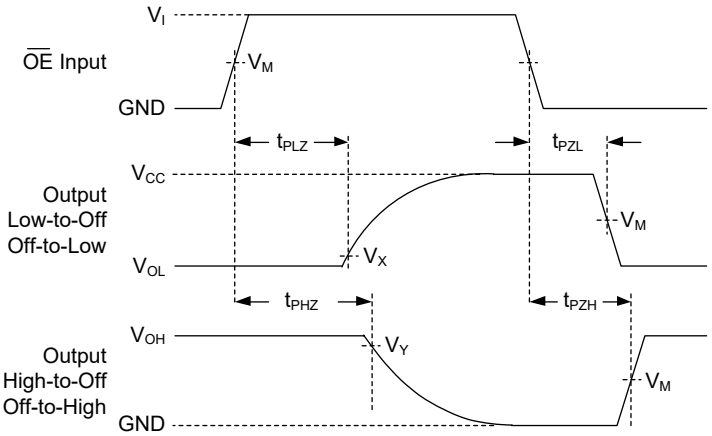
Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 3. Data Set-Up Times for the Dn Input to the CP Input and Hold Times for the CP Input to the Dn Input



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and Disable Times

WAVEFORMS (continued)

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M (1)	V_M	V_X	V_Y
2.0V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}	0.9 × V_{CC}

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 6.0ns.

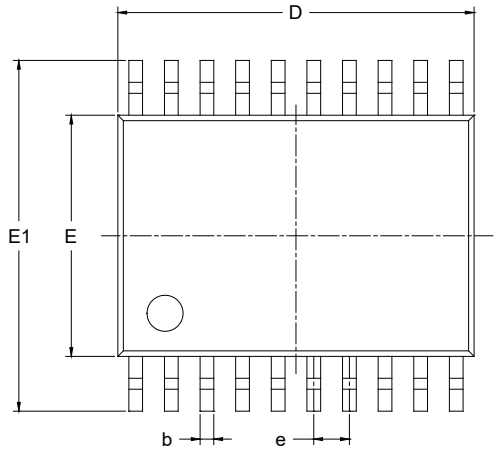
REVISION HISTORY

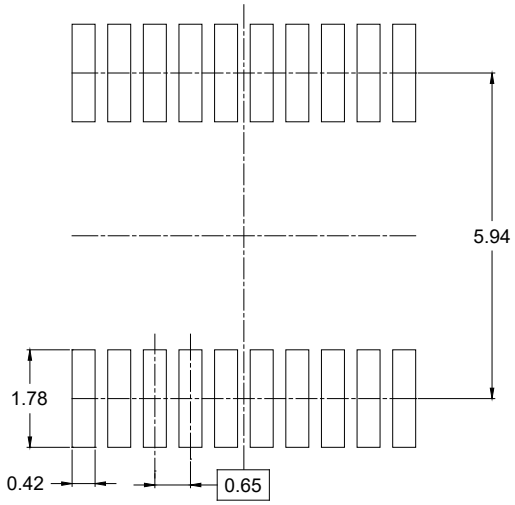
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (JUNE 2023) to REV.A	Page
Changed from product preview to production data	All

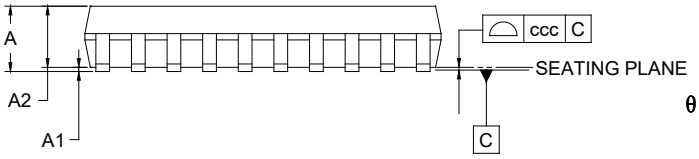
PACKAGE OUTLINE DIMENSIONS

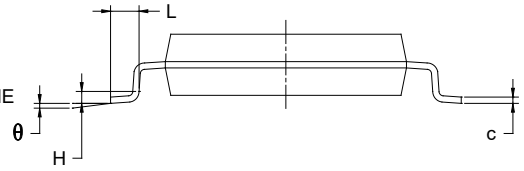
TSSOP-20





RECOMMENDED LAND PATTERN (Unit: mm)



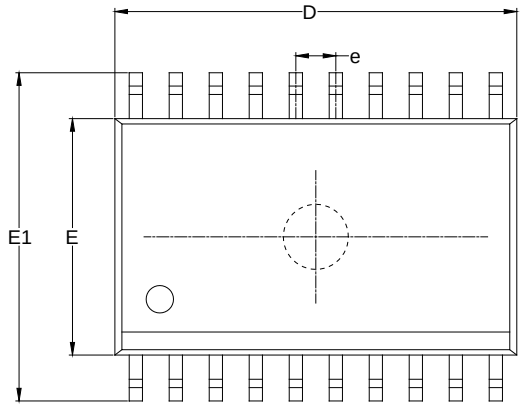


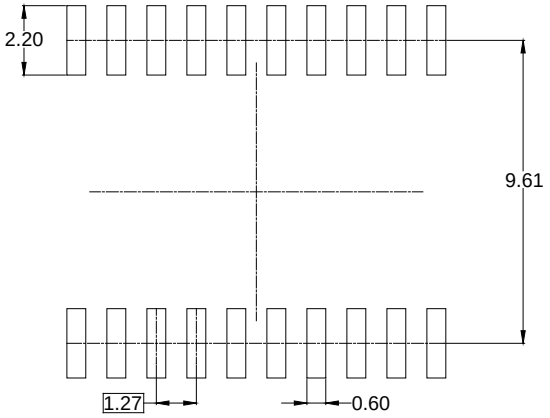
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

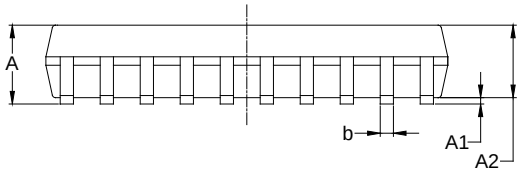
PACKAGE OUTLINE DIMENSIONS

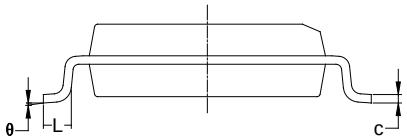
SOIC-20





RECOMMENDED LAND PATTERN (Unit: mm)



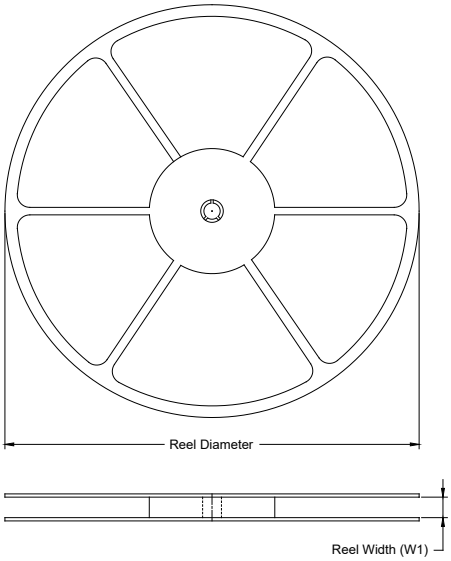


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

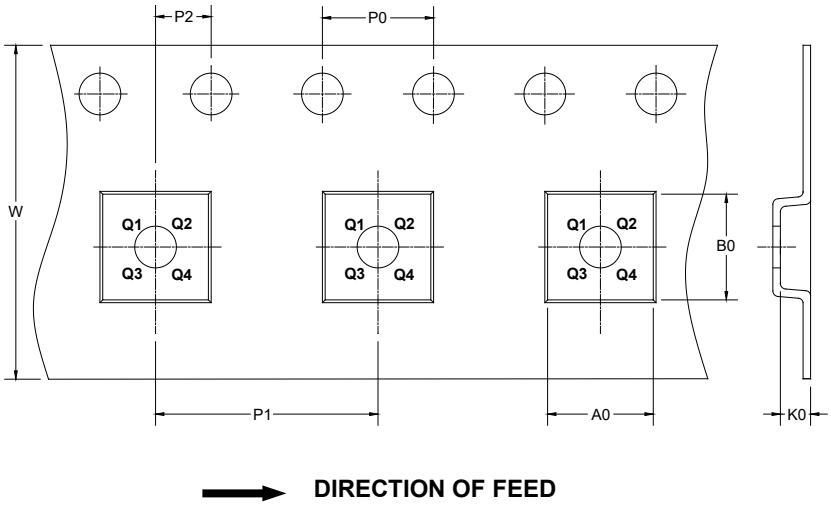
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

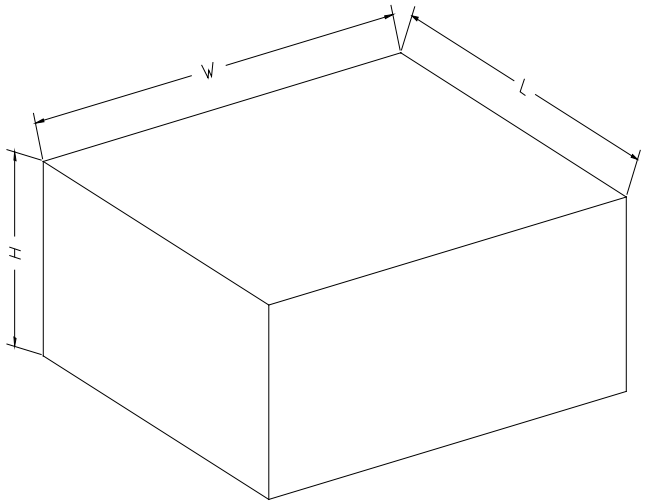
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-20	13"	16.4	6.80	6.90	1.50	4.0	8.0	2.0	16.0	Q1
SOIC-20	13"	24.4	10.90	13.30	3.00	4.0	12.0	2.0	24.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002