



SGM6502A

8-Input, 6-Output Video Switch Matrix with Output Drivers, Input Clamp, and Bias Circuitry

GENERAL DESCRIPTION

The SGM6502A is a video switch matrix which features 8 input channels and 6 output channels. The architecture allows any of the 8 inputs to be routed to any of the 6 outputs, and it supports one input to one output or one input to more outputs switching. The routing map is configured by I²C-compatible serial interface.

The SGM6502A has the input clamp function and bias circuitry, the input clamp or bias mode is selectable through I²C interface. Integrated clamp is supported by each input. The function is to set video output sync level to approximately 600mV. If sync signal (Chroma, Pb, Pr) is absent, the input is biased by approximately 1.3V, which is the center of input voltage range.

The SGM6502A is available in a Green TSSOP-24 package. It operates over an ambient temperature range of -40°C to +85°C.

FEATURES

- **Single-Supply Voltage Range: 3.1V to 5.5V**
- **8 × 6 Crosspoint Switch Matrix**
- **Supports Standard Definition (SD), Progressive Scan (PS), and High Definition (HD) Video**
- **-3dB Bandwidth: 92MHz**
- **Low Crosstalk: -87dB at 1MHz**
- **Programmable Gain Options:
0dB or 6dB**
- **Input Bias Circuitry and Input Clamp Function**
- **Supports I²C Serial Interface**
- **Double-Load 75Ω Output Drivers**
- **AC- or DC-Coupled Inputs and Outputs**
- **Available in a Green TSSOP-24 Package**

APPLICATIONS

Security and Surveillance
TV and HDTV
Automotive Navigation System and Back-Up Camera
Media Centers
Video Routing
Cable and Satellite Set-Top Boxes

8-Input, 6-Output Video Switch Matrix with Output Drivers, Input Clamp, and Bias Circuitry

SGM6502A

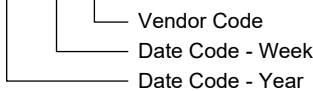
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6502A	TSSOP-24	-40°C to +85°C	SGM6502AYTS24G/TR	SGM6502A YTS24 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXXX = Date Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage Range (DC)..... -0.3V to 6V
- Analog and Digital Input/Output Voltage Range
.....-0.3V to $V_{CC} + 0.3V$
- Output Current per Channel..... 40mA (MAX)
- Junction Temperature..... +150°C
- Storage Temperature Range-65°C to +150°C
- Lead Temperature (Soldering, 10s).....+260°C
- ESD Susceptibility
- HBM..... 6000V
- CDM 2000V
- MM..... 400V

RECOMMENDED OPERATING CONDITIONS

- Operating Temperature Range-40°C to +85°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

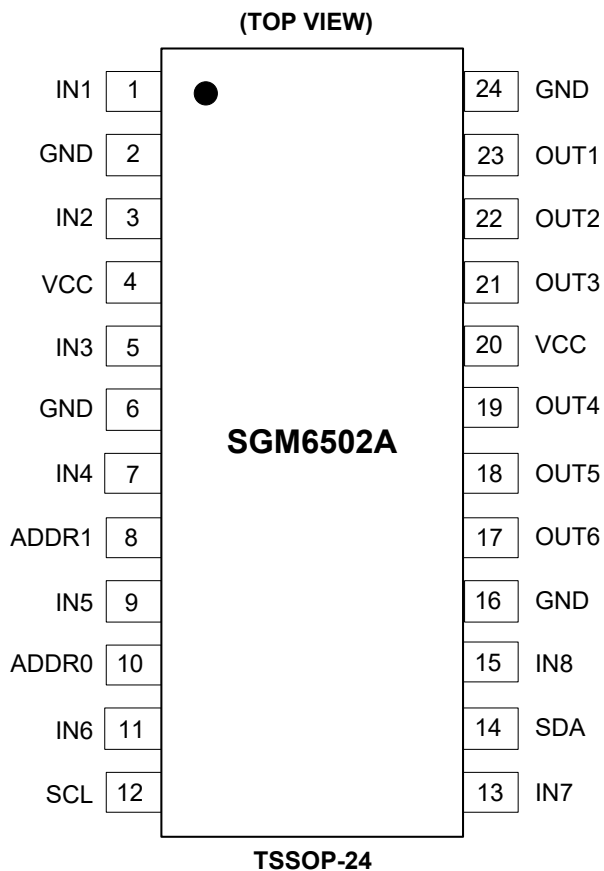
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN1	Input Pin (Channel 1).
2	GND	Ground.
3	IN2	Input Pin (Channel 2).
4	VCC	Positive Power Supply.
5	IN3	Input Pin (Channel 3).
6	GND	Ground.
7	IN4	Input Pin (Channel 4).
8	ADDR1	I ² C Address Selection Pin.
9	IN5	Input Pin (Channel 5).
10	ADDR0	I ² C Address Selection Pin.
11	IN6	Input Pin (Channel 6).
12	SCL	I ² C Clock Signal.
13	IN7	Input Pin (Channel 7).
14	SDA	I ² C Data Signal.
15	IN8	Input Pin (Channel 8).
16	GND	Ground.
17	OUT6	Output Pin (Channel 6).
18	OUT5	Output Pin (Channel 5).
19	OUT4	Output Pin (Channel 4).
20	VCC	Positive Power Supply.
21	OUT3	Output Pin (Channel 3).
22	OUT2	Output Pin (Channel 2).
23	OUT1	Output Pin (Channel 1).
24	GND	Ground.

8-Input, 6-Output Video Switch Matrix with SGM6502A Output Drivers, Input Clamp, and Bias Circuitry

ELECTRICAL CHARACTERISTICS

($T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $V_{IN} = 1V_{PP}$, input bias mode, one-to-one routing, 6dB gain, all inputs AC-coupled with $0.1\mu\text{F}$, unused inputs AC-terminated through 75Ω to GND, all outputs AC-coupled with $220\mu\text{F}$ into 150Ω , referenced to 400kHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
General						
Supply Voltage Range			3.1	5	5.5	V
DC Performance						
Video Output Range	V_{OUT}			2.8		V_{PP}
Supply Current	I_Q	No Load, All Outputs Enabled		63	80	mA
DC Input Level	V_{clamp}	Clamp Mode, All Gain Settings		0.45		V
DC Output Level		Clamp Mode, 0dB Gain Setting		0.45		V
DC Output Level		Clamp Mode, 6dB Gain Setting		0.9		V
DC Input Level	V_{bias}	Bias Mode, All Gain Settings		0.65		V
DC Output Level		Bias Mode, 0dB Gain Setting		0.65		V
DC Output Level		Bias Mode, 6dB Gain Setting		1.3		V
Power Supply Rejection Ratio	PSRR	All Channels, DC Input = 0.5V		75		dB
AC Performance						
Channel Gain	AV_{0dB}	DC, All Channels, 0dB Gain Setting	-0.3	0	0.3	dB
Channel Gain	AV_{6dB}	DC, All Channels, 6dB Gain Setting	5.7	6	6.3	dB
-1dB Bandwidth	f_{-1dB}	$V_{OUT} = 1.4V_{PP}$		70		MHz
-3dB Bandwidth	f_C	$V_{OUT} = 1.4V_{PP}$		92		MHz
Differential Gain	DG	$V_{CC} = 5.0\text{V}$, 4.43MHz		0.1		%
Differential Phase	DP	$V_{CC} = 5.0\text{V}$, 4.43MHz		0.4		°
SD Output Distortion	THD_{SD}	$V_{OUT} = 1.4V_{PP}$, 5MHz, $V_{CC} = 5.0\text{V}$		0.2		%
HD Output Distortion	THD_{HD}	$V_{OUT} = 1.4V_{PP}$, 22MHz, $V_{CC} = 5.0\text{V}$		0.6		%
Input Crosstalk	X_{TALK1}	1MHz, $V_{OUT} = 2V_{PP}$		-87		dB
Input Crosstalk	X_{TALK2}	15MHz, $V_{OUT} = 2V_{PP}$		-65		dB
Output Crosstalk	X_{TALK3}	1MHz, $V_{OUT} = 2V_{PP}$		-75		dB
Output Crosstalk	X_{TALK4}	15MHz, $V_{OUT} = 2V_{PP}$		-53		dB
Multi-Channel Crosstalk	X_{TALK5}	4.43MHz, $V_{OUT} = 2V_{PP}$		-60		dB
Multi-Channel Crosstalk	X_{TALK6}	6.5MHz, $V_{OUT} = 2V_{PP}$		-56		dB
Multi-Channel Crosstalk	X_{TALK7}	9MHz, $V_{OUT} = 2V_{PP}$		-54		dB
Signal-to-Noise Ratio	SNR_{SD}	NTC-7 Weighting, 4.2MHz LP, 100kHz HP		78		dB
Channel Noise	V_{NOISE}	400kHz to 100MHz, Input Referred		20		$\text{nV}/\sqrt{\text{Hz}}$
Amplifier Recovery Time	AMP_{ON}	Post I ² C Programming		200		ns

I²C BUS CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Low	V _{IL}	SDA, SCL, ADDR	0		1.5	V
Digital Input High	V _{IH}	SDA, SCL, ADDR	3		V _{CC}	V
Clock Frequency	f _{SCL}	SCL		100		kHz
Input Rise Time	t _r	1.5V to 3V		1000		ns
Input Fall Time	t _f	1.5V to 3V		300		ns
Clock Low Period	t _{LOW}			4.7		μs
Clock High Period	t _{HIGH}			4.0		μs
Data Set-up Time	t _{SU, DAT}			300		ns
Data Hold Time	t _{HD, DAT}			0		ns
Set-up Time from Clock High to Stop	t _{SU, STO}			4.0		μs
Start Set-up Time Following a Stop	t _{BUF}			4.7		μs
Start Hold Time	t _{HD, STA}			4.0		μs
Start Set-up Time Following Clock Low to High	t _{SU, STA}			4.7		μs

REGISTER MAPS

I²C Slave Address of SGM6502A: 0x06 (0000 0110)

The I²C address is 0x06 (0000 0110). The offset addresses are controlled by the values of the ADDR0 and ADDR1 inputs.

W: Write only bit(s)

PORV: Power-On Reset Value

Table 1. Offset Addresses

ADDR1	ADDR0	Binary	Hex
0	0	0000 0110	0x06
0	1	0100 0110	0x46
1	0	1000 0110	0x86
1	1	1100 0110	0xC6

Output Control Register

Table 2. Output Control Register Maps

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	OUT1, OUT2	B3-Out2	B2-Out2	B1-Out2	B0-Out2	B3-Out1	B2-Out1	B1-Out1	B0-Out1
0x01	OUT3, OUT4	B3-Out4	B2-Out4	B1-Out4	B0-Out4	B3-Out3	B2-Out3	B1-Out3	B0-Out3
0x02	OUT5, OUT6	B3-Out6	B2-Out6	B1-Out6	B0-Out6	B3-Out5	B2-Out5	B1-Out5	B0-Out5

Table 3. OUT1, OUT2 Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7:4]	B3-Out2	Input Selected to Drive this Output 0000 = Off ⁽¹⁾ 0001 = IN1 0010 = IN2 1000 = IN8		0000	W
	B2-Out2				
	B1-Out2				
	B0-Out2				
D[3:0]	B3-Out1	Input Selected to Drive this Output 0000 = Off ⁽¹⁾ 0001 = IN1 0010 = IN2 1000 = IN8		0000	W
	B2-Out1				
	B1-Out1				
	B0-Out1				

NOTE:

1. When the off input selection is used, the output amplifier is powered down and enters a high-impedance state.

Table 4. OUT3, OUT4 Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7:4]	B3-Out4	Input Selected to Drive this Output 0000 = Off ⁽¹⁾ 0001 = IN1 0010 = IN2 1000 = IN8		0000	W
	B2-Out4				
	B1-Out4				
	B0-Out4				
D[3:0]	B3-Out3	Input Selected to Drive this Output 0000 = Off ⁽¹⁾ 0001 = IN1 0010 = IN2 1000 = IN8		0000	W
	B2-Out3				
	B1-Out3				
	B0-Out3				

NOTE:

1. When the off input selection is used, the output amplifier is powered down and enters a high-impedance state.

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REGISTER MAPS (continued)

Table 5. OUT5, OUT6 Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7:4]	B3-Out6	Input Selected to Drive this Output 0000 = Off ⁽¹⁾ 0001 = IN1 0010 = IN2 1000 = IN8		0000	W
	B2-Out6				
	B1-Out6				
	B0-Out6				
D[3:0]	B3-Out5	Input Selected to Drive this Output 0000 = Off ⁽¹⁾ 0001 = IN1 0010 = IN2 1000 = IN8		0000	W
	B2-Out5				
	B1-Out5				
	B0-Out5				

NOTE:

1. When the off input selection is used, the output amplifier is powered down and enters a high-impedance state.

Clamp Control Register

Table 6. Clamp Control Register Map

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x03	CLAMP	Clmp8	Clmp7	Clmp6	Clmp5	Clmp4	Clmp3	Clmp2	Clmp1

Table 7. CLAMP Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7:0]	Clmp8	Clamp/Bias Selection (for Input 1 to Input 8) 0 = Bias 1 = Clamp		0	W
	Clmp7			0	W
	Clmp6			0	W
	Clmp5			0	W
	Clmp4			0	W
	Clmp3			0	W
	Clmp2			0	W
	Clmp1			0	W

REGISTER MAPS (continued)

Gain Control Register

Table 8. Gain Control Register Map

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x04	GAIN	Reserved	Reserved	Gain6	Gain5	Gain4	Gain3	Gain2	Gain1

Table 9. GAIN Control Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE
D[7:6]	Reserved	Reserved.			
D[5:0]	Gain6	Output Gain Selection (for Output 1 to Output 6) 0 = 6dB 1 = 0dB		0	W
	Gain5			0	W
	Gain4			0	W
	Gain3			0	W
	Gain2			0	W
	Gain1			0	W

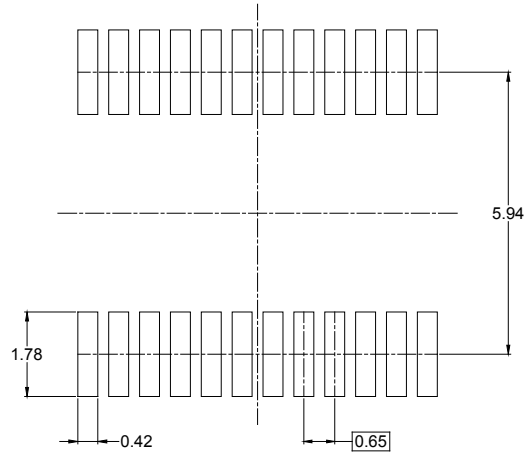
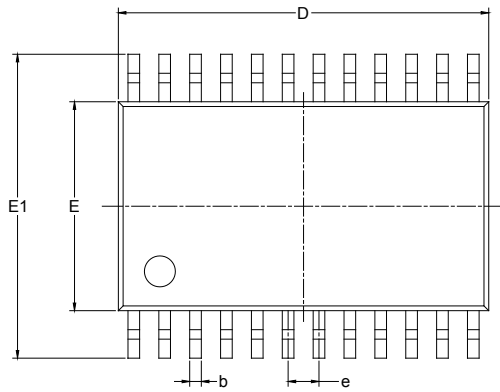
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

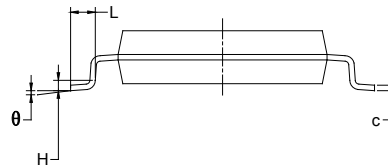
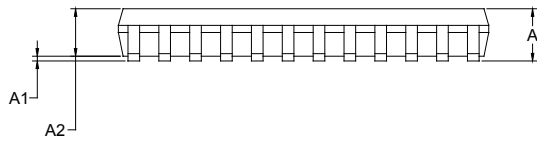
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PACKAGE OUTLINE DIMENSIONS

TSSOP-24



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.020	0.150	0.001	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	7.700	7.900	0.303	0.311
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-24	13"	16.4	6.80	8.30	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002