SGM6040
1.8V to 5.5V, 750mA, 60nA Quiescent Current Buck Converter

GENERAL DESCRIPTION

The SGM6040 is a new generation 60nA (TYP) ultra-low operating quiescent current synchronous Buck converter. The device implements proprietary circuits to allow 120nA I_Q in 100% bypass mode as the input battery source reaches the end of discharge.

The SGM6040 operates from 1.8V to 5.5V, which is suitable for various input batteries such as up to 3S Alkaline, 1S to 2S Li-MnO_2, or 1S Li-Ion/Li-$SOCl_2$. The device offers 16 predefined output voltages via a single resistor connected from VSET pin to GND.

The SGM6040 implements the constant on-time (COT) control architecture to provide excellent line and load transient responses, while it maintains low output ripple at light load for noise sensitive applications. The device operates with a switching frequency of 1.5MHz (TYP) at heavy load conditions. When configured in power-save mode via the MODE pin, the device is capable of achieving excellent efficiency down to 1μA and below.

The device offers a STOP pin function that can immediately terminate the switching of the device to eliminate any switching noise for noise sensitive applications or systems that need to take measurement during a transient event.

The SGM6040 is available in a Green TDFN-2×1.5-8L package.

FEATURES

- **1.8V to 5.5V Input Voltage Range**
- **0.8V to 3.4V Output Voltage Range**
- **Up to 750mA Output Current**
- **60nA (TYP) Quiescent Current**
- **25nA (TYP) Shutdown Current**
- **100% Duty-Cycle Mode**
- **80% Efficiency at 1μA Output Current with 3.6V Input to 1.8V Output**
- **16 Selectable Output Voltages on VSET Pin**
- **COT Control**
- **Output Discharge Function**
- **Transit Automatically in PFM/PWM or Forced PWM Mode**
- **Selectable Forced PWM and Stop Modes**
- **Available in a Green TDFN-2×1.5-8L Package**

APPLICATIONS

Utility Meters
Asset Tracking Devices
Wearable Electronics
Portable Medical Devices
Industrial IoT (Smart Sensors)/NB-IoT

TYPICAL APPLICATION

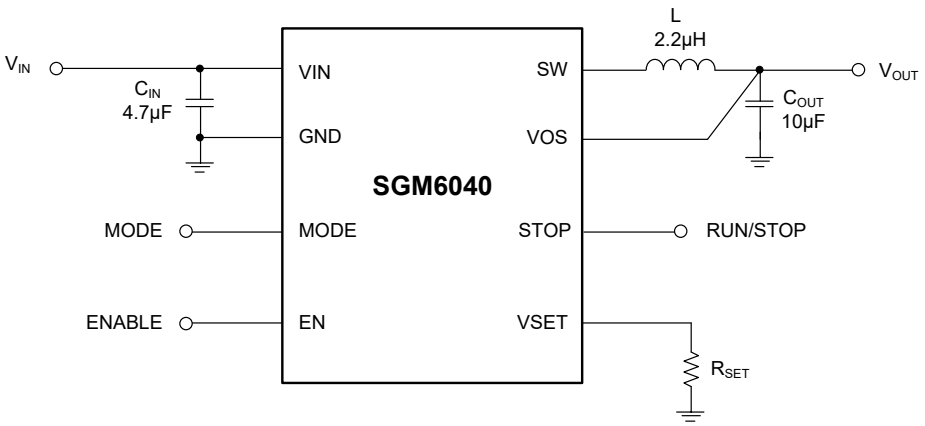


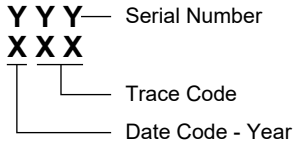
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6040A	TDFN-2×1.5-8L	-40℃ to +125℃	SGM6040AXTHL8G/TR	0XI XXX	Tape and Reel, 3000
SGM6040B	TDFN-2×1.5-8L	-40℃ to +125℃	SGM6040BXTHL8G/TR	0XJ XXX	Tape and Reel, 3000
SGM6040D	TDFN-2×1.5-8L	-40℃ to +125℃	SGM6040DXTHL8G/TR	0XK XXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code, Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

DEVICE OPTIONS

DEVICE	OUTPUT VOLTAGE	OUTPUT CURRENT	OUTPUT DISCHARGE	MODE PIN	STOP PIN	PACKAGE
SGM6040A	1.8V to 3.3V in 100mV steps	750mA	Yes	Yes	Yes	TDFN-2×1.5-8L
SGM6040B	0.8V to 1.55V in 50mV steps	750mA	Yes	Yes	Yes	TDFN-2×1.5-8L
SGM6040D	3.4V fixed output voltage	750mA	Yes	Yes	Yes	TDFN-2×1.5-8L

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} ..... -0.3V to 6.0V
Switch Voltage, SW (DC) ..... -0.3V to V_{IN} + 0.3V
SW, (AC, less than 10ns), while switching ..... -2.0V to 8.5V
EN, MODE, STOP Voltage ..... -0.3V to 5.5V
VEST Voltage ..... -0.3V to V_{IN} + 0.3 < 3.6V
VOS Voltage ..... -0.3V to 3.7V
Package Thermal Resistance
SGM6040A/B/D
TDFN-2×1.5-8L, θ_{JA} ..... 97.4℃/W
TDFN-2×1.5-8L, θ_{JB} ..... 20.0℃/W
TDFN-2×1.5-8L, θ_{JC} ..... 89.0℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 1.8V to 5.5V
Effective Inductance, L ..... 1.51μH to 2.9μH
Effective Output Capacitance, C_{OUT} ..... 3μF to 40μF
Effective Input Capacitance, C_{IN} ..... 1μF (MIN), 4.7μF (NOM)
External Parasitic Capacitance at VSET Pin, C_{VEST} 100pF
Nominal Resistance Range for External Voltage Selection Resistor (E96 Resistor Series), R_{SET} ..... 0.909kΩ to 267kΩ
External Voltage Selection Resistor Tolerance, R_{SET} ..... 1% (MAX)
External Voltage Selection Resistor Temperature Coefficient, R_{SET} ..... ±200ppm/℃
Operating Junction Temperature ..... -40℃ to +125℃
Operating Ambient Temperature ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

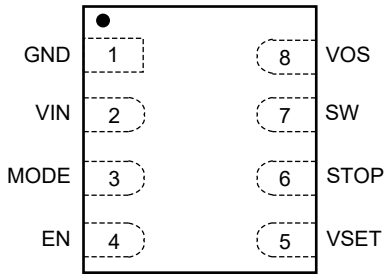
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

SGM6040A/B/D (TOP VIEW)



TDFN-2×1.5-8L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	GND	G	Ground Pin. Connect the C_{IN} and C_{OUT} ground terminals close to this pin.
2	VIN	P	Power Supply Input. Connect a ceramic capacitor (C_{IN}) close to this pin. A 4.7μF ceramic capacitor is recommended.
3	MODE	I	MODE Pin. Power-save mode is configured when this pin is pulled logic low and transits automatically between PFM and PWM modes. Logic high makes the device to operate in PWM mode. It can be toggled during operation and must be terminated.
4	EN	I	Enable Pin. Logic high enables the device and logic low disables the device. An internal pull-down resistor is implemented and it is disabled once the device has started up and the output voltage is in regulation. When a low level occurs, the pull-down resistor is enabled.
5	VSET	I	Connect an accurate resistor between this pin and GND to select a pre-defined output voltage when the device is enabled.
6	STOP	I	STOP Switching Pin. When setting logic high, the device is disabled for a quiet supply rail. The output is powered by the charge available in the output capacitor. When setting logic low, the device is immediately enabled. An internal pull-down resistor is used here and it is disabled once a high level occurs at the input. When a low level occurs, the pull-down resistor is enabled.
7	SW	P	Switching Node Pin. This pin is connected to the internal MOSFET switches. Connect this pin to the inductor.
8	VOS	I	Output Voltage Sense Pin. This pin is internally connected to the feedback loop and a MOSFET to discharge the output (V_{OUT}) when the device is disabled. Connect it with a short trace to the output capacitor.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, STOP = GND, MODE = GND, typical values are measured at T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
No Load Operating Input Current	$I_{Q\_NO\_LOAD}$	EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.8V, device switching		60		nA
		EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.2V, device switching		70		
No Load Operating Input Current (PWM Mode)	$I_{Q\_NO\_LOAD}$	EN = MODE = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.8V, device switching		3		mA
Operating Quiescent Current into VIN Pin	I_{Q_VIN}	T_J = +25℃, EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V, device not switching		40	80	nA
		T_J = -40°C to +85℃, EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V, device not switching		40	300	
Operating Quiescent Current into VOS Pin	I_{Q_VOS}	T_J = +25℃, EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V, device not switching		40	120	nA
		T_J = -40℃ to +85℃, EN = V_{IN}, I_{OUT} = 0μA, V_{OUT} = 1.55V or V_{OUT} = 1.8V, device not switching		40	180	
Operating Quiescent Current into VOS Pin	I_{Q_VOS}	EN = V_{IN}, V_{OUT} = 3.3V, device not switching		56		nA
		EN = V_{IN}, V_{OUT} < 1.5V, device not switching		6		
		T_J = -40℃ to +85℃, EN = STOP = V_{IN}, 3V < V_{OUT} < 3.3V		5	100	
Operating Quiescent Current 100% Mode	$I_{Q\_100\%\_MODE}$	T_J = -40℃ to +85℃, V_{IN} = V_{OUT} = 3.3V		120		nA
Operating Quiescent Current into VIN Pin	$I_{Q\_VIN\_STOP}$	T_J = -40℃ to +85℃, STOP = High, V_{OUT} = 1.8V		80	150	μA
Shutdown Current	I_{SD}	T_J = -40℃ to +85℃, EN = GND, shutdown current into V_{IN}, V_{SET} = GND		25	300	nA
Under-Voltage Lockout Threshold	V_{TH_UVLO+}	V_{IN} rising		1.65	1.80	V
	V_{TH_UVLO-}	V_{IN} falling		1.54	1.68	
EN, MODE and STOP Inputs						
High-Level Input Voltage	V_{IH_TH}		1.10			V
Low-Level Input Voltage	V_{IL_TH}				0.40	V
Input Bias Current	I_{IN}	T_J = -40℃ to +85℃, MODE input		7	25	nA
Internal Pull-Down Resistance	R_{PD}	EN, STOP inputs	420	490		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, STOP = GND, MODE = GND, typical values are measured at T_J = +25℃, unless otherwise noted.)

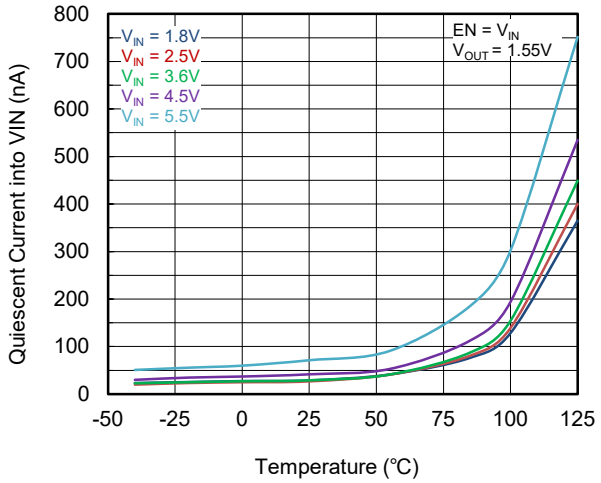
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Switches						
High-side MOSFET On-Resistance	R_{DSON}	T_J = -40℃ to +85℃, V_{IN} = 3.6V, I_{SW} = 200mA		260	360	mΩ
		T_J = -40℃ to +85℃, V_{IN} = 5V, I_{SW} = 200mA		210	285	
Low-side MOSFET On-Resistance		T_J = -40℃ to +85℃, V_{IN} = 3.6V, I_{SW} = 200mA		110	185	mΩ
		T_J = -40℃ to +85℃, V_{IN} = 5V, I_{SW} = 200mA		100	165	
Soft-Start Switch Current Limit (1)	I_{LIMF_SS}		0.065	0.212	0.36	A
High-side MOSFET Switch Current Limit (1)	I_{LIMF}		0.95	1.15	1.35	A
Low-side MOSFET Switch Current Limit				1.0		A
Negative Current Limit	I_{LIMN}			600		mA
Current Limit Propagation Delay	t_{ILIM_DELAY}			50		ns
Leakage Current Into SW Pin	I_{LKG_SW}	T_J = -40℃ to +85℃, V_{SW} = 1.8V		10		nA
Output Voltage Discharge						
Output Discharge Current	I_{DISCRG_VOS}	T_J = -40℃ to +85℃, EN = GND, sink current into VOS pin, over V_{IN} range, V_{OUT} = 1.8V	8	22	36	mA
Thermal Protection						
Thermal Shutdown Temperature	T_{SD}	Rising junction temperature, PWM mode		160		℃
Thermal Shutdown Hysteresis				10		℃
Output						
Output Voltage Accuracy	V_{OUT}	PWM mode, I_{OUT} = 0mA, V_{OUT} ≥ 1.8V	-1.7	0	1.7	%
		PWM mode, I_{OUT} = 0mA, V_{OUT} ≤ 1.55V	-2.8	0	2.8	%
DC Output Voltage Load Regulation	V_{OUT}	PWM mode		0		%/mA
DC Output Voltage Line Regulation		PWM mode, V_{OUT} = 1.8V, I_{OUT} = 200mA, over V_{IN} range		0		%/V
Switching Frequency	f_{SW}	V_{IN} = 3.6V, V_{OUT} = 1.8V, MODE = V_{IN}, I_{OUT} = 0mA		1.5		MHz
Regulator Start-up Delay Time	$t_{STARTUP\_DELAY}$	V_{IN} = 3.6V, from EN = low to high until device starts switching			200	μs
Regulator Start-up Delay Time	$t_{STARTUP\_DELAY}$	EN ramps with V_{IN}, V_{IN} = 0V to 3.6V (< 100μs) until device starts switching		14		ms
Soft-Start Time	t_{SS}	I_{OUT} = 0mA		90		μs
Reduced Current Limit Soft-Start Timeout	t_{SS_ILIMF}			790	1500	μs

NOTE: 1. This is the static current limit. It can be temporarily higher in applications due to internal propagation delay.

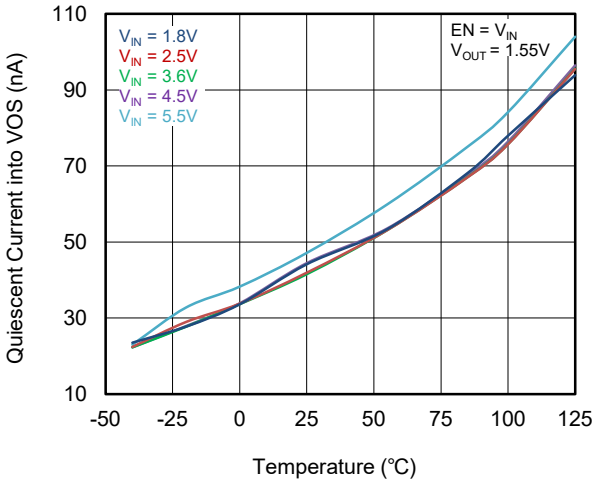
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = -40℃ to +125℃, unless otherwise noted.

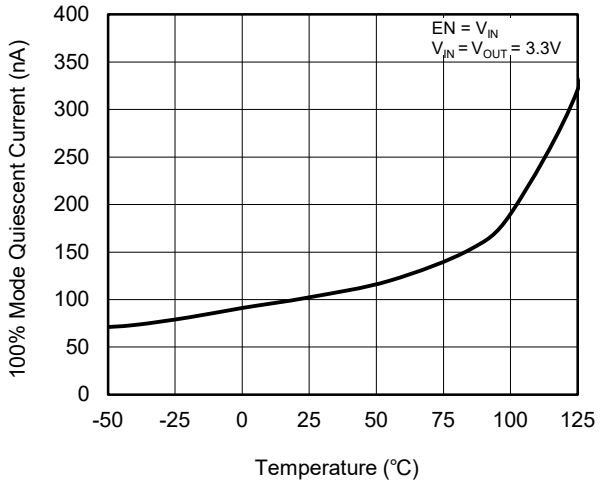
Quiescent Current into VIN vs. Temperature



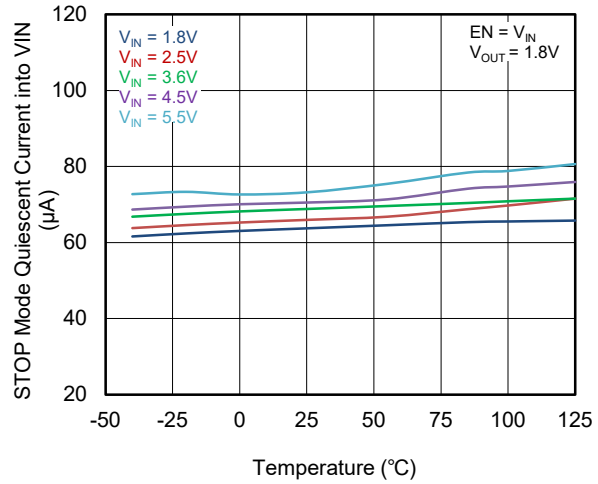
Quiescent Current into VOS vs. Temperature



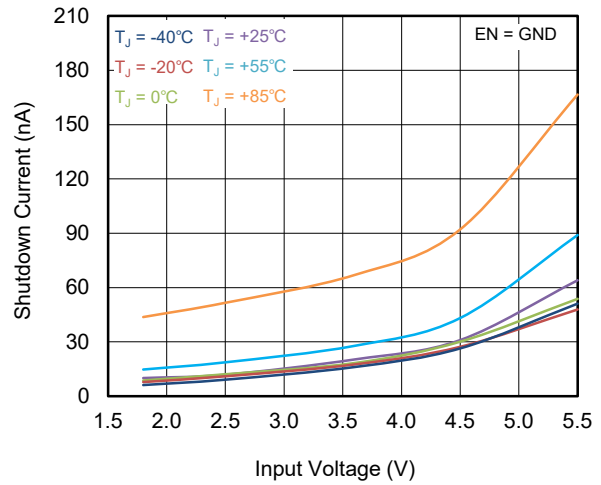
100% Mode Quiescent Current vs. Temperature



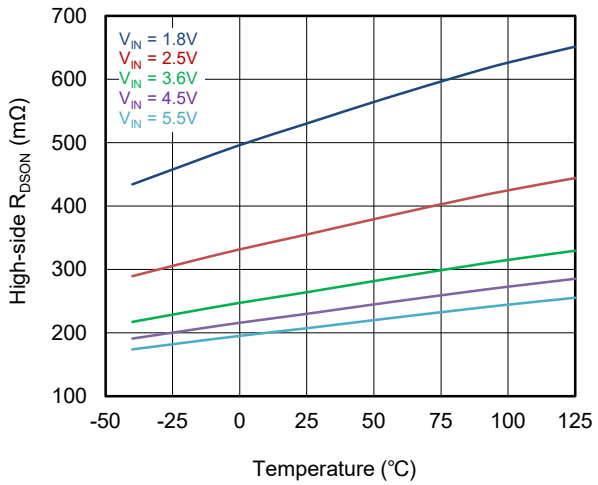
STOP Mode Quiescent Current into VIN vs. Temperature



Shutdown Current vs. Input Voltage



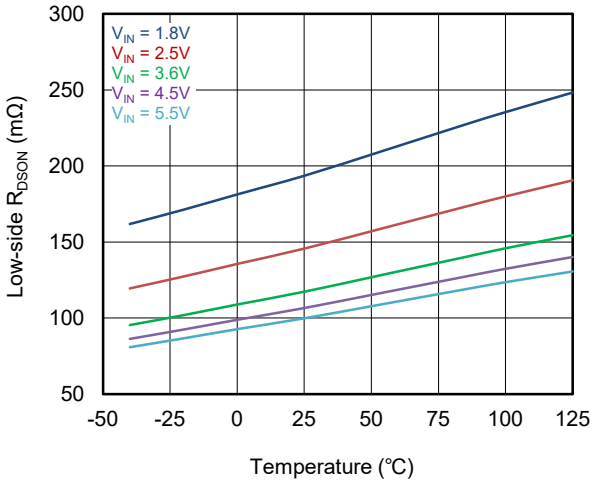
High-side R_{DSON} vs. Temperature



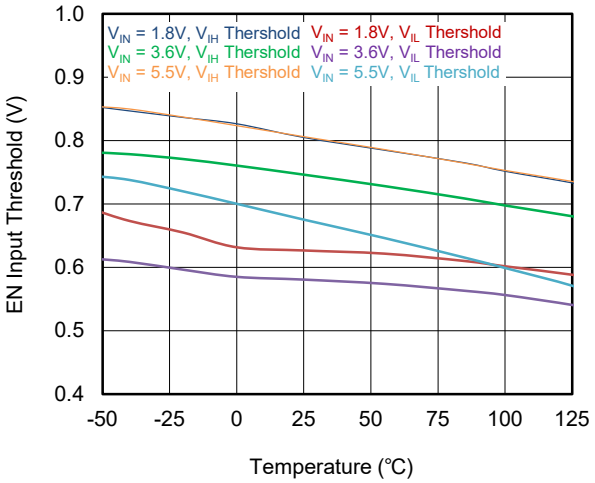
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, unless otherwise noted.

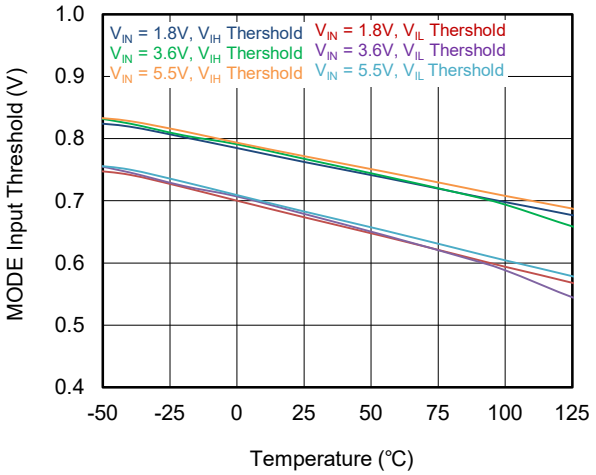
Low-side R_{DSON} vs. Temperature



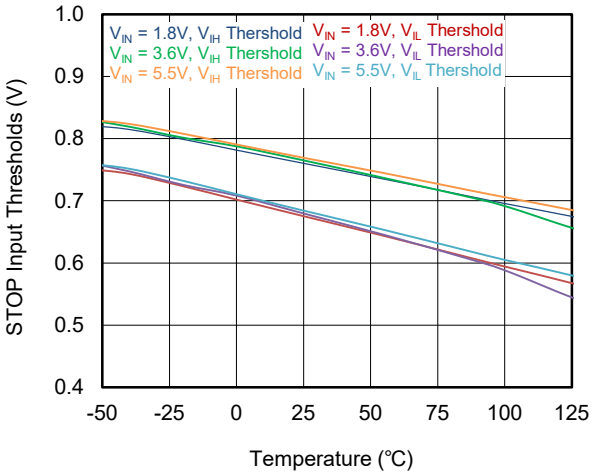
EN Input Threshold vs. Temperature



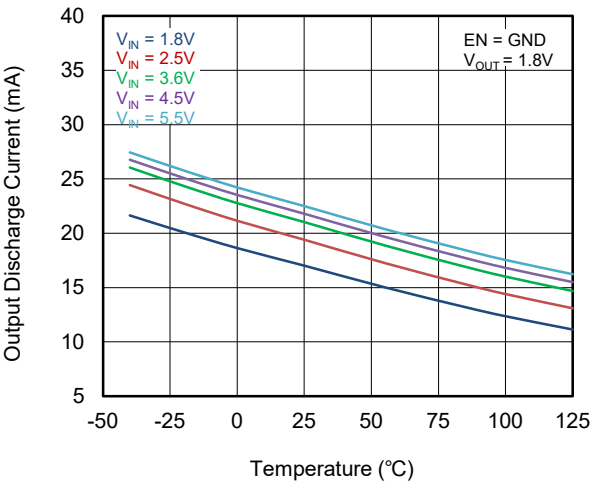
MODE Input Threshold vs. Temperature



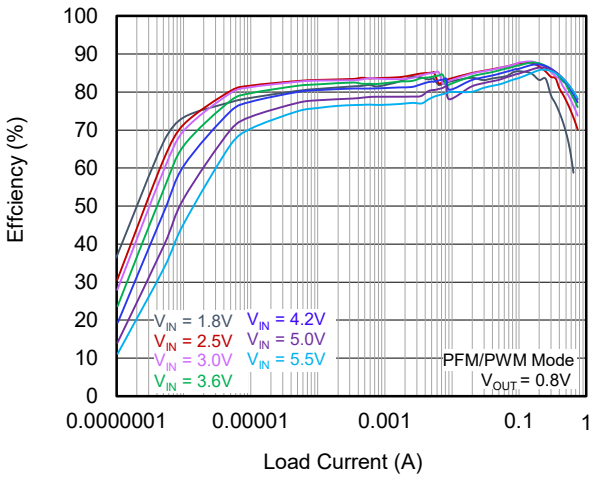
STOP Input Threshold vs. Temperature



Output Discharge Current vs. Temperature



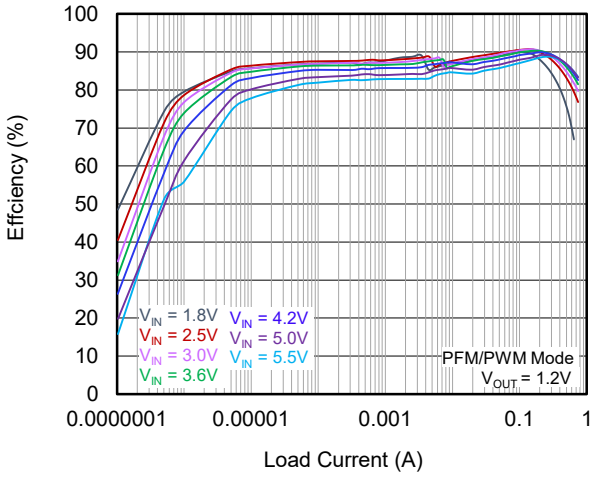
Efficiency vs. Load Current



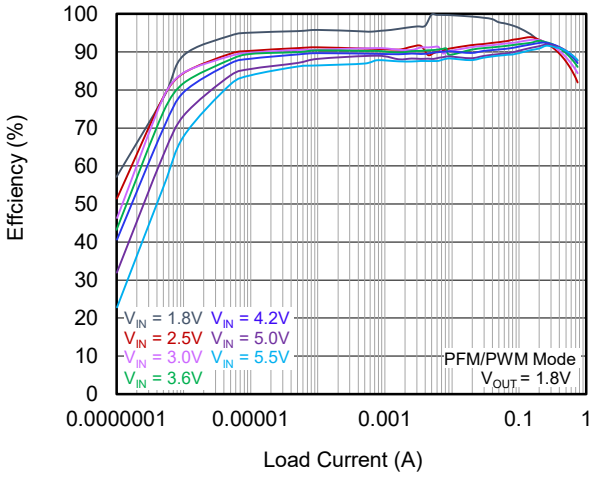
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, unless otherwise noted.

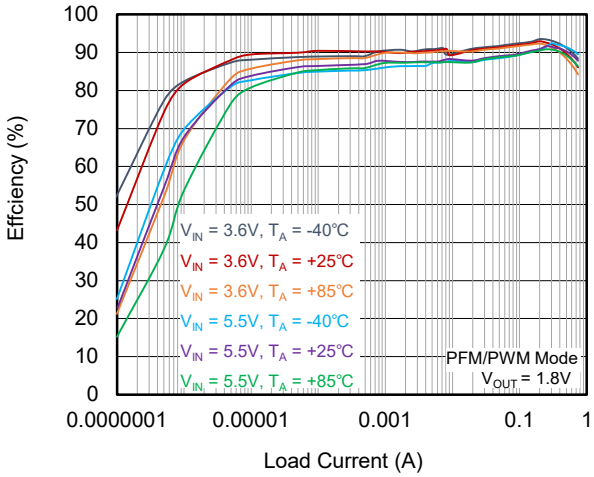
Efficiency vs. Load Current



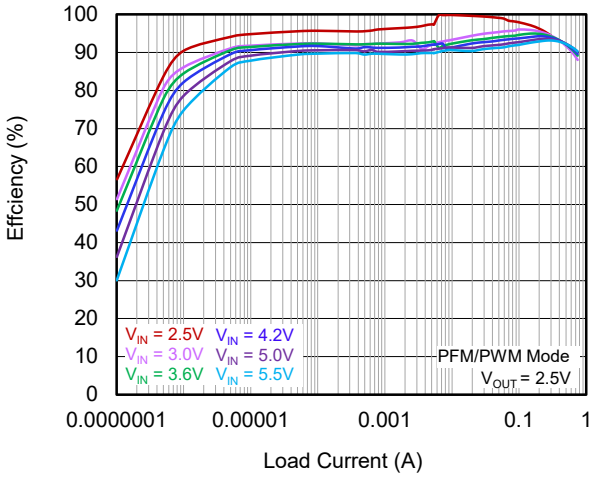
Efficiency vs. Load Current



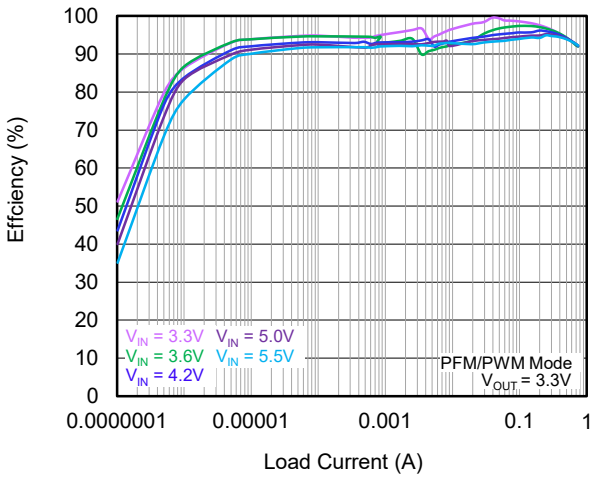
Efficiency vs. Load Current



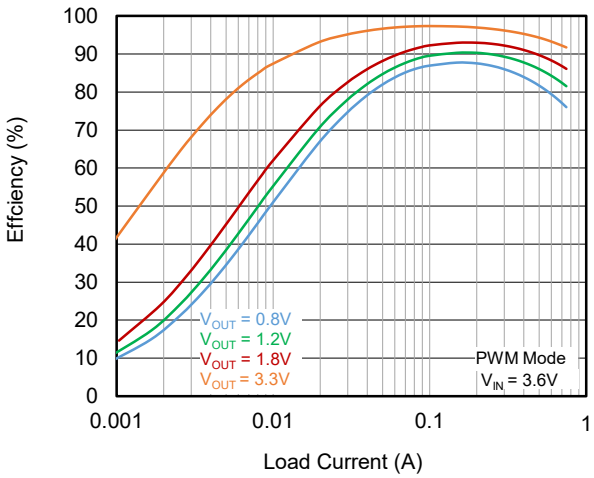
Efficiency vs. Load Current



Efficiency vs. Load Current



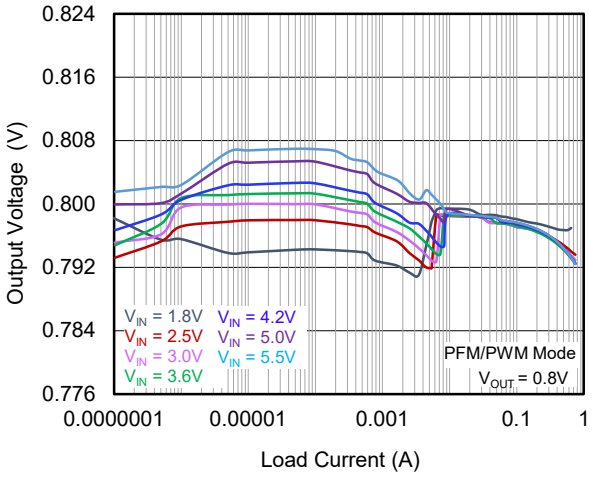
Efficiency vs. Load Current



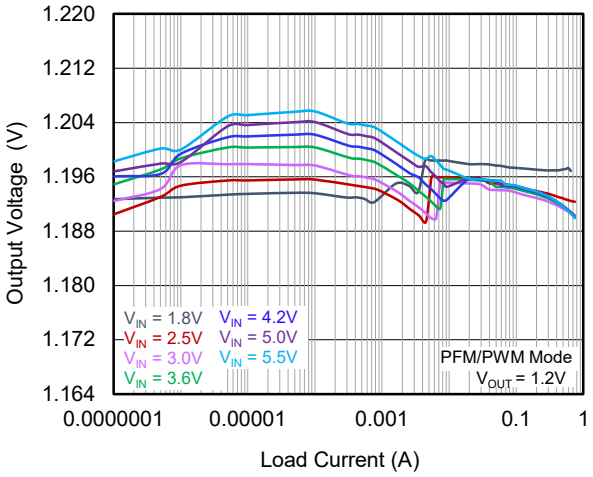
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, unless otherwise noted.

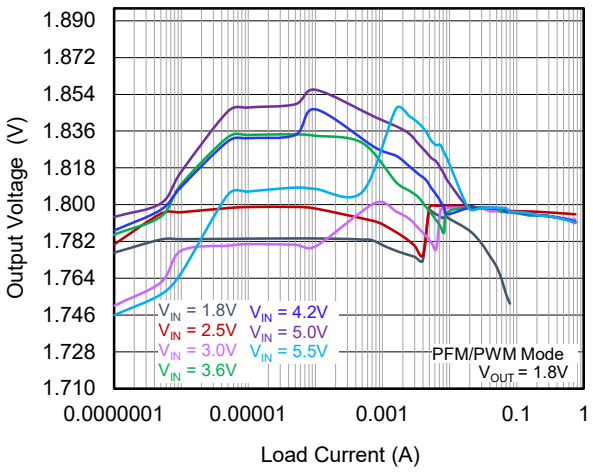
Output Voltage vs. Load Current



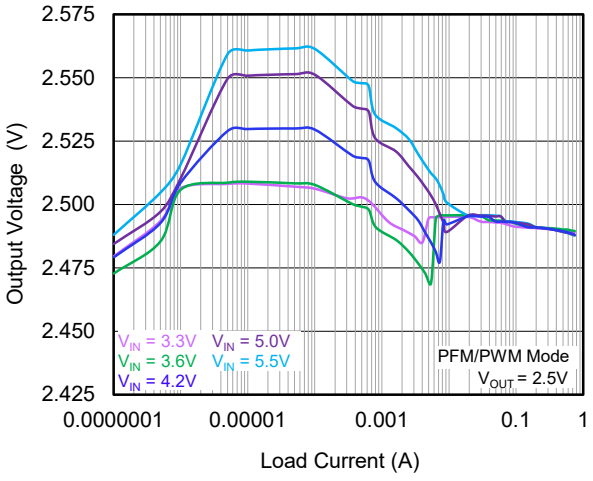
Output Voltage vs. Load Current



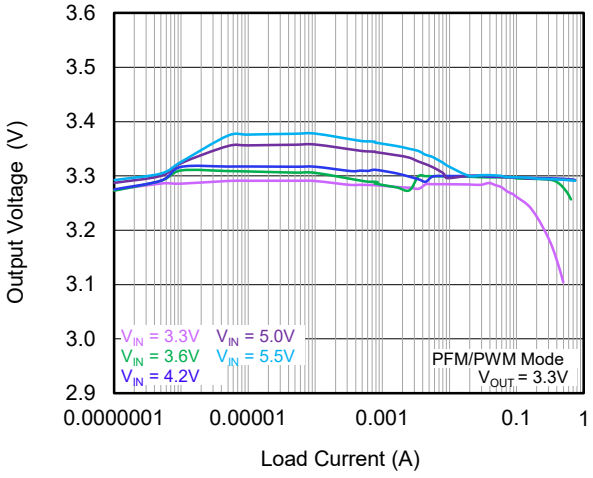
Output Voltage vs. Load Current



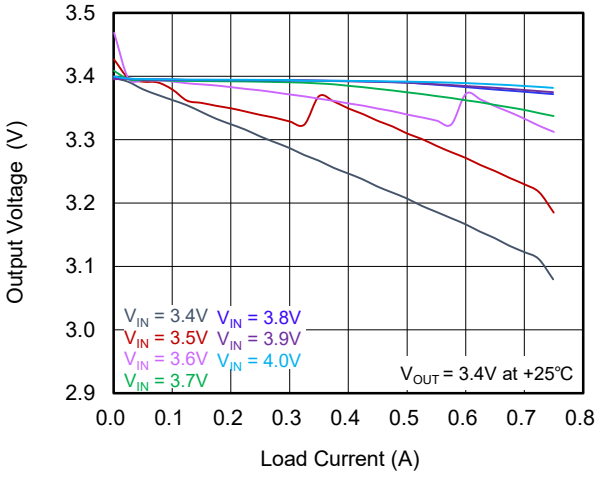
Output Voltage vs. Load Current



Output Voltage vs. Load Current



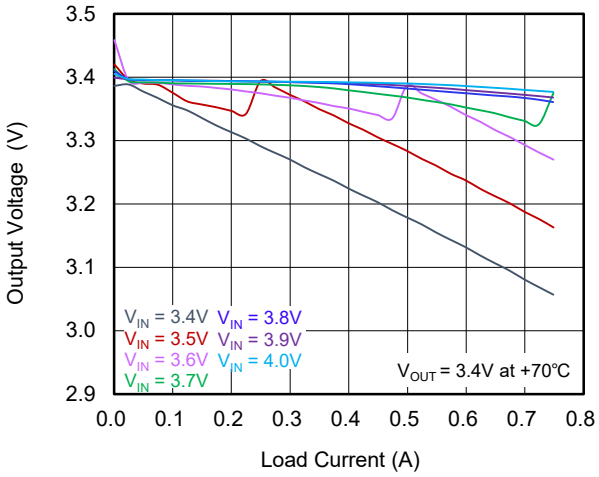
Output Voltage vs. Load Current



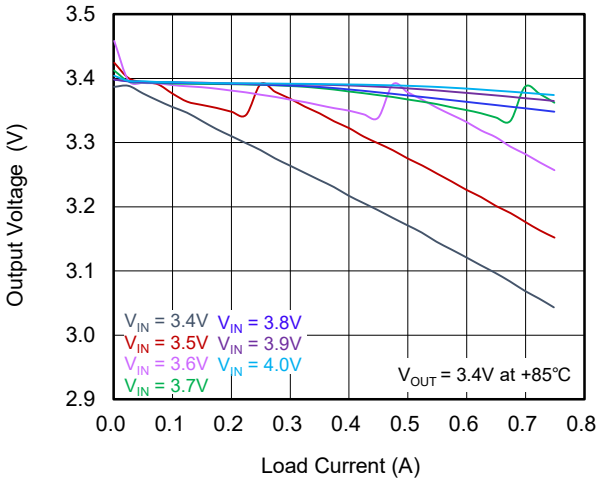
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, unless otherwise noted.

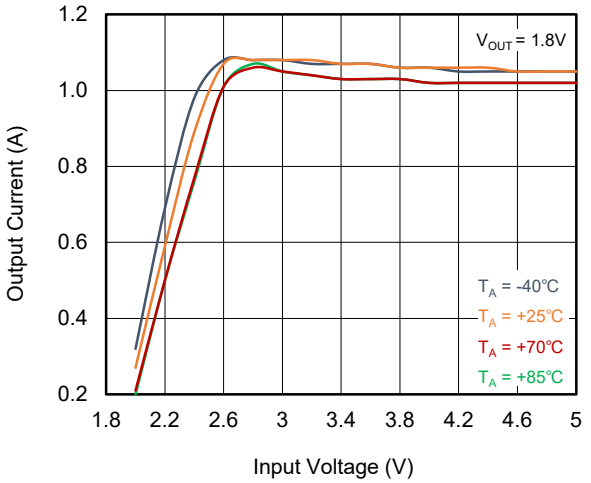
Output Voltage vs. Load Current



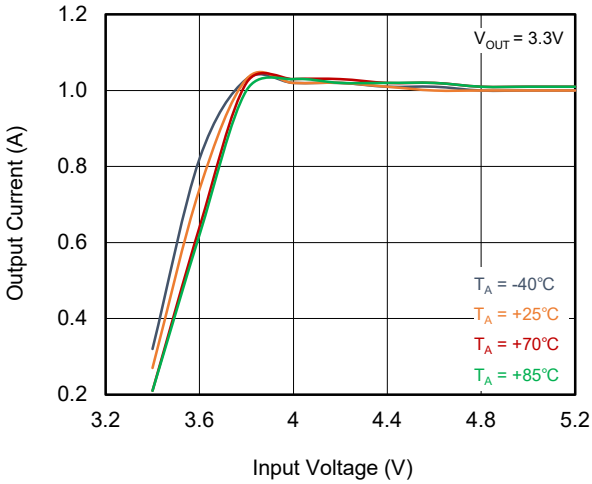
Output Voltage vs. Load Current



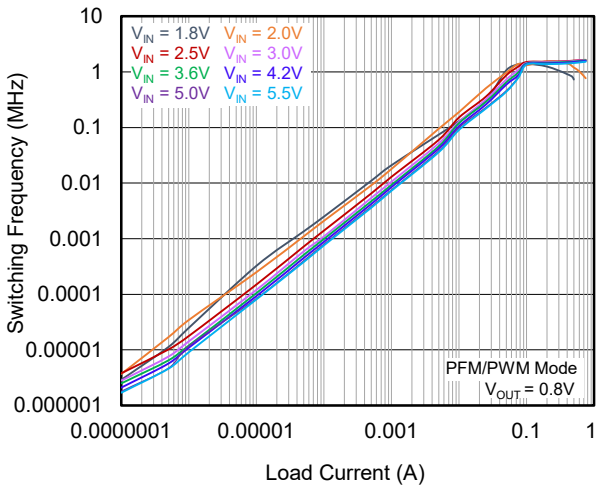
Maximum Output Current vs. Input Voltage



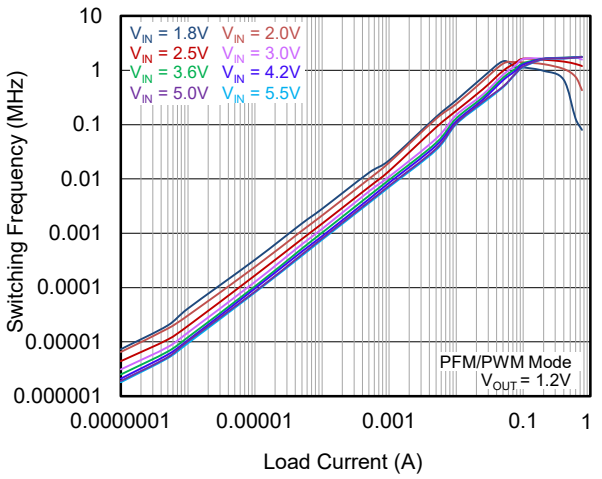
Maximum Output Current vs. Input Voltage



Switching Frequency vs. Load Current



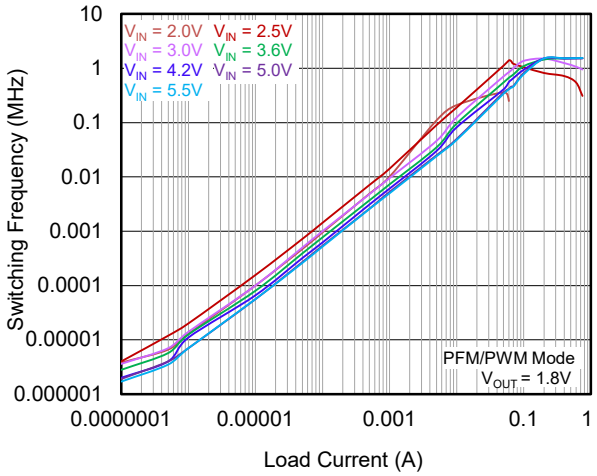
Switching Frequency vs. Load Current



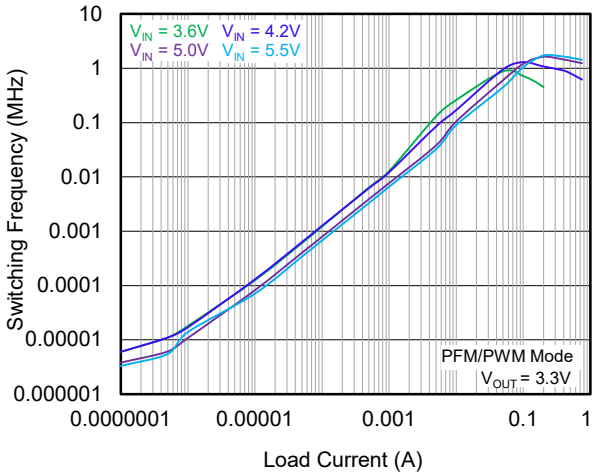
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, unless otherwise noted.

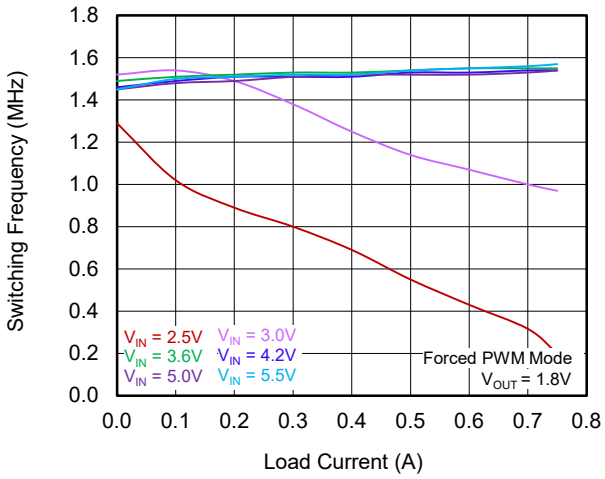
Switching Frequency vs. Load Current



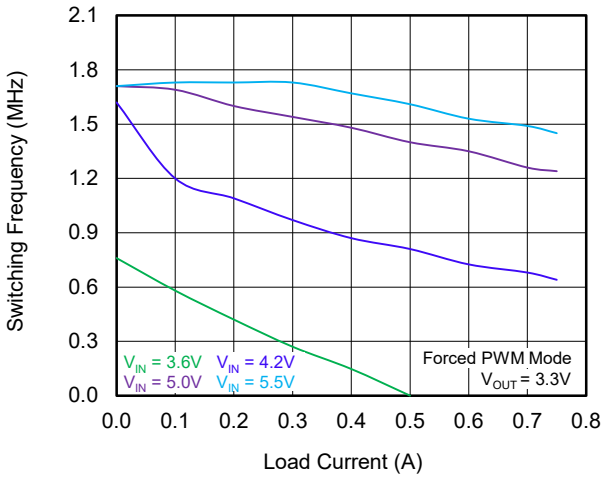
Switching Frequency vs. Load Current



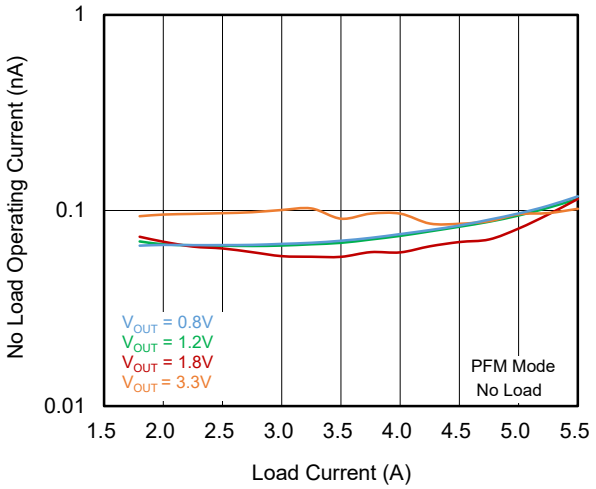
Switching Frequency vs. Load Current



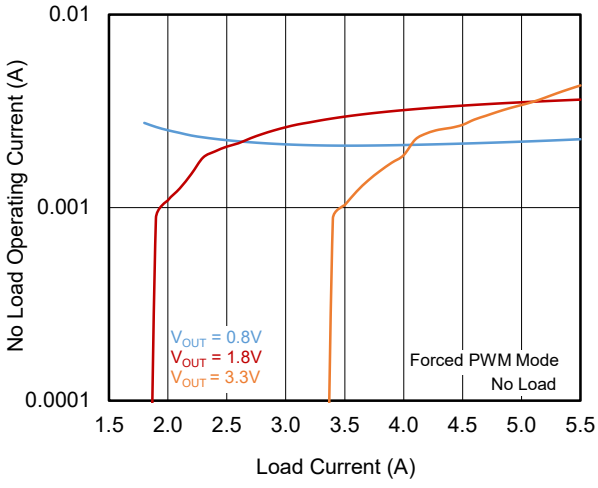
Switching Frequency vs. Load Current



No Load Operating Current vs. Load Current in PFM Mode



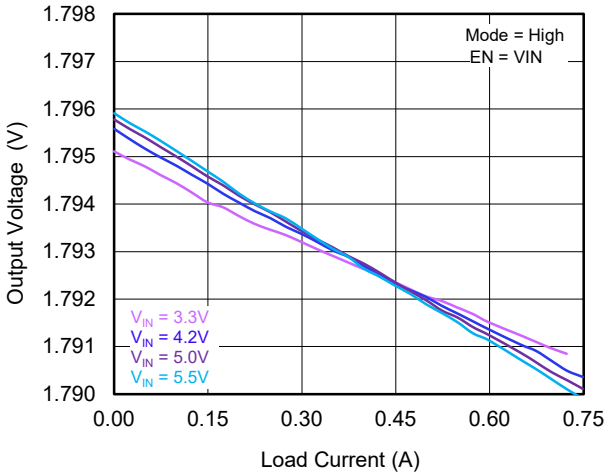
No Load Operating Current vs. Load Current in Forced PWM Mode



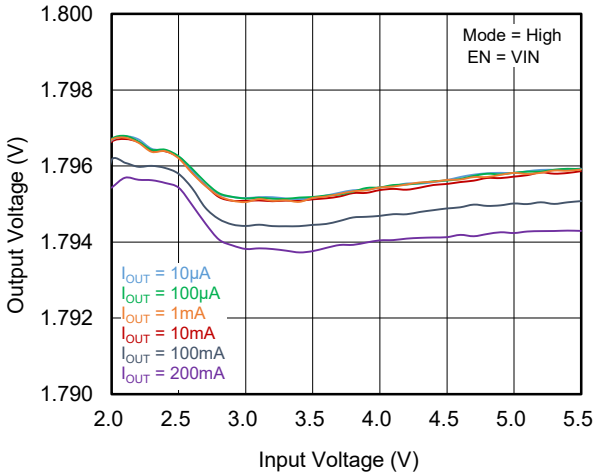
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = -40℃ to +125℃, unless otherwise noted.

Output Voltage vs. Load Current

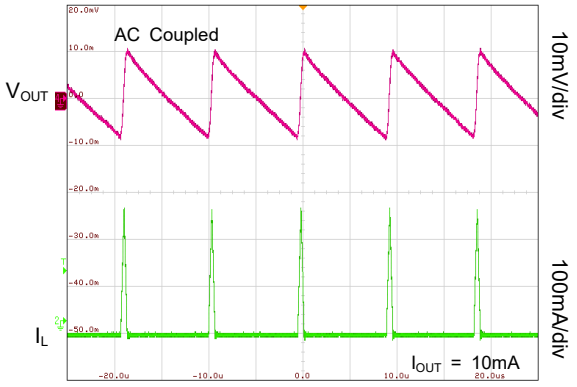


Output Voltage vs. Input Voltage



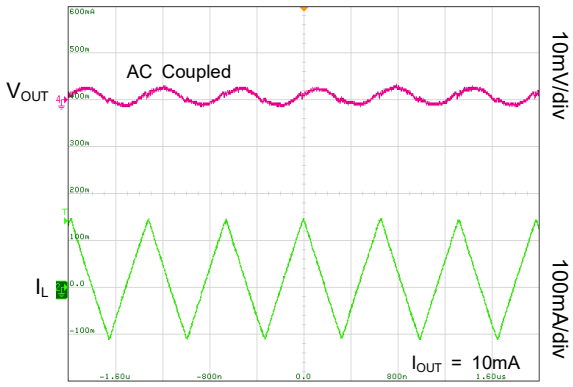
V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = -40℃ to +125℃, unless otherwise noted.

Output Voltage Ripple in PFM Mode



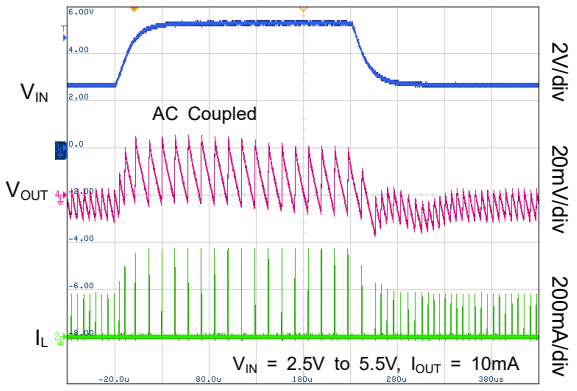
Time (5μs/div)

Output Voltage Ripple in PWM Mode



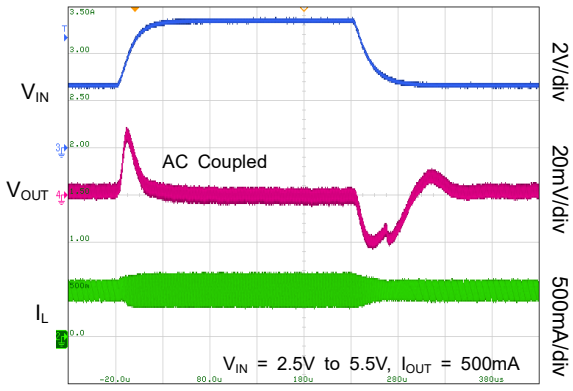
Time (400ns/div)

Line Transient in PFM Mode



Time (50μs/div)

Line Transient in PWM Mode

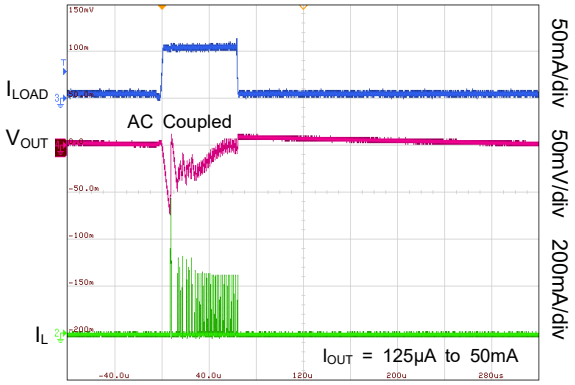


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

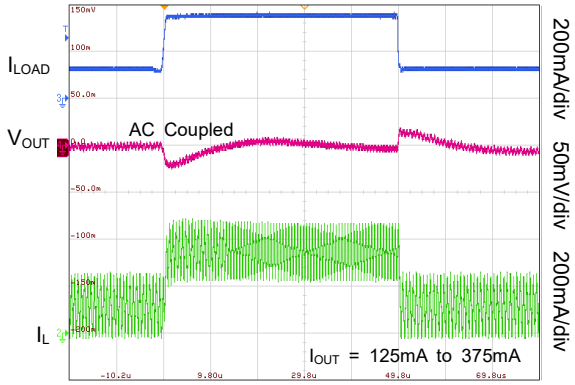
V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = -40℃ to +125℃, unless otherwise noted.

Load Transient in PFM Mode



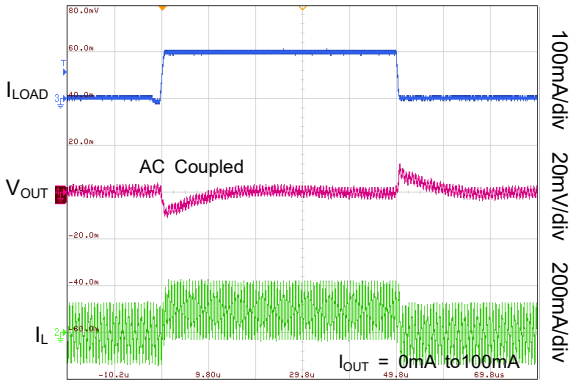
Time (40μs/div)

Load Transient in PFM/PWM Mode



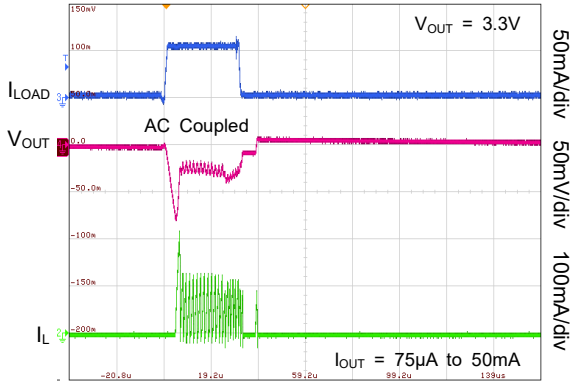
Time (10μs/div)

Load Transient in PFM/PWM Mode with No load



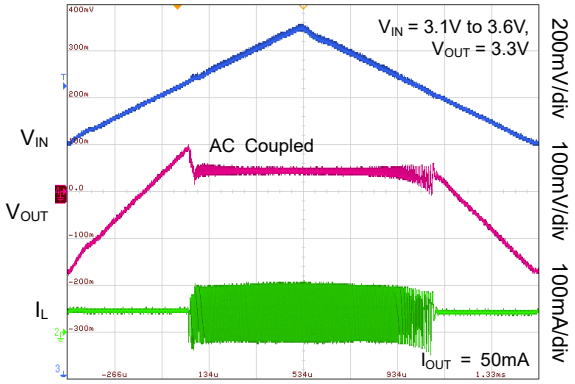
Time (10μs/div)

Load Transient in PFM Mode



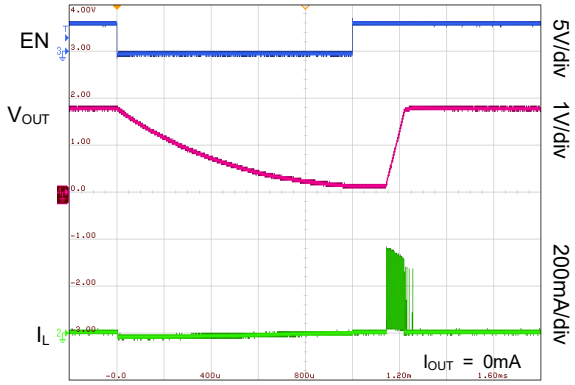
Time (20μs/div)

100% Mode Entry/Exit Operation



Time (200μs/div)

Start-up/Shutdown with No Load

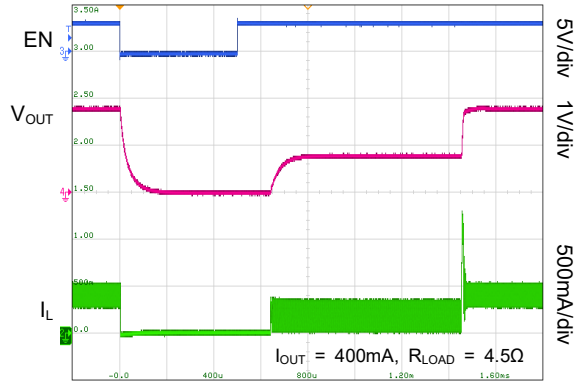


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

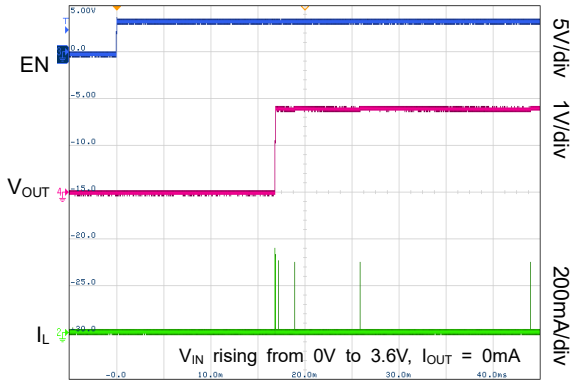
V_{IN} = 3.6V, V_{OUT} = 1.8V, T_A = -40℃ to +125℃, unless otherwise noted.

Start-up/Shutdown with Load



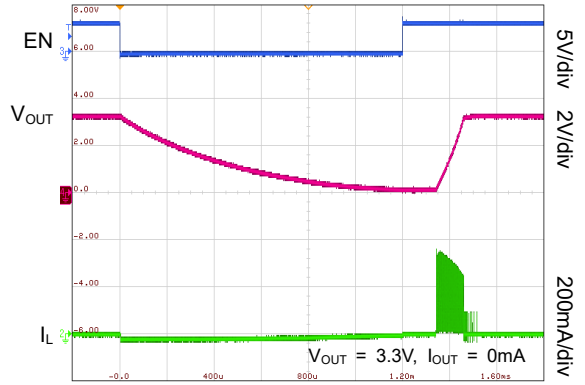
Time (200μs/div)

Start-up/Shutdown with No Load



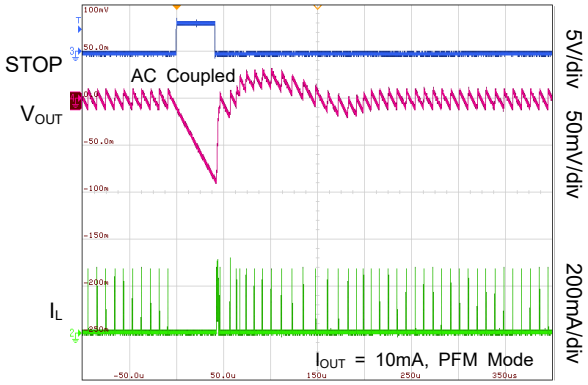
Time (5ms/div)

Start-up/Shutdown with No Load



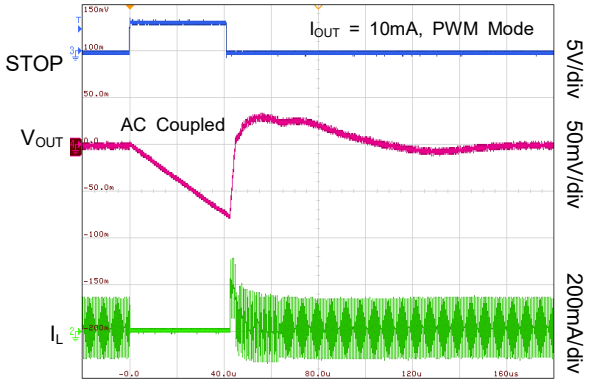
Time (200μs/div)

STOP Operation in PFM Mode



Time (50μs/div)

STOP Operation in PWM Mode



Time (20μs/div)

FUNCTIONAL BLOCK DIAGRAM

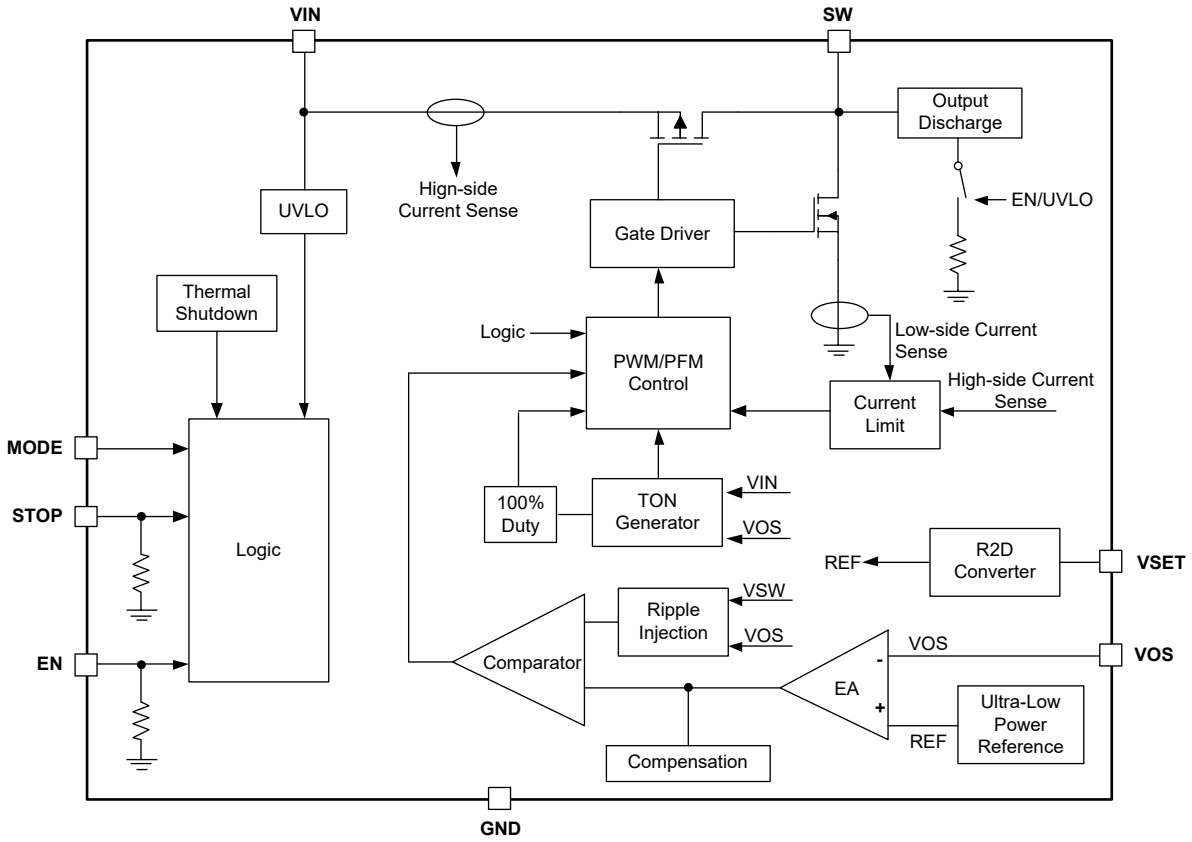


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM6040 is a new generation 60nA (TYP) ultra-low operating quiescent current synchronous Buck converter with 750mA output current capability. The device adopts the constant on-time (COT) control architecture to provide excellent line and load transient responses.

The SGM6040 operates in power-save mode (PSM) at light load to achieve excellent light load efficiency. At medium to heavy load, the device enters PWM mode and operates with constant switching frequency of 1.5MHz (TYP). The device only requires one 10μF ceramic output capacitor to achieve minimal output voltage ripple and superior transient performance.

The device offers a STOP pin function that can immediately terminate the switching of the device to eliminate any switching noise for noise sensitive applications or systems that need to take measurement during a transient event.

Feature Description

Under-Voltage Lockout (UVLO)

The SGM6040 offers input under-voltage lockout (UVLO) with hysteresis to prevent unstable change of input voltage. The device's UVLO rising voltage is 1.65V (TYP) and falling threshold is 1.54V (TYP).

When the input voltage drops below the falling threshold, the device stops working and the output voltage discharge is active. When the device is released from under-voltage lockout condition, it begins to soft start.

Enable and Shutdown

When the EN pin is logic low, the device is in shutdown mode and the output discharge path is enabled to discharge the output voltage. The EN pin has an internal 490kΩ resistor connected to GND to avoid a floating EN input. Pulling the EN pin to logic high enables the device, and internal EN pin's pull-down resistor is disabled.

Soft-Start

The SGM6040 adopts the built-in soft-start function to protect the system from excessive inrush current. When the input voltage is above the UVLO rising threshold and the EN pin is logic high, the device begins to soft start.

Before the output voltage starts ramping up, the device has a delay time ($t_{STARTUP\_DELAY}$). During the delay time, the device establishes the internal reference, and reads the resistor connected to the VSET pin to determine the start-up output voltage. Once $t_{STARTUP\_DELAY}$ expires, the device begins to switch to ramp up the output voltage which follows the internal soft-start circuitry within the soft-start time (t_{SS}). The device operates with a reduced switch current limit (I_{LIMF_SS}) until the reduced current limit soft-start time (t_{SS_ILIMF}) expires or the output voltage rises to the setting voltage value, whichever occurs first.

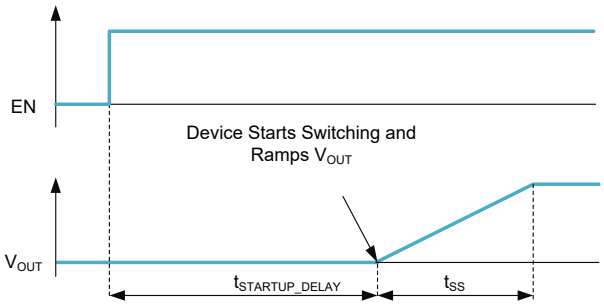


Figure 3. Device Start-up

Output Voltage Selection

The output voltage of SGM6040 is programmed through a resistor connected between the VSET pin and ground. When the device begins to start up, an internal current source injects a current into the resistor on the VSET pin during the $t_{STARTUP\_DELAY}$. The internal ADC reads the voltage and feedbacks this information to the internal circuit. The internal feedback divider network sets the proper output voltage based on the information. The current source is turned off after the $t_{STARTUP\_DELAY}$ to reduce current consumption. In addition to reading the resistor connected on VSET pin, pulling the VSET pin to logic high or logic low also can program different output voltages.

To ensure a proper read of the resistor connected on the VSET pin, additional current path or capacitance greater than 100pF total from VSET to GND should be avoided. The resistor connected on VSET pin is designed to meet the standard resistance value from E96 table, and ±1% accuracy resistor is recommended. Use Table 1 below to select the appropriate resistors for different output voltages.

DETAILED DESCRIPTION (continued)

Table 1. Output Voltage Setting and R_{SET} Resistor (1)

OUTPUT VOLTAGE SETTING VOUT (V)			VSET RESISTANCE TO GND - E96 VALUES (kΩ)		
SGM6040A	SGM6040B	SGM6040D	MIN	NOM	MAX
1.8	0.8	3.4	0	GND	0.01
1.9	0.85		0.87	0.909	0.95
2.0	0.9		1.67	1.74	1.81
2.1	0.95		2.76	2.87	2.98
2.2	1.0		4.15	4.32	4.49
2.3	1.05		5.80	6.04	6.28
2.4	1.1		8.11	8.45	8.79
2.5	1.15		11.04	11.5	11.96
2.6	1.2		15.17	15.8	16.43
2.7	1.25		20.64	21.5	22.36
2.8	1.3		27.55	28.7	29.85
2.9	1.35		36.77	38.3	39.83
3.0	1.4		50.21	52.3	54.39
3.1	1.45		68.64	71.5	74.36
3.2	1.5		97.92	102	106.08
3.3	1.55		256.32	267	277.68

NOTE: 1. The output voltage of the SGM6040D is internally set to 3.4V. Connect VSET directly to GND.

Switch Current Limit/Short-Circuit Protection

The SGM6040 implements current limit function via the high-side and low-side power MOSFETs to protect the device from damage caused by overload or short-circuit conditions. The current through the power MOSFETs is monitored in every switching cycle. During an over-current or short-circuit scenario, the inductor current will reach the current limit threshold. When the current flowing through the high-side FET rises up to the I_{LIMF} of 1.15A (TYP), the device turns off the high-side switch to terminate the inductor current from further increase, and the low-side switch turns on to ramp down the inductor current. When the low-side FET's current drops below the I_{LIMF} of 1.0A (TYP), the low-side FET is turned off and the high-side FET is turned on again. During soft-start, the current limit is reduced to I_{LIMF_SS}. After soft-start has finished, the current limit value increases to the normal value of I_{LIMF}.

When the MODE pin is logic high, the device operates in PWM mode and a negative current limit (I_{LIMN}) is enabled to prevent excessive current flowing backwards to the input supply.

Output Voltage Discharge

The device implements output voltage discharge function to ensure output voltage ramps down to close to 0V in a controlled manner during shutdown state.

The internal discharge path discharges the output voltage through the SW pin to ground.

Here are two scenarios to discharge the output voltage: EN pin is toggled to logic low and input voltage UVLO.

The output discharge function remains active as long as the input voltage is higher than 0.7V (TYP).

Thermal Warning and Shutdown

To prevent the device from overheating, thermal shutdown function is implemented in the SGM6040 device.

The internal temperature sensor monitors the junction temperature (T_J). When the junction temperature exceeds above the 160℃ (TYP), the device enters thermal shutdown and stops switching. When the junction temperature drops by 10℃, the device resumes operation with internal soft-start.

DETAILED DESCRIPTION (continued)

STOP Mode

The SGM6040 includes the STOP input pin. When the STOP pin is logic high, the device stops switching and the load current is supported by the output capacitor. If the STOP pin remains at logic high, the output voltage will decrease until it is clamped to about 0.5V below the set output voltage. The STOP pin function can help the users to temporarily reduce interference to RF and noise-sensitive circuits. Please note that before the output voltage drops to an acceptable minimum value, the STOP pin needs to be set to logic low again. When the STOP pin is set to logic low from high, the device immediately resumes switching operation without a start-up delay or soft-start.

In STOP mode, the device consumes 80μA (TYP) quiescent current from the input supply. The STOP pin has an internal 490kΩ (TYP) pull-down resistor to avoid a floating input. When the STOP pin is logic high, this pull-down resistor is simultaneously disconnected from the STOP pin.

Device Functional Modes

Power-Save Mode Operation

The SGM6040 implements power-save-mode (PSM) operation at light load to achieve high efficiency. At light load, the device generates a single switching pulse to ramp up the inductor current, then the energy is delivered to the load as well as recharging the output capacitor. The device then enters a sleep period until the output voltage is lower than the programmed voltage. After that, a new switching pulse is generated. During the sleep period, the load current is supported by the output capacitor, and most of the internal circuits are turned off to achieve an ultra-low operating quiescent current.

At light load condition, the device operates in pulse frequency modulation (PFM) mode and the switching frequency varies linearly with the load current. At medium and heavy load conditions, the device operates in pulse width modulation (PWM) mode and the switching frequency is 1.5MHz (TYP). The device automatically enters PWM mode from PFM mode based on the load current, and when the inductor current becomes discontinuous, the device enters PFM mode. Equation 1 below calculates the device on-time. The switching frequency in PFM mode is shown in Equation 2.

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 667ns \quad (1)$$

$$f_{PFM} = \frac{2 \times V_{OUT} \times I_{OUT} \times L}{T^2_{ON} \times (V_{IN} - V_{OUT}) \times V_{IN}} \quad (2)$$

Forced PWM Mode Operation

When the MODE input is logic high, the device enters forced PWM mode and operates with a fixed frequency of 1.5MHz (TYP) over the entire load range. This is beneficial for reducing interference to RF and noise-sensitive circuits, while the efficiency at light load decreases.

100% Mode Operation

The Buck converter's duty cycle is calculated as D = V_{OUT}/V_{IN} in PWM mode. When the input voltage is getting close to the output voltage, the duty cycle of the Buck converter gradually approaches to 100%. The SGM6040 enters 100% mode as the input voltage is equal to or below the programmed output voltage, then the device turns the high-side power FET on continuously to bypass the input voltage.

During 100% mode operation, the SGM6040 keeps an ultra-low quiescent current of 120nA (TYP).

APPLICATION INFORMATION

Typical Application

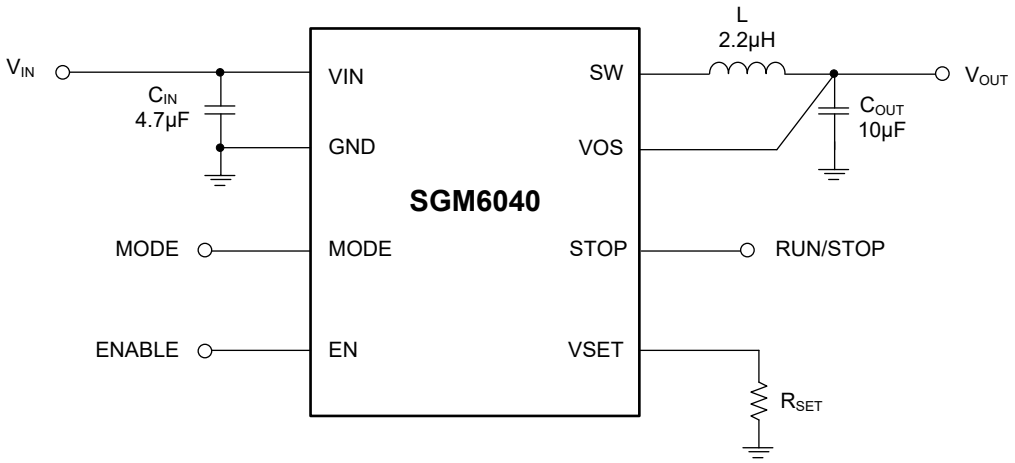


Figure 4. SGM6040 Application Circuits

Design Requirements

Table 2 shows the list of components for the application circuit.

Table 2. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	MANUFACTURER
SGM6040	60nA I_Q Buck Converter	SGMICRO
C_{IN}	4.7μF, ceramic capacitor, 10V, X5R, size 0402, GRM155R61A475MEAAD	muRata
L	2.2μH, power inductor, size 2016, DFE201612E-2R2M=P2	muRata
C_{OUT}	10μF, ceramic capacitor, 4V, X5R, size 0402, GRM155R60G106ME44D	muRata
R_{SET}	See Table 1 Voltage Setting Table.	

Layout Guidelines

Good PCB layout is the key factor for high performance operation of a switching power supply regarding stability, regulation, efficiency, and other performance measures.

A list of guidelines for designing a PCB layout for SGM6040 series is provided below:

- Place the power components close together and connect them with short and wide routes.
- Minimize the area of the SW node and connect it to the inductor with a short and wide trace on the top layer. Keep sensitive analog traces away from this node and inductor.
- Connect the VOS pin to the output capacitor and keep VOS line away from noise sources (such as SW node).

Typical suggested layout is provided in Figure 5.

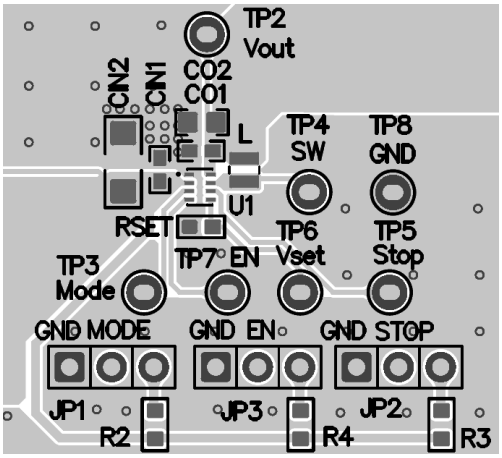


Figure 5. PCB Layout Example

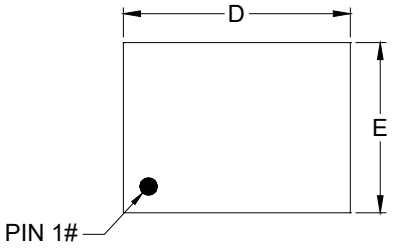
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

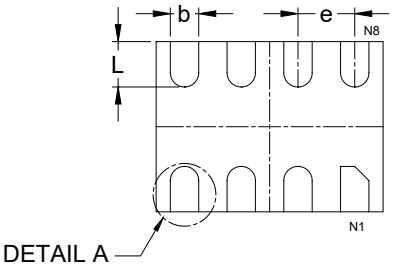
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

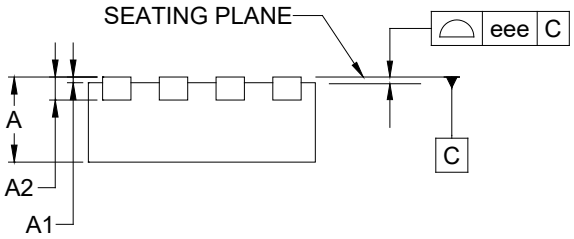
TDFN-2×1.5-8L



TOP VIEW

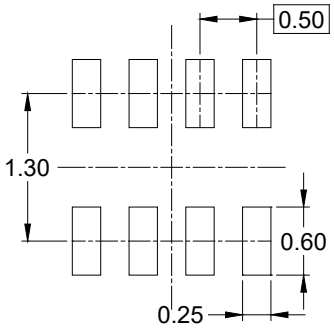


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



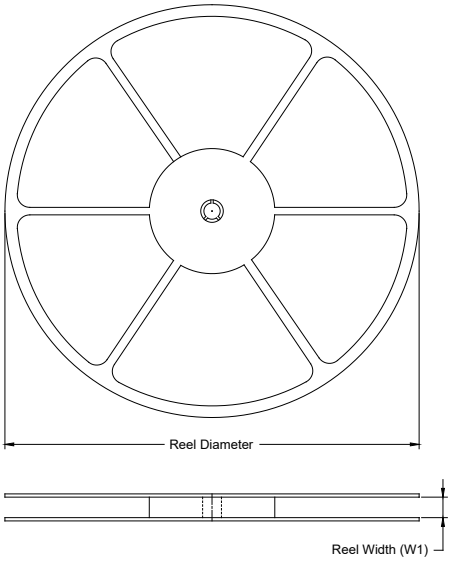
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	1.900	-	2.100
E	1.400	-	1.600
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

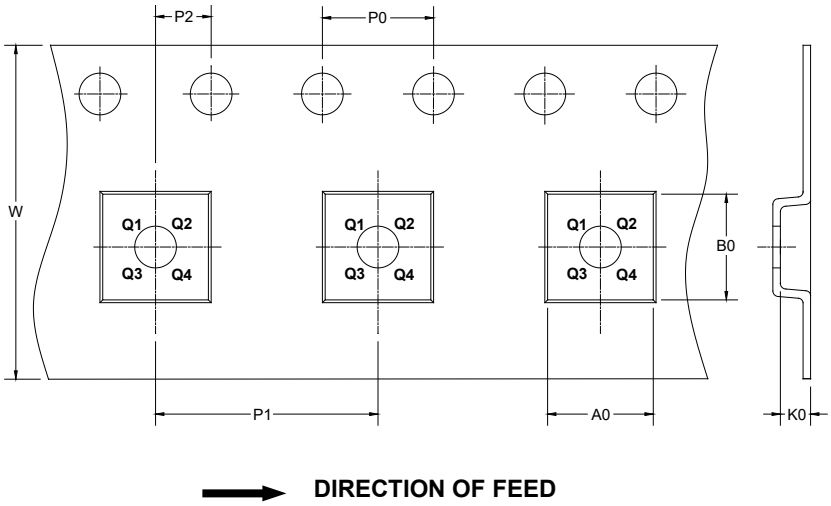
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

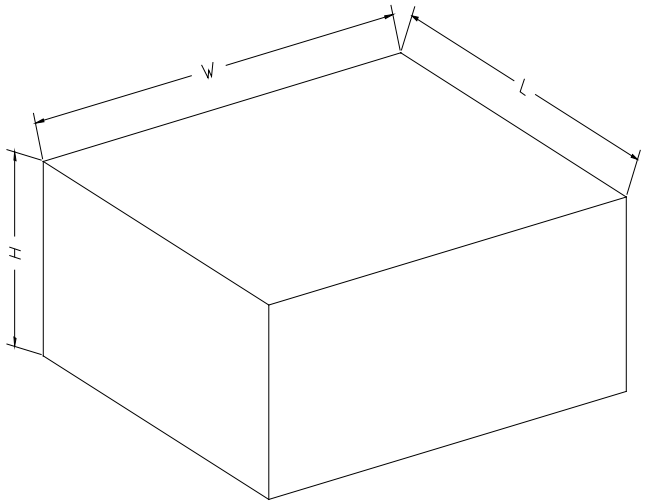
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×1.5-8L	7"	9.5	1.70	2.20	0.90	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002