74AUP1G74
Low Power Single D-Type Positive Edge-Triggered Flip-Flop with Clear and Preset

GENERAL DESCRIPTION

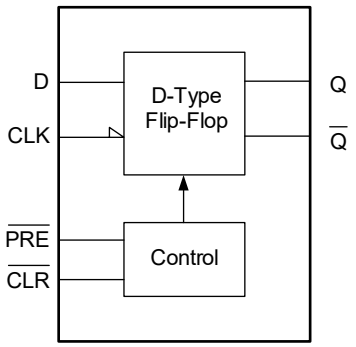
The 74AUP1G74 is a low power single positive edge-triggered D-Type flip-flop with clear and preset functions. This device can operate in the supply voltage range from 0.8V to 3.6V.

No matter what the levels of the other inputs are, the preset ($\overline{PRE}$) input or clear ($\overline{CLR}$) input can be pulled low to set or reset the outputs. When the preset input and clear input are held high, data at the D input that suffices for setup time purposes is moved to the Q output on the low-to-high clock transition. After the hold time interval, data at the D input can be changed without any influence on output levels. Clock triggering appears at a voltage level which is uncorrelated with the rise time of the clock pulse.

This device is highly suitable for partial power-down applications using power-off leakage current (I_{OFF}) circuit.

The 74AUP1G74 is available in a Green VSSOP-8 package. It operates over an ambient temperature range of -40℃ to +125℃.

LOGIC DIAGRAM



FEATURES

- **Wide Supply Voltage Range: 0.8V to 3.6V**
- **Inputs Accept Voltages Higher than the Supply Voltage**
- **+4mA/-4mA Output Current**
- **Low Static Power Dissipation: I_{CC} = 1μA (MAX)**
- **Low Dynamic Power Dissipation: C_{PD} = 5.5pF (TYP) at V_{CC} = 3.3V**
- **Input Capacitance: C_I = 4pF (TYP)**
- **Propagation Delay: t_{PD} = 9ns (MAX) at V_{CC} = 3.3V**
- **The Overshoot and Undershoot of Low Noise are Less than 10% of V_{CC}**
- **Applicable to Point-to-Point**
- **Latch-up Performance (> 100mA) Meets JESD 78 Class II Standard**
- **Outputs in High-Impedance State when V_{CC} = 0V**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green VSSOP-8 Package**

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	*X*	*X*	H	L
X	L	*X*	*X*	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	*X*	Q_0	$\overline{Q}_0$

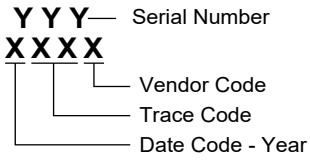
H = High Voltage Level
L = Low Voltage Level
↑ = Low-to-High Clock Transition
X = Don't Care

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AUP1G74	VSSOP-8	-40℃ to +125℃	74AUP1G74XVS8G/TR	0GU XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CC} ..... -0.5V to 4.6V
Input Voltage Range, V_I (2) ..... -0.5V to 4.6V
Output Voltage Range, V_O (2)
High State or Low State ..... -0.5V to MIN(4.6V, V_{CC} + 0.5V)
High-Impedance or Power-Off State ..... -0.5V to 4.6V
Input Clamp Current, I_{IK} (V_I < 0V) .....-50mA
Output Clamp Current, I_{OK} (V_O < 0V) .....-50mA
Continuous Output Current, I_O .....±20mA
Continuous Current through V_{CC} or GND.....±50mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} .....0.8V to 3.6V
Input Voltage Range, V_I (4) .....0V to 3.6V
Output Voltage Range, V_O
High State or Low State ..... 0V to V_{CC}
High-Impedance or Power-Off State .....0V to 3.6V
Output Current, I_O .....±4mA
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 0.8V to 3.6V ..... 200ns/V (MAX)
Operating Temperature Range .....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

4. Unused input pins must be held at V_{CC} or GND to guarantee the device in normal operation.

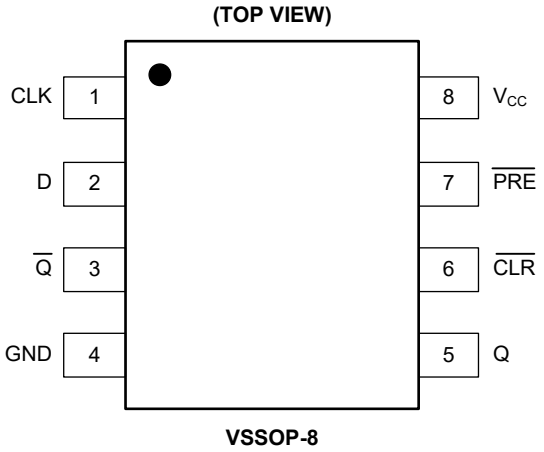
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	CLK	Clock Input (Low-to-High Clock Transition, Edge-Triggered).
2	D	Data Input.
3	$\overline{Q}$	Complementary Output.
4	GND	Ground.
5	Q	Output.
6	$\overline{CLR}$	Clear Input (Active-Low).
7	$\overline{PRE}$	Preset Input (Active-Low).
8	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 0.8V	Full	V_{CC}			V
		V_{CC} = 1.1V to 1.95V	Full	0.7 × V_{CC}			
		V_{CC} = 2.3V to 2.7V	Full	1.6			
		V_{CC} = 3.0V to 3.6V	Full	2.0			
Low-Level Input Voltage	V_{IL}	V_{CC} = 0.8V	Full			0	V
		V_{CC} = 1.1V to 1.95V	Full			0.3 × V_{CC}	
		V_{CC} = 2.3V to 2.7V	Full			0.7	
		V_{CC} = 3.0V to 3.6V	Full			0.9	
High-Level Output Voltage	V_{OH}	V_{CC} = 0.8V to 3.6V, I_{OH} = -20μA	Full	V_{CC} - 0.05	V_{CC} - 0.005		V
		V_{CC} = 1.1V, I_{OH} = -1.1mA	Full	0.77	0.96		
		V_{CC} = 1.4V, I_{OH} = -1.7mA	Full	1.05	1.24		
		V_{CC} = 1.65V, I_{OH} = -1.9mA	Full	1.30	1.50		
		V_{CC} = 2.3V, I_{OH} = -2.3mA	Full	2.0	2.15		
		V_{CC} = 2.3V, I_{OH} = -3.1mA	Full	1.85	2.09		
		V_{CC} = 3.0V, I_{OH} = -2.7mA	Full	2.70	2.84		
		V_{CC} = 3.0V, I_{OH} = -4.0mA	Full	2.55	2.76		
Low-Level Output Voltage	V_{OL}	V_{CC} = 0.8V to 3.6V, I_{OL} = 20μA	Full		0.005	0.05	V
		V_{CC} = 1.1V, I_{OL} = 1.1mA	Full		0.08	0.25	
		V_{CC} = 1.4V, I_{OL} = 1.7mA	Full		0.11	0.30	
		V_{CC} = 1.65V, I_{OL} = 1.9mA	Full		0.12	0.31	
		V_{CC} = 2.3V, I_{OL} = 2.3mA	Full		0.13	0.33	
		V_{CC} = 2.3V, I_{OL} = 3.1mA	Full		0.18	0.40	
		V_{CC} = 3.0V, I_{OL} = 2.7mA	Full		0.15	0.33	
		V_{CC} = 3.0V, I_{OL} = 4.0mA	Full		0.22	0.45	
Input Leakage Current	I_I	Data or control inputs, V_{CC} = 0V to 3.6V, V_I = GND to 3.6V	Full		±0.1	±1	μA
Power-Off Leakage Current	I_{OFF}	V_{CC} = 0V, V_I or V_O = 0V to 3.6V	Full		±0.1	±1	μA
Additional Power-Off Leakage Current	ΔI_{OFF}	V_{CC} = 0V to 0.2V, V_I or V_O = 0V to 3.6V	Full		±0.1	±1	μA
Supply Current	I_{CC}	V_{CC} = 0.8V to 3.6V, V_I = GND or V_{CC} to 3.6V, I_O = 0A	Full		0.1	1	μA
Additional Supply Current	ΔI_{CC}	One input at V_{CC} - 0.6V, other inputs at V_{CC} or GND, V_{CC} = 3.3V, V_I = V_{CC} - 0.6V, I_O = 0A	Full		1.6	20	μA
Input Capacitance	C_I	V_{CC} = 0V, V_I = V_{CC} or GND	+25℃		4		pF
		V_{CC} = 3.6V, V_I = V_{CC} or GND	+25℃		4		
Output Capacitance	C_O	V_{CC} = 0V, V_O = GND	+25℃		5		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, C_L = 30pF, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Clock Frequency	f_{CLOCK}	V_{CC} = 0.8V		+25℃		21		MHz
		V_{CC} = 1.2V ± 0.1V		Full			40	
		V_{CC} = 1.5V ± 0.1V		Full			50	
		V_{CC} = 1.8V ± 0.15V		Full			60	
		V_{CC} = 2.5V ± 0.2V		Full			90	
		V_{CC} = 3.3V ± 0.3V		Full			90	
Hold Time, Data after CLK ↑	t_H	V_{CC} = 0.8V		+25℃		0		ns
		V_{CC} = 1.2V ± 0.1V		Full	2			
		V_{CC} = 1.5V ± 0.1V		Full	2			
		V_{CC} = 1.8V ± 0.15V		Full	1.5			
		V_{CC} = 2.5V ± 0.2V		Full	1.5			
		V_{CC} = 3.3V ± 0.3V		Full	1.5			
Pulse Duration	t_W	CLK high or low	V_{CC} = 0.8V	+25℃		10		ns
			V_{CC} = 1.2V ± 0.1V	Full	6			
			V_{CC} = 1.5V ± 0.1V	Full	5.5			
			V_{CC} = 1.8V ± 0.15V	Full	5			
			V_{CC} = 2.5V ± 0.2V	Full	4.5			
			V_{CC} = 3.3V ± 0.3V	Full	4.5			
		$\overline{PRE}$ or $\overline{CLR}$ low	V_{CC} = 0.8V	+25℃		10		ns
			V_{CC} = 1.2V ± 0.1V	Full	6			
			V_{CC} = 1.5V ± 0.1V	Full	5.5			
			V_{CC} = 1.8V ± 0.15V	Full	5.5			
			V_{CC} = 2.5V ± 0.2V	Full	5			
			V_{CC} = 3.3V ± 0.3V	Full	4.5			
Setup Time before CLK ↑	t_{SU}	Data high	V_{CC} = 0.8V	+25℃		4		ns
			V_{CC} = 1.2V ± 0.1V	Full	2			
			V_{CC} = 1.5V ± 0.1V	Full	2			
			V_{CC} = 1.8V ± 0.15V	Full	2			
			V_{CC} = 2.5V ± 0.2V	Full	1.5			
			V_{CC} = 3.3V ± 0.3V	Full	1.5			
		Data low	V_{CC} = 0.8V	+25℃		5		ns
			V_{CC} = 1.2V ± 0.1V	Full	5			
			V_{CC} = 1.5V ± 0.1V	Full	4			
			V_{CC} = 1.8V ± 0.15V	Full	3			
			V_{CC} = 2.5V ± 0.2V	Full	3			
			V_{CC} = 3.3V ± 0.3V	Full	3			

DYNAMIC CHARACTERISTICS (continued)

(See Figure 1 for test circuit. Full = -40℃ to +125℃, C_L = 30pF, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Setup Time before CLK ↑	t_{SU}	$\overline{PRE}$ or $\overline{CLR}$ inactive	V_{CC} = 0.8V	+25℃		1.5		ns
			V_{CC} = 1.2V ± 0.1V	Full	1.5			
			V_{CC} = 1.5V ± 0.1V	Full	1.5			
			V_{CC} = 1.8V ± 0.15V	Full	1.5			
			V_{CC} = 2.5V ± 0.2V	Full	1.5			
			V_{CC} = 3.3V ± 0.3V	Full	1.5			
Propagation Delay (2)	t_{PD}	CLK to Q	V_{CC} = 0.8V	+25℃		51		ns
			V_{CC} = 1.2V ± 0.1V	Full	5	16.5	27	
			V_{CC} = 1.5V ± 0.1V	Full	2.5	10	17.5	
			V_{CC} = 1.8V ± 0.15V	Full	1.5	8	14	
			V_{CC} = 2.5V ± 0.2V	Full	0.5	4.5	9.5	
			V_{CC} = 3.3V ± 0.3V	Full	0.5	3.5	9	
		CLK to $\overline{Q}$	V_{CC} = 0.8V	+25℃		53		ns
			V_{CC} = 1.2V ± 0.1V	Full	6	17	26	
			V_{CC} = 1.5V ± 0.1V	Full	2.5	7	17	
			V_{CC} = 1.8V ± 0.15V	Full	1.5	6	13.5	
			V_{CC} = 2.5V ± 0.2V	Full	0.8	5	9.5	
			V_{CC} = 3.3V ± 0.3V	Full	0.5	4	9	
		$\overline{PRE}$ or $\overline{CLR}$ to Q or $\overline{Q}$	V_{CC} = 0.8V	+25℃		55		ns
			V_{CC} = 1.2V ± 0.1V	Full	3	17.5	27	
			V_{CC} = 1.5V ± 0.1V	Full	3	11.5	17.5	
			V_{CC} = 1.8V ± 0.15V	Full	2	7.5	14	
			V_{CC} = 2.5V ± 0.2V	Full	1	5.5	10	
			V_{CC} = 3.3V ± 0.3V	Full	0.5	4.5	9	
Power Dissipation Capacitance (3)	C_{PD}	f = 10MHz	V_{CC} = 0.8V	+25℃		5.5		pF
			V_{CC} = 1.2V ± 0.1V	+25℃		5.5		
			V_{CC} = 1.5V ± 0.1V	+25℃		5.5		
			V_{CC} = 1.8V ± 0.15V	+25℃		5.5		
			V_{CC} = 2.5V ± 0.2V	+25℃		5.5		
			V_{CC} = 3.3V ± 0.3V	+25℃		5.5		

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

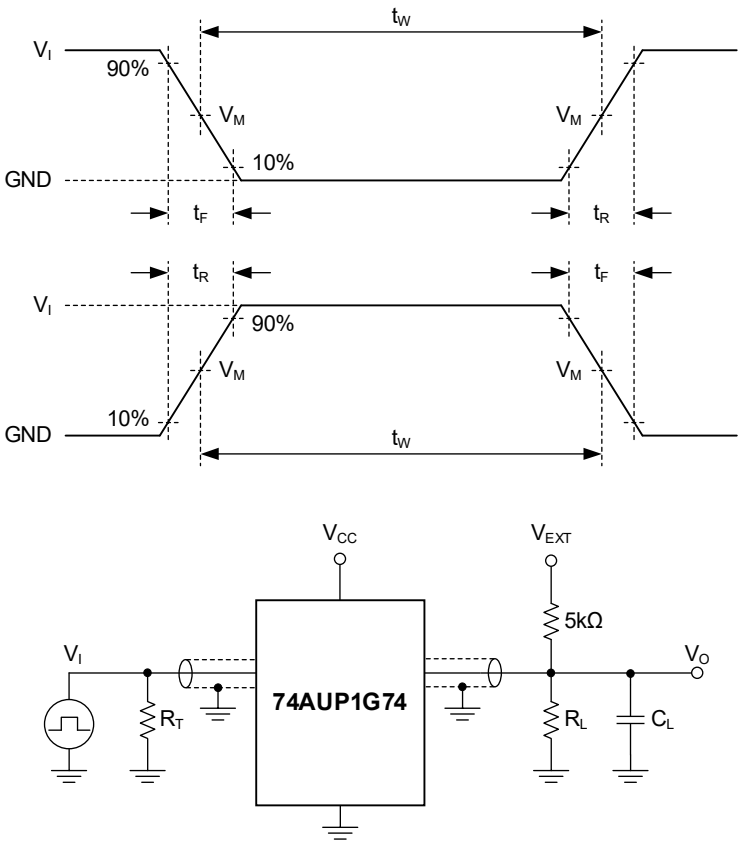
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (including jig and probe).

R_T: Termination resistance (equal to output impedance Z_O of the pulse generator).

V_{EXT}: External voltage is used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

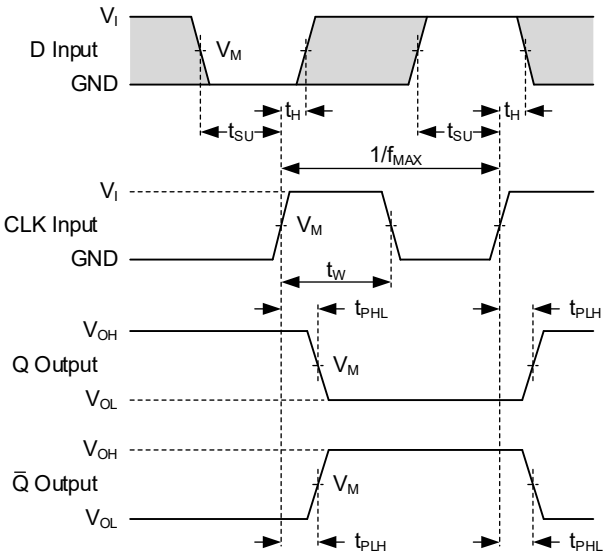
Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		V_{EXT}		
V_{CC}	V_I	t_R, t_F	C_L	R_L (1) (2)	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
0.8V to 3.6V	V_{CC}	≤ 3.0ns	30pF	5kΩ, 1MΩ	GND	2 × V_{CC}	Open

NOTES:

1. R_L = 5kΩ is used to measure enable and disable times.
2. R_L = 1MΩ is used to measure propagation delays, setup and hold times and pulse width.

WAVEFORMS



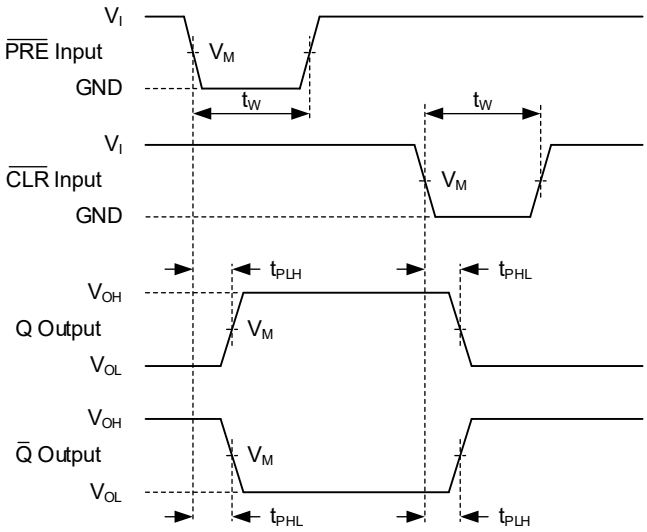
Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas refer to when the input is allowed to change for predictable output performance.

Figure 2. The Clock Input to Output Propagation Delays, Clock Pulse Width, the D to CLK Setup, the CLK to D Hold Times and the Maximum Frequency



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. The $\overline{PRE}$ and $\overline{CLR}$ Input to Output Propagation Delays and Pulse Width

WAVEFORMS (continued)

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
0.8V to 3.6V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.

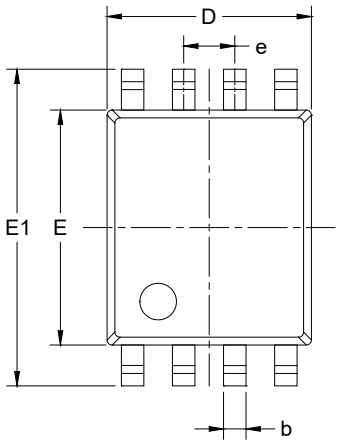
REVISION HISTORY

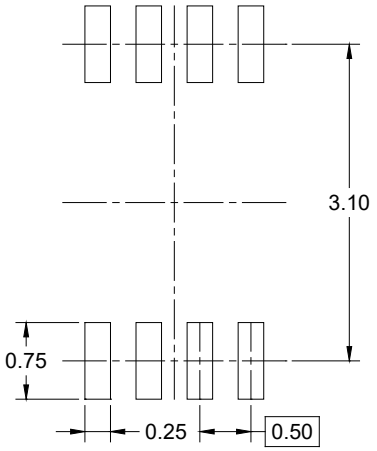
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

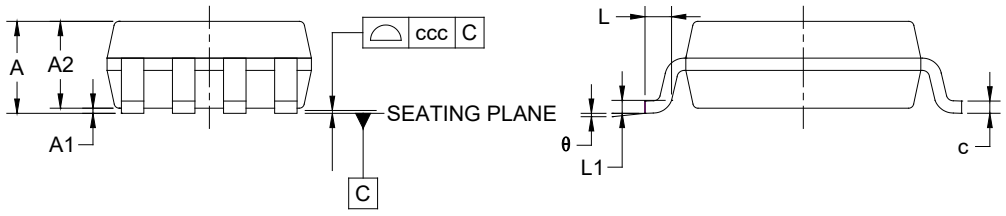
PACKAGE OUTLINE DIMENSIONS

VSSOP-8





RECOMMENDED LAND PATTERN (Unit: mm)

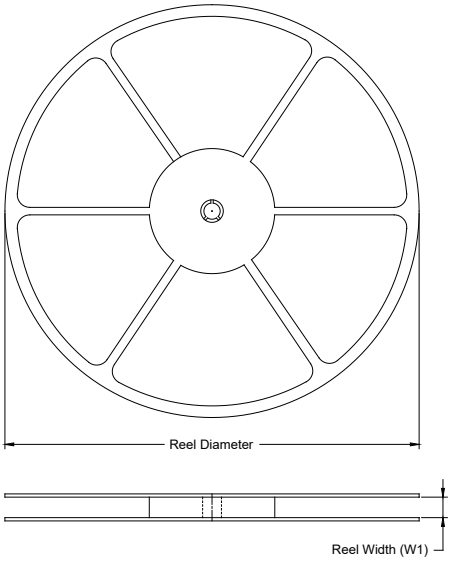


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.000
A1	0.000	-	0.150
A2	0.600		0.850
b	0.170	-	0.270
c	0.080		0.230
D	1.900	-	2.100
E	2.200	-	2.400
E1	3.000	-	3.200
e	0.500 BSC		
L	0.150	-	0.400
L1	0.120 BSC		
θ	0°	-	8°
ccc	0.100		

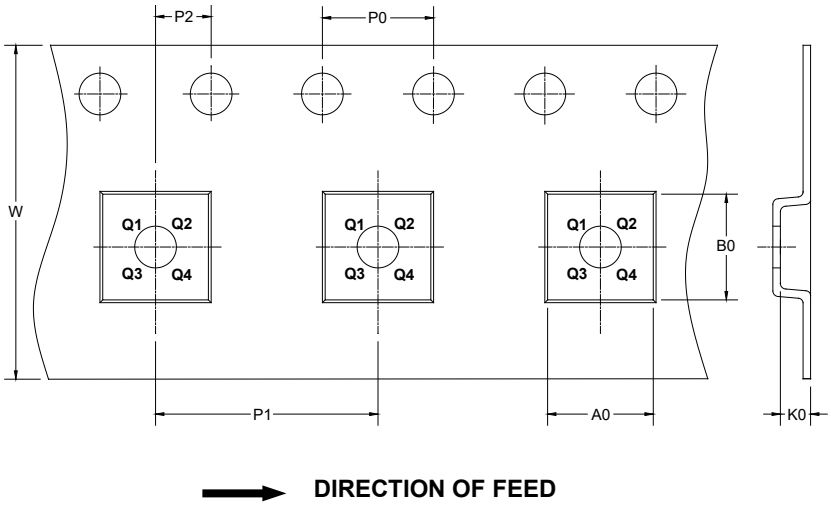
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187 CA.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



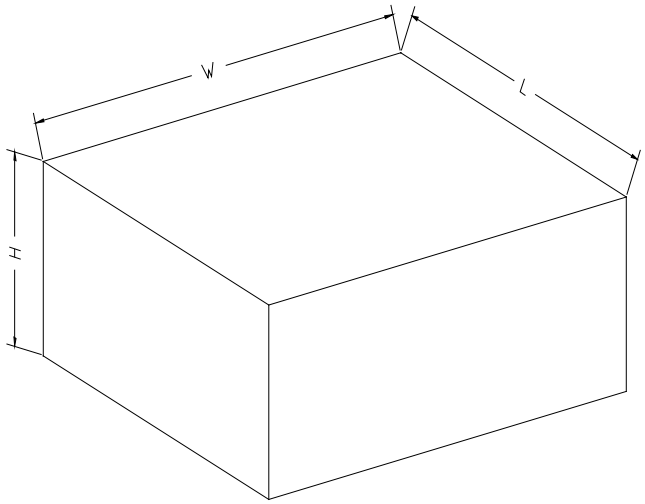
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP-8	7″	9.5	2.25	3.35	1.05	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002