SGM61308
4V to 38V Input, 600mA Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61308 is a synchronous Buck DC/DC converter with a wide 4V to 38V input voltage range and 600mA output current capability. This device accommodates various industrial applications powered from unregulated sources.

The SGM61308A operates in pulse skip modulation (PSM) mode at light load to boost light load efficiency, while the SGM61308B operates in forced pulse width modulation (FPWM) mode over the full load range to maintain constant frequency and reduce output voltage ripple.

The internal soft-start and loop compensation simplify the external components design and save users time and cost.

Protection features include current limit, hiccup mode short-circuit protection, thermal shutdown with auto recovery and output over-voltage protection.

The SGM61308 is available in a Green SOT-23-6 package.

APPLICATIONS

Motor Drive: AC Inverters, VF Drives, Servos, Field Actuators
Factory and Building Automation: PLC, Industrial PC, Elevator Control, HVAC Control
Aftermarket Automotive: Camera
General Purpose Wide V_{IN} Power Supplies

FEATURES

- **Wide 4V to 38V Input Voltage Range**
- **Up to 600mA Continuous Output Current**
- **Minimum Switching-On Time: 80ns**
- **1.1MHz Switching Frequency**
- **98% Maximum Duty Cycle**
- **Monotonic Startup with Pre-Biased Output**
- **Short-Circuit Protection with Hiccup Mode**
- **Precision Enable**
- **Integrated Synchronous Rectification**
- **Internal Compensation and Soft-Start**
- **SGM61308A: PSM at Light Load Condition**
- **SGM61308B: FPWM at Light Load Condition**
- **Available in a Green SOT-23-6 Package**

TYPICAL APPLICATION

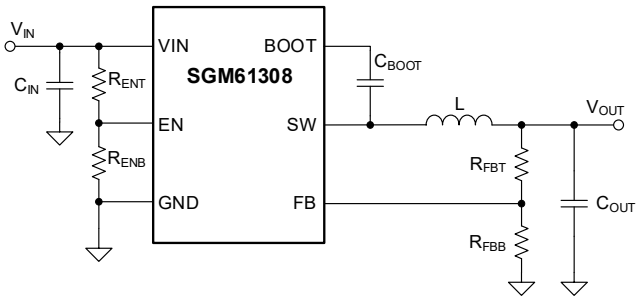


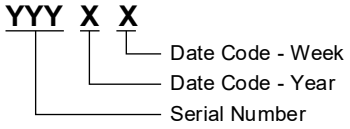
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61308A	SOT-23-6	-40℃ to +125℃	SGM61308AXN6G/TR	0IEXX	Tape and Reel, 3000
SGM61308B	SOT-23-6	-40℃ to +125℃	SGM61308BXN6G/TR	0IFXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltages:
- VIN to GND ..... -0.3V to 42V
- EN to GND ..... -0.3V to (V_{IN} + 0.3V)
- FB to GND ..... -0.3V to 5.5V

Output Voltages:
- SW to GND ..... -0.3V to (V_{IN} + 0.3V)
- SW to GND (Less than 10ns Transient)..... -3.5V to 42V
- BOOT to SW ..... -0.3V to 5.5V

Package Thermal Resistance
- SOT-23-6, θ_{JA} ..... 129.3℃/W

Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM.....2500V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltages:
- VIN to GND .....4V to 38V
- EN..... 0V to V_{IN}
- FB .....0V to 4.5V

Output Voltage Range, V_{OUT} .....0.8V to (95% of V_{IN})
Output Current Range, I_{OUT} .....0mA to 600mA
Operating Junction Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

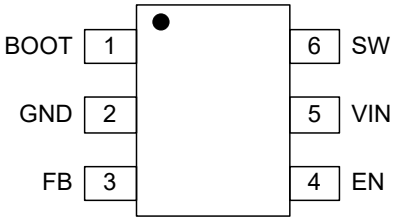
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



SOT-23-6

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	BOOT	O	Bootstrap Pin. BOOT pin is used to provide a drive voltage higher than the input voltage to the high-side power switch. Place a 0.1μF bootstrap capacitor (C_{BOOT}) as close as possible to the IC between this pin and SW pin.
2	GND	G	Ground Pin. It is the reference for input and the regulated output voltages. Special layout considerations are required.
3	FB	I	Feedback Input. Feedback pin for programming the output voltage. Connect a feedback resistor divider tap to this pin.
4	EN	I	Precision Enable Input. The device is enabled if the voltage on this pin exceeds the 1.23V rising threshold. It can be used to program the UVLO with a resistor divider on the VIN pin. Do not leave this pin floating.
5	VIN	P	Power Supply Input Pin. This pin is connected to the input supply voltage and powers the internal control circuitry. VIN voltage is monitored by a UVLO lockout comparator. Due to power switching, this pin has high di/dt transition edges and must be decoupled to the GND by input capacitors as close as possible to the GND pin to minimize the parasitic inductances.
6	SW	P	Switching Node Output. Switching node of the internal power converter and should be connected to the output inductor and bootstrap capacitor. This node should be kept small on the PCB to minimize capacitive coupling, noise coupling and radiation.

NOTE: I = input, O = output, G = ground, P = power.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 4V to 38V, typical values are at T_J = +25℃, unless otherwise noted.)

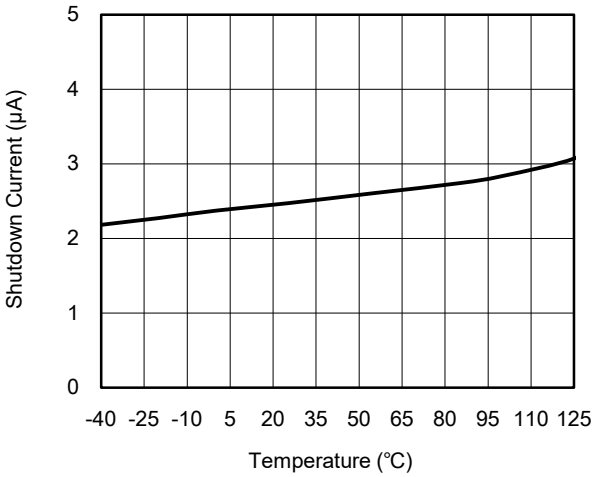
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (VIN Pin)							
Input Voltage Range	V_{IN}			4		38	V
Under-Voltage Lockout Thresholds	V_{IN_UVLO}	Rising threshold		3.55	3.75	3.95	V
		Falling threshold		3.2	3.4	3.6	
Under-Voltage Lockout Hysteresis	V_{IN_HYS}	Hysteresis			0.35		V
Operating Quiescent Current	I_Q	V_{EN} = 3.3V, V_{FB} = 1.1V	SGM61308A only		77	100	μA
			SGM61308B only		1750	1900	
Shutdown Current into VIN	I_{SD}	V_{EN} = 0V			3	5	μA
Enable (EN Pin)							
Enable Rising Threshold Voltage	V_{EN_H}			1.10	1.23	1.30	V
Enable Falling Threshold Voltage	V_{EN_L}			1.00	1.10	1.18	V
Enable Hysteresis Voltage	V_{EN_HYS}				0.13		V
Input Leakage Current at EN Pin	I_{EN}	V_{EN} = 3.3V			5	150	nA
Voltage Reference (FB Pin)							
Reference Voltage	V_{REF}	T_J = +25℃		0.775	0.800	0.825	V
Input Leakage Current at FB Pin	I_{LKG_FB}	V_{FB} = 1.2V			1	50	nA
Current Limits and Hiccup							
Peak Inductor Current Limit	I_{HS_LIMIT}			1.00	1.24	1.48	A
Valley Inductor Current Limit	I_{LS_LIMIT}			0.58	0.78	0.98	A
Zero Cross Current (PSM Version)	I_{LS_ZC}	SGM61308A only			40		mA
Negative Current Limit (FPWM Version)	I_{LS_NEG}	SGM61308B only		-0.70	-0.50	-0.30	A
Hiccup Threshold of FB Pin	V_{HICCUP}	% of reference voltage			30%		
Integrated MOSFETs							
High-side MOSFET On-Resistance	R_{DSON_HS}	T_J = +25℃, V_{IN} = 12V			500		mΩ
Low-side MOSFET On-Resistance	R_{DSON_LS}	T_J = +25℃, V_{IN} = 12V			320		mΩ
Thermal Shutdown (1)							
Thermal Shutdown Threshold	T_{SD}				170		℃
Thermal Shutdown Hysteresis	T_{HYS}				20		℃
Soft-Start (1)							
Internal Soft-Start Time	t_{SS}	The time of V_{OUT} to rise from 0% to 100%, V_{IN} = 12V, no load			1.8		ms
Hiccup (1)							
Hiccup Time	t_{HICCUP}	V_{IN} = 12V			135		ms
Switching Node (SW Pin) (1)							
Minimum Turn-On Time	t_{ON_MIN}	I_{OUT} = 600mA			80		ns
Minimum Turn-Off Time	t_{OFF_MIN}	I_{OUT} = 600mA			120		ns
Maximum Turn-On Time	t_{ON_MAX}				5.6		μs
Oscillator							
Oscillator Frequency	f_{SW}			0.8	1.1	1.4	MHz

NOTE: 1. Guaranteed by design.

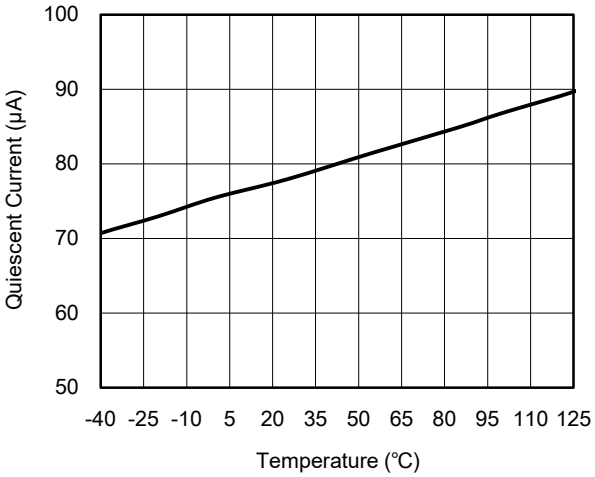
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 18μH, C_{OUT} = 22μF, unless otherwise noted.

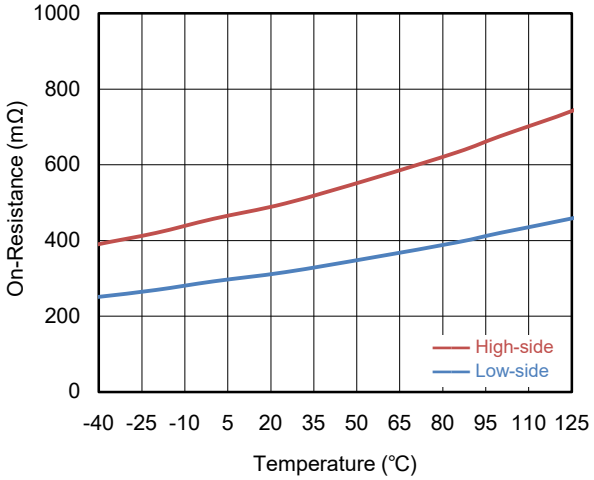
SGM61308A Shutdown Current vs. Temperature



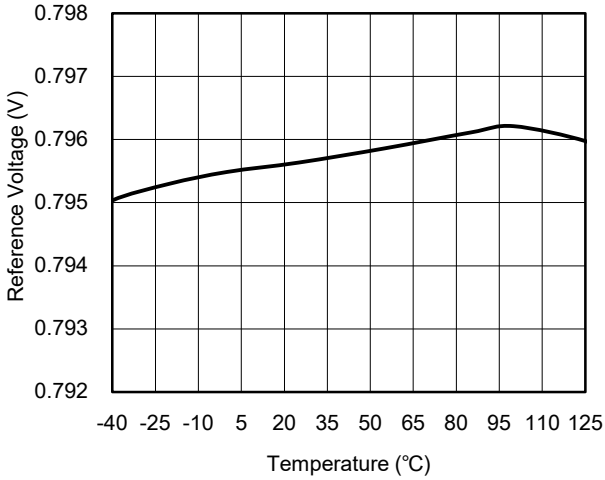
SGM61308A Quiescent Current vs. Temperature



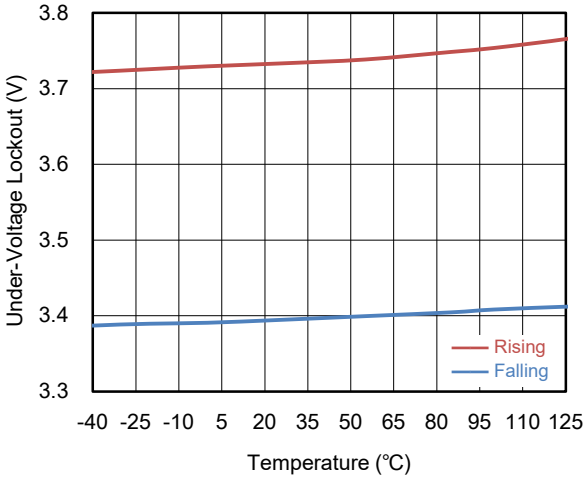
SGM61308A On-Resistance vs. Temperature



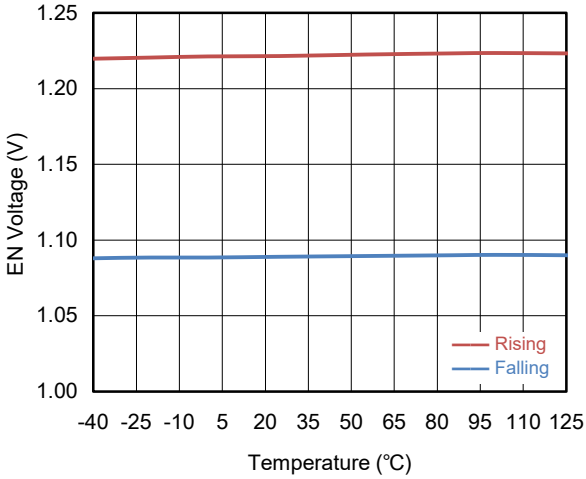
SGM61308A Reference Voltage vs. Temperature



SGM61308A Under-Voltage Lockout vs. Temperature



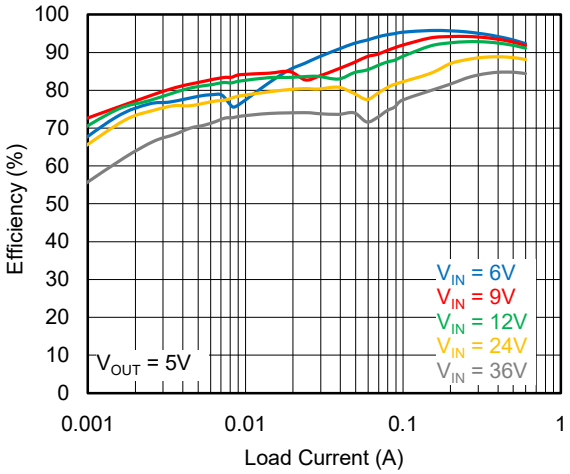
SGM61308A Enable Voltage vs. Temperature



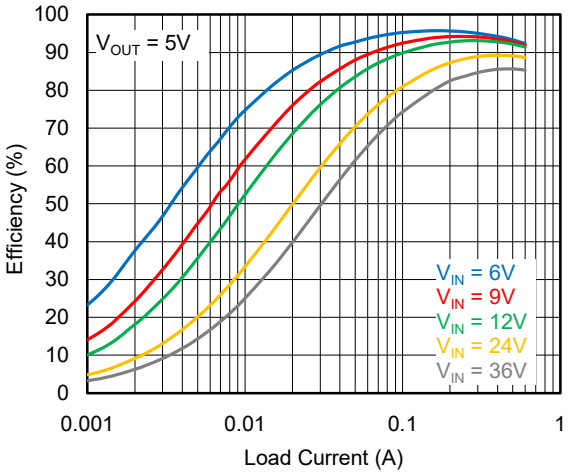
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 18μH, C_{OUT} = 22μF, unless otherwise noted.

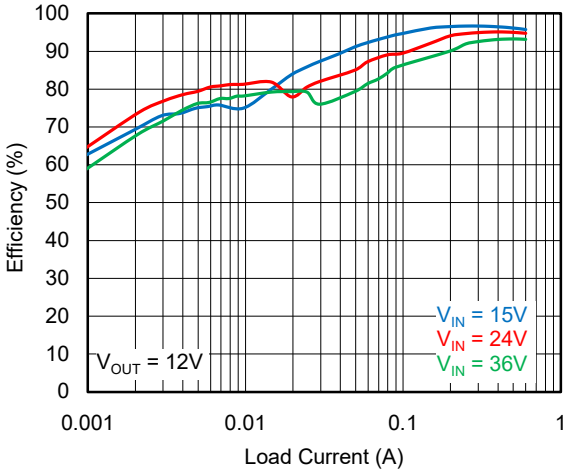
SGM61308A Efficiency vs. Load Current



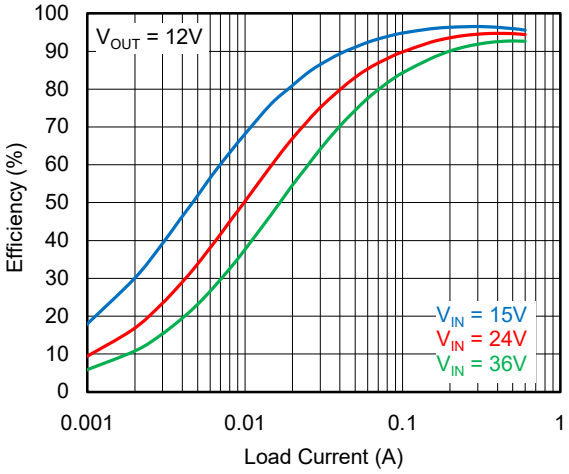
SGM61308B Efficiency vs. Load Current



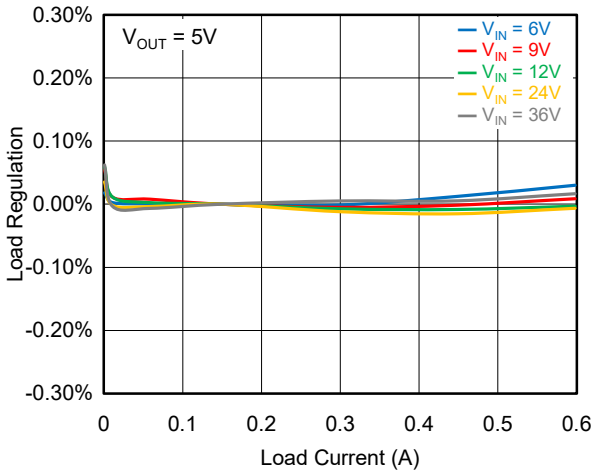
SGM61308A Efficiency vs. Load Current



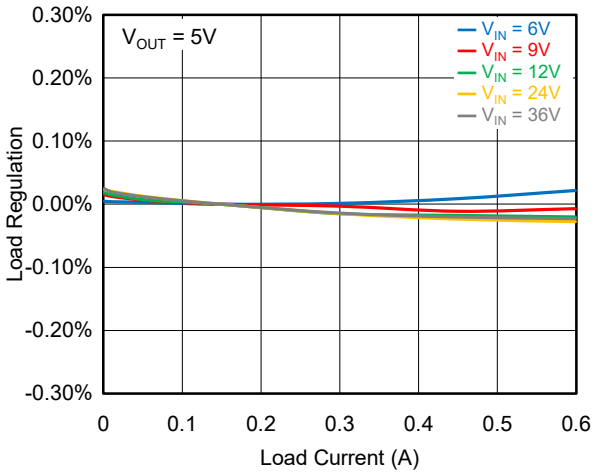
SGM61308B Efficiency vs. Load Current



SGM61308A Load Regulation



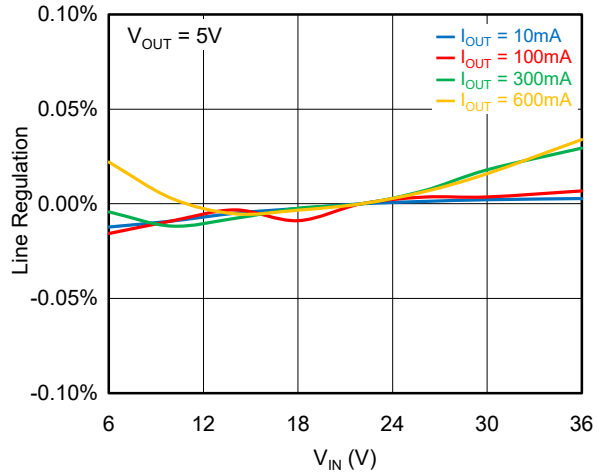
SGM61308B Load Regulation



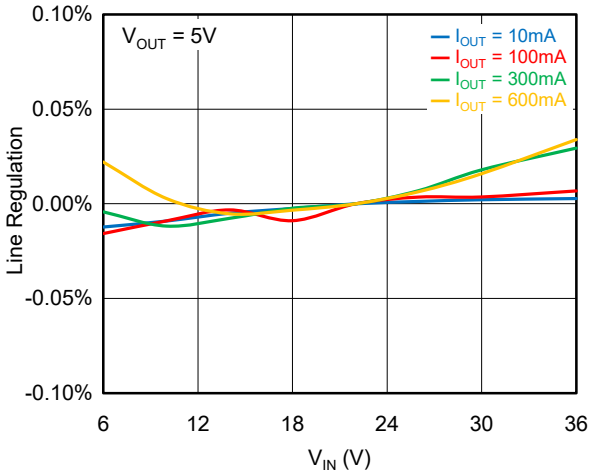
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 18μH, C_{OUT} = 22μF, unless otherwise noted.

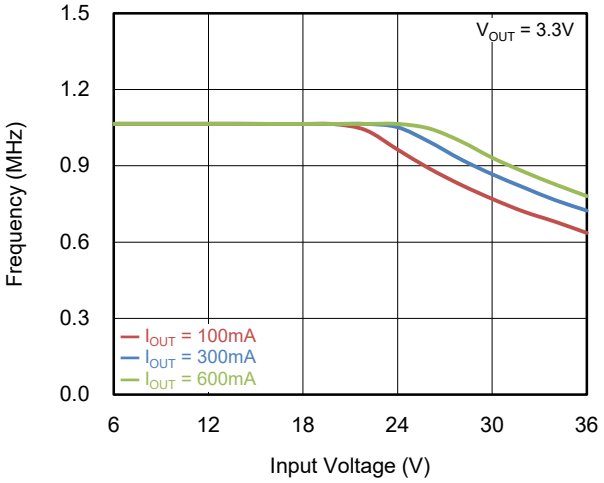
SGM61308A Line Regulation



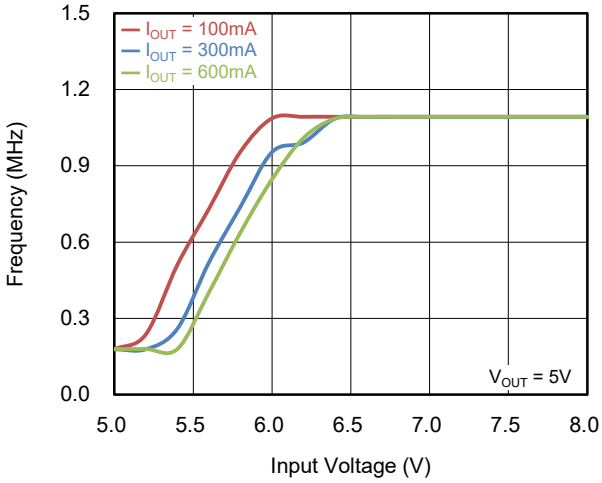
SGM61308B Line Regulation



Frequency Foldback at T_{ON_MIN}



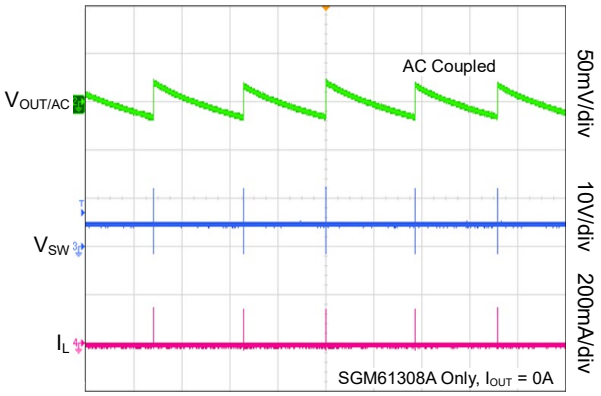
Frequency Foldback at T_{OFF_MIN}



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

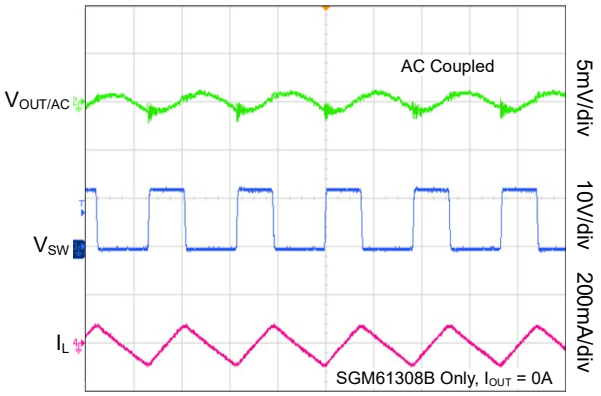
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 18μH, C_{OUT} = 22μF, unless otherwise noted.

Output Voltage Ripple



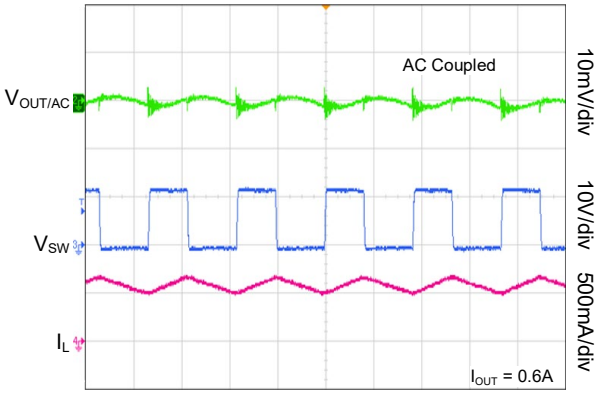
Time (5ms/div)

Output Voltage Ripple



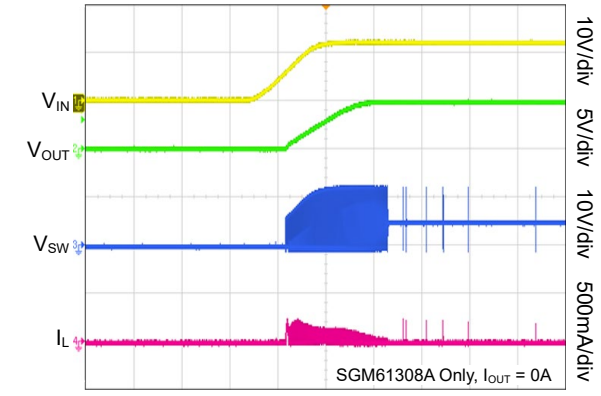
Time (500ns/div)

Output Voltage Ripple



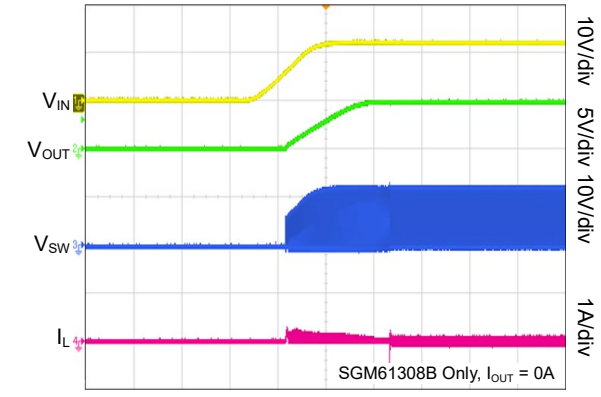
Time (500ns/div)

VIN Startup



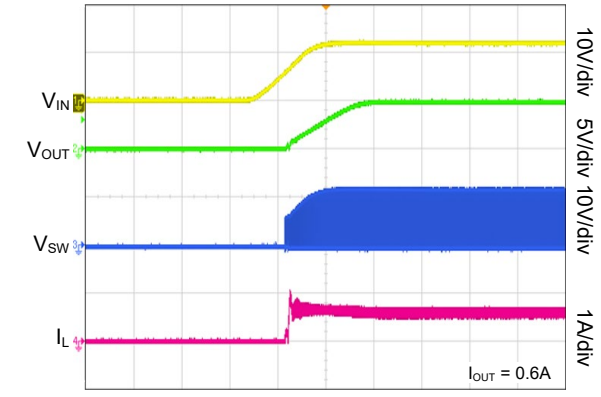
Time (1ms/div)

VIN Startup



Time (1ms/div)

VIN Startup

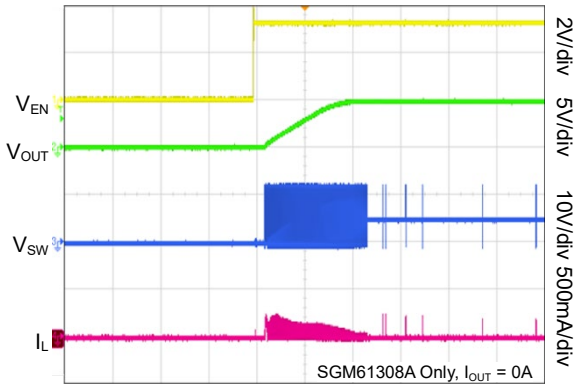


Time (1ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

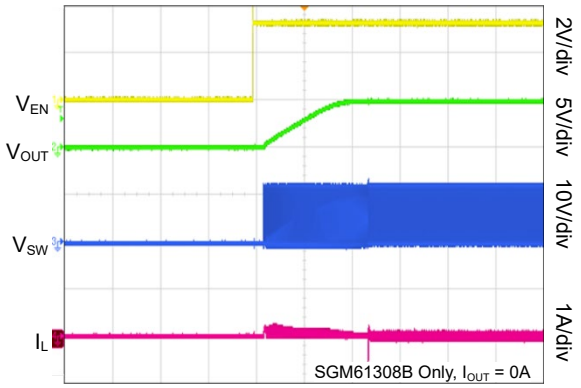
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 18μH, C_{OUT} = 22μF, unless otherwise noted.

EN Startup



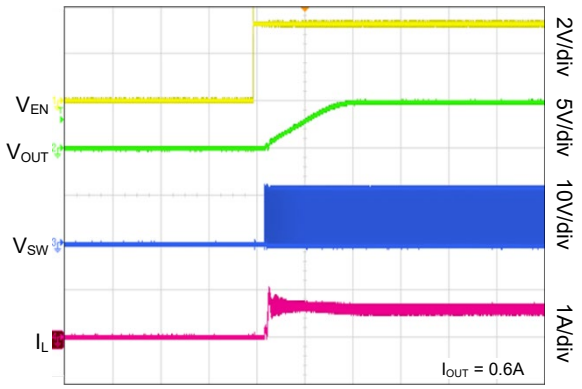
Time (1ms/div)

EN Startup



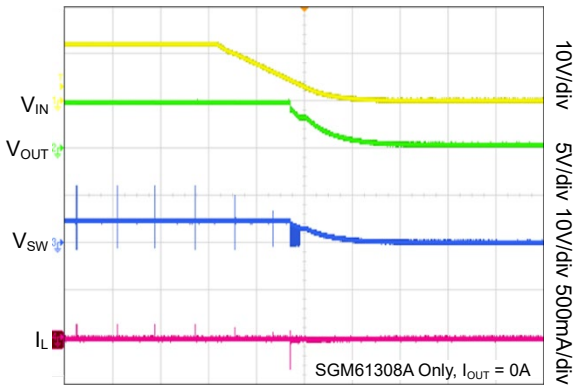
Time (1ms/div)

EN Startup



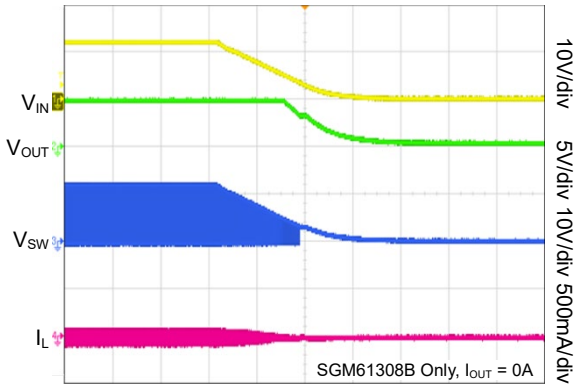
Time (1ms/div)

VIN Shutdown



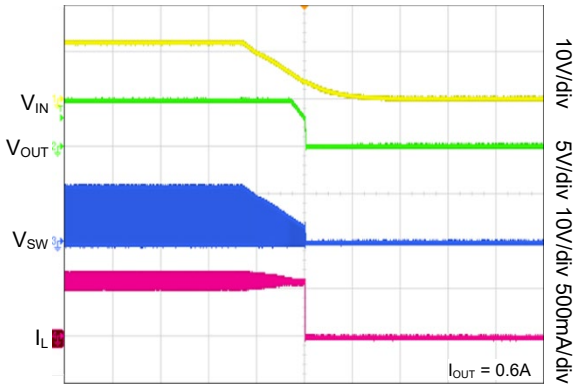
Time (10ms/div)

VIN Shutdown



Time (10ms/div)

VIN Shutdown

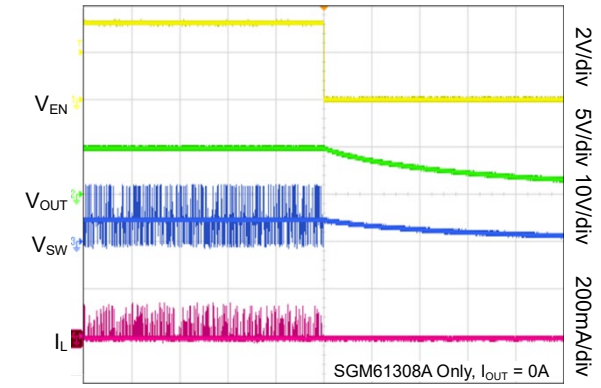


Time (10ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

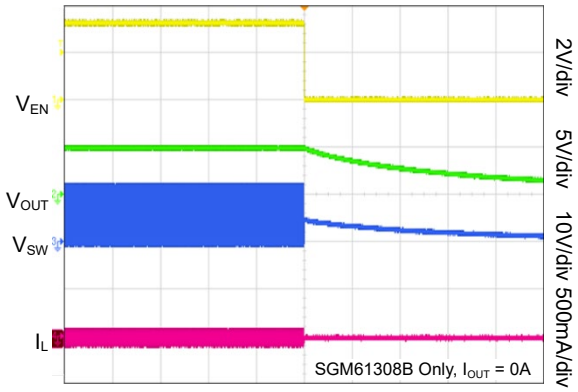
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 18μH, C_{OUT} = 22μF, unless otherwise noted.

EN Shutdown



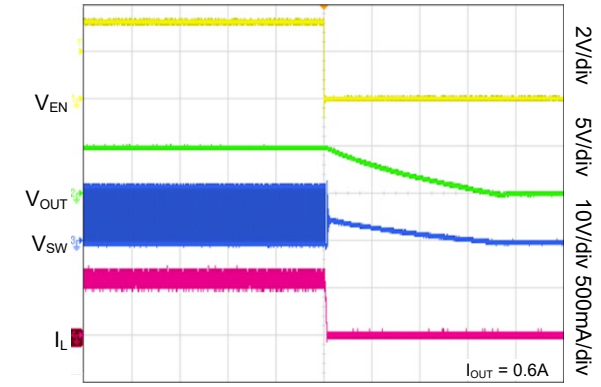
Time (500ms/div)

EN Shutdown



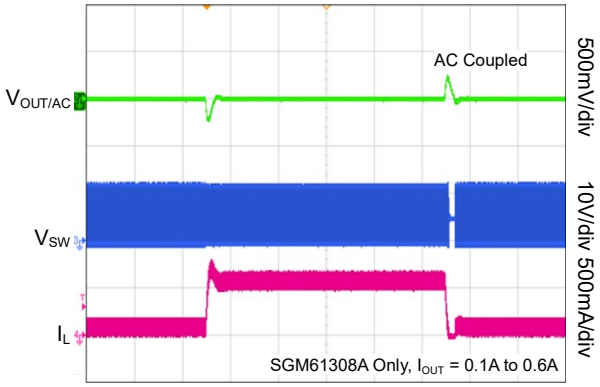
Time (500ms/div)

EN Shutdown



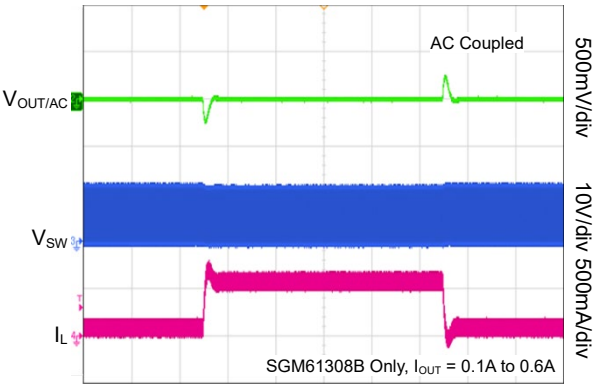
Time (50μs/div)

Load Transient



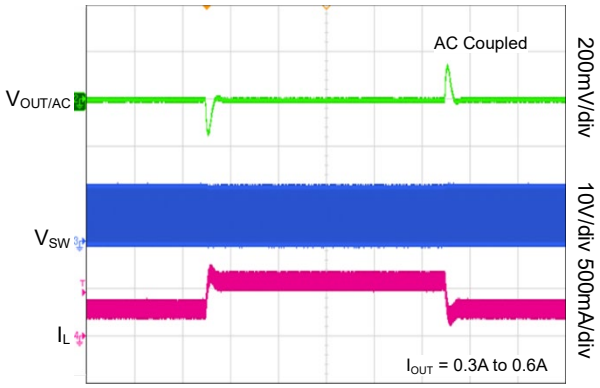
Time (200μs/div)

Load Transient



Time (200μs/div)

Load Transient

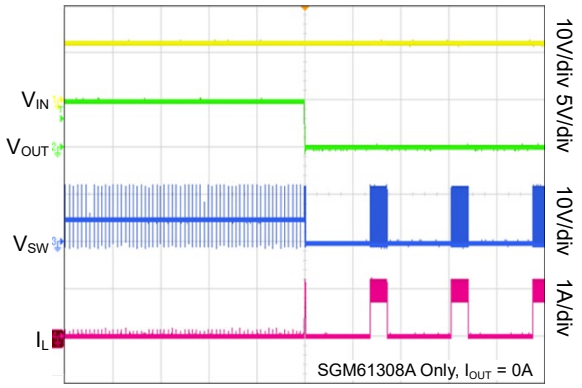


Time (200μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

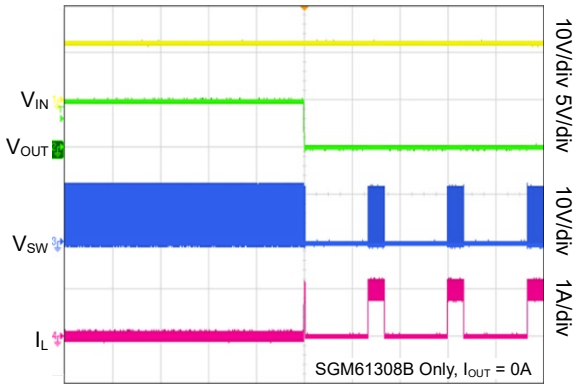
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 18μH, C_{OUT} = 22μF, unless otherwise noted.

Short-Circuit Entry



Time (100ms/div)

Short-Circuit Entry



Time (100ms/div)

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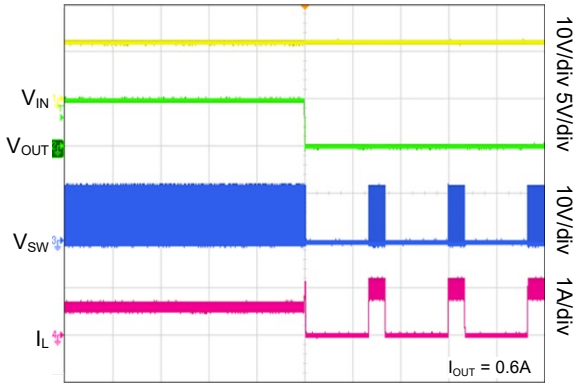
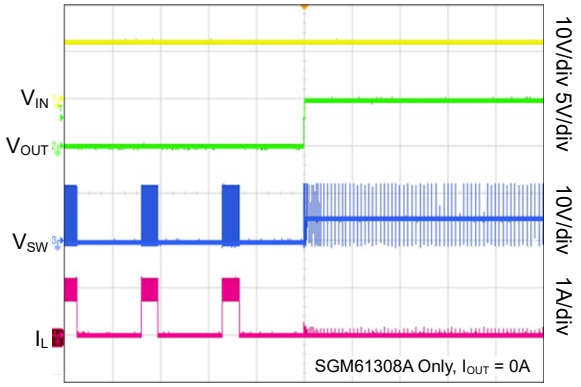


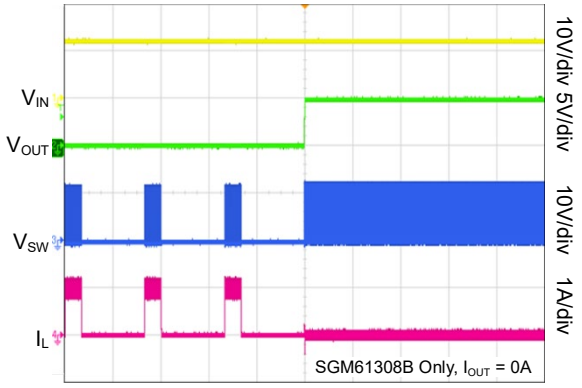
Time (100ms/div)

Short-Circuit Recovery



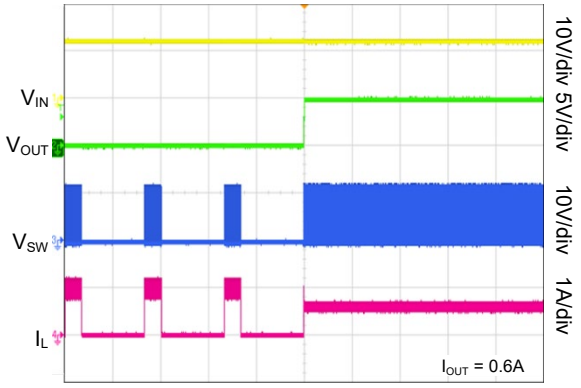
Time (100ms/div)

Short-Circuit Recovery



Time (100ms/div)

Short-Circuit Recovery



Time (100ms/div)

FUNCTIONAL BLOCK DIAGRAM

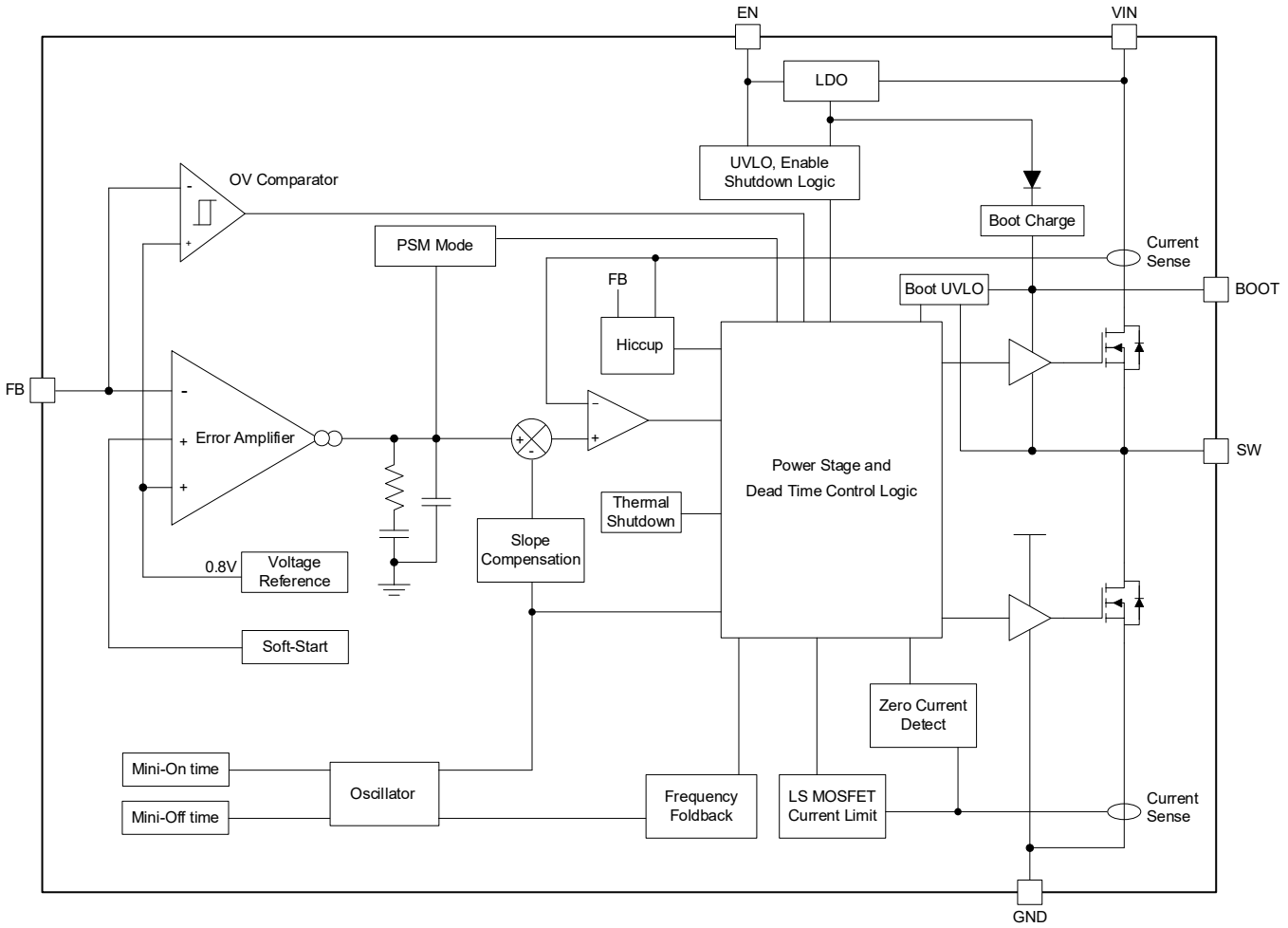


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61308 is an internally loop compensated synchronous Buck DC/DC converter, which simplifies compensation network design and saves users design time and cost. It can deliver up to 600mA to the output over a wide input voltage range from 4V to 38V.

The SGM61308 employs peak-current mode control with fixed-frequency in continuous conduction mode. SGM61308A features a power-save mode in which operating frequency is adaptively reduced under light load conditions to reduce switching and gate drive losses to keep high efficiency. SGM61308B operates in PWM mode over the full load range to maintain constant switching frequency and achieve low output voltage ripple.

The EN pin can achieve the precision enable, and can also be used to increase the input UVLO threshold by using a resistor divider.

An internal precision reference voltage and a fixed soft-start timer are included. Several protection features such as input under-voltage lockout, output over-voltage protection, hiccup mode short-circuit protection, current limit protection, and thermal shutdown are integrated to ensure safe operation.

Peak-Current Mode Control

Figure 2 shows the functional block diagram and Figure 3 shows the switching node operating waveforms of the SGM61308. Switching node voltage is generated by controlling the duty cycles of the complementary high-side and low-side switches. The duty cycle of the high-side switch is used as control parameter of the Buck converter to regulate output voltage and is defined as: $D = t_{ON}/t_{SW}$, where t_{ON} is the high-side switch on-time and t_{SW} is the switching period. During high-side switch on-time, the SW pin voltage swings up to approximate V_{IN}, and the inductor current, I_L, linearly rises with a slope of $(V_{IN} - V_{OUT})/L$. When control logic turns off the high-side switch, the low-side switch will be turned on after a short dead time. During off-time, inductor current discharges through the low-side switch with a slope of $(-V_{OUT}/L)$. In ideal case, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT}/V_{IN}$.

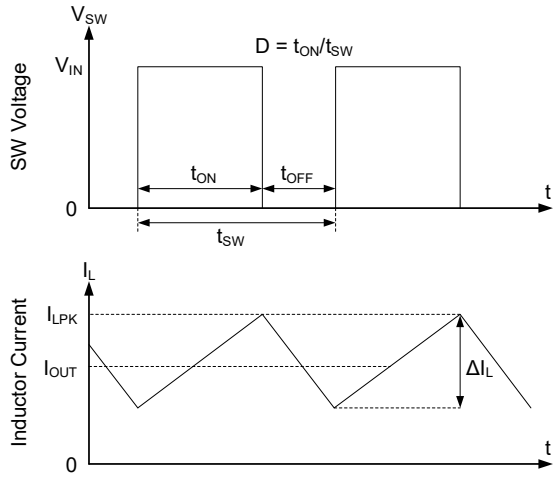


Figure 3. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The SGM61308 employs fixed-frequency peak-current mode control in continuous conduction mode. In light load conditions, the SGM61308A will enter power-save mode to reduce the switching frequency and the associated switching and gate drive losses.

In continuous conduction mode, the controller has an outer voltage feedback loop to get accurate DC voltage regulation. The output of the outer loop is fed to an inner peak-current control loop as reference command that adjusts the peak-current of the inductor. The inductor peak-current is sensed from the high-side switch and is compared to the peak-current reference to control the duty cycle. In other words, as soon as the inductor current reaches the reference peak-current determined by voltage loop, the high-side switch is turned off and the low-side switch is turned on after dead time. The voltage feedback loop is internally compensated, which allows for fewer external components, simpler design, and stable operation with almost any combination of output capacitors.

Minimum Input Voltage (4V) and UVLO

The recommended minimum operating input voltage is 4V. It may operate with lower voltages that are above the V_{IN} rising UVLO threshold (3.75V TYP). If V_{IN} falls below its falling UVLO threshold (3.4V TYP), the device will stop switching. The applications of UVLO include ensuring reliable operation, sequencing, and protections such as battery discharge.

DETAILED DESCRIPTION (continued)

Enable

The voltage on the EN pin provides the precision enable and disable of SGM61308. The device will enable if the EN pin voltage exceeds the enable threshold of 1.23V and V_{IN} exceeds its UVLO threshold. The device will disable if the EN voltage is externally pulled low or the V_{IN} pin voltage falls below its UVLO threshold. The EN pin cannot be left floating and can be connected to V_{IN} to enable the operation of the device.

An external input UVLO adjustment circuit is recommended in Figure 4. The EN input can be driven by an external logic signal to facilitate system sequencing and protection. If V_{EN} < 1.1V (TYP), the device will shut down. Only if V_{EN} > 1.23V (TYP), the device will start operation. It's crucial to note that the voltage supplied to the EN pin should never exceed V_{IN} + 0.3V.

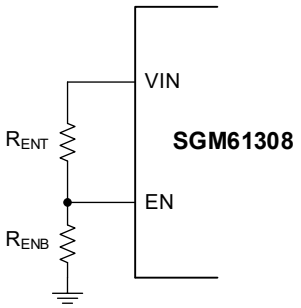


Figure 4. System UVLO by Enable Divider

Bootstrap Voltage

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. X5R or better dielectric types are recommended. The capacitor must have a 10V or higher voltage rating.

The SGM61308 operates at maximum duty cycle when input voltage is closed to output voltage as long as the bootstrap voltage (V_{BOOT} - V_{SW}) is greater than its UVLO threshold. When the bootstrap voltage falls below its UVLO, the high-side switch is turned off, and the integrated low-side switch is turned on to recharge the BOOT capacitor. After the recharge, the high-side switch is turned on again to regulate the output.

Soft-Start

The 1.8ms (TYP) soft-start time is integrated to slow the ramp of output voltage when SGM61308 is first enabled or powered up, which can prevent the input inrush current.

At the beginning of power-up, there is a 35ms (TYP) blank time t_{OCP_BLK} during which the over-current protection is disabled.

Without this feature, the inductor current will be large enough to trigger the current-limit protection when starting up with a large amount of output capacitors, which may results in the hiccup mode and the output voltage cannot ramp up to the regulation voltage.

By disabling the over-current protection during t_{OCP_BLK}, the output voltage of SGM61308 can be charged with the maximum limited current and maximizes the output current capacity.

The inductor current will not be out of control during t_{OCP_BLK} because the peak-current limit (I_{HS_LIMIT}) and valley current limit (I_{LS_LIMIT}) protection function are still available.

Light-Load Operation (PSM Version)

At light loads, SGM61308A enters pulse-skipping power-save mode (PSM) to reduce switching loss and keep high efficiency by lowering the number of switching pulses. When the peak inductor current is below PSM current threshold, the corresponding internal COMP voltage (V_{COMP}) will be lower than the internal threshold, the device will enter PSM.

After entering PSM for a delay time, some modules are shut down to minimum input current, and the device draws only 77μA (TYP) input quiescent current. The high-side MOSFET will not switch until the output voltage falls for the internal V_{COMP} to rise above the internal threshold. Since the integrated current comparator catches the inductor peak-current only, the average load current entering PSM varies with the applications and external output filters.

Light-Load Operation (FPWM Version)

At light loads, SGM61308B still operates in PWM mode. The frequency is constant, output voltage ripple is low and the output voltage regulation is tight.

Minimum On-Time, Minimum Off-Time and Frequency Foldback

Minimum on-time t_{ON_MIN} and minimum off-time t_{OFF_MIN}, are the smallest duration of time that the high-side switch can be on and off. t_{ON_MIN} is typically 80ns and t_{OFF_MIN} is typically 120ns in the SGM61308.

DETAILED DESCRIPTION (continued)

In continuous conduction mode operation, the voltage conversion range is limited by t_{ON_MIN} and t_{OFF_MIN} without frequency foldback.

With fixed switching frequency, the minimum duty cycle allowed is:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (1)$$

The maximum duty cycle allowed is:

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (2)$$

When the output voltage is given, the maximum V_{IN} can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \quad (3)$$

The minimum V_{IN} can be found by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \quad (4)$$

In order to extend the maximum duty cycle and lower the minimum duty cycle, SGM61308 features frequency foldback when the t_{ON_MIN} or t_{OFF_MIN} is triggered.

When V_{IN} voltage increases and the on-time decreases to t_{ON_MIN}, the switching frequency starts to decrease to lower the minimum duty cycle further for keeping V_{OUT} in regulation.

When V_{IN} voltage decreases and the off-time decreases to t_{OFF_MIN}, the switching frequency starts to decrease to extend the maximum duty cycle further for keeping V_{OUT} in regulation.

By frequency foldback, the frequency can be decreased to about 165kHz minimum. For a given output voltage, V_{IN_MAX} is increased and V_{IN_MIN} is lowered. With the wide range of frequency foldback, the output voltage can remain in regulation with a much lower supply voltage, which leads to a lower dropout.

Over-Current and Short-Circuit Protection

The SGM61308 features current limiting on both the peak and valley inductor current under over-current conditions. Hiccup mode is activated if overload or short-circuit condition persists to prevent over-heating.

High-side MOSFET over-current protection is naturally provided by peak-current mode control. In each cycle, the high-side current sensing starts after the high-side switch has been turned on for a short time (blanking time). The sensed high-side switch current is compared with the Error Amplifier (EA) output (V_{COMP}) minus slope compensation. By clamping V_{COMP} to a maximum value, the peak-current can be limited precisely.

The low-side switch current is also sensed and monitored. If the current in the high-side switch exceeds I_{HS_LIMIT}, the high-side switch will automatically be turned off and after a short dead-time, the low-side switch will be turned on to take over the current in the inductor. The low-side switch will not be turned off until the low-side switch current falls below I_{LS_LIMIT}.

Under overload or short-circuit conditions, if the FB voltage decreases to 30% of the reference voltage and the current of the high-side switch triggers I_{HS_LIMIT} for 128 consecutive cycles, the output starts to hiccup and device stops switching for about 135ms. After the 135ms off-period, the device is restarted with a soft-start cycle. If the overload or short-circuit condition is still present, the same hiccup cycle will repeat until the fault is removed. Under over-current conditions, hiccup mode reduces power dissipation and prevents the over-heating to the device.

For SGM61308B, if the inductor current goes negative and exceeds the negative current limit I_{LS_NEG}, the device stops switching. The negative current limit is designed to protect the low-side switch from excessive negative current.

Output Over-Voltage Protection (OVP)

The SGM61308 contains an over-voltage comparator that monitors the FB pin voltage. The over-voltage threshold is approximately 110% of nominal FB voltage. When the voltage at the FB pin exceeds the over-voltage threshold (V_{OUT_OV}), switching will be stopped and both high-side and low-side switches will be turned off. If the over-voltage fault is removed, the regulator will automatically recover.

Thermal Shutdown

To avoid damage from over-heating, the junction temperature is continuously monitored. And if the temperature exceeds the shutdown level (T_{SD} = +170℃, TYP), all power switches are turned off immediately. When the device is cooled off for 20℃ (typical hysteresis), the device automatically resumes normal operation after a soft-start.

APPLICATION INFORMATION

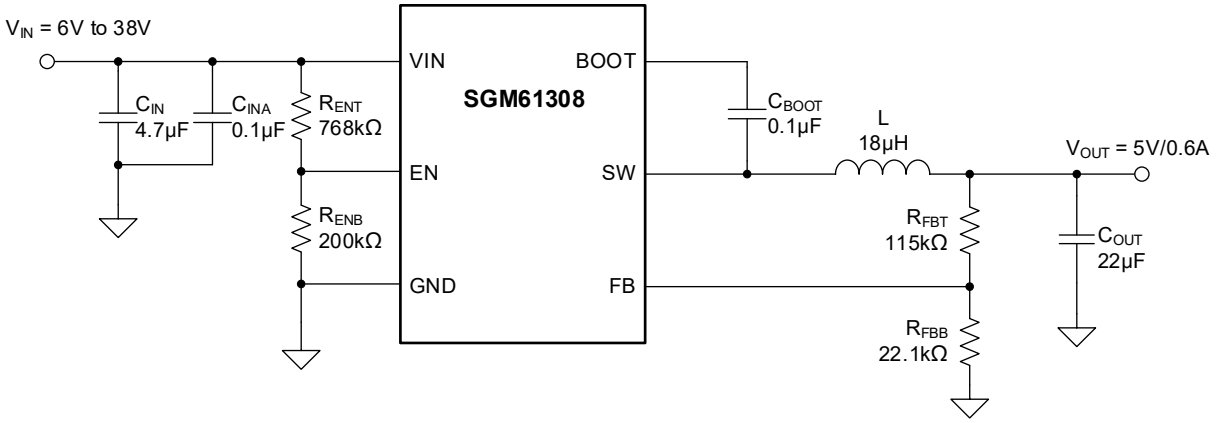


Figure 5. Application Circuit

Application Information

The SGM61308 is a Buck DC/DC converter, which is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 600mA. The following design procedure can be used to select components for the SGM61308.

Typical Application

Few external components are required for SGM61308 to convert from a wide voltage range supply to a lower voltage level output. A basic schematic for the device as a Buck converter is shown in Figure 7.

When select the external components, the needs of the application and the stability criteria of the device's control loop should be taken into consideration. Table 1 can be used to select external components.

Table 1. L and C_{OUT} Typical Values

f_{SW} (MHz)	V_{OUT} (V)	L (μH)	C_{OUT} (μF) (1)	R_{FBT} (kΩ)	R_{FBB} (kΩ)
1.1	3.3	12	22μF/16V	69.8	22.1
	5	18	22μF/16V	115	22.1
	12	33	10μF/25V	316	22.1

NOTE: 1. Ceramic capacitor is used in this table.

Design Requirements

Based on a design example followed, the detailed design procedure is described. The parameters given in Table 2 are used for this design example.

Table 2. Design Example Parameters

Parameter	Value
Input Voltage, V_{IN}	12V (TYP), range from 6V to 38V
Output Voltage, V_{OUT}	5V ± 3%
Maximum Output Current, I_{OUT_MAX}	600mA
Output Over/Undershoot (100mA to 600mA)	5% of V_{OUT}
Output Voltage Ripple (FPWM)	0.5% of V_{OUT}
Operating Frequency	1.1MHz

Output Voltage Programming

Output voltage can be set with a resistor divider feedback network between output and FB pin. The divider network consists of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. The R_{FBT} and R_{FBB} can be selected based on Equation 5.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (5)$$

where V_{REF} = 0.8V.

To keep operating quiescent current small and prevent voltage errors due to leakage currents, it is recommended to choose R_{FBB} in the range of 10kΩ to 100kΩ. Given V_{OUT} = 5V and choose the value of R_{FBB} to be 22.1kΩ, R_{FBT} can be calculated from Equation 5. The calculation result of R_{FBT} is 116.025kΩ, a standard value of 115kΩ is selected.

APPLICATION INFORMATION (continued)

Switching Frequency

Several parameters such as losses, inductor and capacitors sizes and response time are considered in selection of the switching frequency. Higher frequency increases the switching and gate drive losses, and lower frequency requires larger inductance and capacitances, which results in larger overall physical size and higher cost. Therefore, a tradeoff is needed between losses and component size. For this design, a switching frequency of 1.1MHz is selected.

As described in Minimum On-Time, Minimum Off-Time and Frequency Foldback section, the switching frequency is also limited by the t_{ON_MIN}, t_{OFF_MIN}, the input voltage, the output voltage and the frequency foldback minimum limitation.

Input Capacitor Selection

High-quality ceramic capacitor(s) (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61308. At least 2.2μF of capacitance is recommended on the VIN input. The voltage rating should have adequate design margin to handle the highest expected input surge voltage. The VIN capacitor ripple current rating must also be greater than the maximum input current ripple.

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. So, one 4.7μF/50V, X7R capacitor is selected for the input decoupling capacitor. To improve high frequency filtering, a small parallel 0.1μF ceramic capacitor is recommended to place as close as possible to VIN and GND pins.

Inductor Selection

Three parameters of the inductor are critical in the design: nominal inductance value, saturation current and maximum RMS current.

Equation 6 is conventionally used to calculate the output inductance of a Buck converter. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions, especially if a hard-saturation core type inductor (such as ferrite) is chosen. For peak-current mode converter, the saturation current should be greater than the switch current limit.

Typically, a 20% to 40% ripple is selected (K_{IND} = 0.2 to 0.4). Choosing a higher K_{IND} value reduces the selected inductance, however, a too high K_{IND} factor may result in insufficient slope compensation.

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (6)$$

$$\Delta I_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times f_{SW}} \quad (7)$$

Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. But inductor of too low results in larger current ripple, which increases the power dissipation in the inductor and MOSFETs. Larger inductor current ripple also requires more output capacitance to smooth out the larger current ripple. The current limit can be falsely triggered with full load when the inductor current ripple is large. For peak-current mode control, larger current ripple improves the signal to noise ratio of comparator, and too small inductor current ripple is not recommended.

In this example, K_{IND} = 0.4 is chosen, and the minimum inductor value for 38V input voltage is calculated to be 16.45μH. So the nearest larger inductance of 18μH with 1.9A RMS current and 2.2A saturation current is selected. Besides, for an application condition with output voltage lower than 1.5V, minimum on-time frequency foldback may occur, the inductance should be higher than 5.6μH.

Output Capacitor Selection

Three primary criteria must be considered for design of the output capacitor (C_{OUT}):

1. The converter pole location.
2. The output voltage ripple.
3. The transient response to a large change in load current.

APPLICATION INFORMATION (continued)

Equation 8 can be used to calculate the minimum output capacitance that is needed to supply a current step for 8 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT_SHOOT} (overshoot or undershoot).

$$C_{OUT} > \frac{1}{2} \times \frac{8 \times (I_{OH} - I_{OL})}{f_{SW} \times \Delta V_{OUT\_SHOOT}} \quad (8)$$

where:

I_{OL} = Low level output current during load transient
I_{OH} = High level output current during load transient
ΔV_{OUT_SHOOT} = Target output voltage overshoot or undershoot

For example, if the acceptable transient from 0A to 0.6A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V, I_{OH} = 0.6A and I_{OL} = 0A, the minimum required capacitance will be 8.73μF.

The output voltage ripple caused by the output capacitor charging and discharging can be dominated by Equation 9:

$$\Delta V_{OUT\_C} = \frac{\Delta I_L}{(8 \times f_{SW} \times C_{OUT})} = \frac{K_{IND} \times I_{OUT}}{(8 \times f_{SW} \times C_{OUT})} \quad (9)$$

Note that the impact of output capacitor ESR on the transient is not taken into account in Equation 9. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient. However, for aluminum electrolytic and tantalum capacitors, or high current power supplies, the ESR contribution to ΔV_{OUT} must be considered. For a specific output capacitance value, use Equation 10 to calculate the output voltage ripple caused by the ESR of the output capacitor.

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (10)$$

In this example, the target output ripple is 25mV. Given ΔV_{OUT_ESR} = ΔV_{OUT_C} = 25mV, and chose K_{IND} = 0.4. The ESR of output capacitor should be smaller than 104mΩ according to Equation 10. And the C_{OUT} should be larger than 1.09μF according to Equation 9.

Base on the above mentioned, the output capacitor must be larger than 8.73μF. So, one 22μF, 16V, X5R ceramic capacitor is selected after taking derating into consideration.

Bootstrap Capacitor

The SGM61308 requires a small external bootstrap capacitor, C_{BOOT}, between the BOOT and SW pins to provide the gate drive supply voltage for the high-side MOSFET. The bootstrap capacitor is refreshed when the high-side MOSFET is off and the low-side switch is conducted. An X7R or X5R 0.1μF ceramic capacitor with a voltage rating of 10V or higher is recommended for stable operating performance over-temperature and voltage variations.

Under-Voltage Lockout Set-Point

The Input UVLO can be programmed using an external voltage divider on the EN pin of the SGM61308. In this design, R_{ENT} is connected between VIN pin and EN pin and R_{ENB} is connected between EN pin and GND (see Figure 5). The UVLO has two thresholds, V_{IN_RISING} for power-up (turn-on) when the input voltage is rising and $V_{IN\_FALLING}$ for power-down (turn-off) when the voltage is falling. The enable rising threshold voltage V_{EN_H} is 1.23V (TYP) and enable hysteresis voltage V_{EN_HYS} is 0.13V (TYP). Given V_{IN_RISING} as 6.0V, select R_{ENB} to be 200kΩ to minimize input current from the supply, then R_{ENT} and $V_{IN\_FALLING}$ can be calculated by following equations.

$$V_{IN\_RISING} = V_{EN\_H} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (11)$$

$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{EN\_H}} - 1 \right) \times R_{ENB} \quad (12)$$

$$V_{IN\_FALLING} = (V_{EN\_H} - V_{EN\_HYS}) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \quad (13)$$

By Equation 12, R_{ENT} is calculated to be 775.6kΩ, and a standard value of 768kΩ is selected. Based on the value of R_{ENT}, $V_{IN\_FALLING}$ can be calculated to be 5.3V by Equation 13

APPLICATION INFORMATION (continued)

Layout

Layout Guidelines

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. Following the guidelines provided here are necessary to design a good layout:

- Place low-ESR ceramic capacitor (X5R or X7R or better dielectric) C_{IN} as close as possible to VIN pin and GND pin. The grounding for C_{IN} and C_{OUT} should be local on the top side planes that connect to the GND pin.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections, SW pin and GND pin.
- Use short, thick traces or copper pours for high current conduction path like V_{IN}, V_{OUT} and GND.
- Keep the SW area minimal and away from sensitive signals like FB input and divider resistors to avoid capacitive noise coupling.
- Place the resistor divider of R_{FBT} and R_{FBB} as close as possible to the FB pin and avoid long traces in the divider network. Sense V_{OUT} at the load and place the sense path on the other side of a shielded layer.
- Use heat-sinking vias to connect the ground planes on the top and bottom layers or multiple copper layers for heat dissipation. Ensure that there is enough copper for heat dissipation to keep the junction temperature below +125℃.

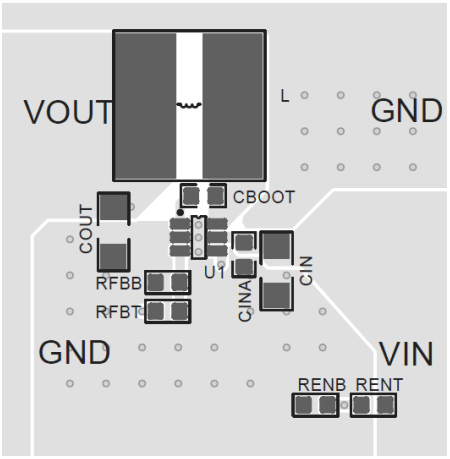


Figure 6. Top Layer

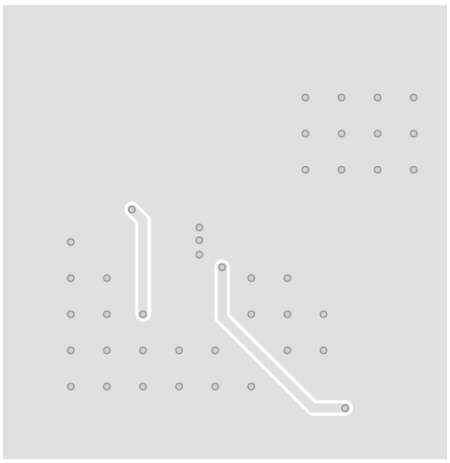


Figure 7. Bottom Layer

REVISION HISTORY

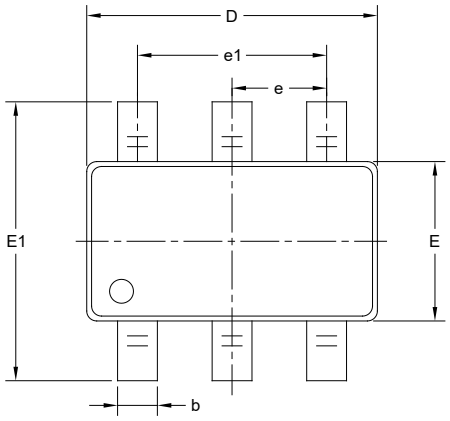
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

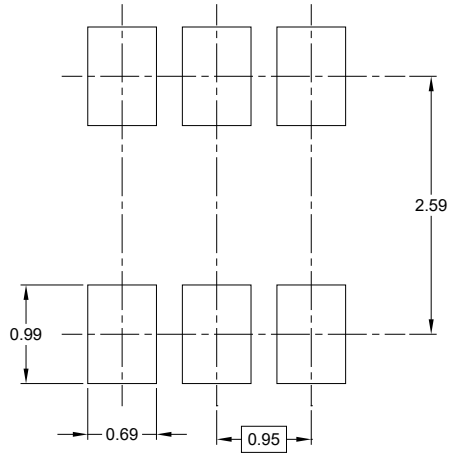
JUNE 2024 – REV.A to REV.A.1	Page
Updated ESD Susceptibility	2

Changes from Original (MAY 2024) to REV.A	Page
Changed from product preview to production data	All

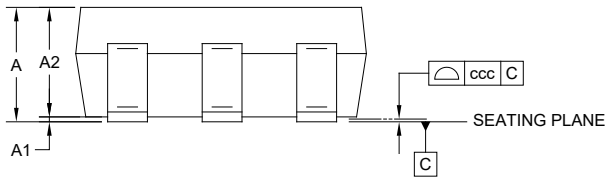
PACKAGE OUTLINE DIMENSIONS

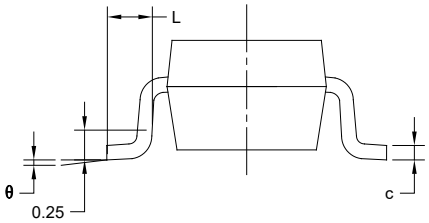
SOT-23-6





RECOMMENDED LAND PATTERN (Unit: mm)



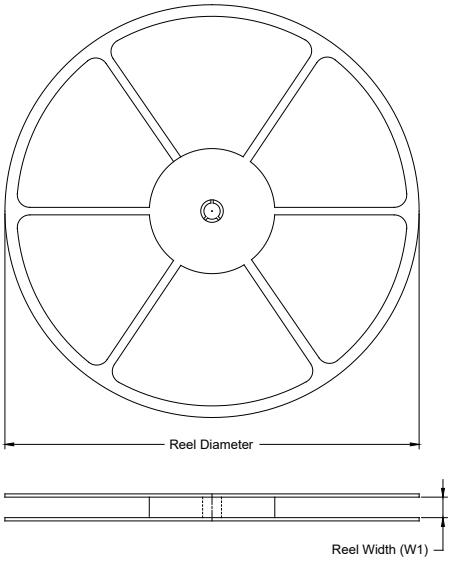


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

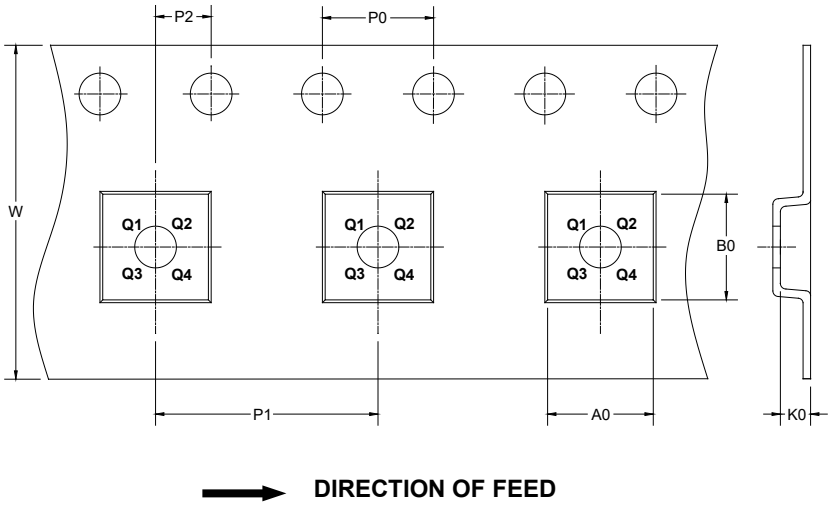
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



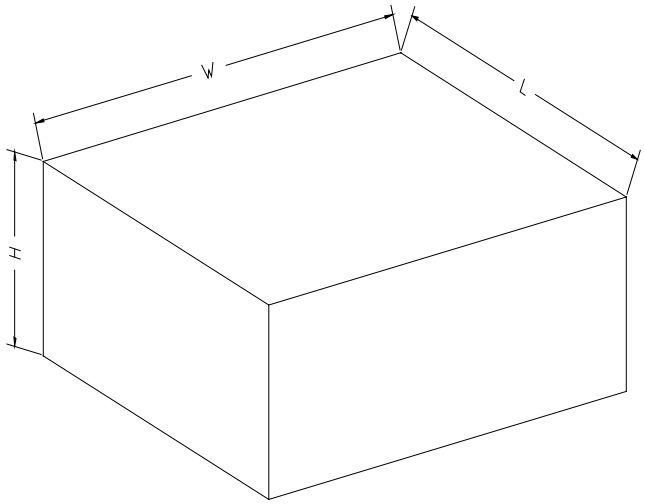
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-6	7"	9.5	3.23	3.17	1.37	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002