SGM41010
Battery Protection IC for 1-Cell Pack

GENERAL DESCRIPTION

The SGM41010 is a battery protection IC for Li-Ion/ polymer rechargeable batteries, including the high-accuracy voltage detection circuits and the delay circuits. The device is designed to protect 1-cell Li-Ion/ polymer rechargeable battery packs against over-charge, over-discharge and over-current.

The SGM41010 uses an external over-current detection resistor to achieve high-accuracy over-current protection with less effect from temperature change.

The SGM41010 is available in Green XTDFN-1.4×1.4-6L and UTDFN-1.4×1.8-6L packages. It can operate in the -40℃ to +85℃ ambient temperature range.

APPLICATIONS

Li-Ion Rechargeable Battery Pack
Lithium Polymer Rechargeable Battery Pack

TYPICAL APPLICATION

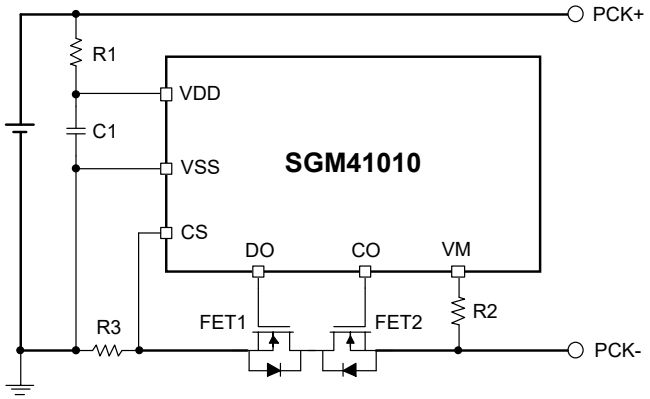


Figure 1. Typical Application Circuit

FEATURES

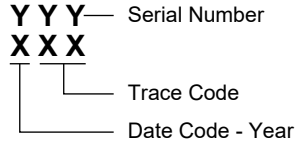
- **High-Accuracy Voltage Detection Circuit**
  - **Over-Charge Detection Voltage: 4.1V to 5.0V (5mV Step), Accuracy: ±15mV**
  - **Over-Charge Hysteresis Voltage: 0mV to 400mV (100mV Step), Accuracy: ±40mV**
  - **Over-Discharge Detection Voltage: 2.1V to 3.0V (10mV Step), Accuracy: ±35mV**
  - **Over-Discharge Hysteresis Voltage: 100mV to 400mV (100mV Step), Accuracy: ±35mV**
  - **Discharge Over-Current Detection Voltage 1: 3mV to 100mV (0.25mV Step), Accuracy: ±0.75mV**
  - **Discharge Over-Current Detection Voltage 2: 6mV to 100mV (0.5mV Step), Accuracy: ±2mV**
  - **Load Short-Circuiting Detection Voltage: 20mV to 100mV (1mV Step), Accuracy: ±3.5mV**
  - **Charge Over-Current Detection Voltage: -100mV to -3mV (0.25mV Step), Accuracy: ±0.75mV**
- **Detection Delay Times are Generated Only by an Internal Circuit (No External Capacitors Required)**
- **Low Voltage Battery Charge Permission Voltage:**
  - **0V, 0.9V**
- **Power-Down Function Available**
- **Output Available during Power-On**
- **Continuously Retry when OCP/SCP Occurs**
- **High-Withstand Voltage: VM and CO Pins: Absolute Maximum Rating -28V**
- **Operating Temperature Range: -40℃ to +85℃**
- **Low Current Consumption**
  - **During Operation: 1.55μA (TYP) (T_J = +25℃)**
  - **During Power-Down: 1nA (TYP) (T_J = +25℃)**
- **Available in Green XTDFN-1.4×1.4-6L and UTDFN-1.4×1.8-6L Packages**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41010AAA-AA	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-AAYUHE6G/TR	0XN XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-AAYXHF6G/TR	0XR XXX	Tape and Reel, 3000
SGM41010AAA-AB	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-ABYUHE6G/TR	0XO XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-ABYXHF6G/TR	0XS XXX	Tape and Reel, 3000
SGM41010AAA-AC	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-ACYUHE6G/TR	0XP XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-ACYXHF6G/TR	0XT XXX	Tape and Reel, 3000
SGM41010AAA-AD	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-ADYUHE6G/TR	0XQ XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-ADYXHF6G/TR	0XU XXX	Tape and Reel, 3000
SGM41010AAA-AE	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-AEYUHE6G/TR	0T2 XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-AEYXHF6G/TR	0T1 XXX	Tape and Reel, 3000
SGM41010AAA-AF	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-AFYUHE6G/TR	1SE XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-AFYXHF6G/TR	1SJ XXX	Tape and Reel, 3000
SGM41010AAA-AG	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-AGYUHE6G/TR	1SF XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-AGYXHF6G/TR	1SK XXX	Tape and Reel, 3000
SGM41010AAA-AH	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-AHYUHE6G/TR	1SG XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-AHYXHF6G/TR	1SL XXX	Tape and Reel, 3000
SGM41010AAA-AJ	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-AJYUHE6G/TR	1SH XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-AJYXHF6G/TR	1SM XXX	Tape and Reel, 3000
SGM41010AAA-AQ	UTDFN-1.4×1.8-6L	-40℃ to +85℃	SGM41010AAA-AQYUHE6G/TR	1SI XXX	Tape and Reel, 3000
	XTDFN-1.4×1.4-6L	-40℃ to +85℃	SGM41010AAA-AQYXHF6G/TR	1SN XXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

PRODUCT LIST

Table 1. Product Name List

Product Name (1)	Over-Charge Detection Voltage (V_{CU})	Over-Charge Release Voltage (V_{CL})	Over-Discharge Detection Voltage (V_{DL})	Over-Discharge Release Voltage (V_{DU})	Discharge Over-Current Detection Voltage 1 (V_{DIOV1})	Discharge Over-Current Detection Voltage 2 (V_{DIOV2})	Load Short-Circuiting Detection Voltage (V_{SHORT})	Charge Over-Current Detection Voltage (V_{CIOV})	0V Battery Charge Inhibition Threshold (V_{0INH})	OCP/SCP Retry Times (2)	Delay Time Combination (3)
SGM41010 AAA-AA	4.500V	4.300V	2.500V	2.900V	5.6mV	8.5mV	22.5mV	-11.3mV	0V	Continuously	(1)
SGM41010 AAA-AB	4.545V	4.345V	2.500V	2.900V	5.5mV	8.5mV	22.5mV	-11.5mV	0V	Continuously	(4)
SGM41010 AAA-AC	4.595V	4.395V	2.500V	2.900V	5.6mV	8.5mV	22.5mV	-11.3mV	0V	Continuously	(4)
SGM41010 AAA-AD	4.610V	4.410V	2.500V	2.900V	5.5mV	8.5mV	22.5mV	-11.5mV	0V	Continuously	(4)
SGM41010 AAA-AE	4.300V	4.100V	2.500V	2.900V	5.5mV	8.5mV	22.5mV	-11.5mV	0V	Continuously	(4)
SGM41010 AAA-AF	4.500V	4.300V	2.500V	2.900V	5.6mV	8.5mV	22.5mV	-11.3mV	0V	Continuously	(1)
SGM41010 AAA-AG	4.495V	4.295V	2.500V	2.900V	14mV	28mV	40mV	-15mV	0V	Continuously	(3)
SGM41010 AAA-AH	4.580V	4.380V	2.600V	3.000V	7mV	14mV	28mV	-15mV	0V	Continuously	(6)
SGM41010 AAA-AJ	4.400V	4.200V	2.500V	2.900V	4mV	8mV	28mV	-4mV	0V	Continuously	(7)
SGM41010 AAA-AQ	4.520V	4.370V	2.100V	2.300V	7mV	14mV	28mV	-14mV	0V	Continuously	(1)

NOTES:

1. The product name is in range of SGM41010AAA-AA to SGM41010AAA-ZZ. For products other than the above, please contact our sales representatives.

2. The OCP/SCP retry times can keep retrying continuously until the OCP/SCP conditions disappear.

3. Please refer to the Table 2 for details of the delay time combinations.

Table 2. Delay Time Combination

Delay Time Combination (5)	Over-Charge Detection Delay Time (t_{CU})	Over-Discharge Detection Delay Time (t_{DL})	Discharge Over-Current Detection Delay Time 1 (t_{DIOV1})	Discharge Over-Current Detection Delay Time 2 (t_{DIOV2})	Load Short-Circuiting Detection Delay Time (t_{SHORT})	Charge Over-Current Detection Delay Time (t_{CIOV})	Discharge Over-Current Retry Time (t_{RETRY})
(1)	512ms	80ms	80ms	25ms (4)	280μs	48ms	512ms
(2)	1024ms	80ms	144ms	40ms (4)	280μs	80ms	512ms
(3)	1024ms	80ms	80ms	25ms (4)	280μs	32ms	512ms
(4)	512ms	80ms	80ms	25ms (4)	280μs	32ms	512ms
(5)	1024ms	80ms	144ms	40ms (4)	280μs	80ms	512ms
(6)	512ms	80ms	80ms	25ms (4)	280μs	32ms	512ms
(7)	1024ms	80ms	144ms	40ms (4)	280μs	80ms	512ms
(8)	512ms	80ms	256ms	40ms (4)	280μs	80ms	512ms

NOTE:

4. Discharge over-current detection voltage 2 can be inhibited.

5. The delay times can be changed within the range shown in Table 3. Please contact our sales representatives for more information.

PRODUCT LIST (continued)

Table 3. Delay Time Options

Delay Time	Symbol	Selection Range				Remark
Over-Charge Detection Delay Time	t_{CU}	512ms	1024ms			Select a value from the left.
Over-Discharge Detection Delay Time	t_{DL}	80ms	144ms			Select a value from the left.
Discharge Over-Current Detection Delay Time 1	t_{DIOV1}	48ms	80ms	144ms	256ms	Select a value from the left.
		512ms	1024ms	2048ms	4096ms	
Discharge Over-Current Detection Delay Time 2	t_{DIOV2}	25ms	40ms			Select a value from the left.
Load Short-Circuiting Detection Delay Time	t_{SHORT}	280μs	560μs			Select a value from the left.
Charge Over-Current Detection Delay Time	t_{CIOV}	32ms	48ms	80ms		Select a value from the left.
Discharge Over-Current Retry Time	t_{RETRY}	512ms				Select a value from the left.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range between VDD Pin and VSS Pin, V_{DS} ..... V_{SS} - 0.3V to V_{SS} + 12V

CS Pin Input Voltage Range, V_{CS} ..... V_{SS} - 0.3V to V_{SS} + 5V

VM Pin Input Voltage Range, V_{VM} ..... V_{DD} - 28V to V_{DD} + 0.3V

DO Pin Output Voltage Range, V_{DO} ..... V_{SS} - 0.3V to V_{DD} + 0.3V

CO Pin Output Voltage Range, V_{CO} ..... V_{DD} - 28V to V_{DD} + 0.3V

Package Thermal Resistance

UTDFN-1.4×1.8-6L, θ_{JA} ..... 158℃/W

UTDFN-1.4×1.8-6L, θ_{JB} ..... 117.9℃/W

UTDFN-1.4×1.8-6L, $\theta_{JC\ (TOP)}$ ..... 127.8℃/W

UTDFN-1.4×1.8-6L, $\theta_{JC\ (BOT)}$ ..... 81.3℃/W

XTDFN-1.4×1.4-6L, θ_{JA} ..... 153℃/W

XTDFN-1.4×1.4-6L, θ_{JB} ..... 93.3℃/W

XTDFN-1.4×1.4-6L, $\theta_{JC\ (TOP)}$ ..... 93.8℃/W

XTDFN-1.4×1.4-6L, $\theta_{JC\ (BOT)}$ ..... 88.8℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±5000V

CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 0V to 6V

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

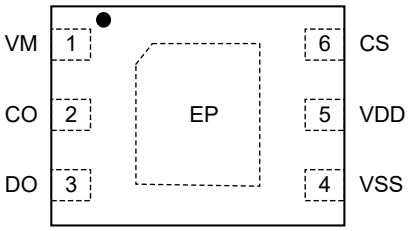
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

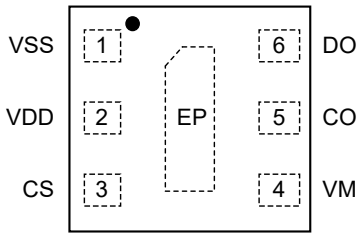
PIN CONFIGURATIONS

(TOP VIEW)



UTDFN-1.4×1.8-6L

(TOP VIEW)



XTDFN-1.4×1.4-6L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
UTDFN-1.4×1.8-6L	XTDFN-1.4×1.4-6L			
1	4	VM	I	External Negative Voltage Input Pin.
2	5	CO	O	Charge Control FET Gate Connection Pin (CMOS Output).
3	6	DO	O	Discharge Control FET Gate Connection Pin (CMOS Output).
4	1	VSS	I	Negative Power Supply Input Pin.
5	2	VDD	I	Positive Power Supply Input Pin.
6	3	CS	I	Over-Current Detection Input Pin.
Exposed Pad	Exposed Pad	EP	–	Exposed Pad. It is recommended to leave this pin floating.

NOTE: I = input, O = output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Detection Voltage							
Over-Charge Detection Voltage (1)	V_{CU}	Test circuit 1, see Figure 3	T_J = +25℃	V_{CU} - 0.015	V_{CU}	V_{CU} + 0.015	V
			T_J = -20℃ to +60℃	V_{CU} - 0.028		V_{CU} + 0.023	
			T_J = -40℃ to +85℃	V_{CU} - 0.040		V_{CU} + 0.030	
Over-Charge Release Voltage (1)	V_{CL}	$V_{CL} \neq V_{CU}$, test circuit 1, see Figure 3	T_J = +25℃	V_{CL} - 0.040	V_{CL}	V_{CL} + 0.040	V
			T_J = -20℃ to +60℃	V_{CL} - 0.050		V_{CL} + 0.050	
			T_J = -40℃ to +85℃	V_{CL} - 0.055		V_{CL} + 0.055	
Over-Charge Hysteresis Voltage	V_{OCHYS}	0mV option	T_J = +25℃		0		mV
			T_J = -20℃ to +60℃		0		
			T_J = -40℃ to +85℃		0		
		100mV option	T_J = +25℃		100		
			T_J = -20℃ to +60℃		100		
			T_J = -40℃ to +85℃		100		
		200mV option	T_J = +25℃		200		
			T_J = -20℃ to +60℃		200		
			T_J = -40℃ to +85℃		200		
		300mV option	T_J = +25℃		300		
			T_J = -20℃ to +60℃		300		
			T_J = -40℃ to +85℃		300		
		400mV option	T_J = +25℃		400		
			T_J = -20℃ to +60℃		400		
			T_J = -40℃ to +85℃		400		
Over-Discharge Detection Voltage	V_{DL}	Test circuit 2, see Figure 4	T_J = +25℃	V_{DL} - 0.035	V_{DL}	V_{DL} + 0.035	V
			T_J = -20℃ to +60℃	V_{DL} - 0.040		V_{DL} + 0.040	
			T_J = -40℃ to +85℃	V_{DL} - 0.045		V_{DL} + 0.045	
Over-Discharge Release Voltage	V_{DU}	Test circuit 2, see Figure 4	T_J = +25℃	V_{DU} - 0.035	V_{DU}	V_{DU} + 0.035	V
			T_J = -20℃ to +60℃	V_{DU} - 0.050		V_{DU} + 0.050	
			T_J = -40℃ to +85℃	V_{DU} - 0.060		V_{DU} + 0.060	
Over-Discharge Hysteresis Voltage	V_{ODHYS}	100mV option	T_J = +25℃		100		mV
			T_J = -20℃ to +60℃		100		
			T_J = -40℃ to +85℃		100		
		200mV option	T_J = +25℃		200		
			T_J = -20℃ to +60℃		200		
			T_J = -40℃ to +85℃		200		
		300mV option	T_J = +25℃		300		
			T_J = -20℃ to +60℃		300		
			T_J = -40℃ to +85℃		300		
		400mV option	T_J = +25℃		400		
			T_J = -20℃ to +60℃		400		
			T_J = -40℃ to +85℃		400		

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Detection Voltage							
Discharge Over-Current Detection Voltage 1 (1)	V_{DIOV1}	Test circuit 5, see Figure 7	T_J = +25℃	V_{DIOV1} - 0.75	V_{DIOV1}	V_{DIOV1} + 0.75	mV
			T_J = -20℃ to +60℃	V_{DIOV1} - 1.25		V_{DIOV1} + 1.25	
			T_J = -40℃ to +85℃	V_{DIOV1} - 1.25		V_{DIOV1} + 1.25	
Discharge Over-Current Detection Voltage 2	V_{DIOV2}	Test circuit 5, see Figure 7	T_J = +25℃	V_{DIOV2} - 2.0	V_{DIOV2}	V_{DIOV2} + 2.0	mV
			T_J = -20℃ to +60℃	V_{DIOV2} - 2.2		V_{DIOV2} + 2.2	
			T_J = -40℃ to +85℃	V_{DIOV2} - 2.2		V_{DIOV2} + 2.2	
Load Short-Circuiting Detection Voltage	V_{SHORT}	Test circuit 2, see Figure 4		V_{SHORT} - 3.5	V_{SHORT}	V_{SHORT} + 3.5	mV
Load Short-Circuiting Detection Voltage 2	V_{SHORT2}	V_{DD} = 3.4V, Test circuit 2, see Figure 4		V_{DD} - 1.2	V_{DD} - 0.65	V_{DD} - 0.5	V
Charge Over-Current Detection Voltage (1)	V_{CIOV}	Test circuit 2, see Figure 4	T_J = +25℃	V_{CIOV} - 0.75	V_{CIOV}	V_{CIOV} + 0.75	mV
			T_J = -20℃ to +60℃	V_{CIOV} - 1.25		V_{CIOV} + 1.25	
			T_J = -40℃ to +85℃	V_{CIOV} - 1.25		V_{CIOV} + 1.25	
Load Short-Circuiting 2 Release Voltage	V_{RIOV}	V_{DD} = 3.4V, test circuit 2, see Figure 4		V_{DD} - 2	V_{DD} - 1.5	V_{DD} - 1	V
0V Battery Charge							
0V Battery Charge Starting Charger Voltage	V_{0CHA}	0V battery charge enabled, test circuit 4, see Figure 6	T_J = +25℃	1.00	1.20	1.60	V
			T_J = -20℃ to +60℃	0.90	1.20	1.65	
			T_J = -40℃ to +85℃	0.80	1.20	1.70	
Internal Resistance							
Resistance between VDD Pin and VM Pin	R_{VMD}	V_{DD} = 1.4V, V_{VM} = 0V, test circuit 3, see Figure 5	T_J = +25℃	850	1150	1500	kΩ
			T_J = -20℃ to +60℃	750	1150	1600	
			T_J = -40℃ to +85℃	650	1150	1700	
Resistance between VM Pin and VSS Pin	R_{VMS}	V_{DD} = 3.4V, V_{VM} = 3.2V, test circuit 3, see Figure 5	T_J = +25℃	9.5	13.5	17.5	kΩ
			T_J = -20℃ to +60℃	8.5	13.5	20.0	
			T_J = -40℃ to +85℃	6.5	13.5	22.0	
Input Voltage							
Operation Voltage between VDD Pin and VSS Pin	V_{DSOP1}			1.5		12	V
Operation Voltage between VDD Pin and VM Pin	V_{DSOP2}			1.5		28	V
Input Current							
Current Consumption during Operation	I_{OPE}	V_{DD} = 3.4V, V_{VM} = 0V, test circuit 3, see Figure 5	T_J = +25℃	1.30	1.55	1.90	μA
			T_J = -20℃ to +60℃	1.05	1.55	2.20	
			T_J = -40℃ to +85℃	1.00	1.55	2.50	
Current Consumption during Power-Down	I_{PDN}	V_{DD} = V_{VM} = 1.4V, test circuit 3, see Figure 5	T_J = +25℃		1	50	nA
			T_J = -20℃ to +60℃		1	60	
			T_J = -40℃ to +85℃		1	100	
Output Resistance							
CO Pin Resistance "H"	R_{COH}	Test circuit 4, see Figure 6	T_J = +25℃	7.0	10.5	15.0	kΩ
			T_J = -20℃ to +60℃	5.5	10.5	16.0	
			T_J = -40℃ to +85℃	4.0	10.5	17.0	

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

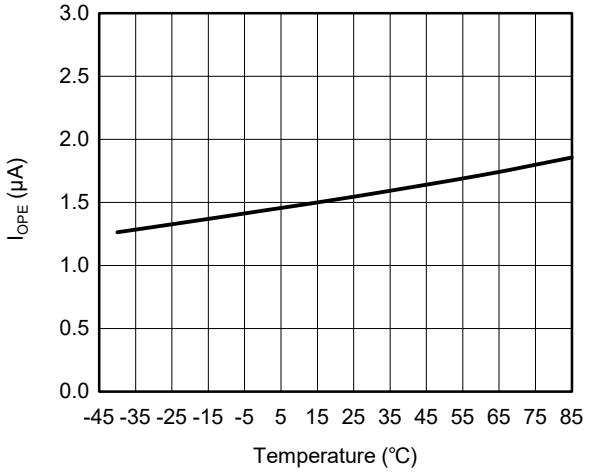
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Resistance							
CO Pin Resistance "L"	R_{COL}	Test circuit 4, see Figure 6	T_J = +25℃	2.0	3.2	5.5	kΩ
			T_J = -20℃ to +60℃	1.8	3.2	6.5	
			T_J = -40℃ to +85℃	1.5	3.2	8.0	
DO Pin Resistance "H"	R_{DOH}	Test circuit 4, see Figure 6	T_J = +25℃	7.0	9.5	14.0	kΩ
			T_J = -20℃ to +60℃	6.5	9.5	14.5	
			T_J = -40℃ to +85℃	6.0	9.5	15.0	
DO Pin Resistance "L"	R_{DOL}	Test circuit 4, see Figure 6	T_J = +25℃	1.6	3.0	5.5	kΩ
			T_J = -20℃ to +60℃	1.5	3.0	6.5	
			T_J = -40℃ to +85℃	1.3	3.0	7.0	
Delay Time (1)							
Over-Charge Detection Delay Time	t_{CU}	Test circuit 5, see Figure 7	T_J = +25℃	t_{CU} × 0.85	t_{CU}	t_{CU} × 1.20	ms
			T_J = -20℃ to +60℃	t_{CU} × 0.78		t_{CU} × 1.31	
			T_J = -40℃ to +85℃	t_{CU} × 0.73		t_{CU} × 1.42	
Over-Discharge Detection Delay Time	t_{DL}	Test circuit 5, see Figure 7	T_J = +25℃	t_{DL} × 0.68	t_{DL}	t_{DL} × 1.35	ms
			T_J = -20℃ to +60℃	t_{DL} × 0.62		t_{DL} × 1.50	
			T_J = -40℃ to +85℃	t_{DL} × 0.58		t_{DL} × 1.60	
Discharge Over-Current Detection Delay Time 1	t_{DIOV1}	Test circuit 5, see Figure 7	T_J = +25℃	t_{DIOV1} × 0.57	t_{DIOV1}	t_{DIOV1} × 1.50	ms
			T_J = -20℃ to +60℃	t_{DIOV1} × 0.52		t_{DIOV1} × 1.67	
			T_J = -40℃ to +85℃	t_{DIOV1} × 0.48		t_{DIOV1} × 1.78	
Discharge Over-Current Detection Delay Time 2	t_{DIOV2}	Test circuit 5, see Figure 7	T_J = +25℃	t_{DIOV2} × 0.54	t_{DIOV2}	t_{DIOV2} × 1.44	ms
			T_J = -20℃ to +60℃	t_{DIOV2} × 0.50		t_{DIOV2} × 1.60	
			T_J = -40℃ to +85℃	t_{DIOV2} × 0.46		t_{DIOV2} × 1.71	
Load Short-Circuiting Detection Delay Time	t_{SHORT}	Test circuit 5, see Figure 7	T_J = +25℃	t_{SHORT} × 0.73	t_{SHORT}	t_{SHORT} × 1.13	μs
			T_J = -20℃ to +60℃	t_{SHORT} × 0.78		t_{SHORT} × 1.25	
			T_J = -40℃ to +85℃	t_{SHORT} × 0.73		t_{SHORT} × 1.34	
Charge Over-Current Detection Delay Time	t_{CIOV}	Test circuit 5, see Figure 7	T_J = +25℃	t_{CIOV} × 0.42	t_{CIOV}	t_{CIOV} × 1.69	ms
			T_J = -20℃ to +60℃	t_{CIOV} × 0.39		t_{CIOV} × 1.88	
			T_J = -40℃ to +85℃	t_{CIOV} × 0.36		t_{CIOV} × 2.00	
Discharge Over-Current Retry Time	t_{RETRY}	Test circuit 5, see Figure 7	T_J = +25℃	t_{RETRY} × 0.85	t_{RETRY}	t_{RETRY} × 1.16	ms
			T_J = -20℃ to +60℃	t_{RETRY} × 0.78		t_{RETRY} × 1.29	
			T_J = -40℃ to +85℃	t_{RETRY} × 0.73		t_{RETRY} × 1.38	

NOTE:

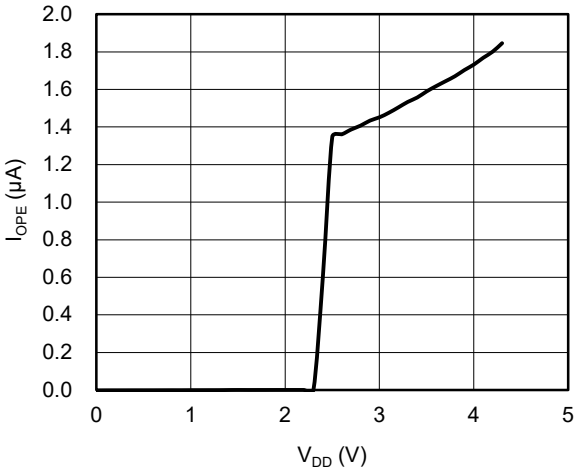
1. The best estimate from product characterization, guaranteed by correlated test in production.

TYPICAL PERFORMANCE CHARACTERISTICS

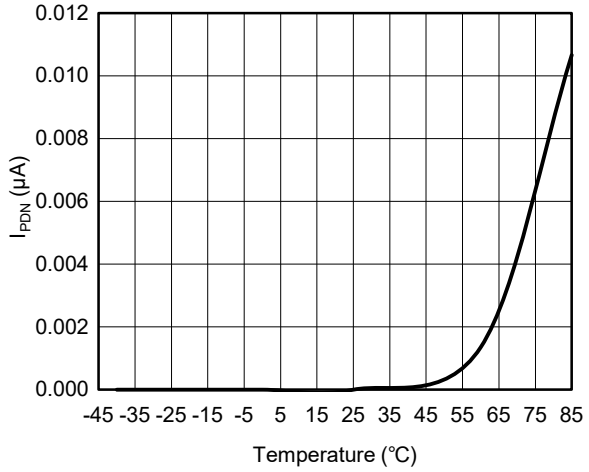
Current Consumption during Operation (I_{OPE}) vs. Temperature



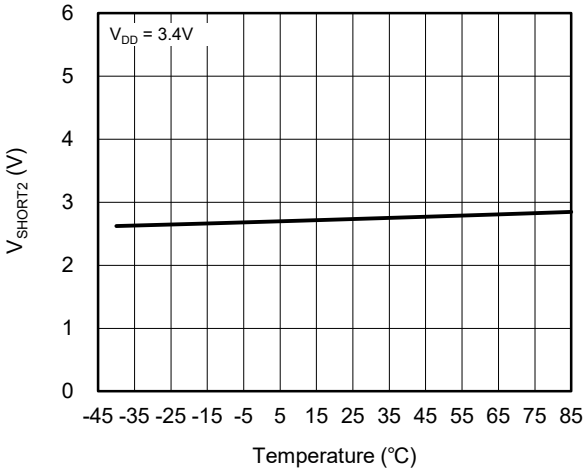
Current Consumption during Operation (I_{OPE}) vs. V_{DD}



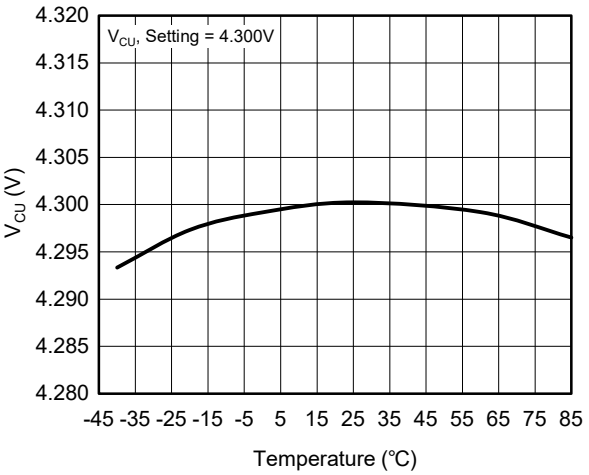
Current Consumption during Power-Down (I_{PDN}) vs. Temperature



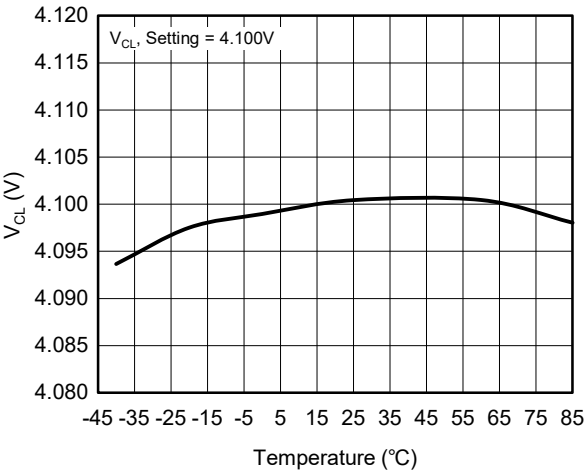
Load Short-Circuiting Detection Voltage 2 (V_{SHORT2}) vs. Temperature



Over-Charge Detection Voltage (V_{CU}) vs. Temperature

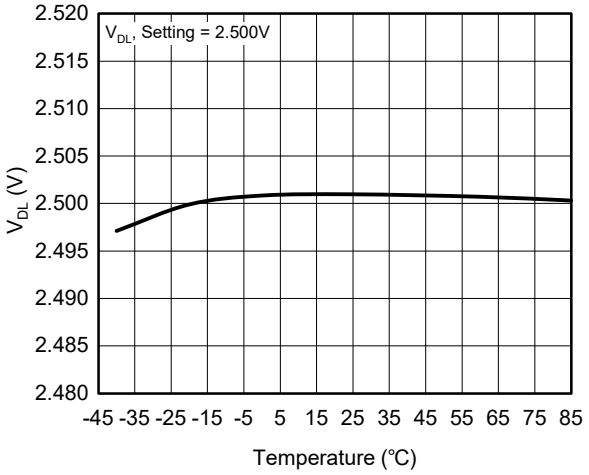


Over-Charge Release Voltage (V_{CL}) vs. Temperature

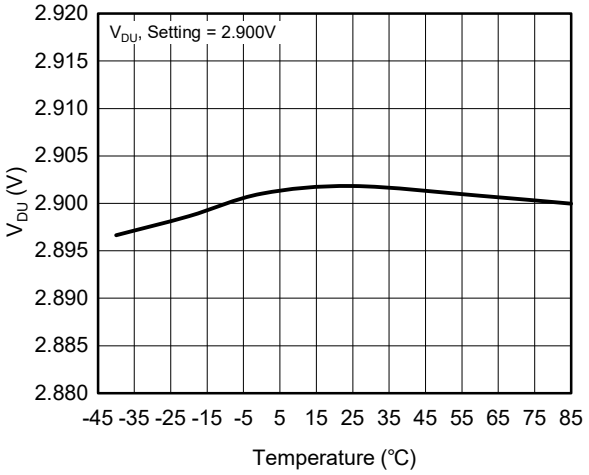


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

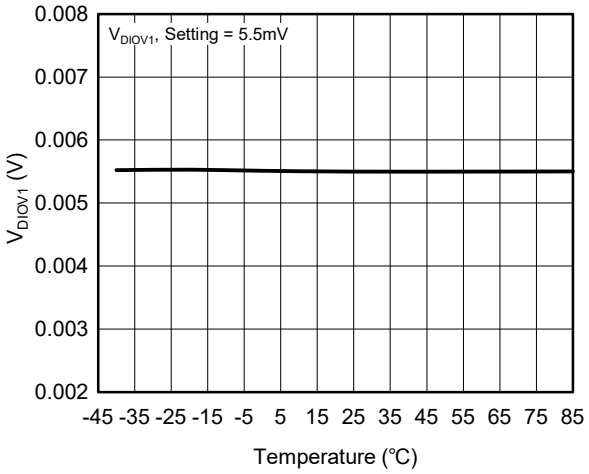
Over-Discharge Detection Voltage (V_{DL}) vs. Temperature



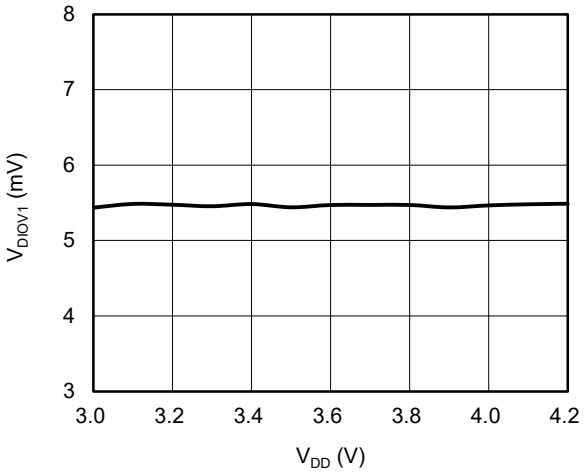
Over-Discharge Release Voltage (V_{DU}) vs. Temperature



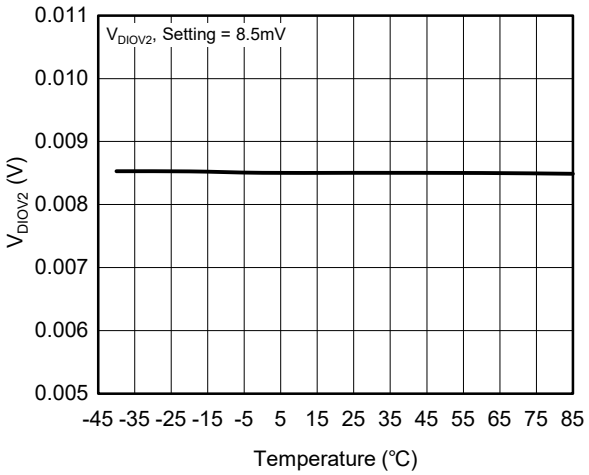
Discharge Over-Current Detection Voltage 1 (V_{DIOV1}) vs. Temperature



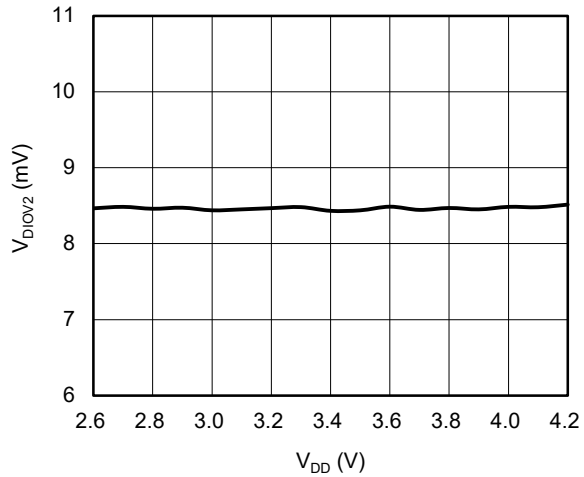
Discharge Over-Current Detection Voltage 1 (V_{DIOV1}) vs. V_{DD}



Discharge Over-Current Detection Voltage 2 (V_{DIOV2}) vs. Temperature

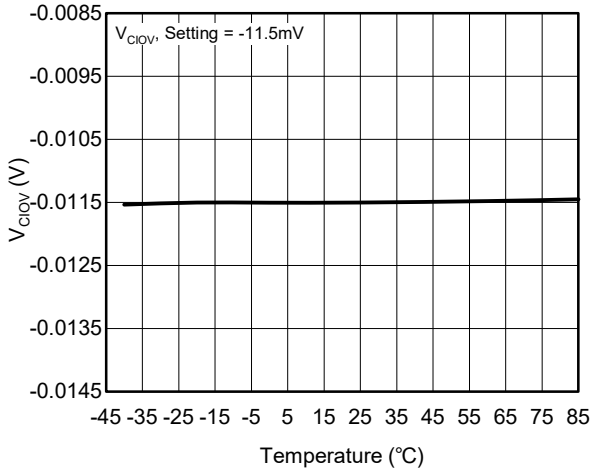


Discharge Over-Current Detection Voltage 2 (V_{DIOV2}) vs. V_{DD}

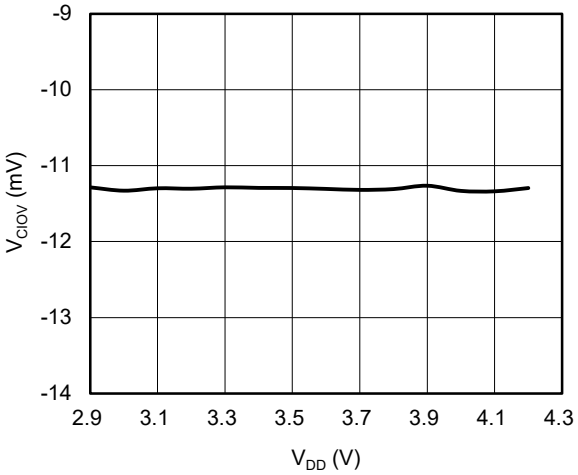


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

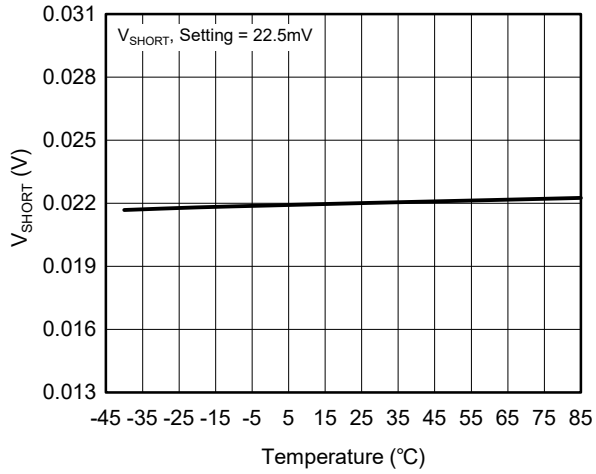
Charge Over-Current Detection Voltage (V_{CIOV}) vs. Temperature



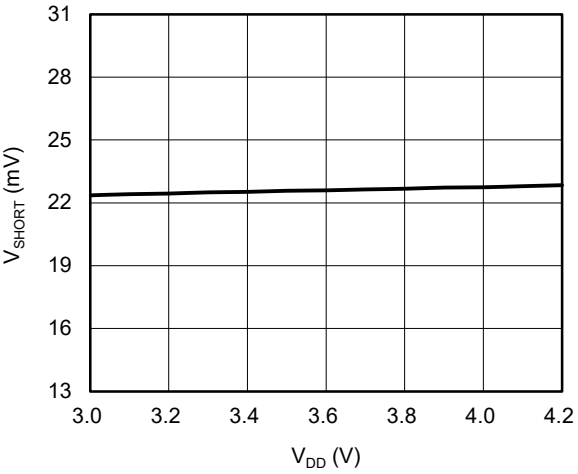
Charge Over-Current Detection Voltage (V_{CIOV}) vs. V_{DD}



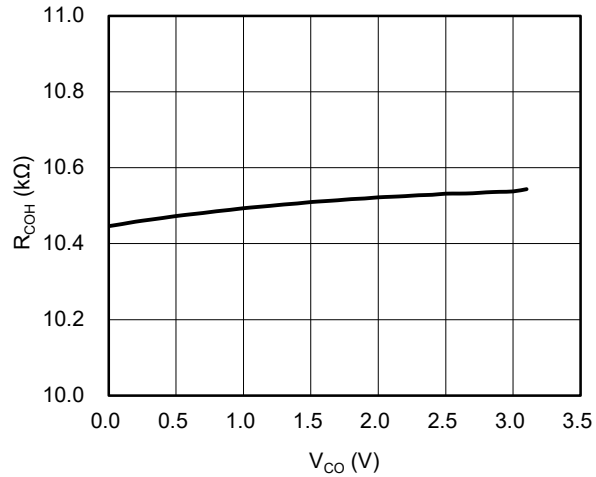
Load Short-Circuiting Detection Voltage (V_{SHORT}) vs. Temperature



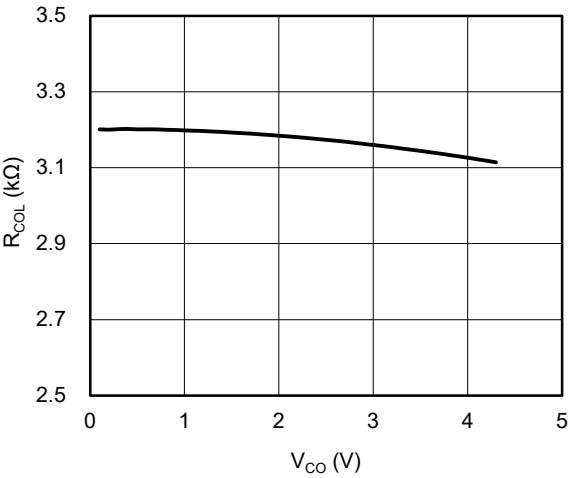
Load Short-Circuiting Detection Voltage (V_{SHORT}) vs. V_{DD}



CO Pin Resistance "H" (R_{COH}) vs. V_{CO}

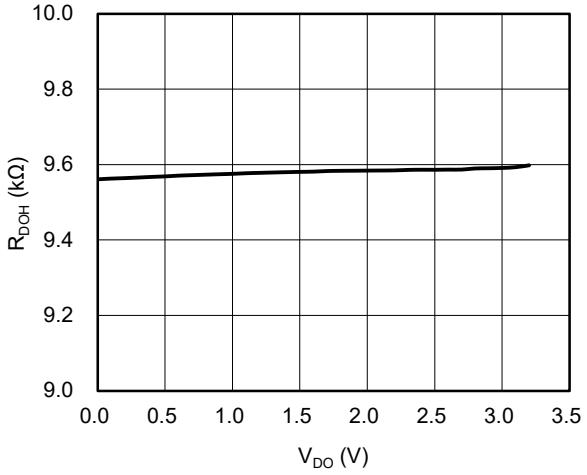


CO Pin Resistance "L" (R_{COL}) vs. V_{CO}

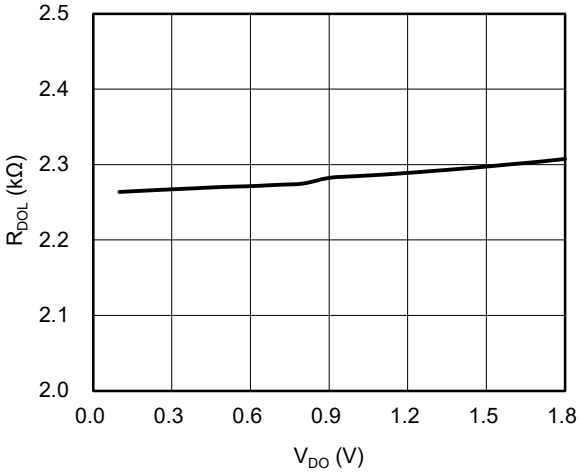


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

DO Pin Resistance "H" (R_{DOH}) vs. V_{DO}



DO Pin Resistance "L" (R_{DOL}) vs. V_{DO}



FUNCTIONAL BLOCK DIAGRAM

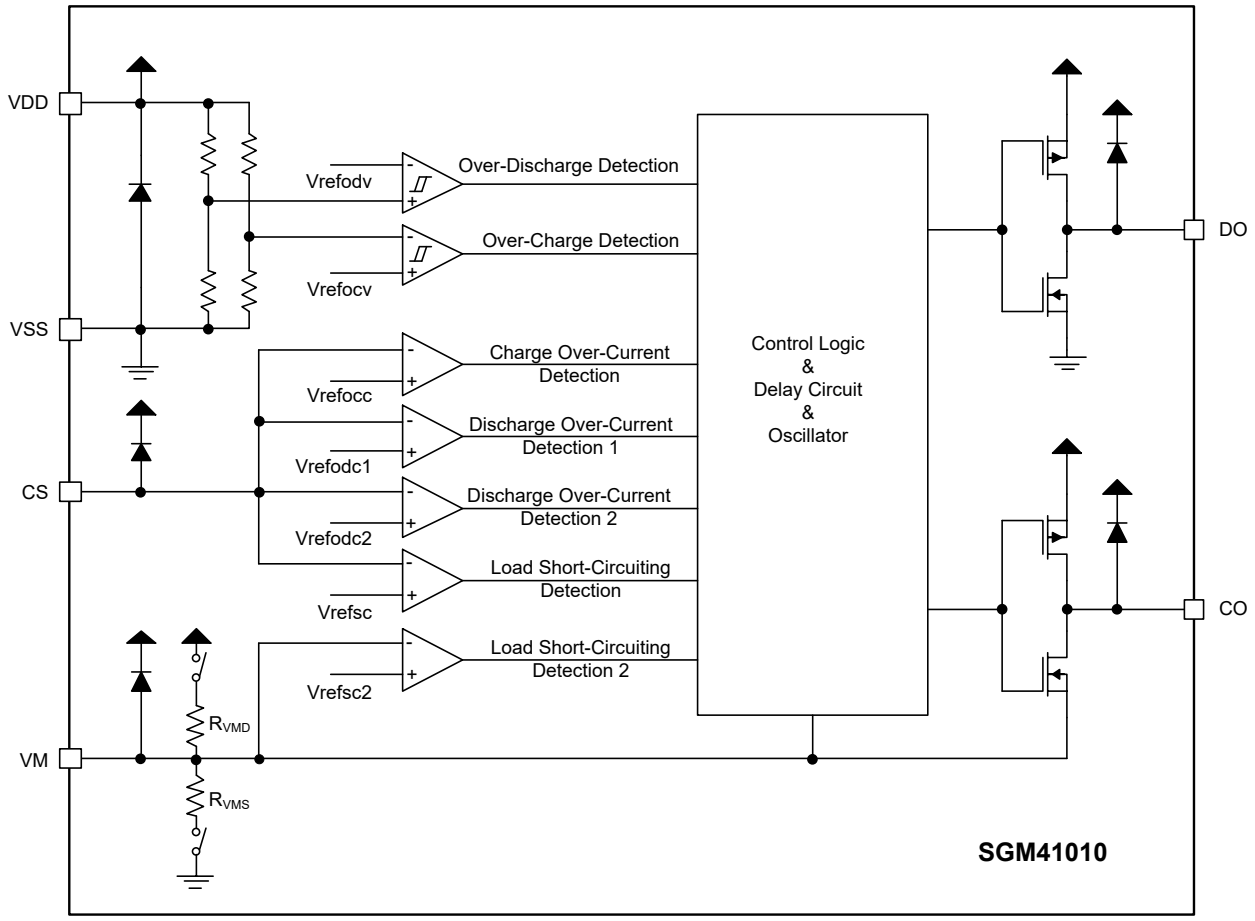


Figure 2. Block Diagram

TEST CIRCUITS

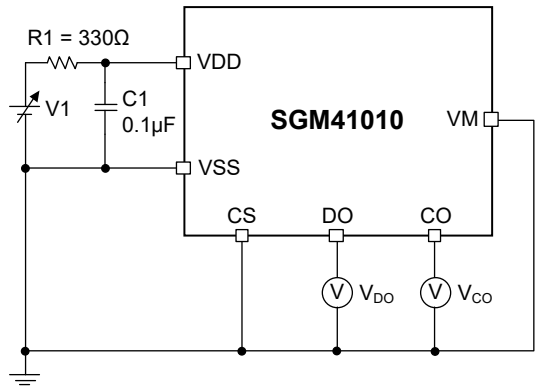


Figure 3. Test Circuit 1

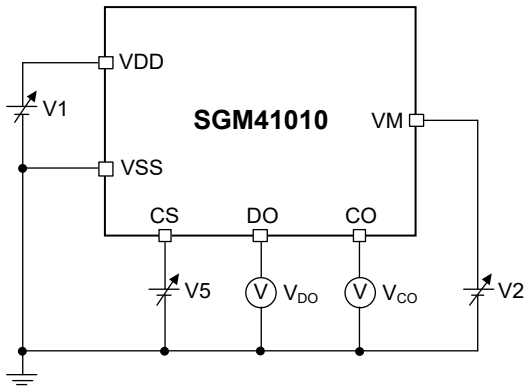


Figure 4. Test Circuit 2

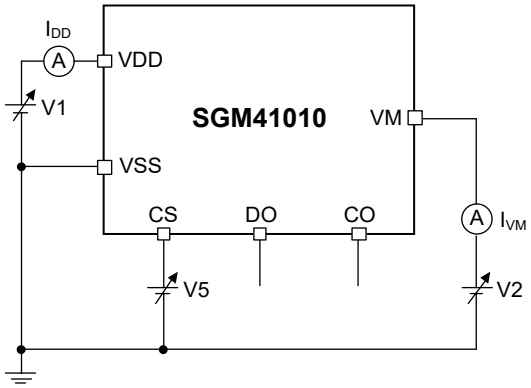


Figure 5. Test Circuit 3

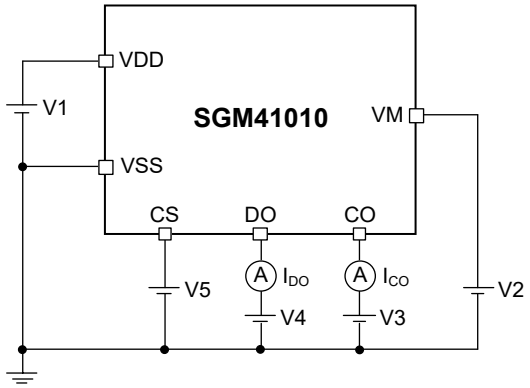


Figure 6. Test Circuit 4

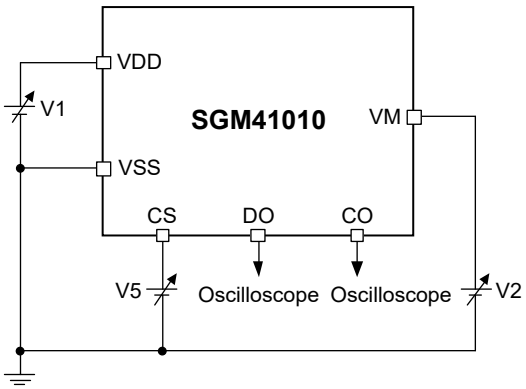


Figure 7. Test Circuit 5

TEST CIRCUITS (continued)

Note that unless otherwise specified, the CO pin output logic level respects to V_{VM} and the DO pin level respects to V_{SS}. And the output voltage levels "H" and "L" at both CO and DO pins are judged by the threshold voltage (typical 1.0V) of the N-FET.

Over-Charge Detection Voltage & Release Voltage (Test Circuit 1)

V_{CU}: Over-charge detection voltage, it is defined as the V1 voltage at which V_{CO} goes from "H" to "L" when gradually increasing V1 voltage after setting V1 = 3.4V.

V_{CL}: Over-charge release voltage, it is defined as the V1 voltage at which V_{CO} goes from "L" to "H" when gradually decreasing the V1 voltage.

V_{OCHYS}: Over-charge hysteresis voltage, it is defined as V_{CU} - V_{CL}.

Over-Discharge Detection & Release Voltage (Test Circuit 2)

V_{DL}: Over-discharge detection voltage, it is defined as the V1 voltage at which V_{DO} goes from "H" to "L" when gradually decreasing V1 voltage after setting V1 = 3.4V, V2 = V5 = 0V.

V_{DU}: Over-discharge release voltage, it is defined as the V1 voltage at which V_{DO} goes from "L" to "H" when setting V2 = 0.01V, V5 = 0V and gradually increasing the V1 voltage.

V_{ODHYS}: Over-discharge hysteresis voltage, it is defined as V_{DU} - V_{DL}.

Discharge Over-Current Detection Voltage 1 (Test Circuit 5)

V_{DIOV1}: Discharge over-current detection voltage 1, it is defined as the V5 voltage at which V_{DO} goes from "H" to "L" with a delay time t_{DIOV1} when increasing the V5 voltage after setting V1 = 3.4V, V2 = 1.4V, V5 = 0V.

Discharge Over-Current Detection Voltage 2 (Test Circuit 5)

V_{DIOV2}: Discharge over-current detection voltage 2, it is defined as the V5 voltage at which V_{DO} goes from "H" to "L" with a delay time t_{DIOV2} when increasing the V5 voltage after setting V1 = 3.4V, V2 = 1.4V, V5 = 0V.

Load Short-Circuiting Detection Voltage (Test Circuit 2)

V_{SHORT}: Load short-circuiting detection voltage, it is defined as the V5 voltage at which V_{DO} changing from "H" to "L" with a delay time t_{SHORT} when the V5 voltage increasing after setting V1 = 3.4V, V2 = 1.4V, V5 = 0V.

Load Short-Circuiting Detection Voltage 2 & Release Voltage (Test Circuit 2)

V_{SHORT2}: Load short-circuiting detection voltage 2, it is defined as the V2 voltage at which V_{DO} changing from "H" to "L" with a delay time t_{SHORT} when the V2 voltage increasing after setting V1 = 3.4V, V2 = V5 = 0V.

V_{RIOV}: Discharge over-current release voltage, it is defined as the V2 voltage at which V_{DO} goes from "L" to "H" when setting V2 = 3.4V, V5 = 0V and then gradually decreasing the V2 voltage.

V_{DO} changes to "H" after the V2 voltage falls lower than V_{RIOV} for 1ms (typical), and it maintains "H" during load short-circuiting detection delay time (t_{SHORT}).

Charge Over-Current Detection Voltage (Test Circuit 2)

V_{CIOV}: Charge over-current detection voltage, it is defined as the V5 voltage at which V_{CO} changing from "H" to "L" with a charge over-current detection delay time (t_{CIOV}) when the V5 voltage decreasing after setting V1 = 3.4V, V2 = V5 = 0V.

Current Consumption (Test Circuit 3)

I_{OPE}: Current consumption during operation, it is defined as the current that flows through the VDD pin (I_{DD}) under conditions of V1 = 3.4V, V2 = V5 = 0V during operation.

I_{PDN}: Current consumption during power-down, it is defined as I_{DD} under conditions of V1 = V2 = 1.4V, V5 = 0V during power-down.

Resistance between VDD Pin and VM Pin (Test Circuit 3)

R_{VMD}: Resistance between VDD pin and VM pin, it is tested under conditions of V1 = 1.4V, V2 = V5 = 0V.

Resistance between VM Pin and VSS Pin (Test Circuit 3)

R_{VMS}: Resistance between VM pin and VSS pin, it is tested under conditions of V1 = 3.4V, V2 = 3.2V, V5 = 0V.

TEST CIRCUITS (continued)

CO & DO Pin Resistance "H" & "L" (Test Circuit 4)

R_{COH}: CO pin resistance "H", it is defined as the resistance between the VDD pin and CO pin under conditions of V1 = 3.4V, V2 = V5 = 0V, V3 = 3.0V.

R_{COL}: CO pin resistance "L", it is defined as the resistance between the VM pin and CO pin under conditions of V1 = 4.7V, V2 = V5 = 0V, V3 = 0.4V.

R_{DOH}: DO pin resistance "H", it is defined as the resistance between the VDD pin and DO pin under conditions of V1 = 3.4V, V2 = V5 = 0V, V4 = 3.0V.

R_{DOL}: DO pin resistance "L", it is defined as the resistance between the VSS pin and DO pin under conditions of V1 = 1.4V, V2 = V5 = 0V, V4 = 0.4V.

Over-Charge & Over-Discharge Detection Delay Time (Test Circuit 5)

t_{CU}: Over-charge detection delay time, it is defined as the interval time from V1 voltage exceeds V_{CU} until V_{CO} goes to "L", after setting V1 = 3.4V, V2 = V5 = 0V and increasing V1 voltage.

t_{DL}: Over-discharge detection delay time, it is defined as the interval time from V1 voltage falls below V_{DL} until V_{DO} goes to "L", after setting V1 = 3.4V, V2 = V5 = 0V and decreasing V1 voltage.

Discharge Over-Current Detection Delay Time 1 & 2 (Test Circuit 5)

t_{DIOV1}: Discharge over-current detection delay time 1, it is defined as the interval time from V5 voltage exceeds V_{DIOV1} until V_{DO} goes to "L", after setting V1 = 3.4V, V2 = 1.4V, V5 = 0V and increasing V5 voltage.

t_{DIOV2}: Discharge over-current detection delay time 2, it is defined as the interval time from V5 voltage exceeds V_{DIOV2} until V_{DO} goes to "L", after setting V1 = 3.4V, V2 = 1.4V, V5 = 0V and increasing V5 voltage.

Load Short-Circuiting Detection Delay Time (Test Circuit 5)

t_{SHORT}: Load short-circuiting detection delay time, it is defined as the interval time from V5 voltage exceeds V_{SHORT} until V_{DO} goes to "L", after setting V1 = 3.4V, V2 = 1.4V, V5 = 0V and increasing V5 voltage.

Charge Over-Current Detection Delay Time (Test Circuit 5)

t_{CIOV}: Charge over-current detection delay time, it is defined as the interval time from V5 voltage falls below V_{CIOV} until V_{CO} goes to "L", after setting V1 = 3.4V, V2 = 1.4V, V5 = 0V and decreasing V5 voltage.

0V Battery Charge Starting Charger Voltage (0V Battery Charge Enabled Option) (Test Circuit 4)

V_{0CHA}: 0V battery charge starting charger voltage, it is defined as the absolute V2 voltage value at which the current flowing through the CO pin (I_{CO}) exceeds 1.0μA when gradually decreasing V2 voltage after setting V1 = V5 = 0V, V2 = V3 = -0.5V.

0V Battery Charge Inhibition Battery Voltage (0V Battery Charge Inhibited Option) (Test Circuit 2)

V_{0INH}: 0V battery charge inhibition battery voltage, it is defined as the V1 voltage at which V_{CO} goes to "L" ($V_{CO} = V_{VM}$) when gradually decreasing V1 voltage after setting V1 = 2.5V, V2 = -2.0V, V5 = 0V.

DETAILED DESCRIPTION

Operation

Normal Status

The SGM41010 monitors the battery voltage between VDD and VSS pins, and the voltage between CS and VSS pins to control charging and discharging.

When the battery voltage is between V_{DL} (over-discharge detection voltage) and V_{CU} (over-charge detection voltage), and the CS pin voltage is between V_{CIOV} (charge over-current detection voltage) and V_{DIOV1} (discharge over-current detection voltage 1), the SGM41010 turns both the charge and discharge control FETs on. This status is defined as normal status.

During normal status, charging and discharging can be freely, the R_{VMD} (resistance between VDD pin and VM pin) and R_{VMS} (resistance between VM pin and VSS pin) are not connected.

Over-Charge Status

$V_{CL} \neq V_{CU}$ Options

In normal status, if the battery voltage rises higher than V_{CU} during charging and it lasts for t_{CU} (over-charge detection delay time) or longer, the SGM41010 will turn the charge control FET off to stop charging. This status is defined as over-charge status, and this status can be released in the following two cases:

1. When V_{VM} < 0.35V (TYP), the SGM41010 releases the over-charge status when the battery voltage falls below V_{CL} (over-charge release voltage).
2. When V_{VM} ≥ 0.35V (TYP), the SGM41010 releases the over-charge status when the battery voltage falls below V_{CU} (over-charge detection voltage).

During over-charge status, the VM pin voltage rises due to the charge control FET's parasitic diode once a load is connected to start discharge. If V_{VM} ≥ 0.35V (TYP), the SGM41010 releases the over-charge status when the battery voltage ≤ V_{CU}.

Caution: When the battery is charged to a voltage higher than V_{CU}, even if a heavy load is connected, the battery voltage does not fall below V_{CU}, then the discharge over-current detection and load short-circuiting detection are not performed until the battery voltage falls below V_{CU}. Because the internal impedance of the actual battery is tens of mΩ, the battery voltage drops immediately after a heavy load that causes over-current is connected, and discharge over-current detection and load short-circuiting detection function.

$V_{CL} = V_{CU}$ Options

In normal status, if the battery voltage rises higher than V_{CU} during charging and it lasts for t_{CU} (over-charge detection delay time) or longer, the SGM41010 will turn the charge control FET off to stop charging. This status is defined as over-charge status.

When the VM pin voltage is equal to or higher than 0.35V (TYP) and the battery voltage falls below V_{CU}, the SGM41010 releases the over-charge status.

During over-charge status, connect a load to start discharging, the discharge current flows through the parasitic diode of the charge control FET, the VM pin voltage is the voltage V_f of the internal parasitic diode higher than the VSS pin voltage. If this VM pin voltage is higher than or equal to 0.35V (TYP), and the battery voltage is lower than or equal to V_{CU}, the SGM41010 releases the over-charge status.

Caution: 1. When the battery is charged to a voltage higher than V_{CU}, even if a heavy load is connected, the battery voltage does not fall below V_{CU}, then the discharge over-current detection and load short-circuiting detection are not performed until the battery voltage falls below V_{CU}. Because the internal impedance of the actual battery is tens of mΩ, the battery voltage drops immediately after a heavy load that causes over-current is connected, and discharge over-current detection and load short-circuiting detection function.

2. Connect a charger in the over-charge state, although the battery voltage is lower than V_{CL} and will not release the over-charge status. The over-charge status is released when the discharge current flows and the VM pin voltage goes over 0.35V (TYP) by removing the charger.

Over-Discharge Status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the over-discharge detection delay time (t_{DL}) or longer, the SGM41010 turns the discharge control FET off to stop discharging and goes to the power-down state. This status is defined as over-discharge status.

During the over-discharging state, VM is pulled up to VDD by R_{VMD}.

When a battery is not connected to a charger, the SGM41010 maintains the over-discharge status even when the battery voltage reaches V_{DU} or higher.

When connecting a charger in the over-discharge status, the battery voltage reaches V_{DL} or higher and the SGM41010 releases the over-discharge status if the VM pin voltage is below -0.35V (TYP).

DETAILED DESCRIPTION (continued)

When connecting a charger in the over-discharge status, the battery voltage reaches the over-discharge release voltage (V_{DU}) or higher and the SGM41010 releases the over-discharge status if the VM pin voltage is not below -0.35V (TYP).

R_{VMS} is disconnected during the over-discharge status.

Discharge Over-Current Status (Discharge Over-Current 1, Discharge Over-Current 2, Load Short-Circuiting, Load Short-Circuiting 2)

Discharge Over-Current 1, Discharge Over-Current 2, Load Short-Circuiting

When the battery is in a normal status, the CS pin voltage is ≥ V_{DIOV1} because the discharge current is equal to or higher than the specified value, and the continuous discharge over-current detection delay time 1 (t_{DIOV1}) or longer in this status, the discharge control FET is turned off and the discharging is stopped. After t_{RETRY}, the discharge control FET is turned on again for retrying. This status is defined as the discharge over-current status.

Under the discharge over-current status, VM pin and VSS pin are shorted by R_{VMS} in the SGM41010. However, as long as the load is connected, the VM pin voltage is the VDD pin voltage. When the load is disconnected, the VM pin voltage is equal to the VSS pin voltage.

The SGM41010 keeps retrying until the discharge over-current condition is released or the battery discharges to low when the SGM41010 turns into over-discharge status.

R_{VMD} is disconnected during the discharge over-current status.

Load Short-Circuiting 2

When the battery is in a normal status, a load causing discharge over-current is connected, and the VM pin voltage is equal to or higher than the load short-circuiting detection voltage 2 (V_{SHORT2}), and the continuous load short-circuiting detection delay time (t_{SHORT}) or longer in this status, the discharge control FET is turned off and discharging is stopped. This status is defined as the load short-circuiting status 2.

Under the load short-circuiting status 2, VM pin and VSS pin are shorted by R_{VMS} in the SGM41010. However, as long as the load is connected, the VM pin voltage is the VDD pin voltage. When the load is disconnected, the VM pin voltage is equal to the VSS pin voltage.

When the VM pin voltage returns to V_{RIOV} or lower, the SGM41010 releases the load short-circuiting status 2.

R_{VMD} is disconnected during the load short-circuiting status 2.

Charge Over-Current Status

When the battery is in a normal status, the CS pin voltage is ≤ V_{CIOV} because the charge current is equal to or higher than the specified value, and the continuous charge over-current detection delay time (t_{CIOV}) or longer in this status, the charge control FET is turned off and charging is stopped. This status is defined as the charge over-current status.

The SGM41010 releases the charge over-current status when the discharge current flows and the VM pin voltage is 0.35V (TYP) or higher by removing the charger.

There is no charge over-current protection function during the over-discharge status.

0V Battery Charge Enabled

The 0V charging function allows the charger to charge a battery with a voltage of 0V due to self-discharge. Connect a charger between PCK+ and PCK- pins, the charger voltage reaches 0V battery charge starting charger voltage (V_{0CHA}) or higher, the gate of the charge control FET is connected to the VDD pin voltage.

The external charger makes the voltage between the gate and source of the charge control FET is equal to or higher than the threshold voltage, the charge control FET begins charging at the same time, the discharge control FET is turned off, and the charging current flows through the parasitic diode of the discharge control FET. If the battery voltage is equal to or higher than V_{DL}, the SGM41010 goes back to the normal status.

Caution: 1. Some battery suppliers do not recommend charging a fully self-discharged Li-Ion rechargeable battery. Please check with your battery supplier to determine whether 0V battery charging is enabled or inhibited.

2. The 0V battery charge priority is higher than the charge over-current detection function. Therefore, a product that enables the use of the 0V battery charge is forced to charge a battery, and when the battery voltage is lower than V_{DL}, the charge over-current cannot be detected.

0V Battery Charge Inhibited

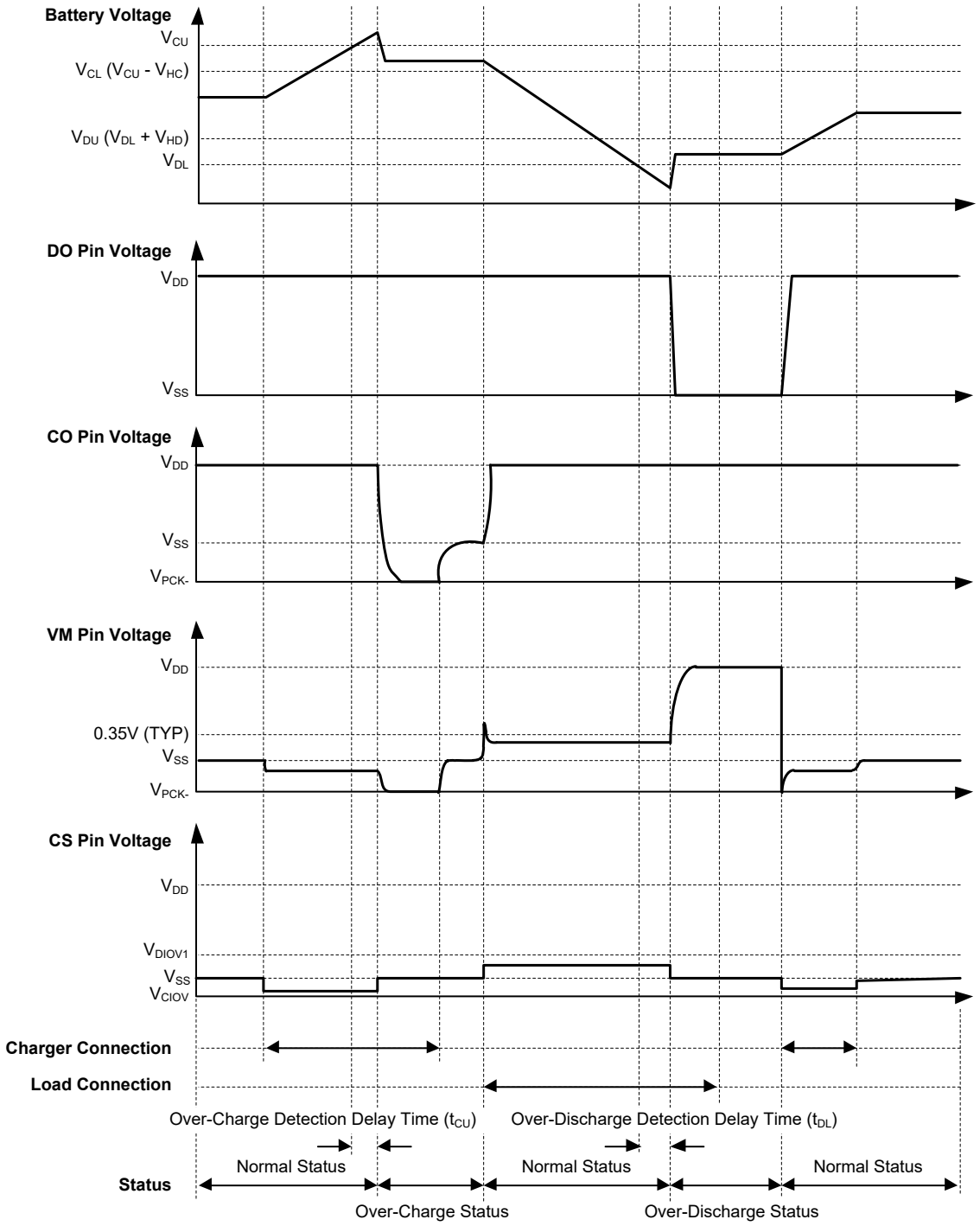
This function inhibits charging when connected to an internal short-circuited battery (0V battery). The battery voltage is equal to or lower than the 0V battery charge inhibition battery voltage (V_{0INH}), the gate of the charge control FET is connected to the PCK- pin voltage to inhibit charging. Charging starts when the battery voltage reaches V_{0INH} or higher.

Caution: Some battery suppliers do not recommend charging a fully self-discharged Li-Ion rechargeable battery. Please check with your battery supplier to determine whether 0V battery charging is enabled or inhibited.

DETAILED DESCRIPTION (continued)

Timing Charts

Over-Charge Detection, Over-Discharge Detection

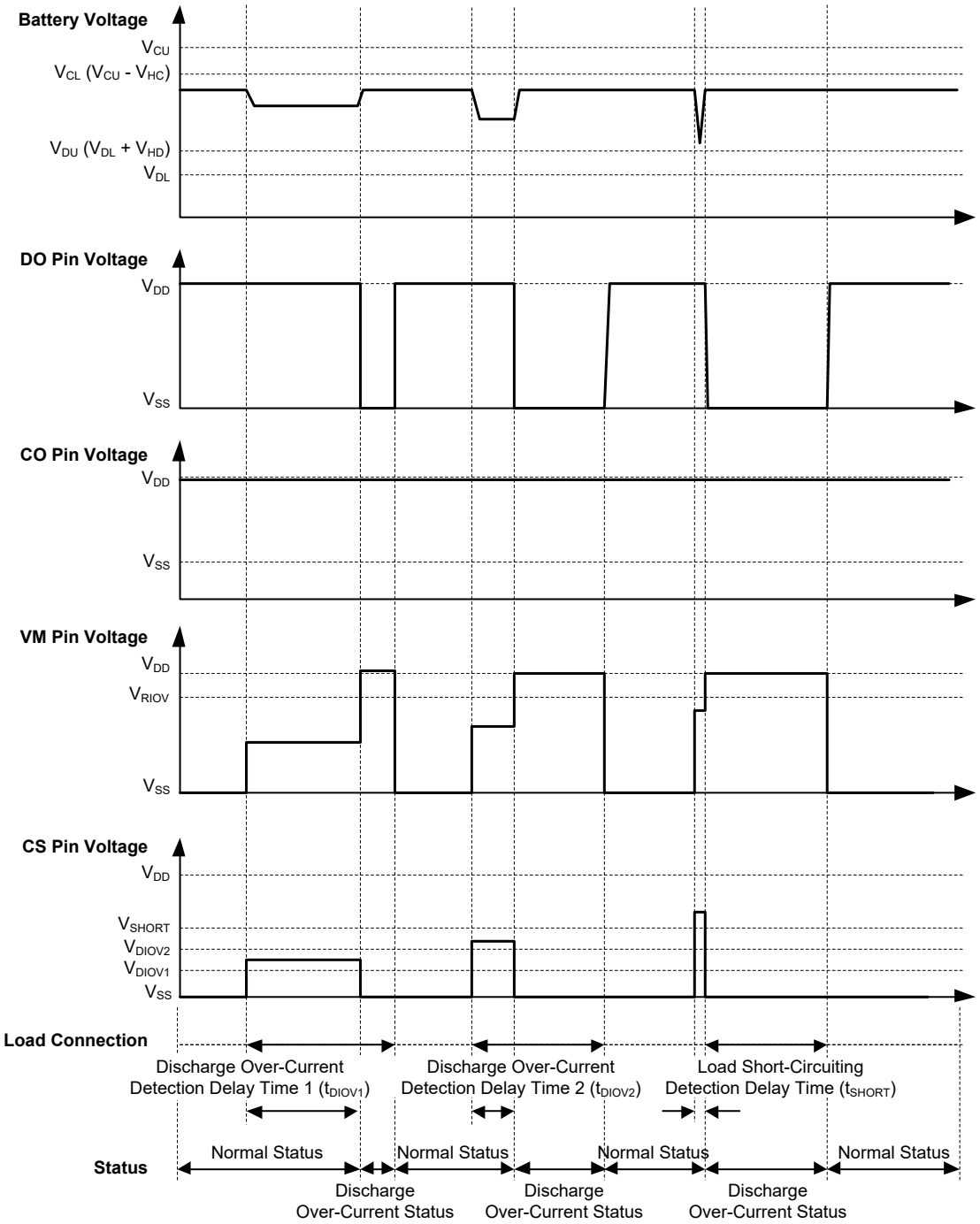


NOTE: Assume that the charger charges at constant current.

Figure 8. Over-Charge Detection, Over-Discharge Detection

DETAILED DESCRIPTION (continued)

Discharge Over-Current Detection

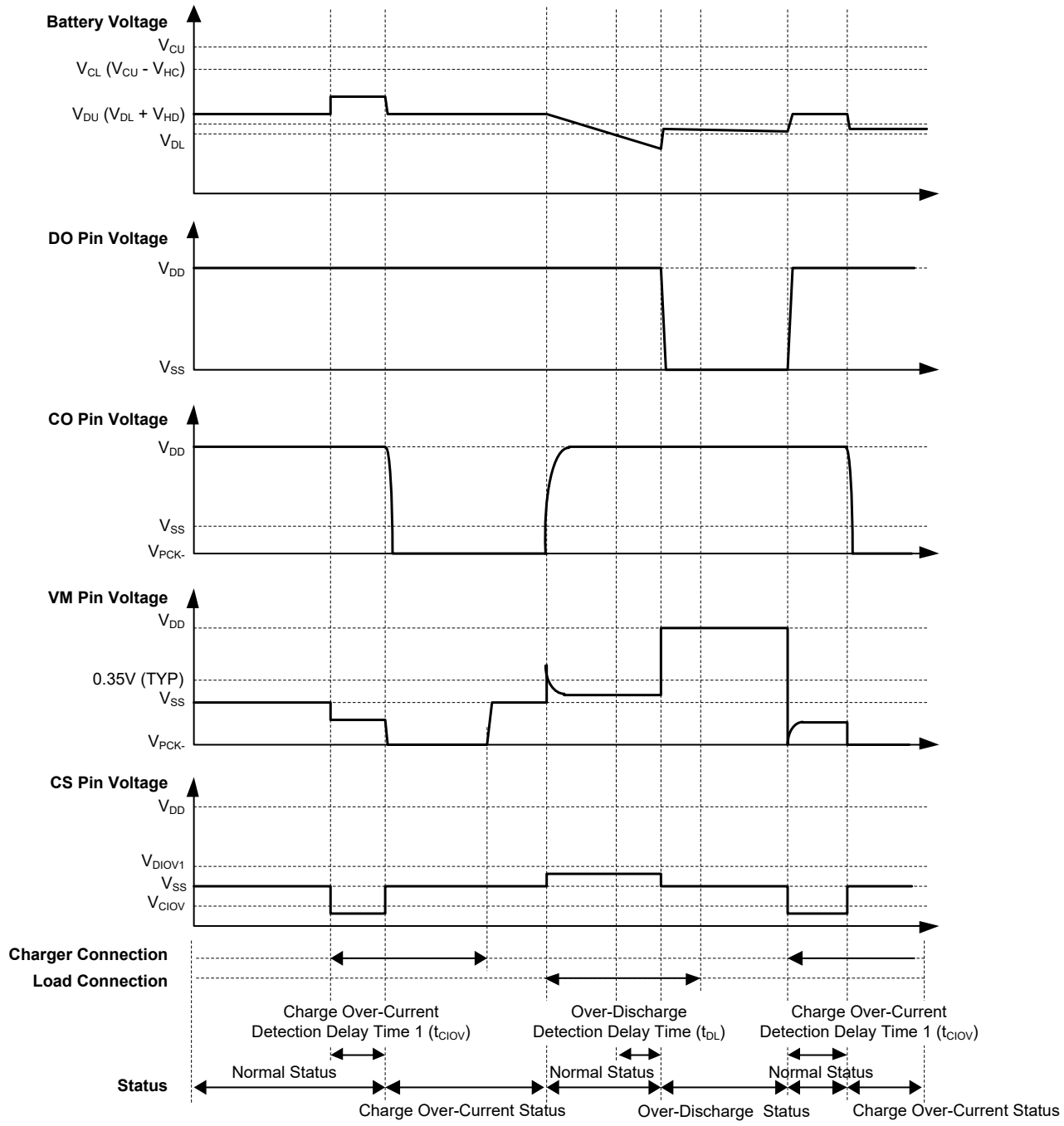


NOTE: Assume that the charger charges at constant current.

Figure 9. Discharge Over-Current Detection

DETAILED DESCRIPTION (continued)

Charge Over-Current Detection



NOTE: Assume that the charger charges at constant current.

Figure 10. Charge Over-Current Detection

DETAILED DESCRIPTION (continued)

Battery Protection IC Connection Example

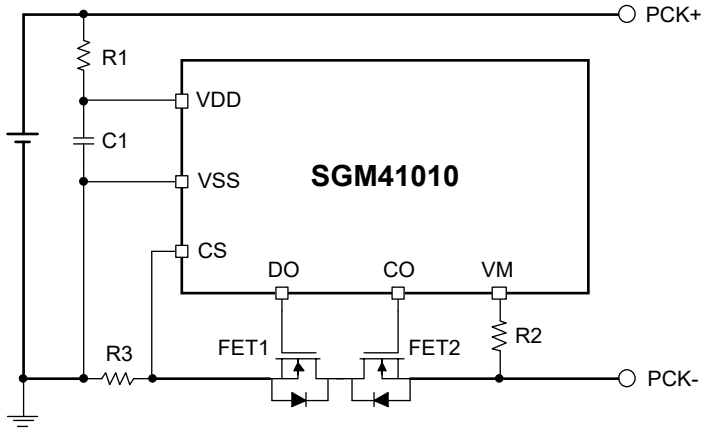


Figure 11. Battery Protection IC Connection Example

Table 4. External Components Constants (3) (4)

PARAMETER	SYMBOL	FUNCTION	MIN	TYP	MAX
Resistor	R1	ESD Protection, for Power Fluctuation	270Ω	330Ω	1.2kΩ (1)
	R2	ESD Protection, Protection for Reverse Connection of a Charger	270Ω	470Ω	1.5kΩ
	R3	Over-Current Detection		0.75mΩ	
Capacitor	C1	For Power Fluctuation	0.068μF	0.1μF	2.2μF
N-Channel MOSFET	FET1	Discharge Control Threshold Voltage ≤ Over-Discharge Detection Voltage (2)			
	FET2	Charge Control Threshold Voltage ≤ Over-Discharge Detection Voltage (2)			

NOTES:

1. The over-charge detection voltage accuracy is guaranteed by R1 = 330Ω. Setting the resistance to the other values will reduce the accuracy.

2. When using a FET with a threshold voltage equal to or higher than the over-discharge detection voltage, the discharging can be stopped before the over-discharge is detected.

3. The parameters are subject to change without notice.

4. The circuits other than the connection example have not been confirmed to operate properly, and the connection examples and constants are not guaranteed to function properly. The parameters are set based on a comprehensive evaluation of the actual application.

Precautions

• The application conditions (including the input voltage, output voltage, and load current) cannot exceed the power dissipation.

• Avoid applying an electrostatic discharge to the IC that goes beyond the rated performance of the integrated electrostatic protection circuit.

• Disclaim any dispute arising out of or in connection with the infringement of third party patents by products including this IC.

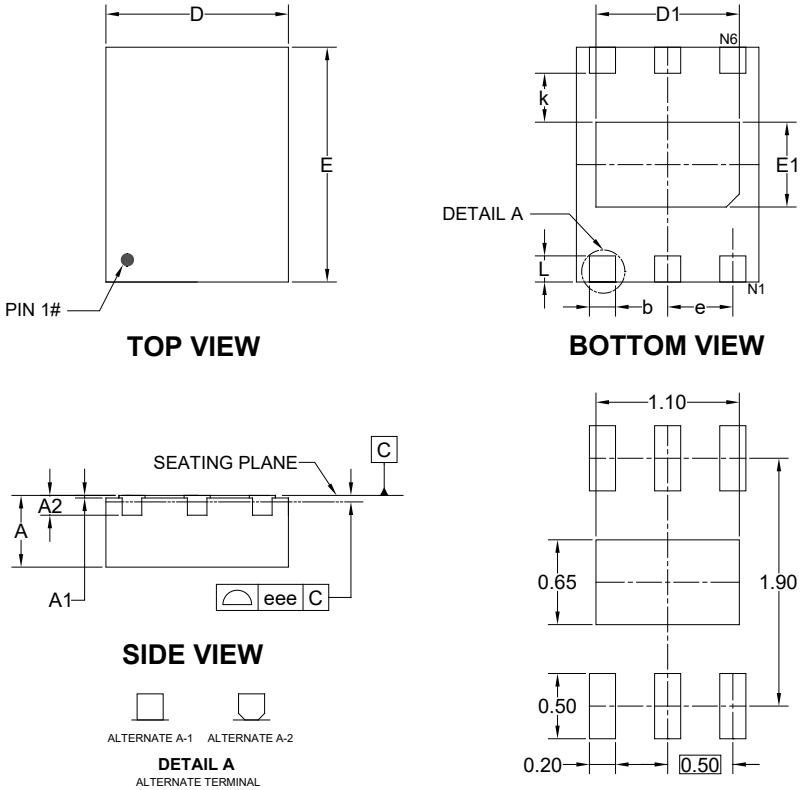
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

UTDFN-1.4×1.8-6L

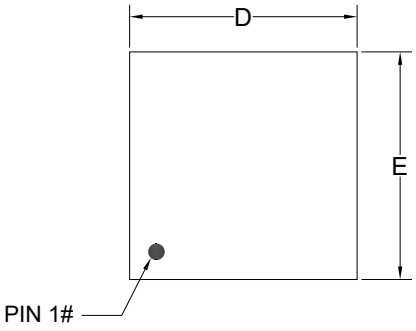


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.500	0.550	0.600
A1	0.000	-	0.050
A2	0.152 REF		
b	0.150	0.200	0.250
D	1.300	1.400	1.500
D1	1.000	1.100	1.200
E	1.700	1.800	1.900
E1	0.550	0.650	0.750
e	0.500 BSC		
k	0.375 REF		
L	0.150	0.200	0.250
eee	-	0.050	-

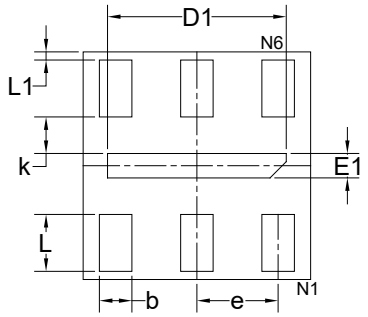
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

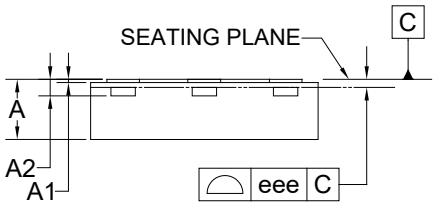
XTDFN-1.4×1.4-6L



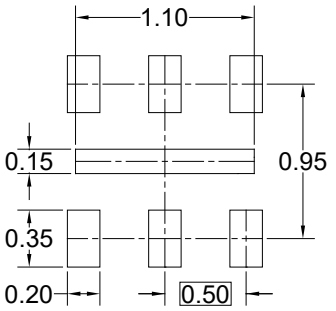
TOP VIEW



BOTTOM VIEW



SIDE VIEW



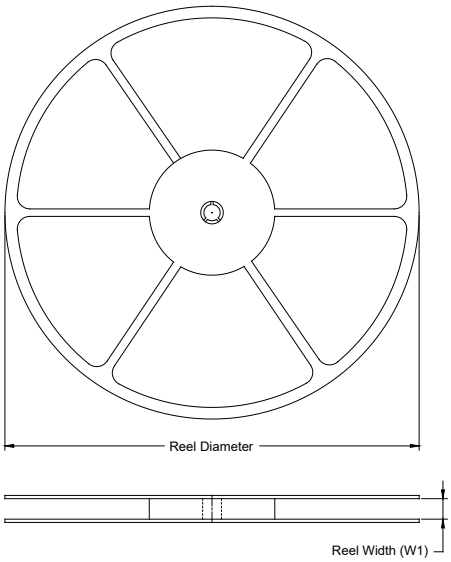
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.320	0.370	0.400
A1	0.000	-	0.050
A2	0.102 REF		
b	0.150	0.200	0.250
D	1.300	1.400	1.500
D1	1.050	1.100	1.150
E	1.300	1.400	1.500
E1	0.100	0.150	0.200
e	0.500 BSC		
k	0.225 REF		
L	0.300	0.350	0.400
L1	0.050 REF		
eee	-	0.050	-

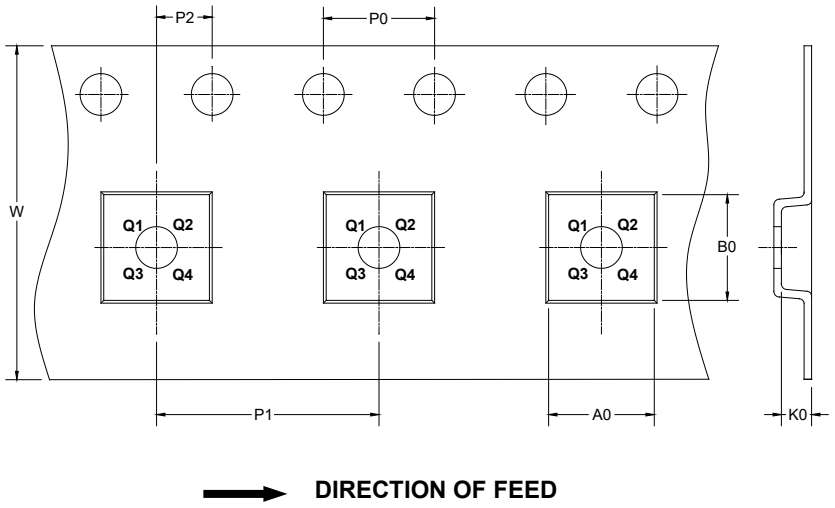
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



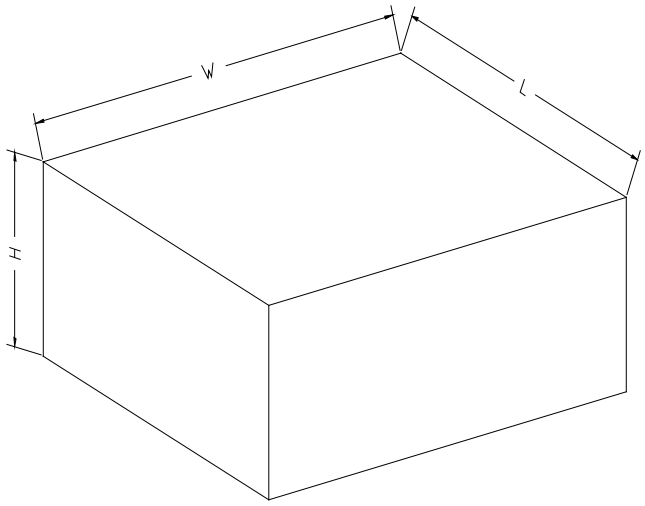
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTDFN-1.4×1.8-6L	7″	9.5	1.60	2.00	0.85	4.0	4.0	2.0	8.0	Q2
XTDFN-1.4×1.4-6L	7″	9.5	1.56	1.56	0.50	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002