# SGM6630
# High-Efficiency, Non-Synchronous Boost, SEPIC and Flyback Controller

## GENERAL DESCRIPTION

The SGM6630 is a wide $V_{IN}$, high-performance, non-synchronous Boost controller. The device is capable to support Boost, SEPIC and Flyback topologies with a low-side FET as the main switch. The device has a high adjustable and synchronizable clock frequency range from 100kHz and 1MHz to reduce the overall solution size. In addition to the cycle-by-cycle current limit, the current mode operation also provides superior bandwidth and transient response. The current limit threshold can be programmed by a single external resistor. The integrated current slope compensation makes the design process simplified.

The SGM6630 equips the built-in protection features such as thermal shutdown, internal soft-start, over-voltage protection and short-circuit protection. It consumes 3μA current in shutdown mode. The internal soft-start function can limit the inrush current when the device is turned on.

The SGM6630 is available in a Green MSOP-10 package.

## FEATURES

- **Wide Supply Voltage Range: 2.97V to 48V**
- **1A Peak Current Internal Push-Pull Driver**
- **100kHz to 1MHz Switching Frequency**
- **160mV (±20mV) Current-Sense Threshold Voltage**
- **6.5μA Shutdown Current (Over-Temperature)**
- **+27mV/-24mV Internal Reference (Over-Temperature)**
- **Frequency Compensation Optimized with a Capacitor and a Resistor**
- **Current Mode Control**
- **Adjustable Under-Voltage Lockout (UVLO) with Hysteresis**
- **Pulse Skipping at Light Loads**
- **Cycle-by-Cycle Current Limit**
- **Internal Soft-Start**
- **Thermal Shutdown**
- **Available in a Green MSOP-10 Package**

## APPLICATIONS

Start-Stop Applications
Isolated Bias Supply
One-Cell/Two-Cell Li-Ion Battery Powered Portable

## TYPICAL APPLICATION

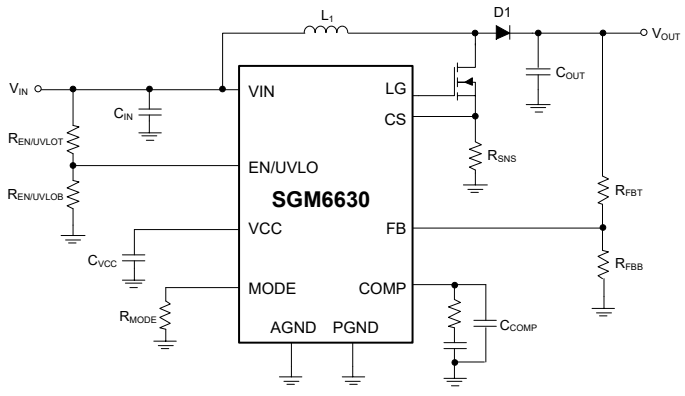
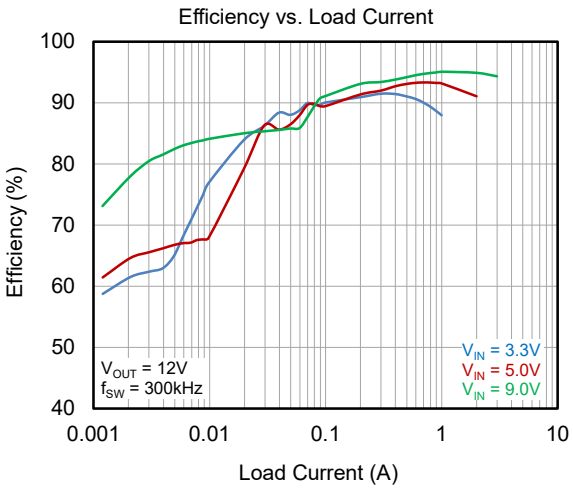



**Figure 1. Typical Application Circuit**

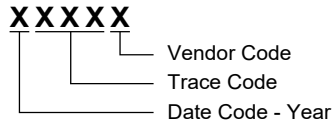


# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM6630 | MSOP-10 | -40℃ to +125℃ | SGM6630XMS10G/TR | SGM6630<br>XMS10<br>XXXXX | Tape and Reel, 4000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Pin Voltage
- VIN ..... -0.4V to 50V
- FB ..... -0.4V to 6V
- MODE ..... -0.4V to 6V
- COMP ..... -0.4V to 6V
- EN/UVLO ..... -0.4V to 6V
- VCC ..... -0.4V to 6V
- LG ..... -0.4V to 6V
- CS ..... -400mV to 600mV

Peak Driver Output Current ..... 1A

Package Thermal Resistance
- MSOP-10, $\theta_{JA}$ ..... 132.0℃/W
- MSOP-10, $\theta_{JB}$ ..... 80.4℃/W
- MSOP-10, $\theta_{JC}$ ..... 48.7℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility (1) (2)

HBM ..... ±3000V

CDM ..... ±1000V

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage, $V_{IN}$ ..... 2.97V to 48V

Switching Frequency Range ..... 100kHz to 1MHz

Operating Junction Temperature Range ..... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

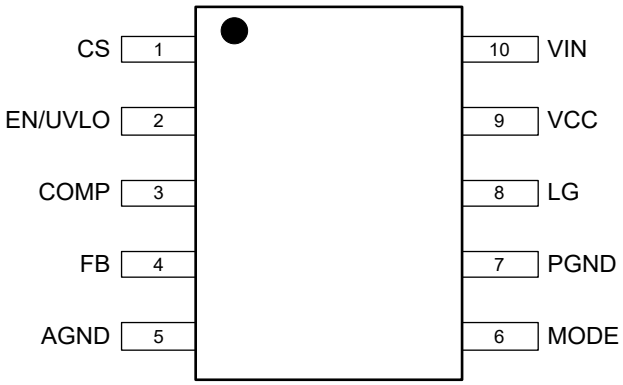
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




MSOP-10

## PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| 1 | CS | A | Current-Sense Input Pin. The voltage generated by the external sensing resistor is fed into this pin. |
| 2 | EN/UVLO | A | Under-Voltage Lockout Pin. This pin connects a resistor divider that is put between the VIN pin and AGND. The ratio of the resistance determines the input voltage that allows switching and the hysteresis to disable switching. |
| 3 | COMP | A | Compensation Pin. The control loop's compensation is provided by the resistor and capacitor connected to the COMP pin. |
| 4 | FB | A | Voltage Feedback. Inverting input of the error amplifier. |
| 5 | AGND | G | Analog Ground. Internal bias circuitry reference. Connected to power ground at a single point. |
| 6 | MODE | I/A | Frequency Adjust, Synchronization, and Shutdown Pin. A resistor is used to program the oscillator frequency. The external clock signal in this pin will synchronize the controller to the clock frequency. A high level on this pin (≥ 30μs) will disable the device and it will draw 3μA from the power supply. |
| 7 | PGND | G | Power Ground. External power circuitry reference. Should be connected to AGND at a single point. |
| 8 | LG | O | Drive Pin. Connect the gate of the external MOSFET to this pin. |
| 9 | VCC | O | Supply Voltage Pin. Connect this pin to ground with a bypass capacitor. Do not bias externally. |
| 10 | VIN | P | Power Supply. |

NOTE: A = analog, I = input, I/A = input/analog, O = output, P = power, G = ground.

# ELECTRICAL CHARACTERISTICS

($T_J$ = -40℃ to +125℃, $V_{IN}$ = 12V, $R_{MODE}$ = 40kΩ, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Feedback Voltage | $V_{FB}$ | $V_{COMP}$ = 1.4V, 2.97V ≤ $V_{IN}$ ≤ 48V | 1.254 | 1.278 | 1.305 | V |
| Feedback Voltage Line Regulation | $\Delta V_{LINE}$ | 5V ≤ $V_{IN}$ ≤ 48V, $I_{OUT}$ = 1A | | 0.003 | | %/V |
| Output Voltage Load Regulation | $\Delta V_{LOAD}$ | $V_{IN}$ = 12V, 10mA ≤ $I_{OUT}$ ≤ 2A | | 0.05 | | %/A |
| Under-Voltage Lockout Reference Voltage | $V_{UVLO\_SEN}$ | $V_{UVLO}$ ramping down | 1.38 | 1.44 | 1.495 | V |
| UVLO Source Current | $I_{UVLO}$ | Enabled | 1.5 | 5 | 8.7 | μA |
| UVLO Shutdown Voltage | $V_{UVLO\_SD}$ | $T_J$ = +25℃ | 0.65 | 0.71 | 0.78 | V |
| COMP Pin Sink Current | $I_{COMP}$ | $V_{FB}$ = 0V | | 850 | | μA |
| COMP Pin Voltage | $V_{COMP}$ | $V_{FB}$ = 1.278V | | 1.2 | | V |
| Nominal Switching Frequency | $f_{NOM}$ | $R_{MODE}$ = 40kΩ | 410 | 460 | 520 | kHz |
| Threshold for Synchronization on MODE Pin | $V_{SYNC\_H}$ | Synchronization voltage rising | | 1.4 | | V |
| | $V_{SYNC\_L}$ | Synchronization voltage falling | | 0.7 | | |
| High-side On-Resistance | $R_{DSON\_H}$ | $I_{LG}$ = 0.2A, $V_{IN}$ = 5V | | 3.6 | | Ω |
| Low-side On-Resistance | $R_{DSON\_L}$ | $I_{LG}$ = 0.2A | | 0.92 | | Ω |
| Maximum Drive Voltage Swing (1) | $V_{LG\_MAX}$ | $V_{IN}$ < 5V | | VIN | | V |
| | | $V_{IN}$ ≥ 5V | | 5 | | |
| Maximum Duty Cycle | $D_{MAX}$ | $R_{MODE}$ = 40kΩ | 82 | 88.5 | | % |
| Minimum On-Time | $t_{MIN\_ON}$ | | | 250 | 360 | ns |
| Supply Current (Switching) (2) | $I_{SUPPLY}$ | | | 0.64 | 0.97 | mA |
| Quiescent Current in Shutdown Mode (3) | $I_Q$ | $V_{MODE}$ = 3V, $V_{IN}$ = 12V | | 8.6 | 14.5 | μA |
| | | $V_{MODE}$ = 3V, $V_{IN}$ = 5V | | 3 | 6.5 | |
| Current-Sense Threshold Voltage | $V_{SENSE}$ | | 140 | 160 | 180 | mV |
| Over-Load Current Limit Sense Voltage | $V_{SC}$ | | 200 | 220 | 240 | mV |
| Internal Compensation Ramp Voltage | $V_{SL}$ | | | 150 | | mV |
| Output Over-Voltage Protection (with Respect to Feedback Voltage) (4) | $V_{OVP}$ | $V_{COMP}$ = 1.4V | 40 | 76 | 107 | mV |
| Output Over-Voltage Protection Hysteresis | $V_{OVP\_HYS}$ | $V_{COMP}$ = 1.4V | | 60 | 119 | mV |
| Error Amplifier Transconductance | Gm | $V_{COMP}$ = 1.4V | 312 | 470 | 620 | μmho |
| Error Amplifier Voltage Gain | $A_{VOL}$ | $V_{COMP}$ = 1.4V, $I_{EAO}$ = 100μA (Source/Sink) | | 60 | | dB |
| Error Amplifier Output Current (Source/Sink) | $I_{EAO}$ | Source, $V_{COMP}$ = 1.2V, $V_{FB}$ = 1.1V | 318 | 610 | 898 | μA |
| | | Sink, $V_{COMP}$ = 1.2V, $V_{FB}$ = 1.4V | 324 | 400 | 470 | |
| Error Amplifier Output Voltage Swing | $V_{EAO}$ | Upper limit: $V_{FB}$ = 0V, COMP pin floating | 2.57 | 2.73 | 2.88 | V |
| | | Lower limit: $V_{FB}$ = 1.4V | 0.56 | 0.6 | 0.63 | |

NOTES:

1. When the input voltage is less than 5V, $V_{LG}$ is equal to it. When the input voltage is greater than or equal to 5V, $V_{LG}$ is equal to 5V.
2. In this design, the MODE pin is pulled to AGND with a 40kΩ resistor.
3. In this design, the MODE pin is pulled to 3V with a 40kΩ resistor.
4. The over-voltage protection is specified with respect to the feedback voltage, because the over-voltage protection tracks the feedback voltage. The over-voltage threshold can be calculated by adding the feedback voltage ($V_{FB}$) to the over-voltage protection specification.

## ELECTRICAL CHARACTERISTICS (continued)

($T_J$ = -40℃ to +125℃, $V_{IN}$ = 12V, $R_{MODE}$ = 40kΩ, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Internal Soft-Start Delay | $t_{SS}$ | $T_J$ = +25℃, $V_{FB}$ = 1.2V, COMP pin floating | 13 | 20 | 28 | ms |
| Drive Pin Rise Time | $t_R$ | Cgs = 3000pF, $V_{LG}$ = 0V to 3V | | 26 | | ns |
| Drive Pin Fall Time | $t_F$ | Cgs = 3000pF, $V_{LG}$ = 3V to 0V | | 13 | | ns |
| MODE Pin Shutdown Signal Threshold (5) | $V_{SD}$ | Output = high (shutdown) | | 1.39 | 1.56 | V |
| | | Output = low (enable) | 0.35 | 0.72 | | |
| MODE Pin Shutdown Pin Current | $I_{SD}$ | $V_{SD}$ = 5V | | 0.01 | | μA |
| | | $V_{SD}$ = 0V | | 67 | | |
| Thermal Shutdown | $T_{SD}$ | | | 165 | | ℃ |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | 10 | | ℃ |

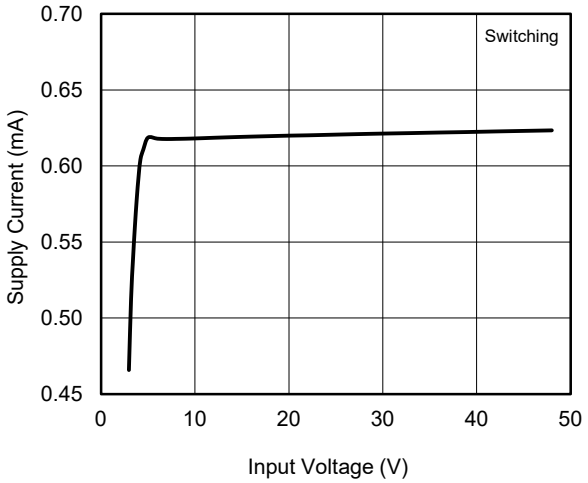
NOTE:

5. The MODE pin should be pulled to VIN through a resistor to disable the device. The voltage on the MODE pin must exceed the maximum limit for the Output = High (≥ 30μs) to disable the regulator and must be below the minimum limit for output = low to enable the regulator.

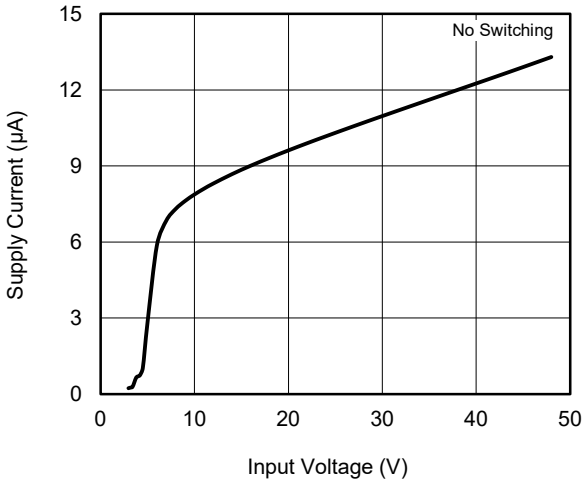
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 12V, $T_J$ = +25℃, unless otherwise noted.

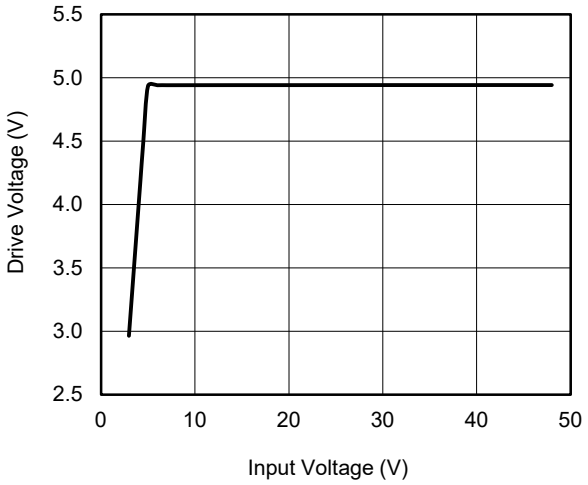
Supply Current vs. Input Voltage (Switching)



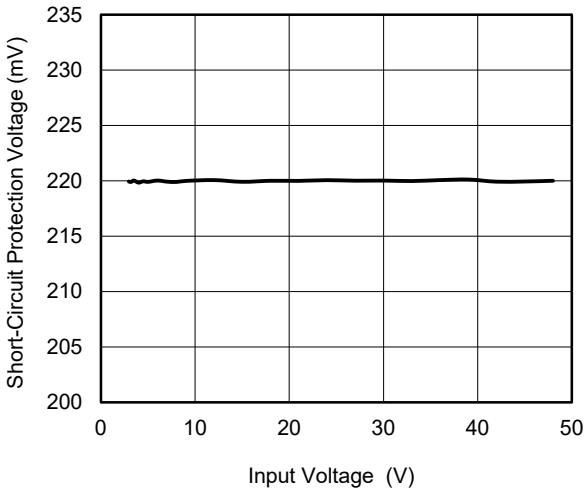

Supply Current vs. Input Voltage (No Switching)



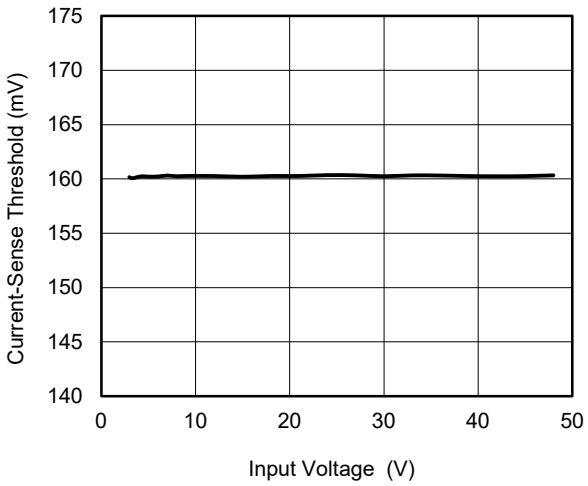

Drive Voltage vs. Input Voltage



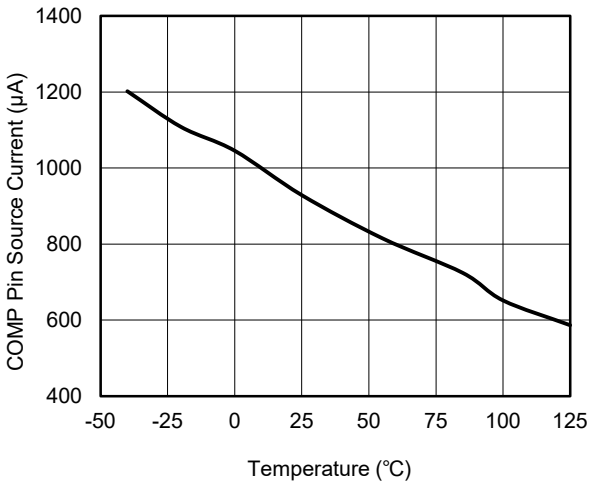

Short-Circuit Protection Voltage vs. Input Voltage




Current-Sense Threshold vs. Input Voltage



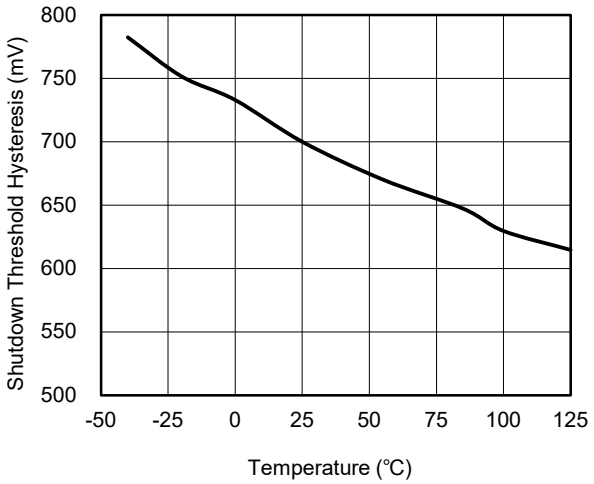

COMP Pin Source Current vs. Temperature



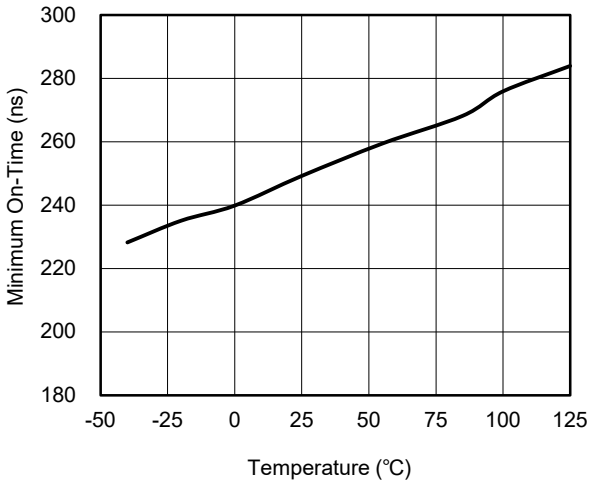
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}$ = 12V, $T_J$ = +25℃, unless otherwise noted.

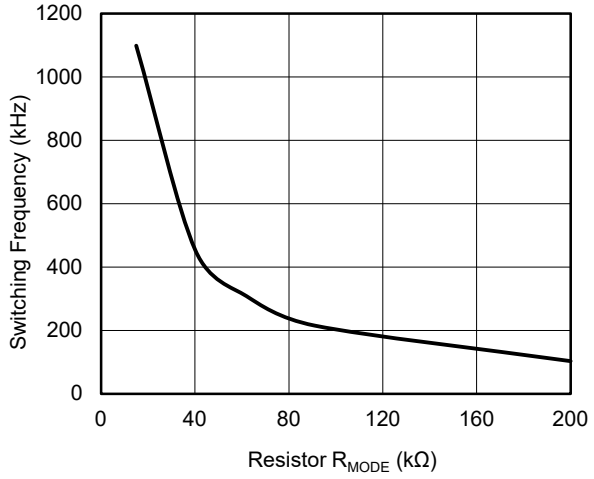
Shutdown Threshold Hysteresis vs. Temperature



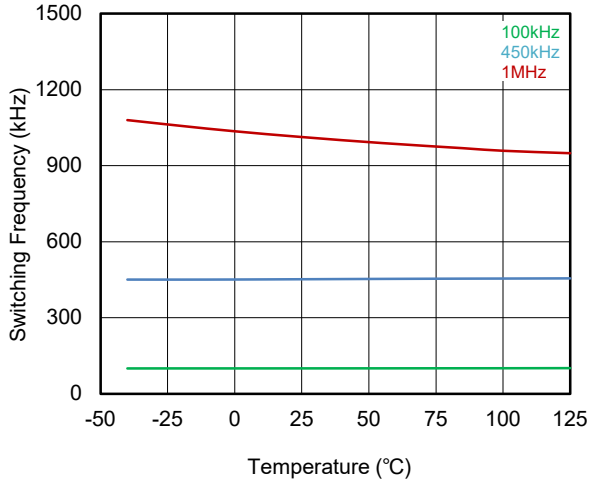

Minimum On-Time vs. Temperature



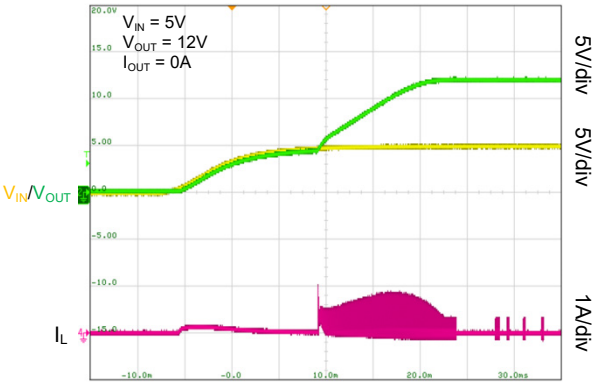

Switching Frequency vs. $R_{MODE}$




Switching Frequency vs. Temperature




Start-up




Time (5ms/div)

## FUNCTIONAL BLOCK DIAGRAM

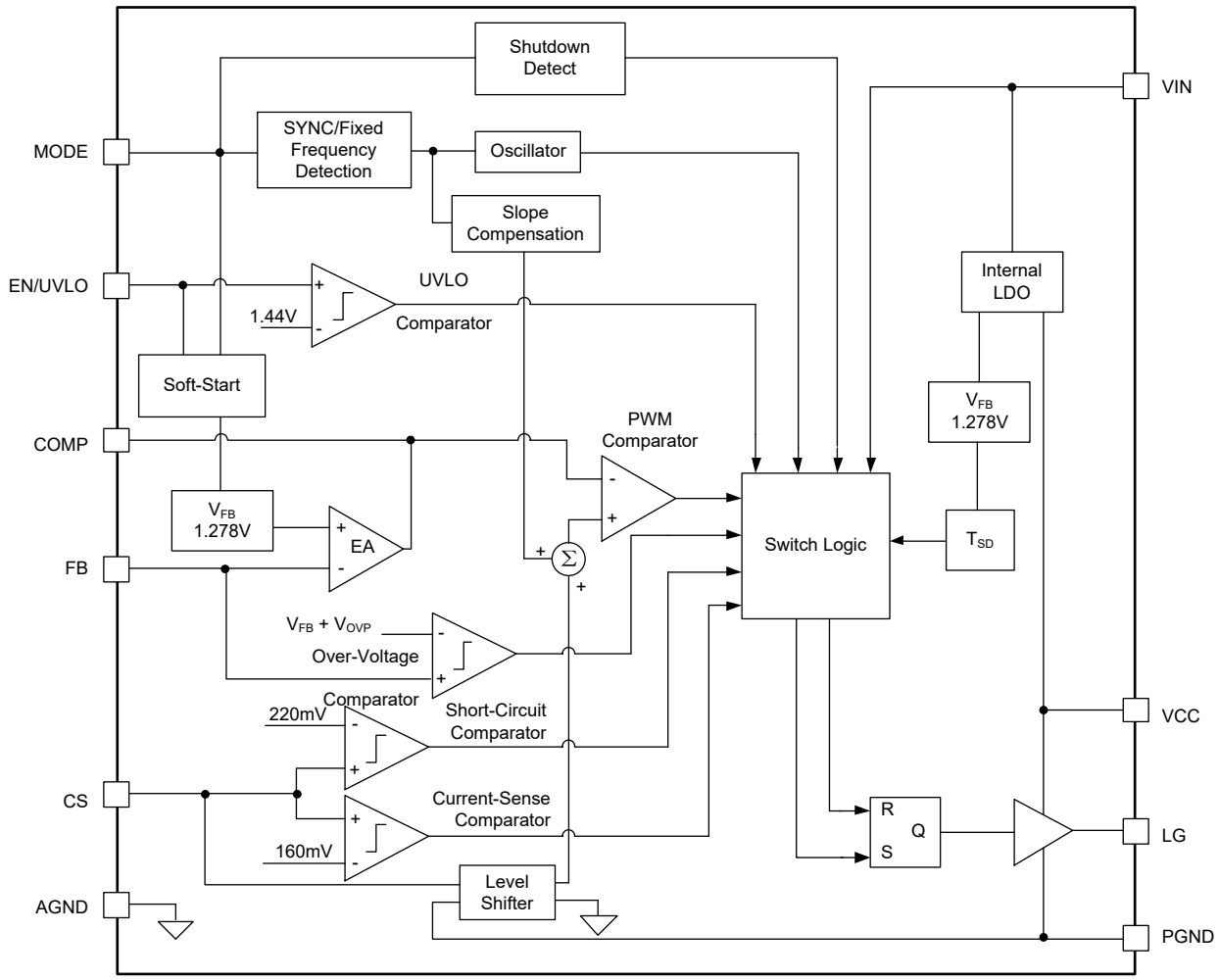



**Figure 2. Block Diagram**

# DETAILED DESCRIPTION

## Overview

The SGM6630 is a wide $V_{IN}$, high-performance, low-side N-FET controller with a fixed frequency current mode control architecture. SGM6630 generates a PWM signal through the LG pin to drive the low-side N-FET, achieving the purpose of controlling the output voltage. The peak current flowing through the external N-FET is detected through an external detection resistor and the voltage across the resistor is fed to the CS pin. This voltage, after being internally converted, is fed to the positive terminal of the comparator. The negative voltage of the PWM comparator is constituted by the voltage at the COMP pin super-imposed with the ramp compensation voltage. The output voltage, after being divided down by a certain ratio, is fed through the FB pin to the negative terminal of the error amplifier inside the controller, and the output of the error amplifier is the COMP pin.

The clock of SGM6630 periodically causes the RS latch to output high. At this time, the LG pin generates a high-level signal to turn on the low-side N-FET. When the PWM comparator output toggles to logic high, it provides a reset signal to the RS latch, and turns off the low-side N-FET.

When the low-side N-FET is turned on, it generates parasitic noise spikes across the current sensing resistor. These stray noise spikes may cause the PWM comparator to output incorrectly, leading to the premature shutdown of the low-side N-FET. Therefore, for an extremely short period after the low-side N-FET is turned on, the signal from the CS pin is blanked.

## Under-Voltage Lockout (UVLO)

SGM6630 offers a UVLO (under-voltage lockout) scheme that allows flexible configuration of enable and shutdown thresholds. The EN/UVLO pin is compared with an internal reference, and the enable threshold is determined by a resistor voltage divider. When the controller is enabled, the EN/UVLO pin provides a 5μA current, which makes the shutdown threshold lower than the enable threshold, thus creating hysteresis. The method of using UVLO is referenced in Figure 3. The actual setting of the enable threshold and the shutdown threshold can refer to Equation 1 and Equation 2. $V_{EN}$ represents the actual enable threshold, and $V_{SH}$ represents the actual shutdown threshold.

$$R_2 = \frac{1.44V}{I_{UVLO}} \times \left(1 + \frac{1.44V - V_{SH}}{V_{EN} - 1.44V}\right) \quad (1)$$

$$R_1 = R_2 \times \left(\frac{V_{EN}}{1.44V} - 1\right) \quad (2)$$

If SGM6630 is applied under a wide range of input voltages, there is a risk of over-voltage for the EN/UVLO pin, and it is recommended to connect a Zener diode to GND at the EN/UVLO pin.

When the UVLO function is not required, it is recommended to select two resistors with the same resistance greater than 100kΩ for $R_1$ and $R_2$ as shown in Figure 3. The EN/UVLO pin may also be used to implement the enable function, > 1.44V enables the device, or < 1.44V disable the device.

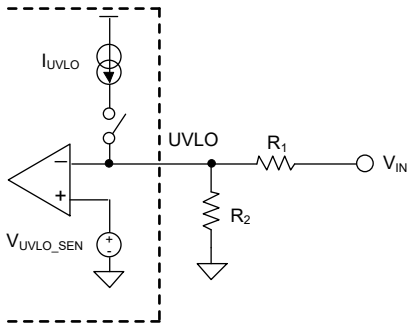



**Figure 3. UVLO Pin Resistor Divider**

## Frequency Adjust, Synchronization and Shutdown

SGM6630 can adjust the controller's switching frequency (100kHz to 1MHz) by connecting an external resistor to the MODE pin. The required external resistor can be calculated using the following Equation:

$$R_{MODE} = \frac{20158}{f_S} - 3.4 \quad (3)$$

In the Equation 3, the unit for $f_S$ is kHz, and the unit for $R_{MODE}$ is kΩ.

SGM6630 can adjust the controller's switching frequency and synchronize with an external clock by connecting an external clock to the MODE pin. As shown in Figure 4, when synchronized with an external clock, the frequency adjustment resistor can also be connected to the MODE pin, and when the external signal stops, the switching frequency is determined by the frequency adjustment resistor. It is recommended that the duty cycle of the clock synchronization signal be greater than the actual working duty cycle of the controller, and the pulse width should be ≥ 300ns.

## DETAILED DESCRIPTION (continued)

The MODE pin can be used for enabling and disabling functions. When it is high, SGM6630 will shut down and enter a low-power mode.

Figure 5 and Figure 6 respectively illustrate the shutdown function implementation schemes when operating in synchronous mode and frequency adjustment mode. In frequency adjustment mode, turning on the MOSFET as shown in the Figure 5 will force the clock to operate at a specific frequency. Turning off the MOSFET will shut down the controller. In any mode, a high-level signal exceeding 30μs will shut down the controller.

When the frequency synchronization function is not used, it is recommended to connect a 100pF in parallel with $R_{MODE}$.

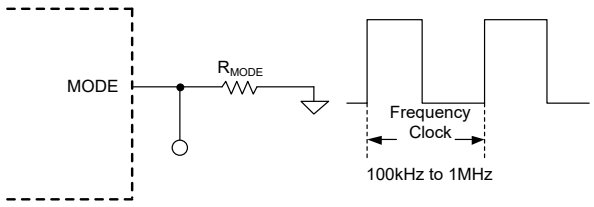



**Figure 4. Frequency Synchronization**

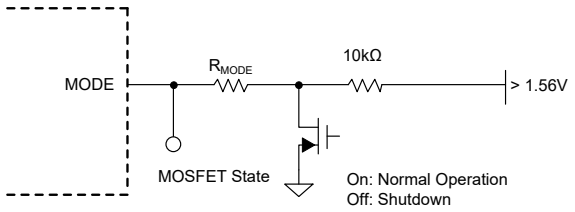



**Figure 5. Shutdown in Frequency Adjustment Mode**

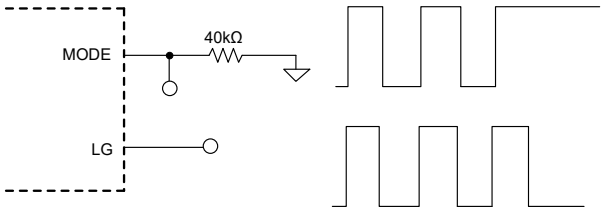



**Figure 6. Shutdown in Synchronization Mode**

### Slope Compensation Ramp

SGM6630 adopts a current mode control scheme. Current mode control has the advantages of simple loop design and a fixed switching frequency. However, in current mode operation at a duty cycle greater than 50%, there may be instability, hence there is the need for slope compensation.

The current mode control scheme samples the inductor current ($I_L$), compares the sampling signal ($V_{SENSE}$) with the internally generated control signal ($V_{COMP}$) to control the turn-off of the MOSFET, while the clock signal controls the turn-on of the MOSFET, achieving control of a switching cycle. SGM6630's current sampling is achieved by feeding the sampled voltage signal $V_{SENSE}$, through the sampling resistor $R_{SNS}$, to the CS pin.

$$V_{SENSE} = I_L \times R_{SNS} \quad (4)$$

$K_1$ represents the rising slope of $V_{SENSE}$, and $K_2$ represents the falling slope of $V_{SENSE}$.

For the Boost topology:

$$K_1 = \frac{V_{IN}}{L} \times R_{SNS} \quad (5)$$

$$K_2 = \frac{V_{OUT} - V_{IN}}{L} \times R_{SNS} \quad (6)$$

When there is no slope compensation, the control signal slope $K_C$ is equal to zero, current mode control has inherent instability when the duty cycle is greater than 50%. In Figure 7, transient load fluctuations cause changes in inductor current, leading to a $\Delta V_{SENSE0}$ change in $V_{SENSE}$. When the first switching cycle ends, $\Delta V_{SENSE1}$ becomes:

$$\Delta V_{SENSE1} = -\frac{K_2}{K_1} \times \Delta V_{SENSE0} = -\left(\frac{V_{OUT} - V_{IN}}{V_{IN}}\right) \times \Delta V_{SENSE0}$$
$$= -\left(\frac{D}{1-D}\right) \times \Delta V_{SENSE0} \quad (7)$$

From Equation 7, when the duty cycle (D) is greater than 50%, the absolute value of $\Delta V_{SENSE1}$ is greater than that of $\Delta V_{SENSE0}$. This disturbance continuously amplifies within the system, making it unstable. To ensure the convergence of the disturbance signal, it must maintain:

$$\left|-\frac{K_2}{K_1}\right| < 1 \quad (8)$$

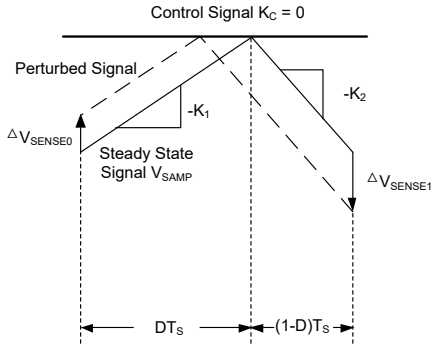



**Figure 7. Sub-harmonic Oscillation for D > 50%**

## DETAILED DESCRIPTION (continued)

In order to make the system stable, a ramp compensation signal is added to the control signal $V_{COMP}$. Then the relationship between $\Delta V_{SENSE0}$ and $\Delta V_{SENSE1}$ is as follows:

$$\Delta V_{SENSE1} = -\left(\frac{K_2 - K_C}{K_1 + K_C}\right) \times \Delta V_{SENSE0} \quad (9)$$

The condition for system stability then becomes:

$$\left|-\frac{K_2 - K_C}{K_1 + K_C}\right| < 1 \quad (10)$$

SGM6630 has built-in ramp compensation, and the designed compensation values can meet the needs of the vast majority of application scenarios. And the ramp compensation value varies proportionally with frequency:

$$K_C = f_S \times V_{SL} \quad (11)$$

In Equation 11, $f_S$ represents the switching frequency of the controller, and $V_{SL}$ is the amplitude of the internal compensation ramp.

### Over-Voltage Protection (OVP)

SGM6630 features the output over-voltage protection detected through the FB pin. When the voltage at the FB pin exceeds $V_{FB}$ + $V_{OVP}$, the over-voltage protection (OVP) is triggered.

When OVP is triggered, it forces the low-side N-FET to shut down. After the low-side N-FET is turned off, the output voltage drops. Once the output voltage falls below $V_{FB}$ + $V_{OVP}$ - $V_{OVP\_HYS}$, the device resumes normal operation. The error amplifier continues to operate normally during the OVP period.

### Short-Circuit Protection

When the voltage on the CS pin exceeds 220mV, it triggers the short-circuit protection. At this point, the switching frequency of SGM6630 will be reduced by a factor of 8 until the short-circuit condition is cleared.

### Device Function Modes

When the UVLO threshold is exceeded, SGM6630 will operate at the frequency set by the MODE pin, or at the frequency of the externally synchronized clock.

If the MODE pin is pulled high, SGM6630 will shut down.

### Bias Voltage

When the input voltage exceeds 5V, the internal bias of SGM6630 comes from the internal bias voltage generator. Otherwise, the bias voltage is directly derived from the input voltage. VCC requires an external bypass capacitor, and the choice of different MOSFETs also affects the selection of the bypass capacitor.

# APPLICATION INFORMATION

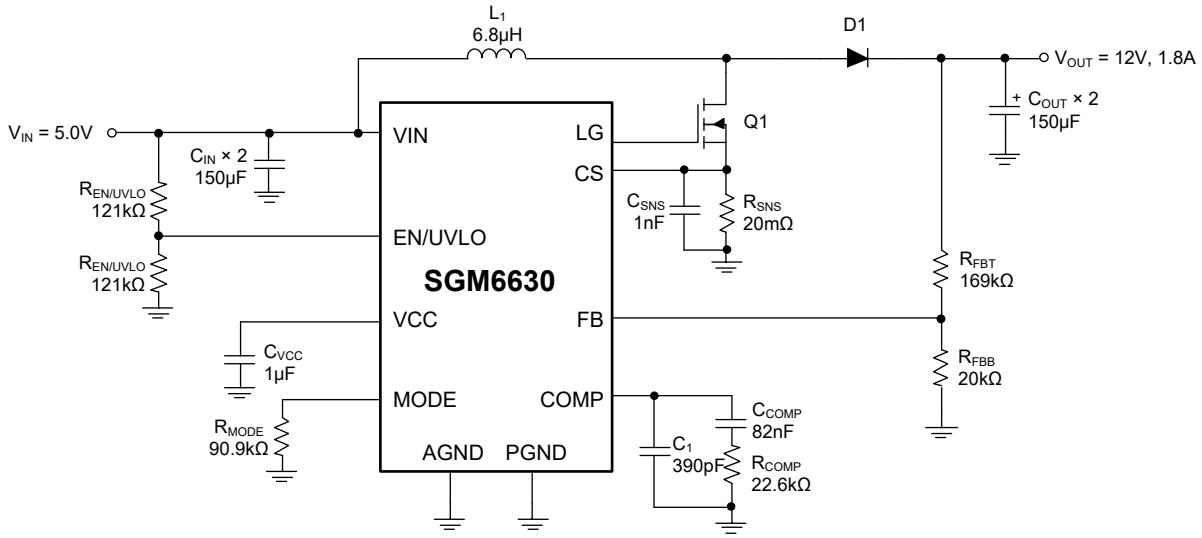



**Figure 8. Typical Boost Converter Circuit**

SGM6630 can operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The following application is designed according to continuous conduction mode (CCM).

## Working Principle of Boost Converter

SGM6630 can be used in a Boost topology. The Boost regulator solution is shown in Figure 8. When operating in continuous conduction mode (CCM), a switching cycle can be divided into two parts. In the first part, the low-side N-FET is turned on to charge the inductor. At this time, the diode is reverse-biased, and the output capacitor supplies energy to the load.

In the second part, the low-side N-FET is turned off, at which point the diode becomes forward-biased, and the inductor supplies power to the load while also charging the output capacitor. The Boost regulator controls the proportion of time for these two parts within a switching cycle to determine the output voltage.

The relationship between the output voltage and the input voltage is as follows:

$$V_{OUT} = \frac{V_{IN}}{1-D} \quad (12)$$

If considering the voltage drop across the diode and the MOSFET:

$$V_{OUT} + V_D - V_Q = \frac{V_{IN} - V_Q}{1-D} \quad (13)$$

Where D is the duty cycle, $V_D$ is the forward voltage drop of the diode, and $V_Q$ is the on-resistance voltage drop of the MOSFET. Next, it will introduce how to select the components of a Boost converter.

### Inductor

Figure 9 illustrates the changes in the inductor of the Boost converter during operation. The relationship between inductor current and voltage is known as follows:

$$V_L(t) = L \times \frac{dI_L(t)}{dt} \quad (14)$$

## APPLICATION INFORMATION (continued)

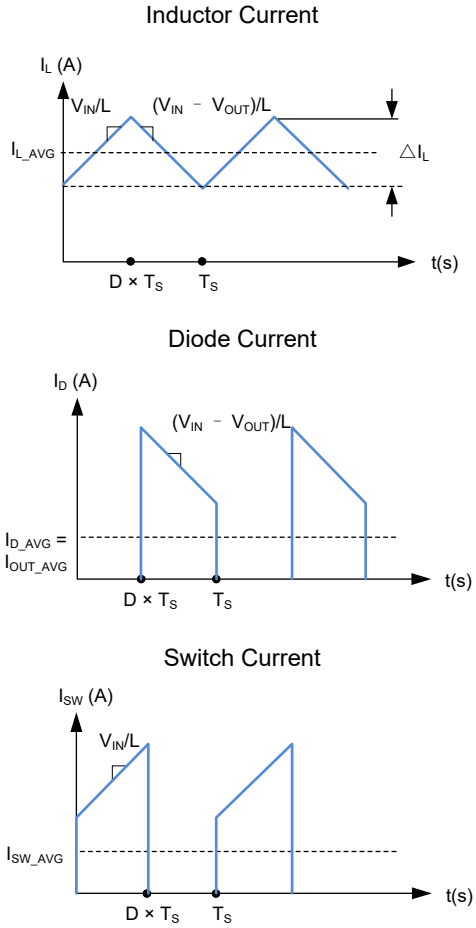



**Figure 9. Inductor Current vs. Diode Current vs. Switch Current**

With the input voltage and output voltage determined, the rise and fall slopes of the inductor current are also established.

When determining the inductance value, it is necessary to first confirm the desired ripple current $\Delta I_L$. When $\Delta I_L/2$ is greater than the average inductor current $I_L$, the Boost converter operates in discontinuous conduction mode. Conversely, the Boost converter operates in continuous conduction mode. Therefore, the condition for the Boost converter to operate in continuous conduction mode is as follows:

$$I_L > \frac{\Delta I_L}{2} \quad (15)$$

$$\frac{I_{OUT}}{1-D} = \frac{DV_{IN}}{2f_SL} \quad (16)$$

$$L > \frac{D(1-D)V_{IN}}{2I_{OUT}f_S} \quad (17)$$

Select the minimum output current ($I_{OUT}$) for operation in continuous conduction mode to determine the minimum inductance. Typically, the ripple current $\Delta I_L$ is set to 30% of the inductor current $I_L$ at maximum load. When selecting the inductor, the expected peak current is also required. The peak current calculation for the Boost converter is as follows:

$$I_L = \frac{I_{OUT}}{1-D} \quad (18)$$

$$\Delta I_L = \frac{DV_{IN}}{f_SL} \quad (19)$$

$$I_{L\_PEAK} = I_{L(MAX)} + \frac{\Delta I_L}{2} \quad (20)$$

If the inductor's rated current is too small, it may cause the inductor to saturate during use, leading to issues such as low efficiency and abnormal inductor current.

SGM6630 can flexibly set the switching frequency. When set at a higher switching frequency, the Boost converter can use an inductor with a relatively lower inductance value.

SGM6630 detects the peak current passing through the low-side N-FET, which is the same as the first half of the inductor current.

### Output Voltage and Output Current Programming

The output voltage of the Boost converter is determined by the voltage divider ratio between the output voltage and the FB Pin. The voltage division method is shown in Figure 10. The output voltage calculation Equation is as follows:

$$V_{OUT} = 1.278 \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right) \quad (21)$$

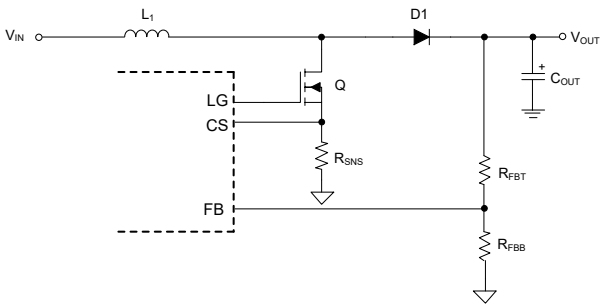



**Figure 10. Adjusting the Output Voltage**

## APPLICATION INFORMATION (continued)

In some cases, a 100pF capacitor can be connected between the FB pin and GND to improve noise performance.

The maximum peak current of the inductor in the Boost converter can be controlled by the detection resistor $R_{SNS}$. The actual corresponding inductor current limit relationship is shown in the following Equation:

$$I_{SW\_PEAK} \times R_{SNS} = 160mV - D \times V_{SL} \quad (22)$$

From the above, it is known that:

$$I_{SW\_PEAK} = I_{L\_MAX} + \frac{\Delta I_L}{2} \quad (23)$$

So in the application of a Boost converter:

$$I_{SW\_PEAK} = \frac{I_{OUT\_MAX}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L} \quad (24)$$

It can be deduced that $R_{SNS}$ can be calculated according to the following Equation:

$$R_{SNS} = \frac{V_{SENSE} - (D \times \Delta V_{SL})}{\frac{I_{OUT\_MAX}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L}} \quad (25)$$

It is recommended to calculate $R_{SNS}$ under the conditions of the maximum and minimum values of $V_{IN}$, and finally take the smaller value.

### Power Diode

The average current through the diode is equal to the output current of Boost converter. The current stress of the diode is the same as the peak current so that the rated current of the diode should be greater than the peak inductor current. The rated current can be calculated by a certain formula as shown below:

$$I_{D\_PEAK} = \left(\frac{I_{OUT}}{1-D}\right) + \frac{\Delta IL}{2} \quad (26)$$

Where $I_{OUT}$ is the load current and $\Delta I_L$ is the current ripple of inductor.

The voltage stress of the diode is the same as the output voltage. It is recommended to select a diode which rated voltage is greater than the peak regulated voltage. For better efficiency, a Schottky diode with a low forward voltage drop is recommended.

### MOSFET

The LG pin of SGM6630 is used to drive the external power MOSFET. The voltage of the LG is 5V when $V_{IN}$ is higher than 5V. It follows $V_{IN}$ when $V_{IN}$ < 5V. In this way, a common MOS is suitable for this application. For extremely low input voltages, a sub-logic level MOSFET should be used. The voltage stress of the MOSFET is the same as the output voltage. It is recommended to choose an appropriate MOS by checking the parameters as shown:

- $V_{GSTH}$
- $V_{DS\_MAX}$
- $R_{DSON}$ vs. $V_{LG}$

The MOSFET affects the efficiency directly by the parameters as shown below:

- Qg
- $R_{DSON}$
- $E_{ON}/E_{OFF}$

To check the worst case for conduction loss, the minimum input voltage leads to the maximum duty cycle. The conduction loss is calculated by:

$$P_{COND\_MAX} = \left(\frac{I_{OUT\_MAX}}{1-D_{MAX}}\right)^2 \times D_{MAX} \times R_{DSON} \quad (27)$$

Where $D_{MAX}$ is derived as:

$$D_{MAX} = \left(1 - \frac{V_{IN\_MIN}}{V_{OUT}}\right) \quad (28)$$

Equation 29 below provides a method to evaluate the switching loss:

$$P_{SW} = (E_{ON} + E_{OFF}) \times f_{SW} \quad (29)$$

## APPLICATION INFORMATION (continued)

### $C_{IN}$

In a Boost converter, the inductor at the input makes the input current waveform continuous and triangular. It reduces ripple currents for the input capacitor. A smaller input capacitor leads to increased input ripple. The equation below calculates the RMS current of input capacitor:

$$I_{CIN\_RMS} = \frac{\Delta I_L}{2\sqrt{3}} = \left( \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times L \times f_S} \right) \quad (30)$$

To avoid impedance interactions and switching noise in Boost converters, choose 100μF to 200μF capacitors. For $V_{IN}$ below 8V, add a 20Ω resistor at input in series with VIN pin to realize a RC filter. It is necessary to put a 0.1μF to 1μF ceramic capacitor as bypass and connect to VIN pin directly. The 100μF to 200μF bulk capacitor and inductor are connected to the other side of the resistor with power supply.

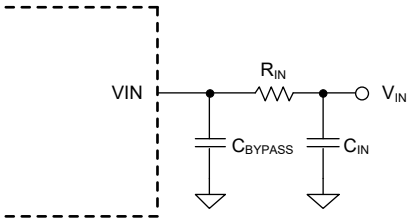



**Figure 11. Reducing IC Input Noise**

### $C_{OUT}$

When MOS of Boost is switched on to charge the inductor, $C_{OUT}$ supports output voltage individually without any input. In this way, the ripple current is so large that the output capacitor needs to filter the ripple currents with large RMS value:

$$I_{COUT\_RMS} = \sqrt{(1-D)\left[ I_{OUT}^2 \frac{D}{(1-D)^2} + \frac{\Delta I_L^2}{12} \right]} \quad (31)$$

Output capacitors ESR and ESL affect the $V_{OUT}$ ripple. Select low ESR/ESL capacitors at output to achieve high efficiency and low ripple.

### VCC Capacitor

It is necessary to use a 0.47μF to 4.7μF bypass capacitor between VCC and PGND pins. The capacitor filters the transient current spike generated by MOSFET driver on-chip.

### Layout Guidelines

1. Keep transient current loop small to eliminate Ldi/dt noise.

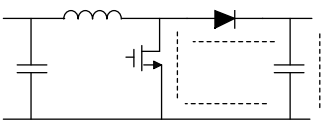


**Figure 12. Current Flow in a Boost Application**

2. Place bypassed $C_{IN}$ close to the VIN pin.
3. The PGND and AGND plane should be close to the device. Connect two GND at only one point.

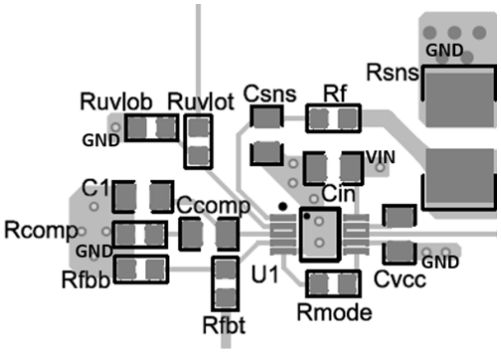



**Figure 13. PCB Layout Example**

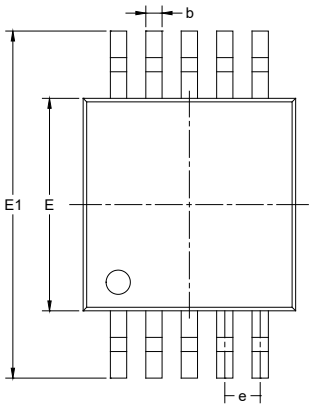
## REVISION HISTORY

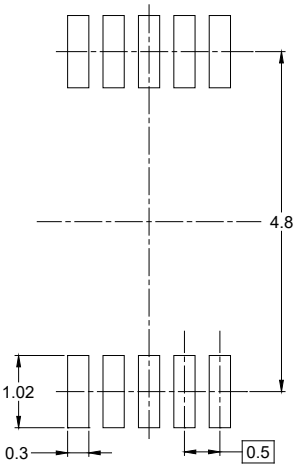
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (DECEMBER 2024) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

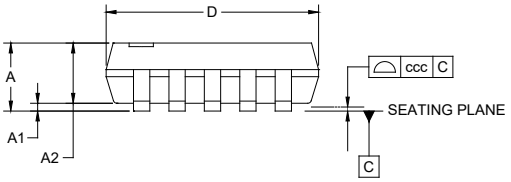
# PACKAGE OUTLINE DIMENSIONS

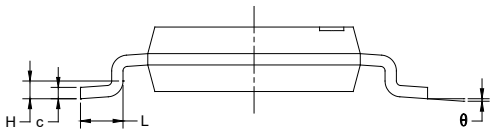
## MSOP-10




**RECOMMENDED LAND PATTERN** (Unit: mm)



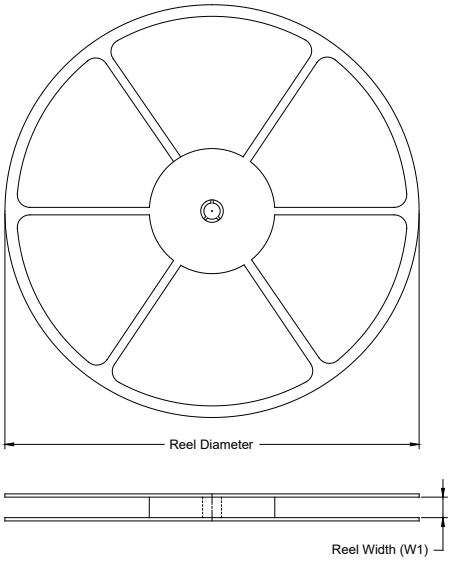




| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | - | - | 1.100 |
| A1 | 0.000 | - | 0.150 |
| A2 | 0.750 | - | 0.950 |
| b | 0.170 | - | 0.330 |
| c | 0.080 | - | 0.230 |
| D | 2.900 | - | 3.100 |
| E | 2.900 | - | 3.100 |
| E1 | 4.750 | - | 5.050 |
| e | 0.500 BSC | | |
| H | 0.250 TYP | | |
| L | 0.400 | - | 0.800 |
| θ | 0° | - | 8° |
| ccc | 0.100 | | |

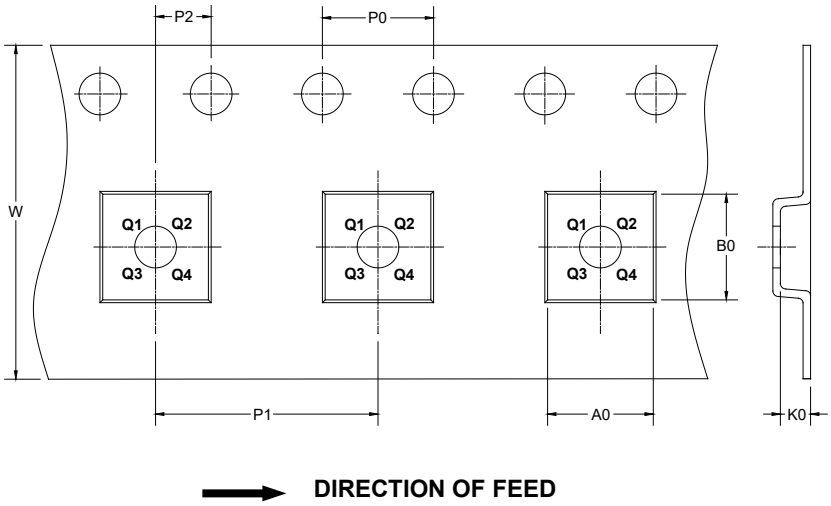
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-187.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS




DIRECTION OF FEED

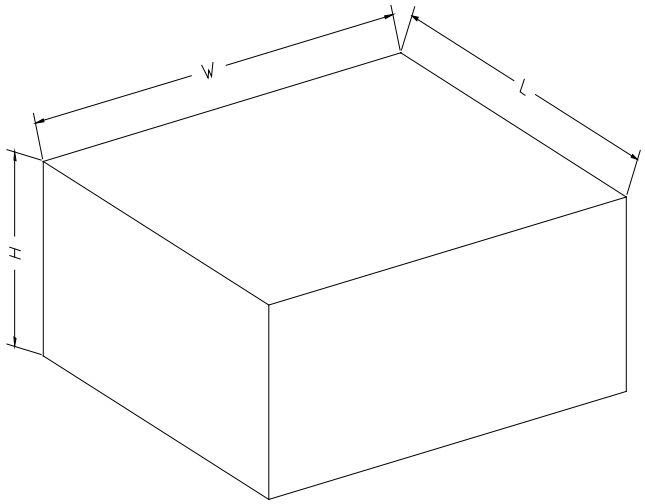
NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| MSOP-10 | 13" | 12.4 | 5.20 | 3.30 | 1.50 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002