SGM854
Ultra-Low Quiescent Current Load Switch Controller with Reset Timer

GENERAL DESCRIPTION

The SGM854 is a load switch controller with 2.4V to 12V input voltage range and is used to turn the main power P-channel MOSFET on or off. It integrates reset and power sequence functions which are controlled by RST0, RST1 and OFF pins with factory-set fixed delay time.

The SGM854 is suitable for mobile phones, tablet computers or other portable equipment with tiny package. For mobile applications, it also features system discharge path and charger insertion detection.

The SGM854 is available in a Green UTQFN-1.8×1.4-10L package. It operates over the junction temperature range of -40℃ to +125℃.

FEATURES

- **Supply Voltage Range: 2.4V to 12V**
- **P-MOSFET Gate Driver**
- **Auto Output Discharge: 180Ω**
- **Low Quiescent Current: 2μA (MAX)**
- **Shipping Mode Current: 2.5μA (MAX)**
- **Factory-Set Fixed Reset Delay**
- **Available in a Green UTQFN-1.8×1.4-10L Package**

APPLICATIONS

Mobile Phones
Tablet Computers
Bluetooth Speakers
Wearable Devices
Portable Equipment

TYPICAL APPLICATION

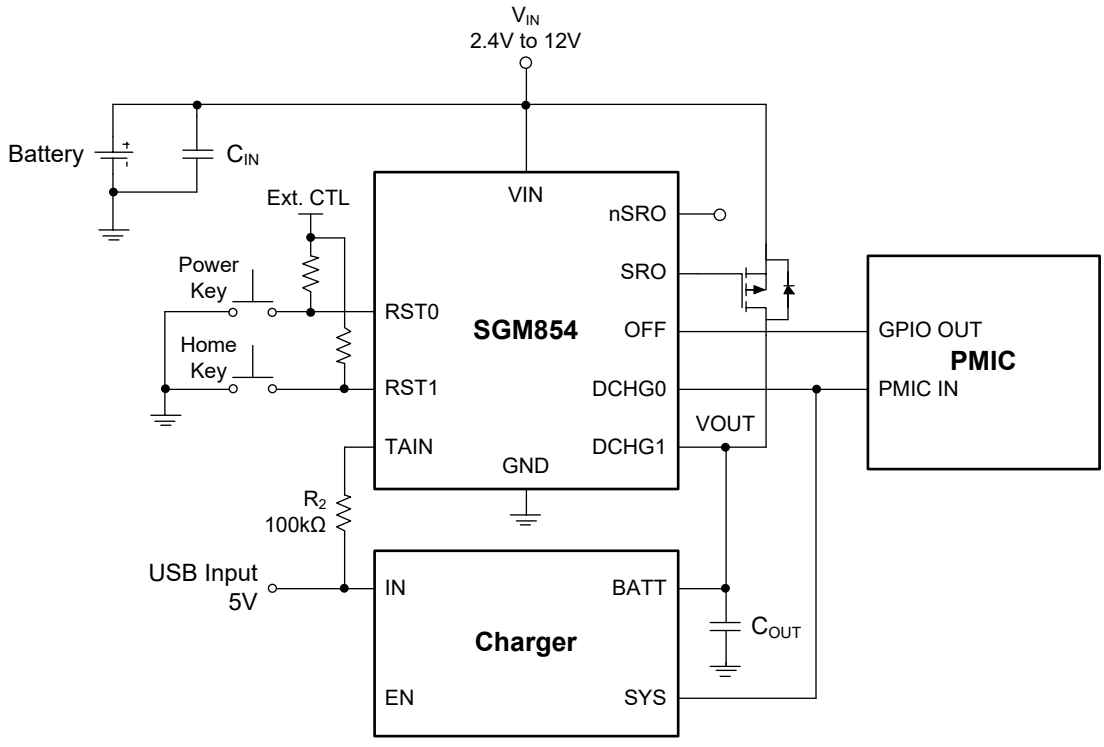


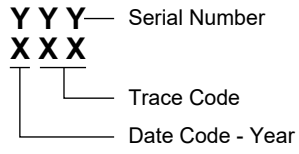
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM854	UTQFN-1.8×1.4-10L	-40℃ to +125℃	SGM854XUWQ10G/TR	0UQ XXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IN} ..... -0.3V to 14V
RST0, RST1 Voltage ..... -0.3V to 6V
OFF Voltage ..... -0.3V to 6V
TAIN, DCHG0, DCHG1, SRO, nSRO Voltage ... -0.3V to 14V
Package Thermal Resistance
UTQFN-1.8×1.4-10L, θ_{JA} ..... 151.4℃/W
UTQFN-1.8×1.4-10L, θ_{JB} ..... 74.3℃/W
UTQFN-1.8×1.4-10L, θ_{JC} ..... 128.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{IN} ..... 2.4V to 12V
RST0, RST1 Voltage ..... 0V to 5.5V
OFF Voltage ..... 0V to 5.5V
nSRO, TAIN, DCHG0, DCHG1 Voltage ..... 0V to 12V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

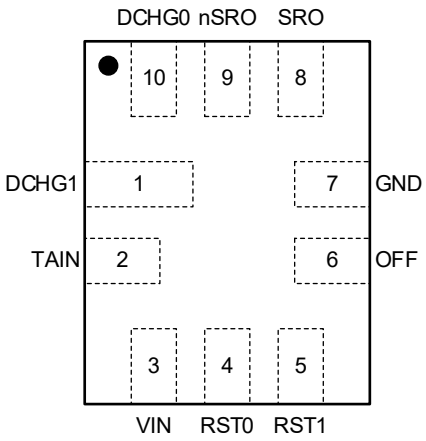
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



UTQFN-1.8×1.4-10L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	DCHG1	Discharge Path 1. When the device is in reset mode and the TAIN is low, DCHG1 starts to discharge.
2	TAIN	Charger Insert Detect Pin. It is pulled down to GND via an internal resistor. And it can be pulled high with an external charger if the charger is inserted.
3	VIN	Supply Voltage Pin.
4	RST0	Active-Low Reset Input 0. Do not leave it floating.
5	RST1	Active-Low Reset Input 1. Do not leave it floating.
6	OFF	Turn Off Input Pin to Enter Shipping Mode. It is pulled down to GND via an internal resistor.
7	GND	Ground.
8	SRO	Push-Pull System Reset Output Pin. It is connected to the gate of the external P-MOSFET.
9	nSRO	Open-Drain System Reset Negative Output Pin. When SRO is pulled low, the open-drain MOSFET turns off. And when SRO is pulled high, the open-drain MOSFET turns on. It keeps floating in shipping mode.
10	DCHG0	Discharge Path 0. When the device is in reset mode and the TAIN is low, DCHG0 starts to discharge.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.6V, T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, unless otherwise noted.)

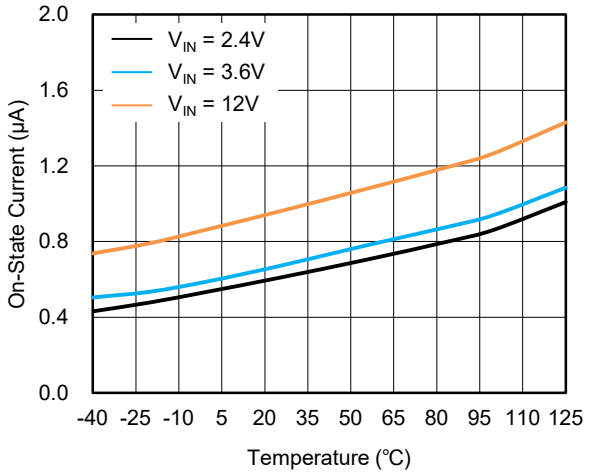
PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input and Supply Voltage Range						
Input Voltage	V_{IN}		2.4		12	V
Supply Current						
Shipping Mode Current	I_{OFF}	V_{IN} = 3.6V, load switch off, shipping mode		0.9	2.5	μA
On-State Current	I_{ON1}	V_{IN} = 3.6V, load switch on, no load, no action assert		0.7	2	μA
	I_{ON2}	V_{IN} = 3.6V, load switch on, no load, action assert to turn OSC on			10	μA
Gate Driver						
SRO Rising Time	t_{RISE}	V_{IN} = 4V, Qg = 20nC	0.5	0.75	1	ms
SRO Logic High-Level Voltage			V_{IN} - 0.3			V
SRO Logic Low-Level Voltage					0.3	V
VDCHG0/VDCHG1 Discharge Resistance		Force 1mA current		80	120	Ω
		V_{DCHG0} = V_{DCHG1} = 4V, T_J = +25℃		155	180	Ω
Discharge Delay	t_{DD}		4.0	5.2	6.0	ms
Under-Voltage Protection						
VIN Under-Voltage Lockout Threshold	V_{IN_UVLO}			1.75		V
UVLO Hysteresis	V_{UVLO_HYS}			150		mV
RST0/RST1/OFF Logic (Input)						
RST0/RST1 High-Level Voltage	V_H		1			V
RST0/RST1 Low-Level Voltage	V_L				0.4	V
OFF High-Level Voltage	V_{H_OFF}		1			V
OFF Low-Level Voltage	V_{L_OFF}				0.4	V
OFF Internal Pull-Down Resistor				1		MΩ
RST0/RST1 Leakage Current		V_{IN} = V_{RST0} = V_{RST1} = 3.6V			200	nA
Debounce Time	t_{DG1}	RST0, RST1, TAIN		10.8		ms
	t_{DG2}	OFF		250		μs
nSRO Logic (Open-Drain Output)						
High-Level Voltage		V_{IN} = 3.3V, pull up VIN through external 100kΩ	V_{IN} × 0.8	V_{IN}		V
Low-Level Voltage		Sink 1mA			0.4	V
nSRO Leakage Current/Logic High		V_{IN} = 3.3V, pull up VIN through external 100kΩ		50		nA
TAIN Logic (Input)						
TAIN Rising			3.0	3.18	3.4	V
TAIN Hysteresis				100		mV
TAIN Confirm Delay Time	t_7		45	53	60	ms
TAIN Internal Pull-Down Resistor				2		MΩ
Reset Time						
Power Reset Entry Time	t_1		9.2	10.9	12.0	s
Power Reset Off Time	t_2		0.38	0.44	0.48	s
Turn Off Response Time	t_3	After OFF rising/falling edge then keep	0.9	1.4	2.0	ms
Turn Off Confirm Cycle (1)				5		Cycle
Turn Off Confirm Time	t_4		90	100	120	ms
Turn Off Delay Time	t_5		14.1	16.3	18.0	s
Turn On Response Time	t_6		1.6	2.0	2.4	s
SRO Pull-Up Current		V_{IN} = 4V		10		μA

NOTE: 1. Guaranteed by engineering sample test, not tested in production.

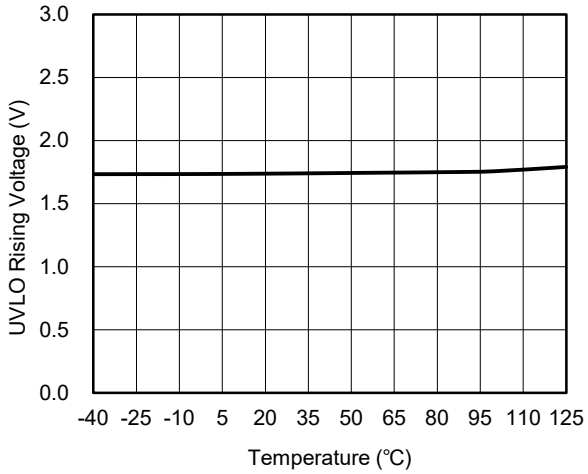
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6V, T_J = +25℃, unless otherwise noted.

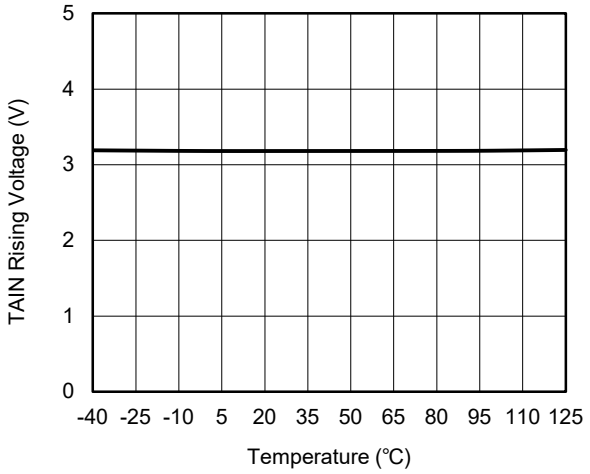
On-State Current vs. Temperature



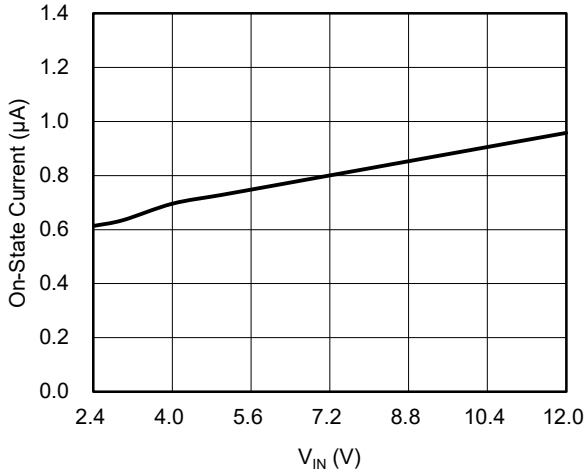
UVLO Rising Voltage vs. Temperature



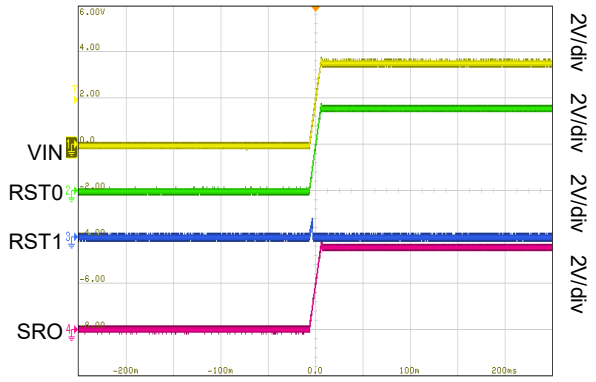
TAIN Rising Voltage vs. Temperature



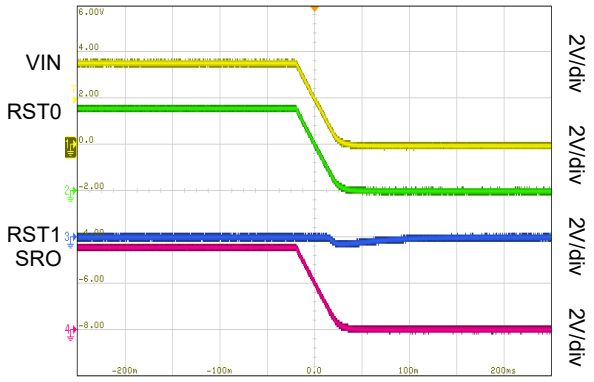
On-State Current vs. V_{IN}



Startup



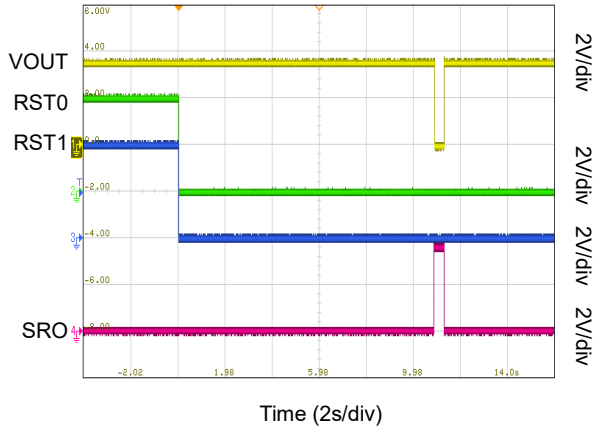
Shutdown



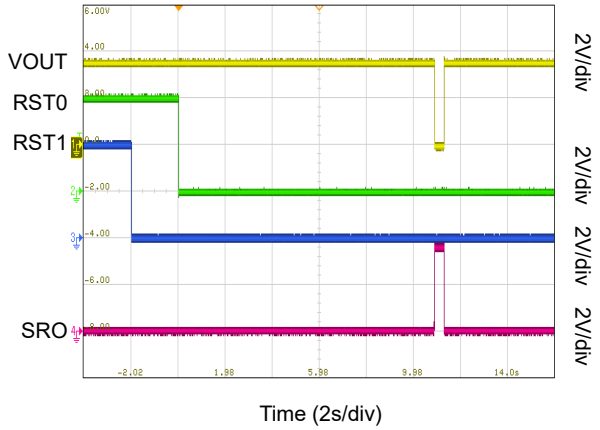
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 3.6V, T_J = +25℃, unless otherwise noted.

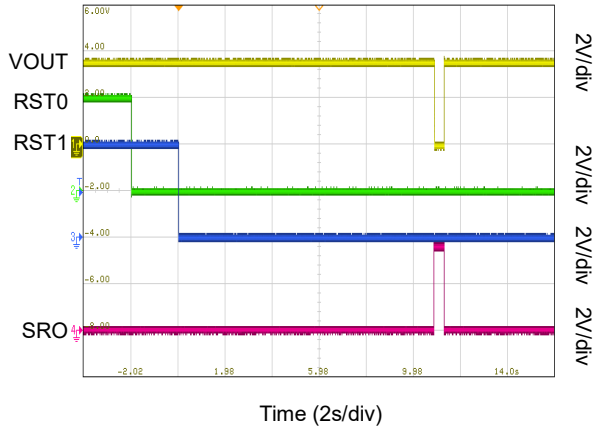
Reset Function



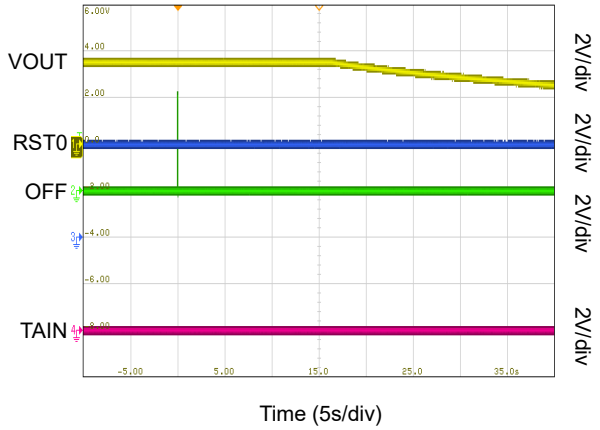
Reset Function (RST1 First)



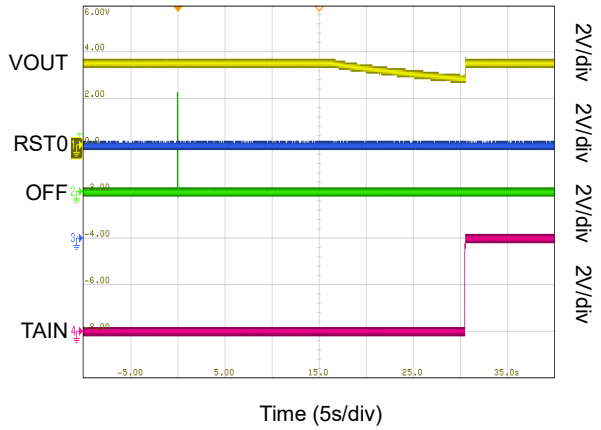
Reset Function (RST0 First)



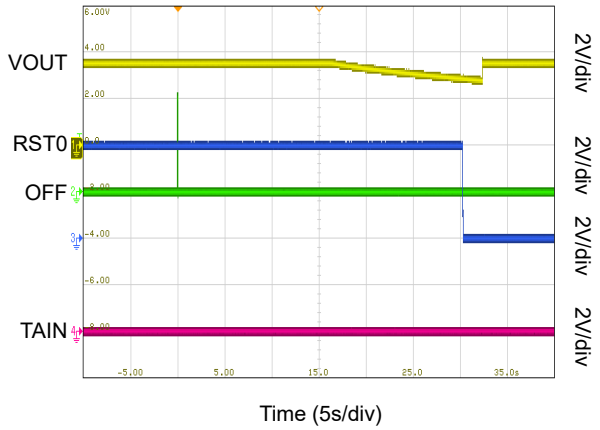
Shipping Mode Enter



Shipping Mode Exit with TAIN



Shipping Mode Exit with RST0



FUNCTIONAL BLOCK DIAGRAM

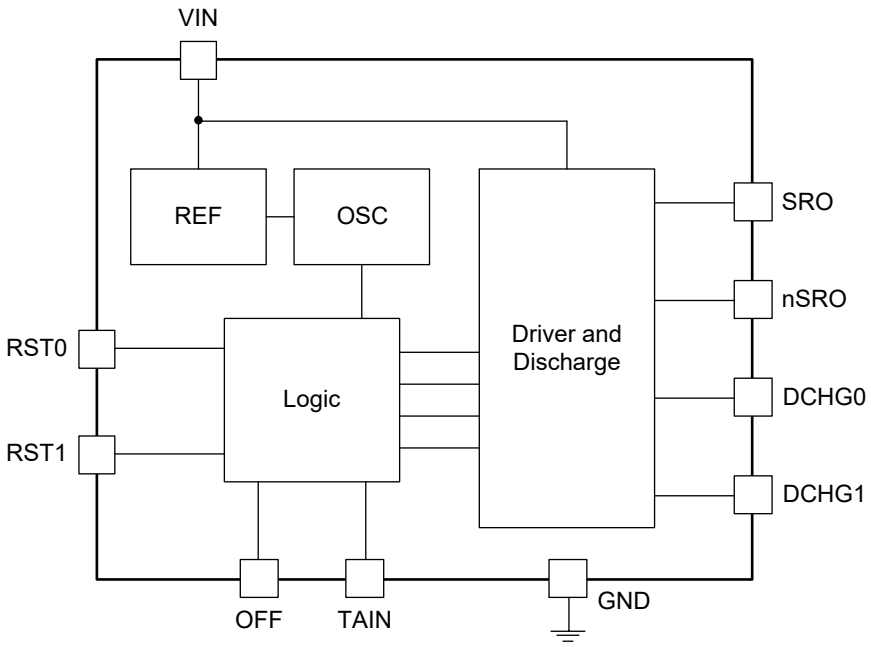


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM854 can be used as a load switch to control the main power P-MOSFET. The operating input voltage range is from 2.4V to 12V. It integrates reset and power sequence functions which are controlled by RST0, RST1 and OFF pins with factory-set fixed delay time.

The SGM854 is suitable for mobile phones, tablet computers or other portable equipment with tiny package. For mobile applications, it also features system discharge path and charger insertion detection.

Reset Function

The SGM854 can turn off the outside P-MOSFET to reset the system as users demand. If so, the present state will be cleared and a new state will be generated. Pull down the RST0 pin and the RST1 pin for 10.9s to enter the reset procedure. Note that $t_2' = t_2 + 2 \times t_{DD}$.

Figure 3 shows the reset procedure and Figure 4 shows the zoomed in version during t_2'.

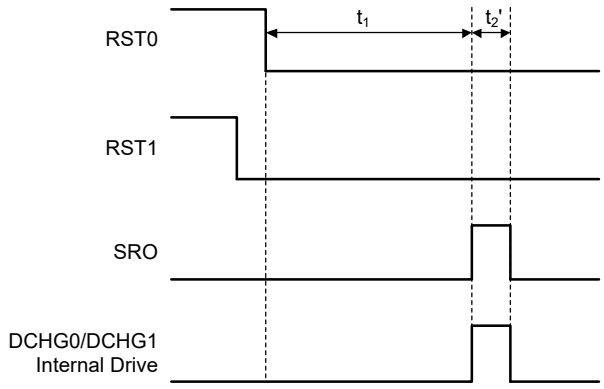


Figure 3. Reset Procedure

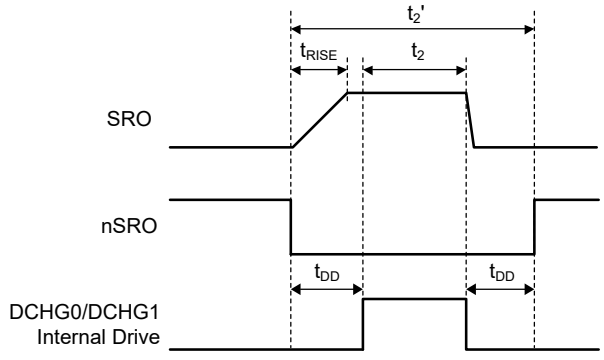


Figure 4. SRO and Discharge Procedure

DETAILED DESCRIPTION (Continued)

The SGM854 introduces a debounce time (t_{DG1}) to reject the error trigger of RST0 and RST1. The undesired glitch of the pulse that is larger than t_{DG1} will be ignored (see Figure 5).

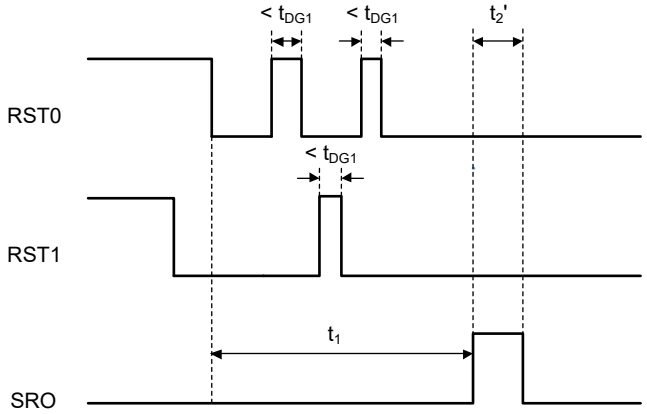


Figure 5. Debounce Procedure

Normally, the SGM854 will turn off the P-MOSFET for t_2' (440ms + 2 × 5.2ms) once RST0 and RST1 maintain low for 10.9s. In t_2 period, DCHG0 and DCHG1 will be activated and the corresponding discharge paths are open to pull respective port voltage low. One reset procedure can only be enabled if RST0 or RST1 is pulled again low. A new procedure will be enabled for a new active-low RST0 or RST1 as shown in Figure 6 and Figure 7.

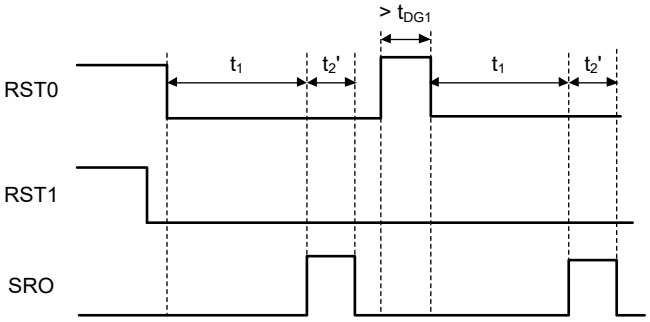


Figure 6. Multiple RST0 Reset

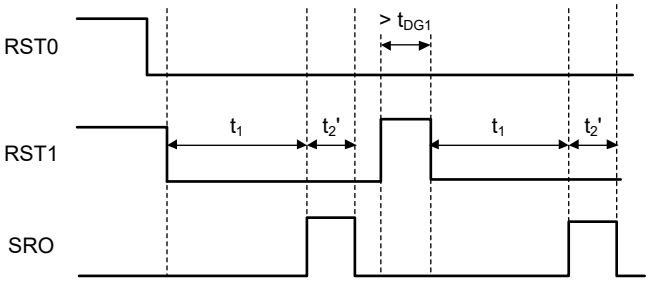


Figure 7. Multiple RST1 Reset

After both RST0 and RST1 turn low, whether in reset procedure or not, the reset action is prior to other logics (TAIN logic or shipping mode trigger function) and is the top priority. No other signals are accepted.

Enter Shipping Mode

The SGM854 can turn off the P-MOSFET and enter the shipping mode to reduce the supply current for IC. As a result, the battery is removed from the system and can work for more time in shipping or stock mode.

To enter the shipping mode, a particular waveform of the OFF signal where on-time > t_3, off-time > t_3 and 5 continuous cycles in 100ms is needed. In this condition, the nSRO pin is floating. Details please see Figure 8.

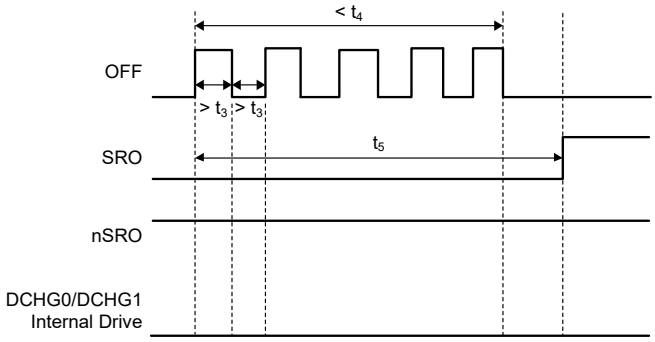


Figure 8. Enter Shipping Mode

Discharge function will not be activated in this mode.

The signal is no longer accepted between the time the shipping mode is confirmed and the time SRO rises to high.

The SGM854 introduces a debounce time (t_{DG2}) to reject the error trigger of OFF. The undesired glitch of the pulse that is larger than t_{DG2} will be ignored (see Figure 9).

OFF signal has lower priority than RST0 and RST1 signal. The shipping mode entry will be terminated if RST0 and RST1 turn low before t_4 (t_{DG1} in advance). See Figure 10.

The OFF signal is prior to the TAIN signal. The TAIN signal can only confirm the exit of shipping mode after entering shipping mode. See below Figure 11.

DETAILED DESCRIPTION (Continued)

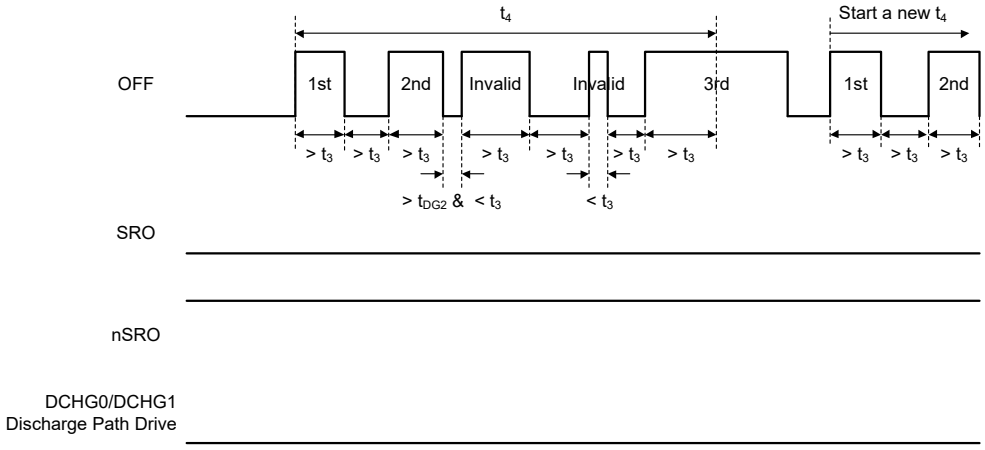


Figure 9. Not Enter Shipping Mode

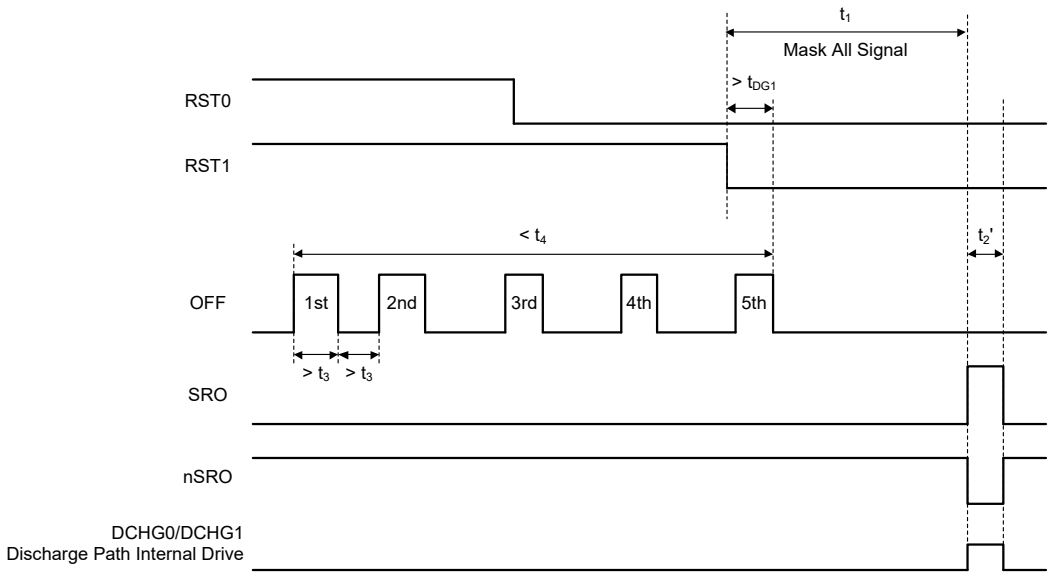


Figure 10. OFF Priority Procedure 1

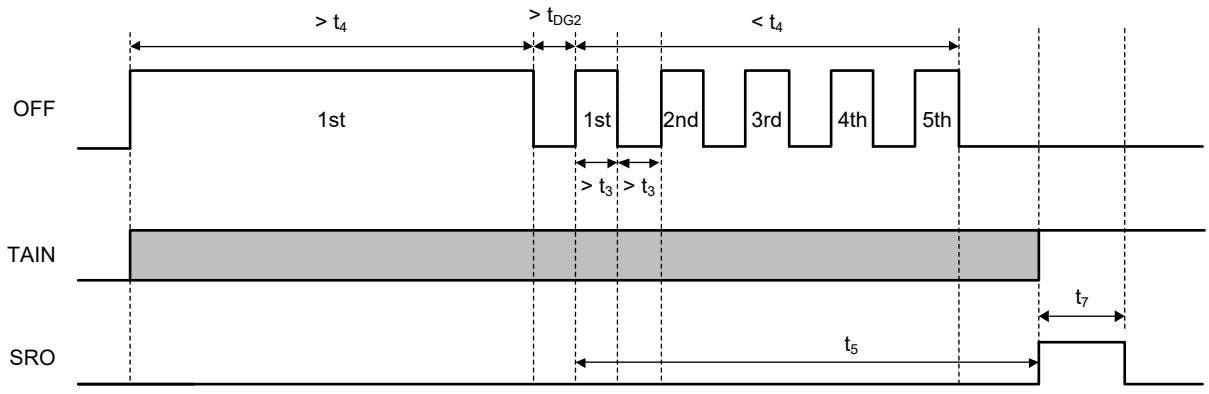


Figure 11. OFF Priority Procedure 2

DETAILED DESCRIPTION (Continued)

Exit Shipping Mode

The SGM854 has two ways to turn on the P-MOSFET and exit the shipping mode. The first one is pulling down the RST0 pin for t_6 under the condition that V_{IN} is larger than the UVLO threshold. The other way is pulling up the TAIN pin for t_7 and this action is usually finished by inserting a charger through a 100kΩ resistor.

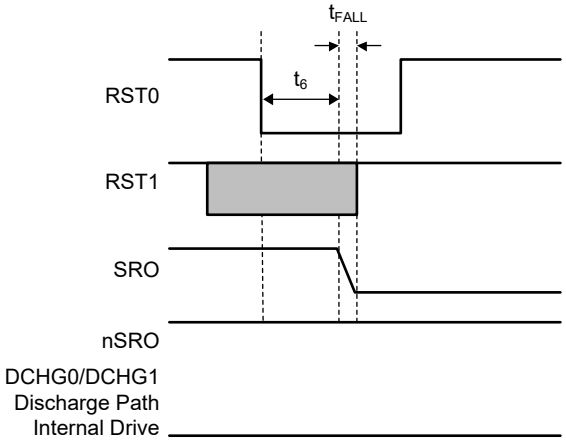


Figure 12. Exit Shipping Mode Procedure

In Figure 13, the SGM854 is under shipping mode at the beginning, TAIN and RST0 both want to wake up SGM854. However, the RST0 confirmation time (t_6) is larger than the TAIN confirmation time (t_7). Hence, the TAIN signal will wake up the SGM854 first.

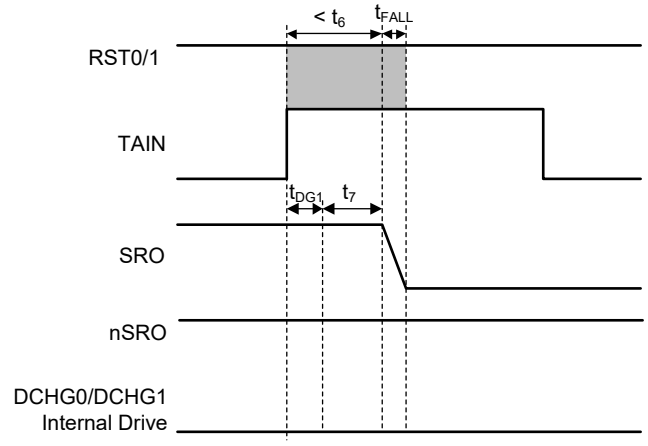


Figure 13. TAIN Procedure

In order to exit the shipping mode, the SGM854 needs to toggle the logic of RST0 or TAIN for new confirmation time. It means that continuous low state of RST0 is unable to help the device to exit the shipping mode. See Figure 14 and Figure 15.

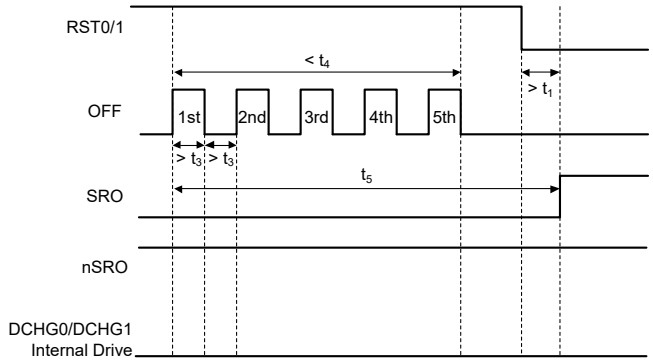


Figure 14. RST0/RST1 not Wake Up Shipping

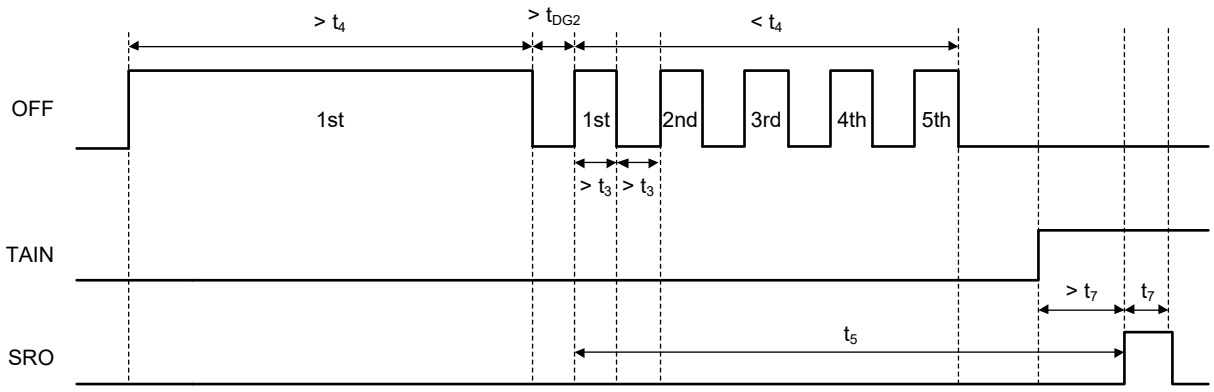


Figure 15. TAIN Cycle Wake Up Shipping

DETAILED DESCRIPTION (Continued)

TAIN Feature

There is a 100kΩ external resistor (R_{EXT}) connected to the TAIN pin to the charger and a sum of 2MΩ internal pull-down resistor (R_{INT} = R_{INT1} + R_{INT2}) at the TAIN pin. The TAIN pin voltage (V_{TAIN}) is given below.

$$V_{TAIN} = \frac{R_{INT}}{R_{INT} + R_{EXT}} \times V_{CHG} \quad (1)$$

V_{CHG} is the external charger voltage.

Figure 16 shows TAIN internal structure. When V_{CHG} voltage is high (30V, MAX), the internal diode clamps the TAIN voltage to 11.5V. Note that the maximum current allowed to flow through the TAIN is 1mA. Take V_{CHG} = 30V as an example, 18.5V voltage falls on the 100kΩ resistor. At this time, the current flows through the TAIN pin is 185μA.

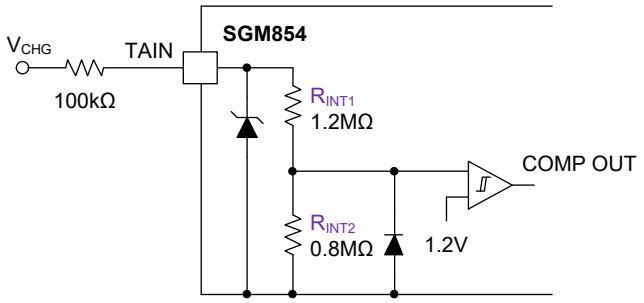


Figure 16. TAIN Structure

Power-On

During power-on procedure, VIN rises over the UVLO threshold. A resistor is connected from nSRO to VIN, therefore, nSRO rises to high as VIN (see Figure 17).

The reset function is triggered if RST1 is low and the IC recognizes the falling edge of RST0 (see Figure 18).

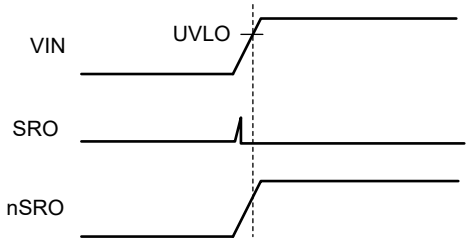


Figure 17. Power-On Priority

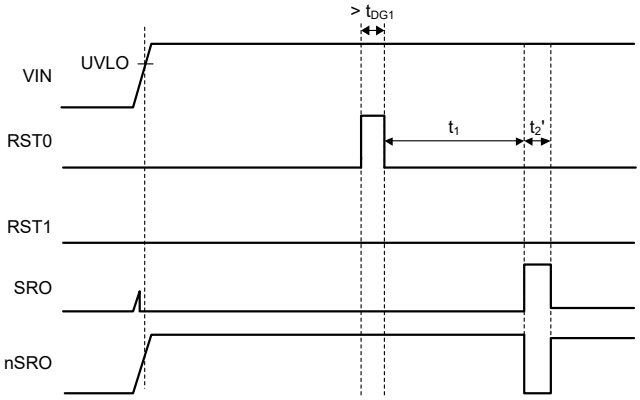


Figure 18. Reset after Power-On

Discharge

The SGM854 provides two discharge pins (DCHG0 and DCHG1) to bleed charge. These pins are enabled to discharge with internal resistor in the period of t_2. However, the resistor discharge capability is unable to pull down DCHG0 and DCHG1 once the charger is inserted in. Hence, the logic high of TAIN disables DCHG0 and DCHG1 at once during t_2. Refer to Figure 19 and Table 1.

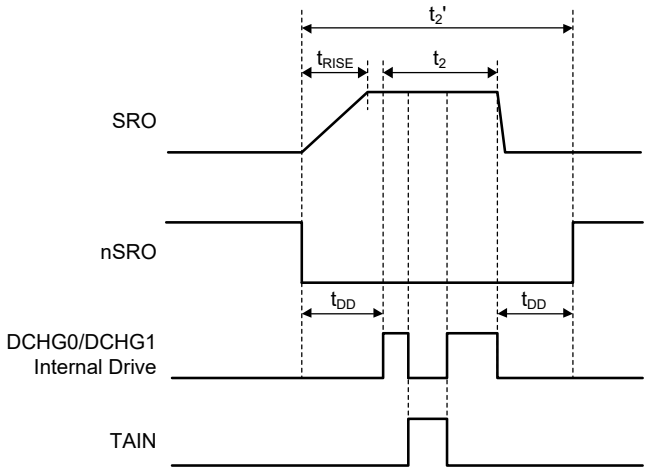


Figure 19. TAIN Disable Discharge

DETAILED DESCRIPTION (Continued)

Table 1. State Change Table

	Event 0					STATE 0			Event 0 for (in seconds)	STATE 1			Duration Between State1 and 2	STATE 2		
	VIN	RST0	RST1	TAIN	OFF	SRO	nSRO	DCHGx		SRO	nSRO	DCHGx		SRO	nSRO	DCHGx
POR	↑	X	X	X	X	0	Open	Open	t_{SRO}	H	X	X	t_{FALL}	L	Open	Open
Reset	VIN	L	H	X	X	L	Open	Open		L	Open	Open		L	Open	Open
	VIN	L	L	H	X	L	Open	Open	t_1	↑	↓	Open	t_2'	↓	↑	Open
	VIN	L	L	L	X	L	Open	Open	t_1	↑	↓	↓	t_2'	↓	↑	↑
	VIN	H	L	X	X	L	Open	Open		L	Open	Open		L	Open	Open
Enter Sleep	VIN	H	X	X	5 pulse	L	Open	Open	t_5	↑	Open	Open	0	H	Open	Open
	VIN	X	H	X	5 pulse	L	Open	Open	t_5	↑	Open	Open	0	H	Open	Open
	VIN	X	X	X	H	L	Open	Open		L	Open	Open		L	Open	Open
	VIN	X	X	X	L	L	Open	Open		L	Open	Open		L	Open	Open
	VIN	X	X	X	< 5 pulse	L	Open	Open		L	Open	Open		L	Open	Open
Exit Sleep	VIN	H	X	L	X	H	Open	Open		H	Open	Open		H	Open	Open
	VIN	X	X	H	X	H	Open	Open	t_7	H	Open	Open	t_{FALL}	L	Open	Open
	VIN	L	X	X	X	H	Open	Open	t_6	H	Open	Open		L	Open	Open

Conflicts Strategy

The SGM854 has different response action when RST0, RST1, OFF and TAIN inputs are in action at the same time. To avoid the input conflicts, the input priority is shown as below:

Table 2: Signal Priority

Priority	Action
1	Reset
2	OFF
3	TAIN

The table shows that the highest priority is reset. If multiple actions occur at the same time, the SGM854 responses only to the one with higher priority. After one action is actived and confirmed first, the other actions are ignored. For instance, once 5 effective and continuous cycles within t_4 for OFF is confirmed, the following 16.3s cannot be interrupted by other signals such as RST0, RST1 and TAIN.

nSRO Function

nSRO is an open-drain output pin that is used as an index for the state of P-MOSFET. For example, the nSRO is logic low when the P-MOSFET is turned off, and the nSRO is logic high when the P-MOSFET is turned on. Notice that nSRO has neither soft-start up nor power-down behavior like SRO. If SGM854 enters shipping mode, the nSRO signal will be floating.

Select Input Capacitor

When hot plugged in condition is considered, an input capacitor should be located at the VIN pin to attenuate the transient spike. X5R or X7R ceramic capacitor has low ESR and small temperature coefficients. Hence, an X5R or X7R capacitor of 1μF is recommended as the input capacitor.

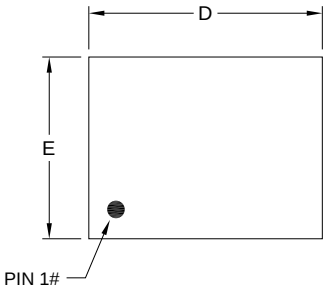
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

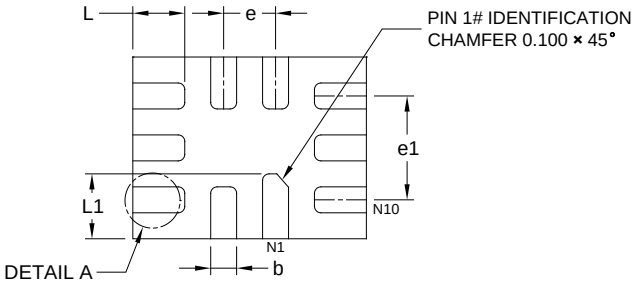
Changes from Original (JUNE 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

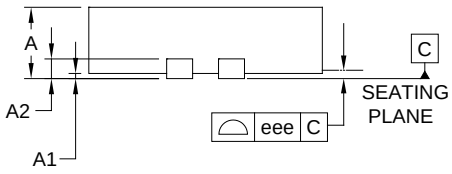
UTQFN-1.8×1.4-10L



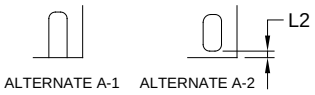
TOP VIEW



BOTTOM VIEW

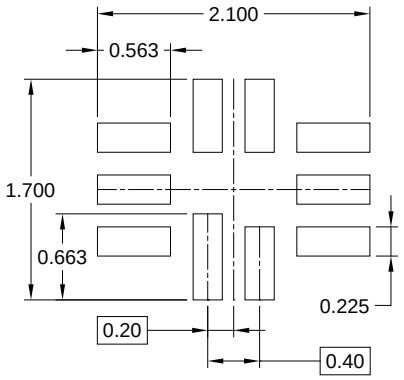


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



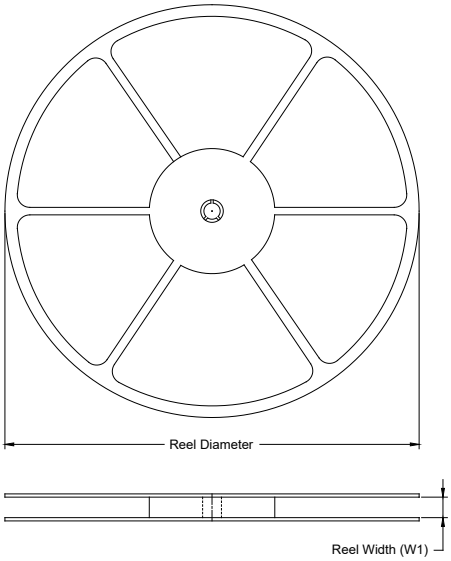
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.450	-	0.600
A1	0.000	-	0.050
A2	0.152 REF		
b	0.150	0.200	0.250
D	1.750	1.800	1.850
E	1.350	1.400	1.450
e	0.400 TYP		
e1	0.800 REF		
L	0.350	0.400	0.450
L1	0.450	0.500	0.550
L2	0.000	-	0.100
eee	-	0.080	-

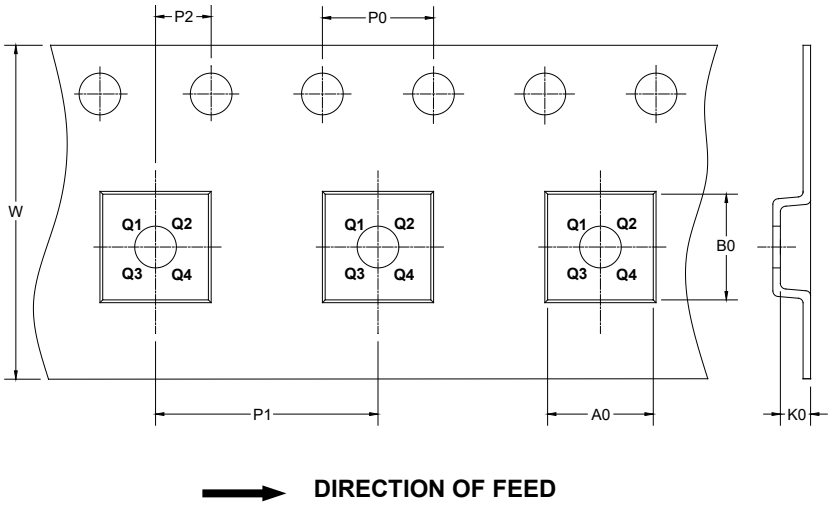
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

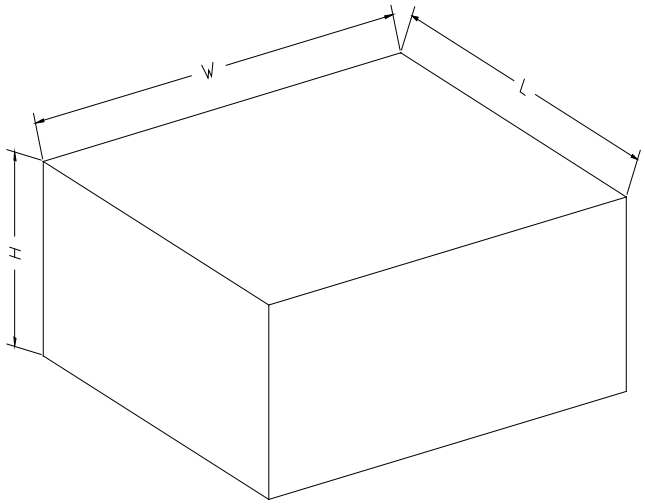
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
UTQFN-1.8×1.4-10L	7"	9.0	1.75	2.10	0.70	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002