SGM5208-14/SGM5209-14
Low-Power, 14-Bit, 500kSPS, 8 Channels and 4 Channels Unipolar Inputs Analog-to-Digital Converters

GENERAL DESCRIPTION

The SGM5208-14 and SGM5209-14 are 14-bit, high-precision, multi-channel input, successive approximation (SAR) analog-to-digital converters (ADCs).

The SGM5208-14 supports 8 single-ended inputs. The SGM5209-14 supports 4 single-ended inputs. The SGM5208-14 and SGM5209-14 need to work with an external voltage reference. Its available range is 1.2V to 4.2V. The digital interface is compatible to the traditional SPI protocol.

The SGM5208-14 and SGM5209-14 are available in Green TQFN-4×4-24L and TSSOP-24 packages. It operates over an ambient temperature range -40℃ to +125℃.

APPLICATIONS

Industrial Process Control
Factory Automation Equipment
Lab Instrumentations

FEATURES

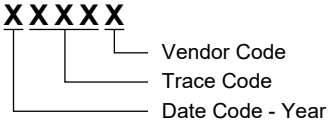
- **Supply Voltage Ranges:**
  - **Analog Supply: 2.7V to 5.5V**
  - **Digital I/O Supply: 2.7V to V_A + 0.2V**
- **Sampling Rate: Up to 500kSPS**
- **Excellent DC Performance**
  - **Integral Nonlinearity (INL): ±2LSB (TYP), 6LSB (MAX) at 2.7V**
  - **Differential Nonlinearity (DNL): ±0.7LSB (TYP), 3LSB (MAX) at 2.7V**
- **Excellent AC Performance at 5V, f_{IN} = 1kHz**
  - **Signal-to-Noise Ratio (SNR): 81.5dB (TYP)**
  - **Spurious Free Dynamic Range (SFDR): 90.4dB (TYP)**
  - **Total Harmonic Distortion (THD): -87.9dB (TYP)**
- **Flexible Input Multiplexer**
- **Support Daisy-Chain Connection**
- **SPI-Compatible Serial Interface**
- **Available in Green TQFN-4×4-24L and TSSOP-24 Packages**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5208-14	TQFN-4×4-24L	-40℃ to +125℃	SGM5208-14XTQF24G/TR	SGMS00Z XTQF24 XXXXX	Tape and Reel, 3000
	TSSOP-24	-40℃ to +125℃	SGM5208-14XTS24G/TR	SGM520814 XTS24 XXXXX	Tape and Reel, 4000
SGM5209-14	TQFN-4×4-24L	-40℃ to +125℃	SGM5209-14XTQF24G/TR	SGMGJS XTQF24 XXXXX	Tape and Reel, 3000
	TSSOP-24	-40℃ to +125℃	SGM5209-14XTS24G/TR	SGM520914 XTS24 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to AGND)
IN_X, MUXOUT, ADCIN, REFP ..... -0.3V to VA + 0.3V
COM, REF- ..... -0.3V to 0.3V
VA ..... -0.3V to 6.5V
Voltage Range (with Respect to DGND)
VBD ..... -0.3V to 6.5V
AGND ..... -0.3V to 0.3V
Digital Input Voltage ..... -0.3V to VBD + 0.3V
Digital Output Voltage ..... -0.3V to VBD + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage Range, V_A
..... 2.7V to 5.5V, 3V (TYP)
Digital Supply Voltage Range, V_{BD}
..... 2.7V to V_A + 0.2V, 3V (TYP)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

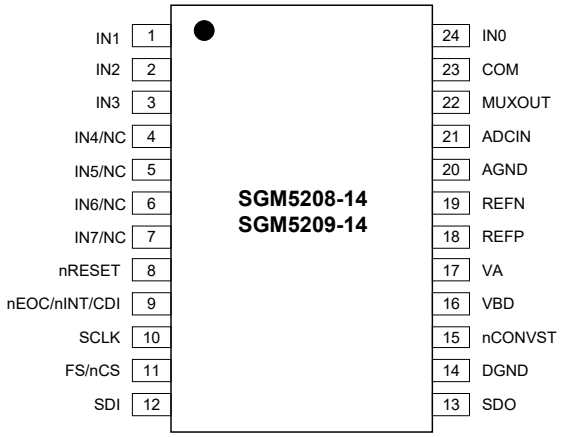
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

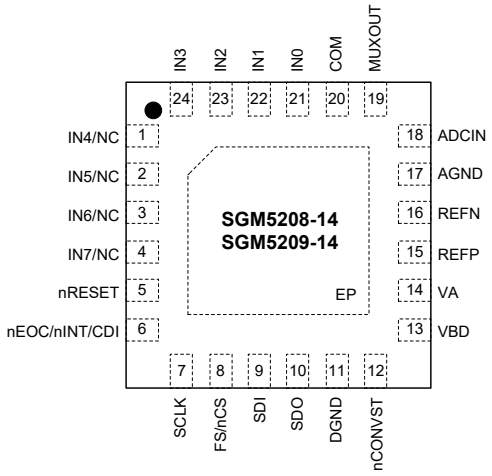
PIN CONFIGURATIONS

SGM5208-14/SGM5209-14 (TOP VIEW)



TSSOP-24

SGM5208-14/SGM5209-14 (TOP VIEW)



TQFN-4×4-24L

PIN DESCRIPTION

PIN		NAME	TYPE (1)	FUNCTION
TSSOP-24	TQFN-4×4-24L			
1-7, 24	1-4, 21-24	IN0 to IN7	I	Channel 0 to Channel 7 Inputs to MUX (Multiplexer).
4-7	1-4	NC	—	No Connection. (SGM5209-14 only)
8	5	nRESET	I	External Reset Pin. Active low.
9	6	nEOC/ nINT/ CDI	O/O/I	Status Output Pin. Used as end-of-conversion (nEOC) pin: active low (default) while a conversion is in progress. The nEOC polarity is programmable. Used as an interrupt (nINT) pin: active low (default) after the end-of-conversion and returns high after FS/nCS goes low. The nINT polarity is programmable. Used as a chain data input (CDI) pin: when it is operated in daisy-chain mode.
10	7	SCLK	I	SPI Serial Clock Input.
11	8	FS/nCS	I	Frame Synchronization Signal for Host Controller or Chip Select Input for SPI.
12	9	SDI	I	SPI Serial Data Input.
13	10	SDO	O	SPI Serial Data Output.
14	11	DGND	—	Digital Ground.
15	12	nCONVST	I	Conversion Start Pin. Freeze sample and hold, start conversion.
16	13	VBD	—	Digital Power Supply.
17	14	VA	—	Analog Power Supply.
18	15	REFP	I	External Positive Reference Input.
19	16	REFN	—	External Negative Reference Input.
20	17	AGND	—	Analog Ground.
21	18	ADCIN	I	ADC Input.
22	19	MUXOUT	O	Mux Output.
23	20	COM	I	Common ADC Input. Connect it to AGND usually.
—	Exposed Pad	EP	—	Exposed pad. Connect it to analog ground.

NOTE: 1. I = Input, O = Output.

ELECTRICAL CHARACTERISTICS

(V_A = 2.7V, V_{BD} = 2.7V, V_{REF} = 2.5V, and f_{SAMPLE} = 500kSPS, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input						
Full-Scale Input Voltage (1)		IN_X - COM, ADCIN - COM	0		V_{REF}	V
Absolute Input Voltage		IN_X, ADCIN	AGND - 0.2		V_A + 0.2	V
		COM	AGND - 0.2		AGND + 0.2	
Input Capacitance		ADCIN		40		pF
Input Leakage Current		Unselected ADC input	-1		1	μA
System Performance						
Resolution				14		Bits
Integral Nonlinearity	INL		-6	±2	6	LSB (2)
Differential Nonlinearity	DNL			±0.7	3	LSB (2)
Offset Error (3)	E_O		-3.5	±0.2	3.5	mV
Offset Error Drift				2		PPM/℃
Offset Error Matching				±0.2		mV
Gain Error	E_G			-0.08		%FSR
Gain Error Drift				±0.18		PPM/℃
Gain Error Matching				0.003		%FSR
Transition Noise				65		$μV_{RMS}$
Power Supply Rejection Ratio	PSRR			70		dB
Sampling Dynamics						
Conversion Time	t_{CONV}			18		CCLK
Acquisition Time	$t_{SAMPLE1}$	Manual-trigger mode	3			CCLK
	$t_{SAMPLE2}$	Auto-trigger mode		3		
Throughput Rate					500	kSPS
Dynamic Characteristics						
Total Harmonic Distortion (4)	THD	V_{IN} = 2.5V_{PP} at 1kHz		-86.7	-73.3	dB
		V_{IN} = 2.5V_{PP} at 10kHz		-85.9	-72.7	
Signal-to-Noise Ratio	SNR	V_{IN} = 2.5V_{PP} at 1kHz	73.3	81.1		dB
		V_{IN} = 2.5V_{PP} at 10kHz	74.1	80.6		
Signal-to-Noise + Distortion	SINAD	V_{IN} = 2.5V_{PP} at 1kHz	71.3	80.0		dB
		V_{IN} = 2.5V_{PP} at 10kHz	71.9	79.4		
Spurious-Free Dynamic Range	SFDR	V_{IN} = 2.5V_{PP} at 1kHz	72	89.1		dB
		V_{IN} = 2.5V_{PP} at 10kHz	71.1	89.1		
Crosstalk		V_{IN} = 2.5V_{PP} at 1kHz		120		dB
		V_{IN} = 2.5V_{PP} at 100kHz		106		
-3dB Small-Signal Bandwidth		IN_X - COM with MUXOUT tied to ADCIN		17		MHz
		ADCIN - COM		30		

ELECTRICAL CHARACTERISTICS (continued)

(V_A = 2.7V, V_{BD} = 2.7V, V_{REF} = 2.5V, and f_{SAMPLE} = 500kSPS, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock							
Internal Conversion Clock Frequency (7)				8.6	10.6	12.6	MHz
SCLK External Serial Clock (8)			Used as I/O clock only			21	MHz
			Used as both I/O clock and conversion clock	0.5		21	MHz
External Voltage Reference Input							
Input Reference Range (5)	(REF+) - (REF-)	V_{REF}		1.2		2.525	V
	(REF-) - AGND			-0.1		0.1	
Resistance (6)			Reference input		50		kΩ
Digital Input/Output							
Logic Family				CMOS			
High-Level Input Voltage		V_{IH}	2.7V < V_{BD} < V_A	0.8 × V_{BD}		V_{BD} + 0.3	V
Low-Level Input Voltage		V_{IL}	2.7V < V_{BD} < V_A	-0.3		0.1 × V_{BD}	V
Input Current		I_I	V_{IN} = V_{BD} or DGND	-1		1	μA
Input Capacitance		C_I			3		pF
High-Level Output Voltage		V_{OH}	V_A ≥ V_{BD} ≥ 2.7V, I_O = 1mA	V_{BD} - 0.4		V_{BD}	V
Low-Level Output Voltage		V_{OL}	V_A ≥ V_{BD} ≥ 2.7V, I_O = -1mA	0		0.4	V
SDO Pin Capacitance		C_O	3-state high impedance state		3		pF
Load Capacitance		C_L				20	pF
Data Format				Straight binary			
Power Supply Requirements							
Analog Supply Voltage (5)		V_A		2.7		3.6	V
Digital I/O Supply Voltage		V_{BD}		2.7		V_A + 0.2	V
Analog Supply Current		I_A	f_{SAMPLE} = 500kSPS		5.5	8.1	mA
			f_{SAMPLE} = 250kSPS in Auto-Nap mode		4.4	6.8	
			Nap mode, SCLK = V_{BD} or DGND		2.4	4	mA
			Deep PD mode, SCLK = V_{BD} or DGND		20	48	μA
Digital I/O Supply Current		I_{BD}	f_{SAMPLE} = 500kSPS		0.8	2.1	mA
			f_{SAMPLE} = 250kSPS in Auto-Nap mode		0.6	1.7	
Power Dissipation			V_A = 2.7V, V_{BD} = 2.7V, f_{SAMPLE} = 500kSPS		17	27.6	mW
			V_A = 2.7V, V_{BD} = 2.7V, f_{SAMPLE} = 250kSPS in Auto-Nap mode		13.5		

NOTES:
1. Ideal input range, do not consider gain error or offset error.
2. LSB = Least Significant Bit.
3. The measurement is performed relative to an ideal full-scale input (IN_X - COM) of 2.5V at V_A = 2.7V.
4. Accumulate the first nine harmonics of the input frequency.
5. The chip operates with V_A from 2.7V to 5.5V and V_{REF} from 1.2V to V_A (maximum V_{REF} ≤ 4.2V). However, when V_A is between 3.6V and 4.5V, the chip may not meet the specifications shown in the Electrical Characteristics table.
6. Vary ±30%.
7. Sampling rate is up to 500kSPS in auto-trigger mode, while the internal conversion clock frequency is 10.5MHz.
8. Guaranteed by design and laboratory test, not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

(V_A = 5V, V_{BD} = 2.7V to 5V, V_{REF} = 4.096V, and f_{SAMPLE} = 500kSPS, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input						
Full-Scale Input Voltage (1)		IN_X - COM, ADCIN - COM	0		V_{REF}	V
Absolute Input Voltage		IN_X, ADCIN	AGND - 0.2		V_A + 0.2	V
		COM	AGND - 0.2		AGND + 0.2	
Input Capacitance		ADCIN		40		pF
Input Leakage Current		Unselected ADC input	-1		1	μA
System Performance						
Resolution				14		Bits
Integral Nonlinearity	INL		-6	±2	6	LSB (2)
Differential Nonlinearity	DNL			±0.7	2.5	LSB (2)
Offset Error (3)	E_O		-4.3	±0.8	4.3	mV
Offset Error Drift				±1		PPM/℃
Offset Error Matching				±0.5		mV
Gain Error	E_G			-0.08		%FSR
Gain Error Drift				±0.18		PPM/℃
Gain Error Matching				±0.005		%FSR
Transition Noise				60		$μV_{RMS}$
Power Supply Rejection Ratio	PSRR			73		dB
Sampling Dynamics						
Conversion Time	t_{CONV}			18		CCLK
Acquisition Time	$t_{SAMPLE1}$	Manual-trigger mode	3			CCLK
	$t_{SAMPLE2}$	Auto-trigger mode		3		
Throughput Rate					500	kSPS
Dynamic Characteristics						
Total Harmonic Distortion (4)	THD	V_{IN} = 4.096V_{PP} at 1kHz		-87.9	-72.3	dB
		V_{IN} = 4.096V_{PP} at 10kHz		-85.7	-72	
Signal-to-Noise Ratio	SNR	V_{IN} = 4.096V_{PP} at 1kHz	74.7	81.5		dB
		V_{IN} = 4.096V_{PP} at 10kHz	74.6	81.8		
Signal-to-Noise + Distortion	SINAD	V_{IN} = 4.096V_{PP} at 1kHz	71.8	80.5		dB
		V_{IN} = 4.096V_{PP} at 10kHz	71.9	80.2		
Spurious-Free Dynamic Range	SFDR	V_{IN} = 4.096V_{PP} at 1kHz	70.9	90.4		dB
		V_{IN} = 4.096V_{PP} at 10kHz	70.6	89.1		
Crosstalk		V_{IN} = 4.096V_{PP} at 1kHz		120		dB
		V_{IN} = 4.096V_{PP} at 100kHz		101		
-3dB Small-Signal Bandwidth		IN_X - COM with MUXOUT tied to ADCIN		22		MHz
		ADCIN - COM		40		

ELECTRICAL CHARACTERISTICS (continued)

(V_A = 5V, V_{BD} = 2.7V to 5V, V_{REF} = 4.096V, and f_{SAMPLE} = 500kSPS, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock							
Internal Conversion Clock Frequency (7)				8.6	10.7	12.9	MHz
SCLK External Serial Clock (8)			Used as I/O clock only			25	MHz
			Used as both I/O clock and conversion clock	0.5		21	
External Voltage Reference Input							
Input Reference Range (5)	(REF+) - (REF-)	V_{REF}		1.2	4.096	4.2	V
	(REF-) - AGND			-0.1		0.1	
Resistance (6)			Reference input		50		kΩ
Digital Input/Output							
Logic Family				CMOS			
High-Level Input Voltage		V_{IH}	2.7V < V_{BD} < V_A	0.8 × V_{BD}		V_{BD} + 0.3	V
Low-Level Input Voltage		V_{IL}	2.7V < V_{BD} < V_A	-0.3		0.1 × V_{BD}	V
Input Current		I_I	V_{IN} = V_{BD} or DGND	-1		1	μA
Input Capacitance		C_I			3		pF
High-Level Output Voltage		V_{OH}	V_A ≥ V_{BD} ≥ 2.7V, I_O = 1mA	V_{BD} - 0.3		V_{BD}	V
Low-Level Output Voltage		V_{OL}	V_A ≥ V_{BD} ≥ 2.7V, I_O = -1mA	0		0.3	V
SDO Pin Capacitance		C_O	HIZ state		3		pF
Load Capacitance		C_L				20	pF
Data Format				Straight binary			
Power Supply Requirements							
Analog Supply Voltage (5)		V_A		4.5	5	5.5	V
Digital I/O Supply Voltage		V_{BD}		2.7		V_A + 0.2	V
Analog Supply Current		I_A	f_{SAMPLE} = 500kSPS		6.5	10	mA
			f_{SAMPLE} = 250kSPS in Auto-Nap mode		5.3	7.5	
			Nap mode, SCLK = V_{BD} or DGND		2.6	4	mA
			Deep PD mode, SCLK = V_{BD} or DGND		25.2	55	μA
Digital I/O Supply Current		I_{BD}	f_{SAMPLE} = 500kSPS		1.5	3.9	mA
			f_{SAMPLE} = 250kSPS in Auto-Nap mode		1.2	2.9	
Power Dissipation			V_A = 5V, V_{BD} = 5V, f_{SAMPLE} = 500kSPS		21.6	37.6	mW
			V_A = 5V, V_{BD} = 5 V, f_{SAMPLE} = 250kSPS in Auto-Nap mode		17.6		

NOTES:
1. Ideal input range, do not consider gain error or offset error.
2. LSB = Least Significant Bit.
3. The measurement is performed relative to an ideal full-scale input (IN_X - COM) of 4.096V at V_A = 5V.
4. Accumulate the first nine harmonics of the input frequency.
5. The chip operates with V_A from 2.7V to 5.5V and V_{REF} from 1.2V to V_A (maximum V_{REF} ≤ 4.2V). However, when V_A is between 3.6V and 4.5V, the chip may not meet the specifications shown in the Electrical Characteristics table.
6. Vary ±30%.
7. Sampling rate is up to 500kSPS in auto-trigger mode, while the internal conversion clock frequency is 10.5MHz.
8. Guaranteed by design and laboratory test, not tested in production.

TIMING REQUIREMENTS

(V_A = V_{BD} = 2.7V, T_A = -40℃ to +125℃, unless otherwise noted.) (1) (2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency, Conversion Clock, CCLK	f_{CCLK}	External, f_{CCLK} = 1/2 f_{SCLK}	0.5		10.5	MHz
		Internal	8.6	10.6	12.6	
Pulse Duration, nCONVST Low	t_1		40			ns
nCS Hold Time with Respect to nEOC (3)	t_2	Read while sampling	25			ns
Setup Time, Rising Edge of nCS to EOS	t_3	Read while sampling	25			ns
Cycle Time, SCLK	t_4	I/O clock only	40			ns
		I/O and conversion clocks	47.6		1000	
		I/O clock, daisy-chain mode	40			
		I/O and conversion clocks, daisy-chain mode	47.6		1000	
Delay Time, Falling Edge of nCS to SDO Valid, SDO MSB Output	t_5	C_{LOAD} = 10pF			35	ns
Delay Time, Falling Edge of SCLK to SDO Invalid	t_6	C_{LOAD} = 10pF	8			ns
Delay Time, Falling Edge of SCLK to SDO Valid	t_7	C_{LOAD} = 10pF			35	ns
Delay Time, Rising Edge of nCS to SDO 3-State	t_8	C_{LOAD} = 10pF			15	ns
Setup Time, SDI to Falling Edge of SCLK	t_9		8			ns
Hold Time, SDI to Falling Edge of SCLK	t_{10}		8			ns
nCS Hold Time with Respect to EOS	t_{11}	Read while converting	25			ns
Setup Time, Rising Edge of nCS to nEOC (3)	t_{12}	Read while converting	1			CCLK
Setup Time, Falling Edge of nCS to First Falling Edge of SCLK	t_{13}		14			ns
Pulse Duration, SCLK Low	t_{14}		17		t_{SCLK} - t_{WH2}	ns
Pulse Duration, SCLK High	t_{15}		12		t_{SCLK} - t_{WL2}	ns
Hold Time, Last Falling Edge of SCLK before Rising Edge of nCS	t_{16}		2			ns
Setup Time, Last Falling Edge of SCLK before Rising Edge of nCS	t_{17}		15			ns
Delay Time, Falling Edge of nCS to Deactivation of nINT	t_{18}	C_{LOAD} = 10pF			40	ns
Setup Time, Rising Edge of SCLK to Rising Edge of nCS	t_{19} (4)		10			ns
Hold Time, Rising Edge of SCLK to Rising Edge of nCS	t_{20} (4)		2			ns

NOTES:
1. All input signals are specified with rising up time which is 1.5ns and falling down time which is 1.5ns (10% to 90% of V_{BD}), and timed from a voltage level of (V_{IL} + V_{IH})/2.
2. Refer to the timing diagrams.
3. The EOS is the end of sampling. The nEOC is the end of conversion. They are the inverse of each other.
4. When sending 4-bit or 16-bit commands, this applies to the 5th or 17th rising SCLK.

TIMING REQUIREMENTS (continued)

(V_A = V_{BD} = 5V, T_A = -40℃ to +125℃, unless otherwise noted.) (1) (2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency, Conversion Clock, CCLK	f_{CCLK}	External, f_{CCLK} = 1/2 f_{SCLK}	0.5		10.5	MHz
		Internal	8.6	10.7	12.9	
Pulse Duration, nCONVST Low	t_1		40			ns
nCS Hold Time with Respect to nEOC (3)	t_2	Read while sampling	20			ns
Setup Time, Rising Edge of nCS to EOS	t_3	Read while sampling	20			ns
Cycle Time, SCLK	t_4	I/O clock only	25			ns
		I/O and conversion clocks	47.6		1000	
		I/O clock, daisy-chain mode	25			
		I/O and conversion clocks, daisy-chain mode	47.6		1000	
Delay Time, Falling Edge of nCS to SDO Valid, SDO MSB Output	t_5	C_{LOAD} = 10pF			20	ns
Delay Time, Falling Edge of SCLK to SDO Invalid	t_6	C_{LOAD} = 10pF	5			ns
Delay Time, Falling Edge of SCLK to SDO Valid	t_7	C_{LOAD} = 10pF			20	ns
Delay Time, Rising Edge of nCS to SDO 3-State	t_8	C_{LOAD} = 10pF			10	ns
Setup Time, SDI to Falling Edge of SCLK	t_9		8			ns
Hold Time, SDI to Falling Edge of SCLK	t_{10}		8			ns
nCS Hold Time with Respect to EOS	t_{11}	Read while converting	20			ns
Setup Time, Rising Edge of nCS to nEOC (3)	t_{12}	Read while converting	1			CCLK
Setup Time, Falling Edge of nCS to First Falling Edge of SCLK	t_{13}		8			ns
Pulse Duration, SCLK Low	t_{14}		12		t_{SCLK} - t_{WH2}	ns
Pulse Duration, SCLK High	t_{15}		11		t_{SCLK} - t_{WL2}	ns
Hold Time, Last Falling Edge of SCLK before Rising Edge of nCS	t_{16}		2			ns
Setup Time, Last Falling Edge of SCLK before Rising Edge of nCS	t_{17}		10			ns
Delay Time, Falling Edge of nCS to Deactivation of nINT	t_{18}	C_{LOAD} = 10pF			20	ns
Setup Time, Rising Edge of SCLK to Rising Edge of nCS	t_{19} (4)		10			ns
Hold Time, Rising Edge of SCLK to Rising Edge of nCS	t_{20} (4)		2			ns

NOTES:

1. All input signals are specified with rising up time which is 1.5ns and falling down time which is1.5ns (10% to 90% of V_{BD}), and timed from a voltage level of (V_{IL} + V_{IH})/2.
2. Refer to the timing diagrams.
3. The EOS is the end of sampling. The nEOC is the end of conversion. They are the inverse of each other.
4. When sending 4-bit or 16-bit commands, this applies to the 5^{th} or 17^{th} rising SCLK.

TIMING DIAGRAM

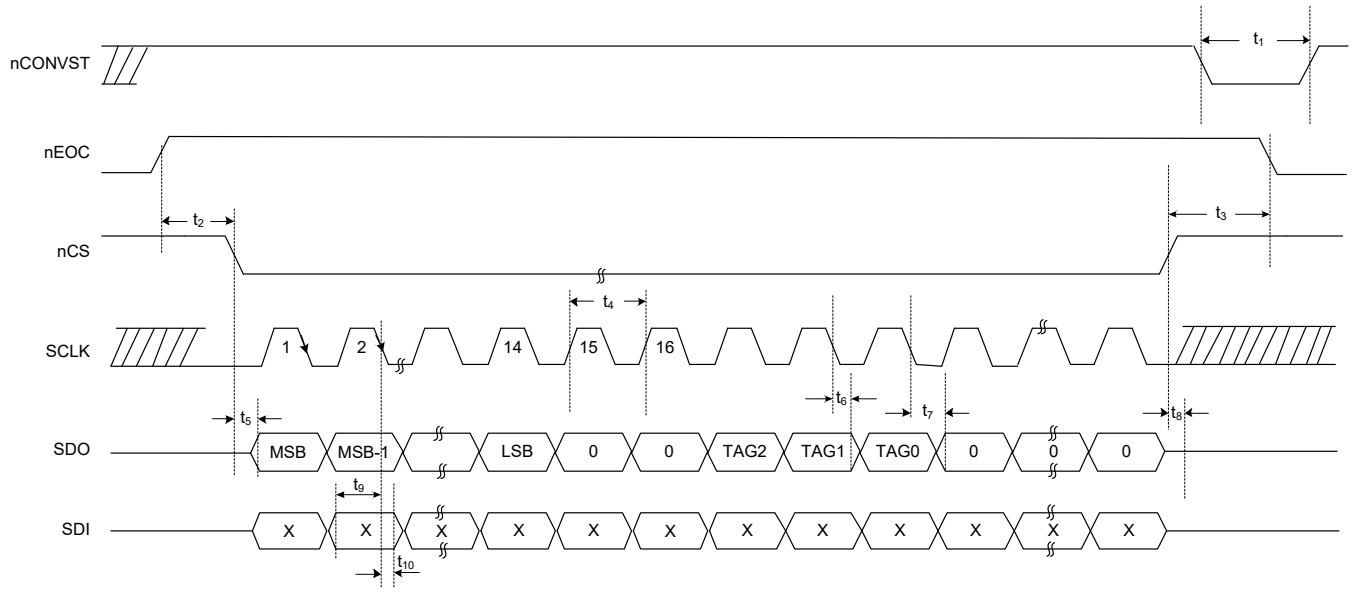


Figure 1. Read While Sampling (Manual-Trigger Mode)

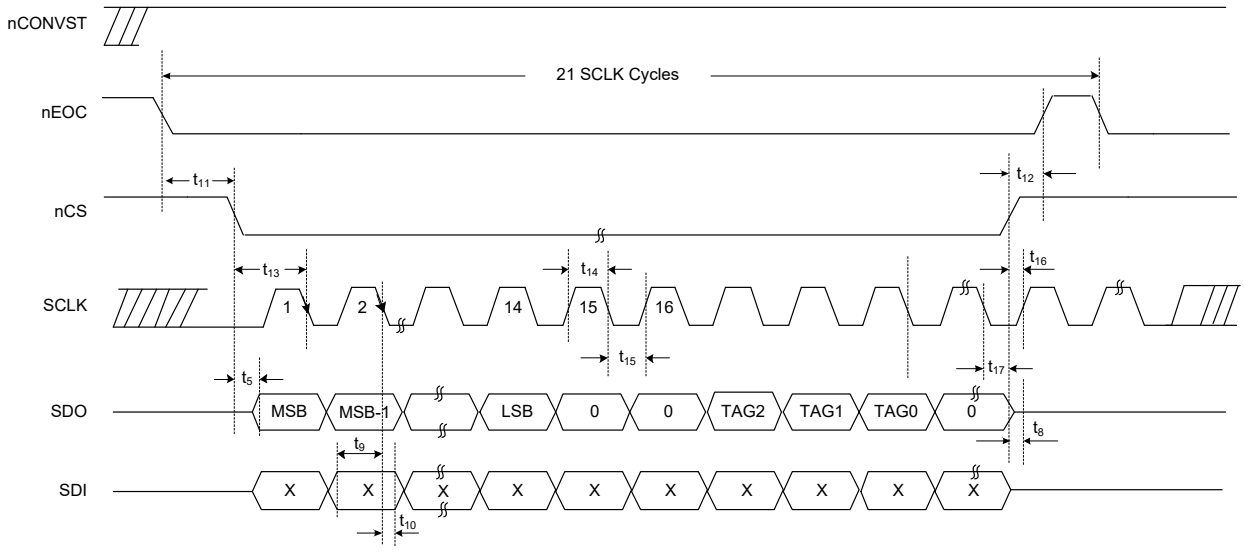


Figure 2. Read While Converting (Auto-Trigger Mode at 500kSPS)

TIMING DIAGRAM (continued)

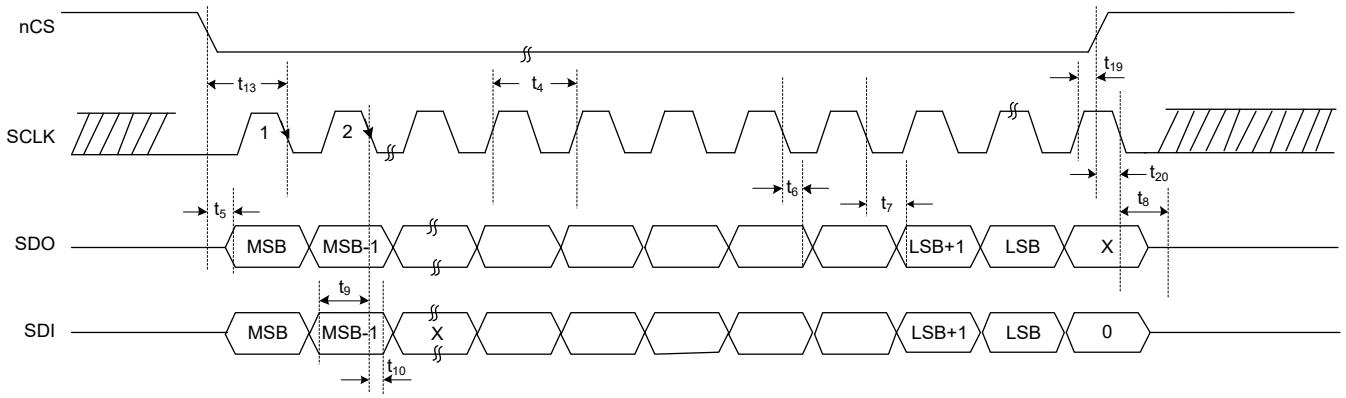


Figure 3. SPI I/O

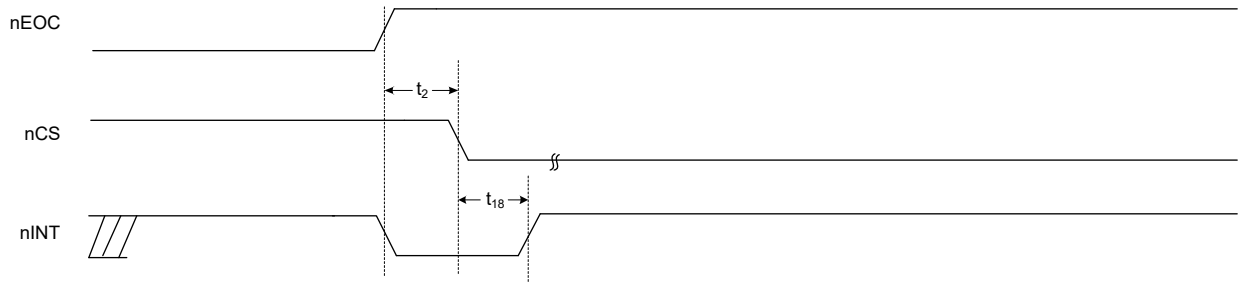
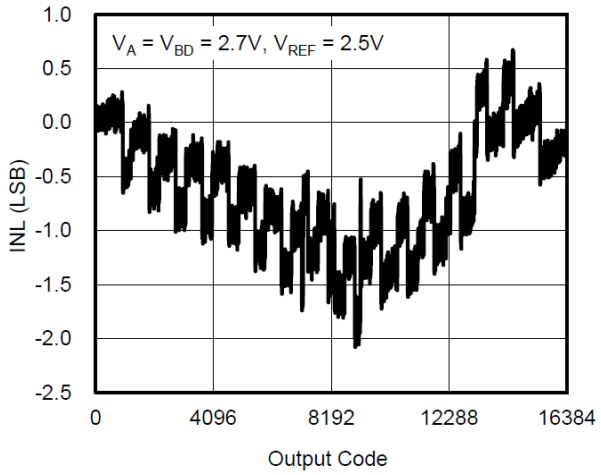


Figure 4. nCS, nEOC, and nINT Timing Diagram

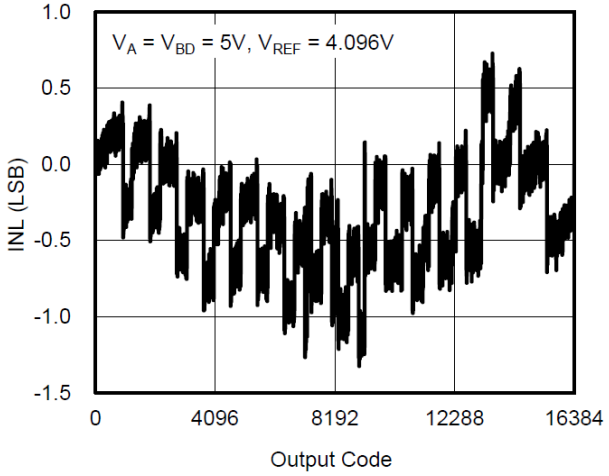
TYPICAL PERFORMANCE CHARACTERISTICS: DC PERFORMANCE

T_A = +25℃, V_{REF} (REF+ - REF-) = 4.096V when V_A = V_{BD} = 5V or V_{REF} (REF+ - REF-) = 2.5V when V_A = V_{BD} = 2.7V, f_{SCLK} = 21MHz, and f_{SAMPLE} = 500kSPS, unless otherwise noted.

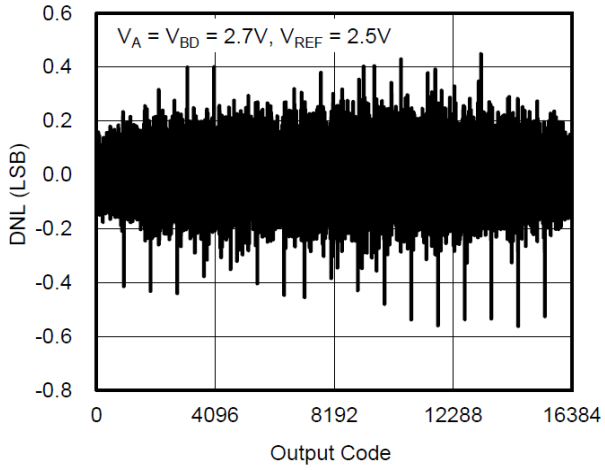
Integral Nonlinearity vs. Output Code



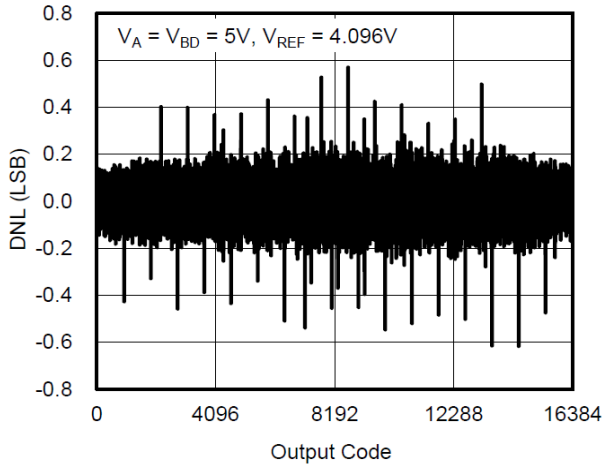
Integral Nonlinearity vs. Output Code



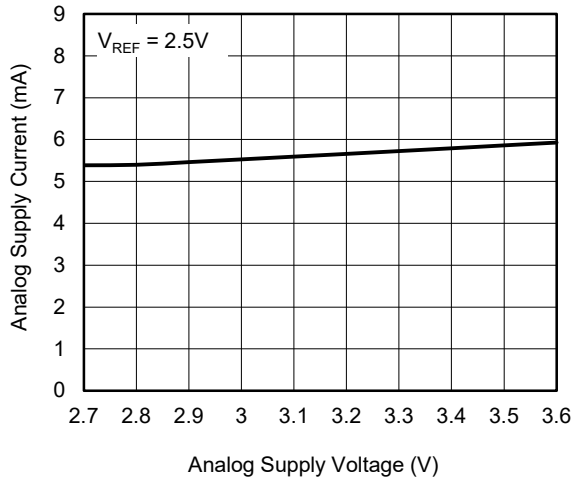
Differential Nonlinearity vs. Output Code



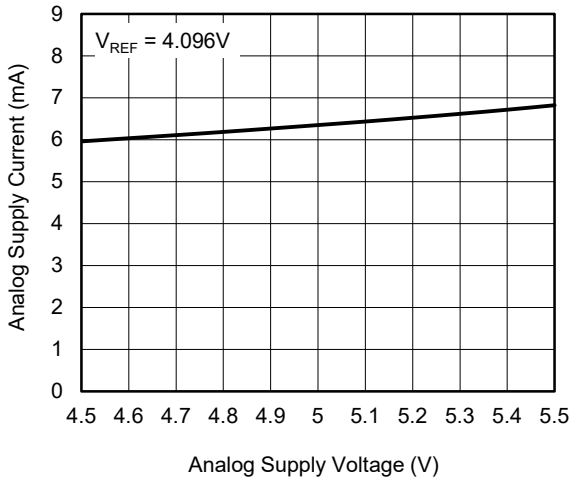
Differential Nonlinearity vs. Output Code



Analog Supply Current vs. Analog Supply Voltage



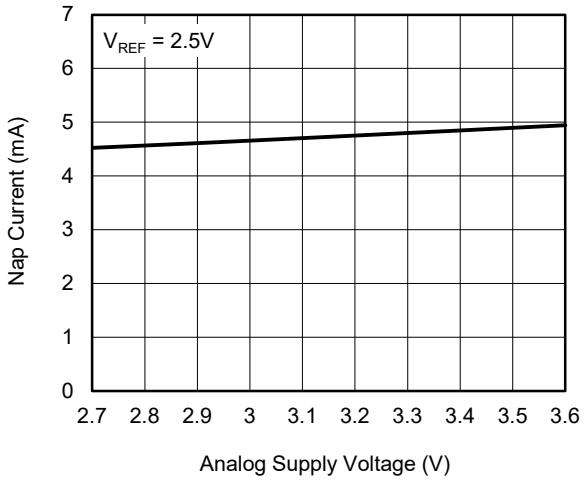
Analog Supply Current vs. Analog Supply Voltage



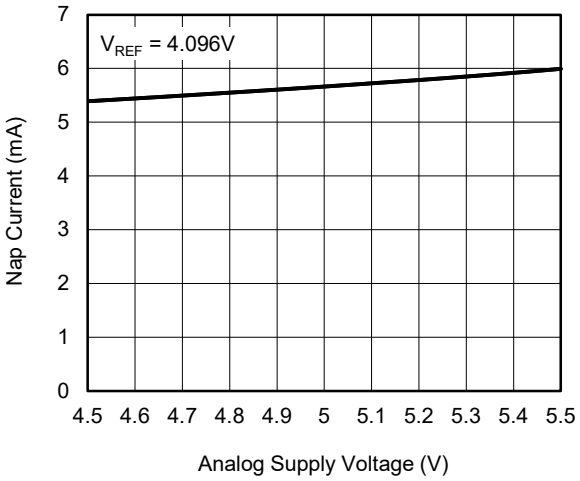
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{REF} (REF+ - REF-) = 4.096V when V_A = V_{BD} = 5V or V_{REF} (REF+ - REF-) = 2.5V when V_A = V_{BD} = 2.7V, f_{SCLK} = 21MHz, and f_{SAMPLE} = 500kSPS, unless otherwise noted.

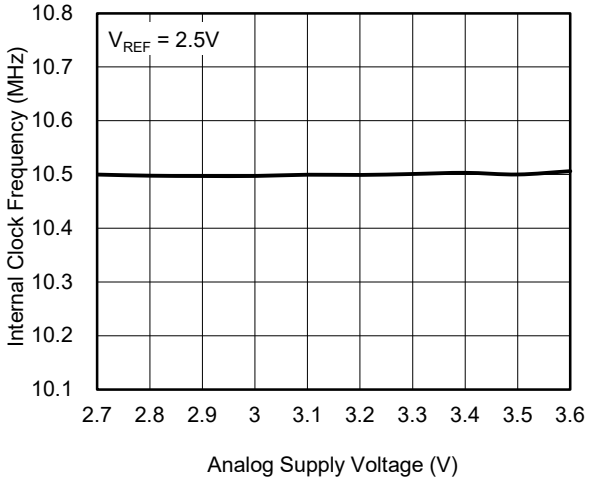
Analog Supply Current in NAP Mode vs. Analog Supply Voltage



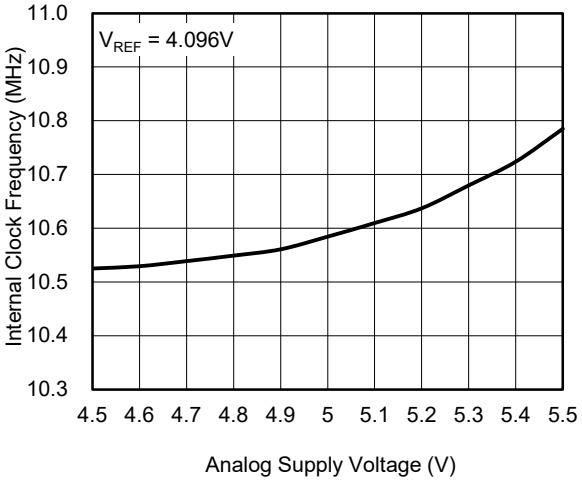
Analog Supply Current in NAP Mode vs. Analog Supply Voltage



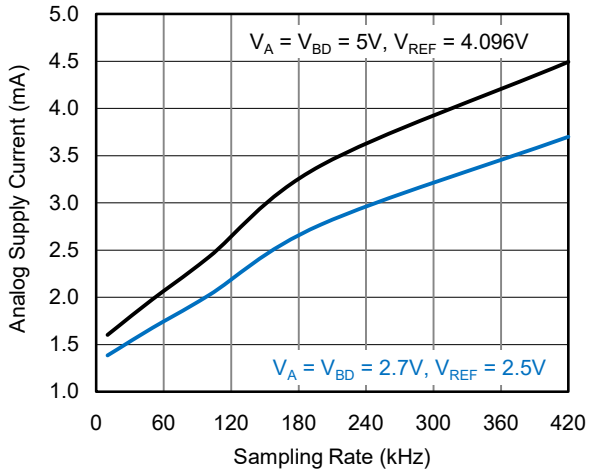
Internal Clock Frequency vs. Analog Supply Voltage



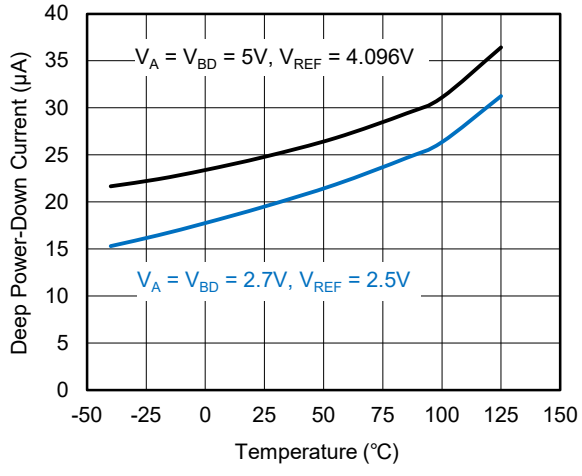
Internal Clock Frequency vs. Analog Supply Voltage



Analog Supply Current vs. Sampling Rate in Auto-NAP Mode



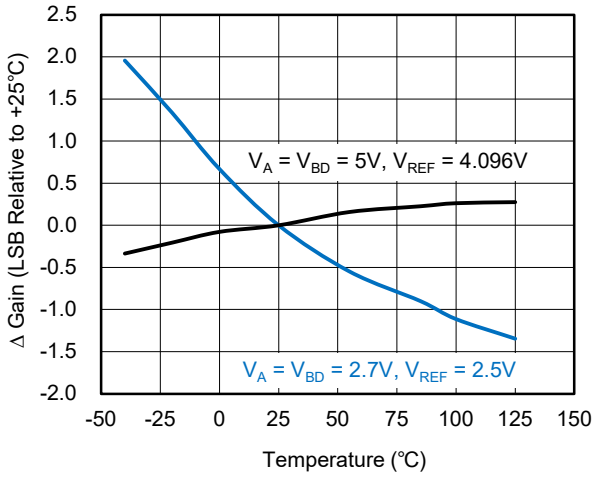
Deep Power-Down Current vs. Temperature



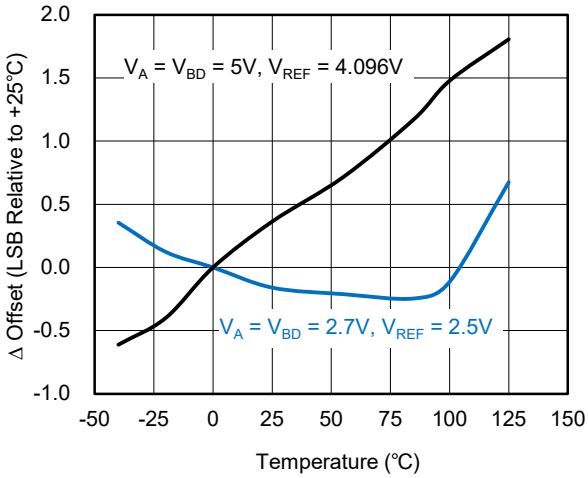
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{REF} (REF+ - REF-) = 4.096V when V_A = V_{BD} = 5V or V_{REF} (REF+ - REF-) = 2.5V when V_A = V_{BD} = 2.7V, f_{SCLK} = 21MHz, and f_{SAMPLE} = 500kSPS, unless otherwise noted.

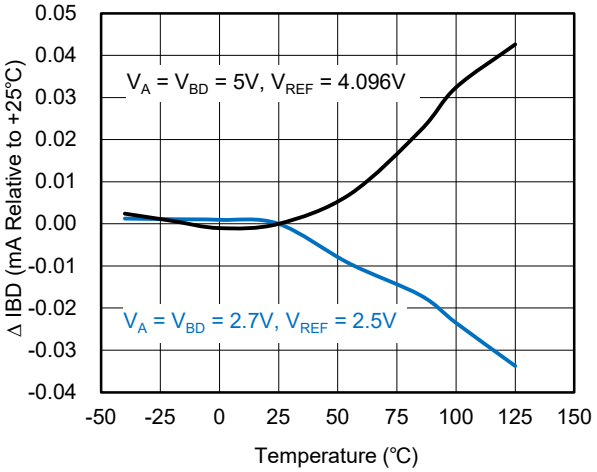
Change in Gain vs. Temperature



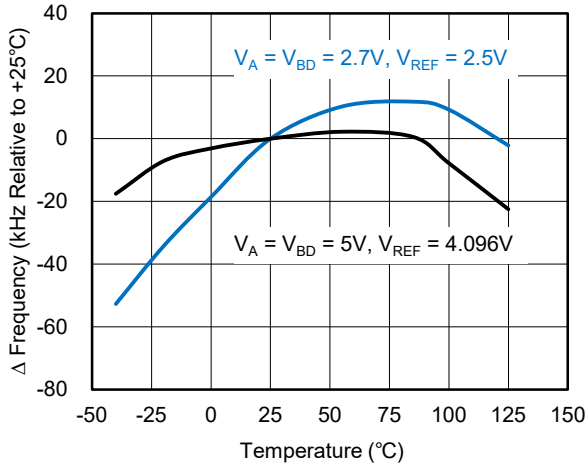
Change in Offset vs. Temperature



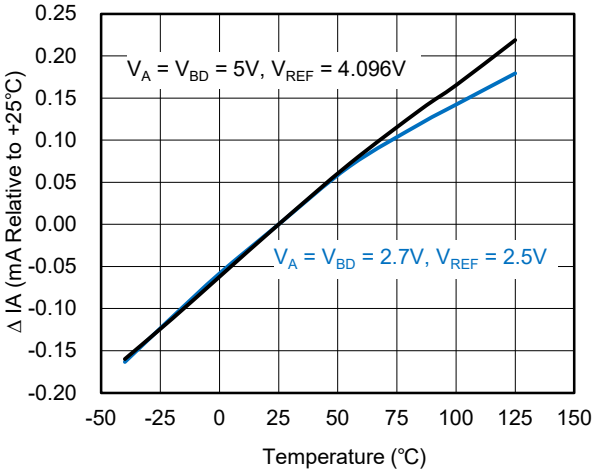
Change in Digital Supply Current vs. Temperature



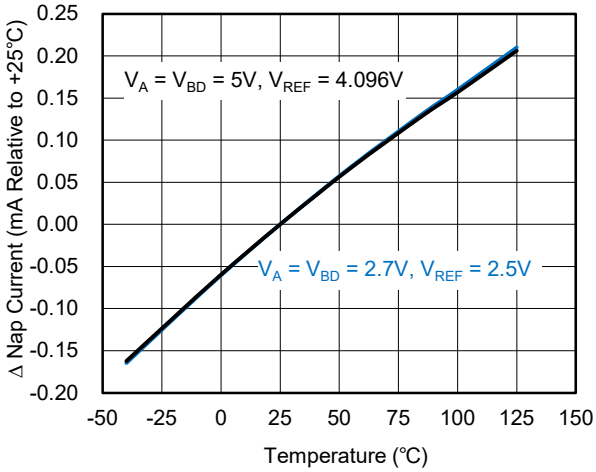
Change in Internal Clock Frequency vs. Temperature



Change in Analog Supply Current vs. Temperature



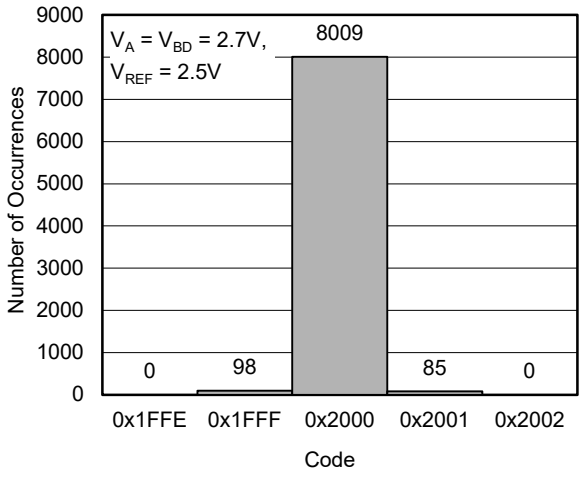
Change in Analog Supply Current in NAP Mode vs. Temperature



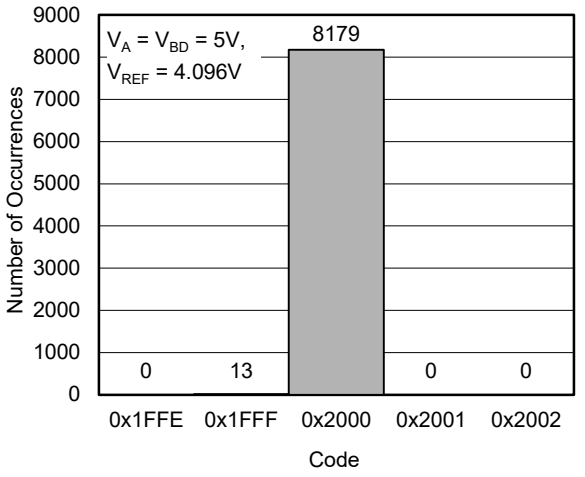
TYPICAL PERFORMANCE CHARACTERISTICS: AC PERFORMANCE

T_A = +25℃, V_{REF} (REF+ - REF-) = 4.096V when V_A = V_{BD} = 5V or V_{REF} (REF+ - REF-) = 2.5V when V_A = V_{BD} = 2.7V, f_{SCLK} = 21MHz, and f_{SAMPLE} = 500kSPS, unless otherwise noted.

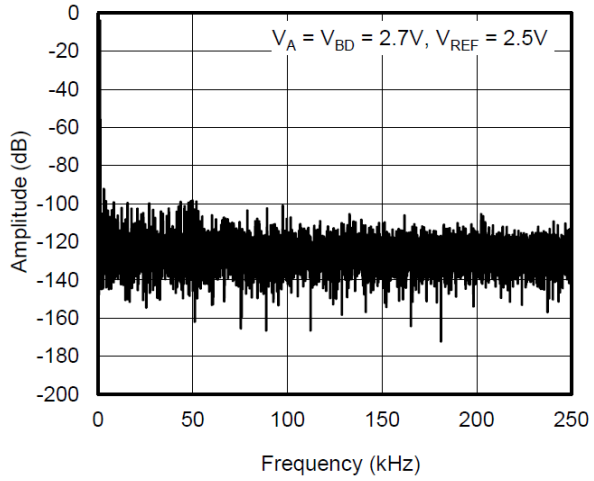
Output Code Histogram for a DC Input (8192 Conversions)



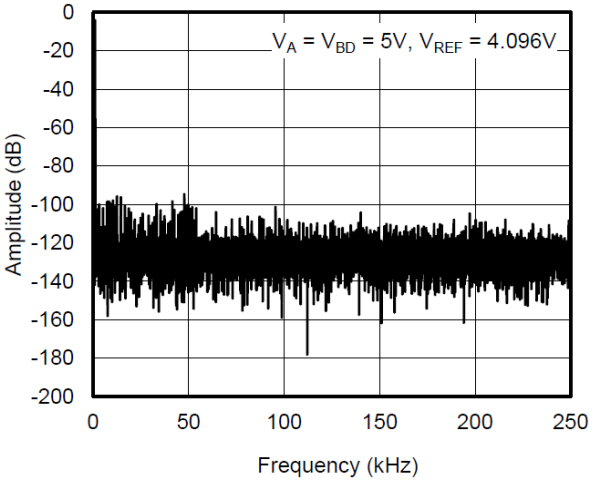
Output Code Histogram for a DC Input (8192 Conversions)



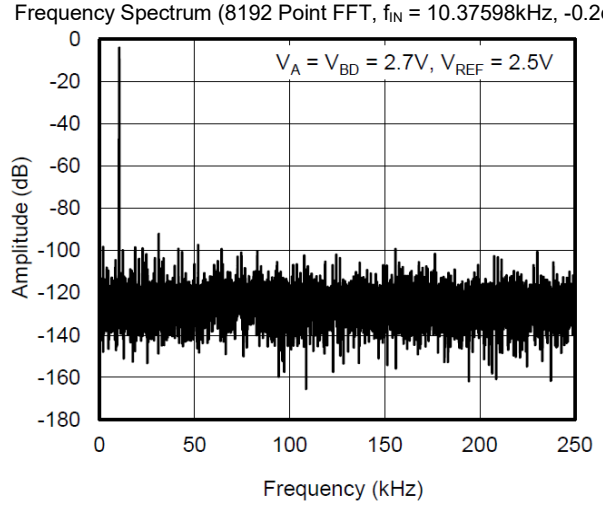
Frequency Spectrum (8192 Point FFT, f_{IN} = 1.0376kHz, -0.2dB)



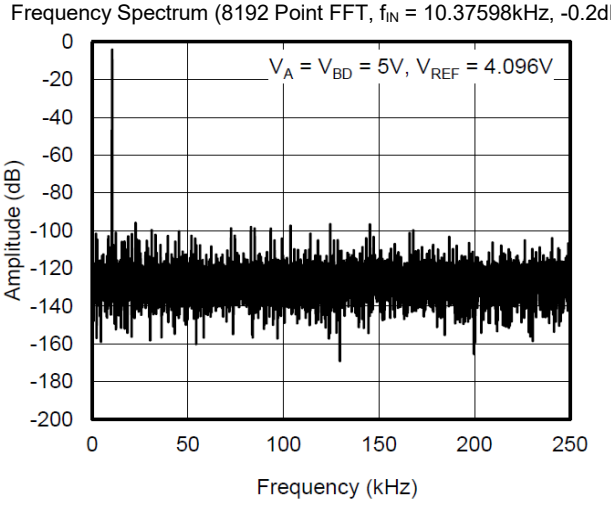
Frequency Spectrum (8192 Point FFT, f_{IN} = 1.0376kHz, -0.2dB)



Frequency Spectrum (8192 Point FFT, f_{IN} = 10.37598kHz, -0.2dB)



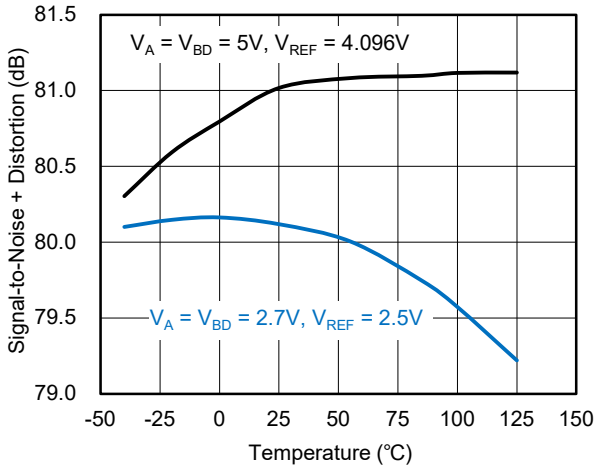
Frequency Spectrum (8192 Point FFT, f_{IN} = 10.37598kHz, -0.2dB)



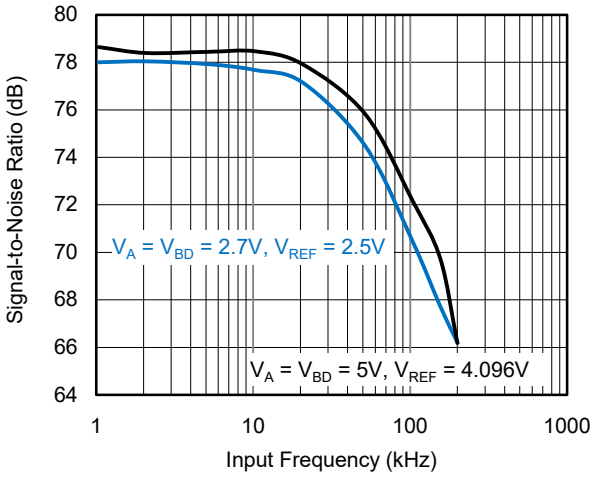
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{REF} (REF+ - REF-) = 4.096V when V_A = V_{BD} = 5V or V_{REF} (REF+ - REF-) = 2.5V when V_A = V_{BD} = 2.7V, f_{SCLK} = 21MHz, and f_{SAMPLE} = 500kSPS, unless otherwise noted.

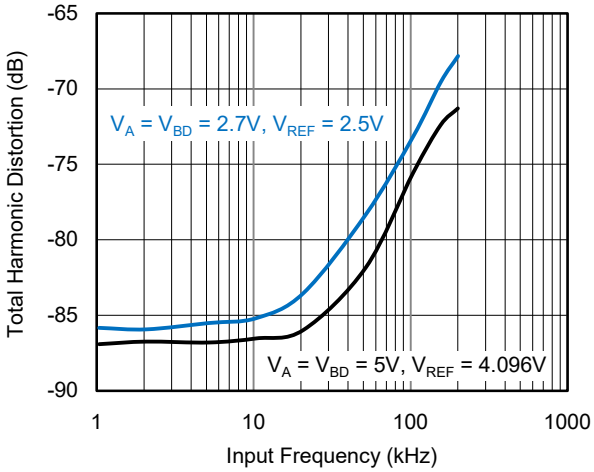
Signal-to-Noise + Distortion vs. Temperature



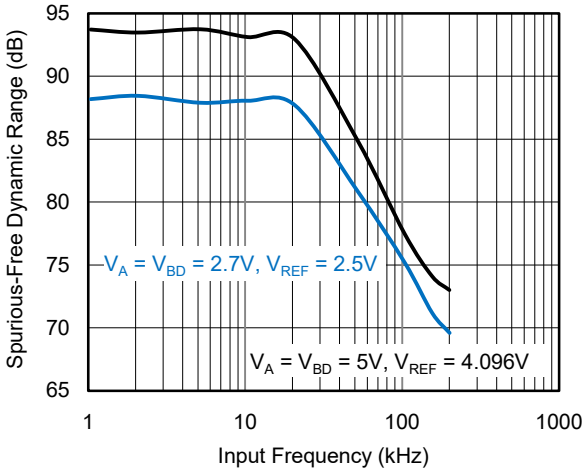
Signal-to-Noise Ratio vs. Input Frequency



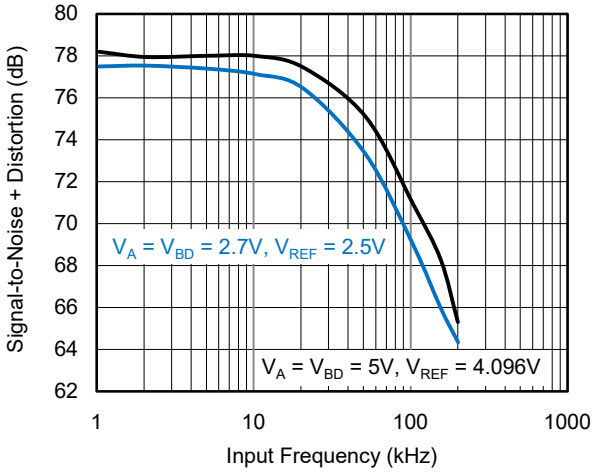
Total Harmonic Distortion vs. Input Frequency



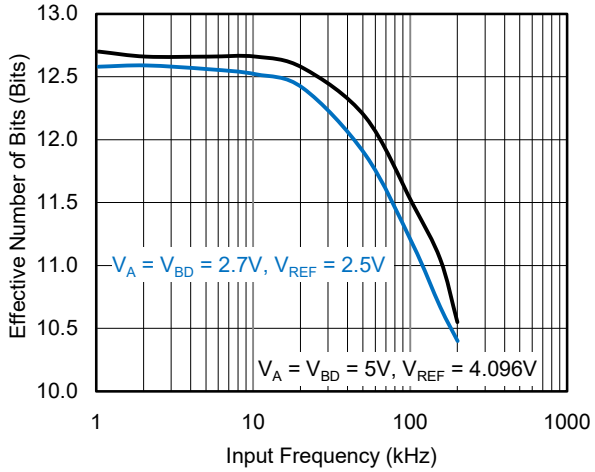
Spurious-Free Dynamic Range vs. Input Frequency



Signal-to-Noise + Distortion vs. Input Frequency



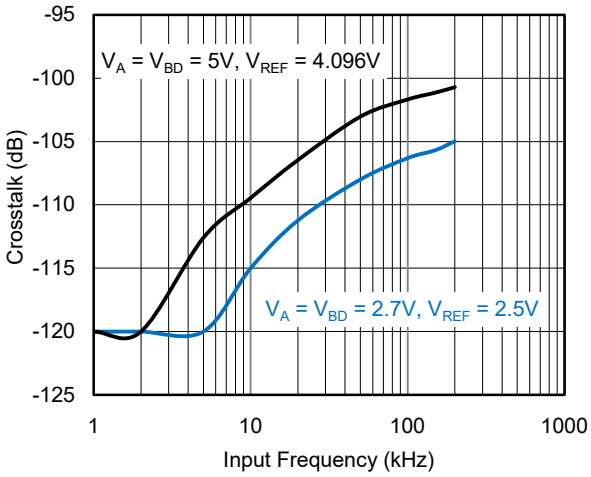
Effective Number of Bits vs. Input Frequency



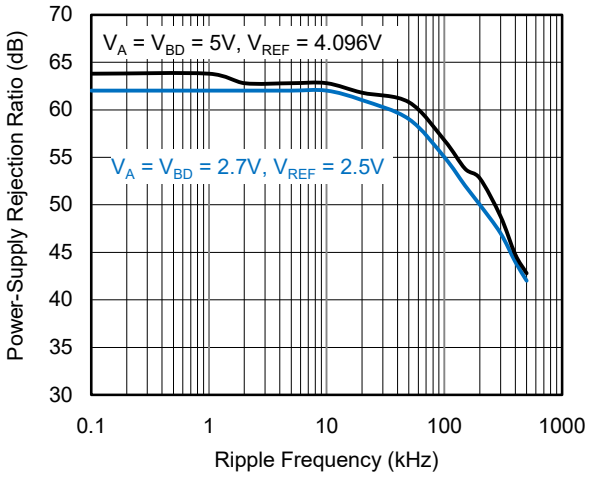
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{REF} (REF+ - REF-) = 4.096V when V_A = V_{BD} = 5V or V_{REF} (REF+ - REF-) = 2.5V when V_A = V_{BD} = 2.7V, f_{SCLK} = 21MHz, and f_{SAMPLE} = 500kSPS, unless otherwise noted.

Crosstalk vs. Input Frequency



Power-Supply Rejection Ratio vs. Power-Supply Ripple Frequency



FUNCTIONAL BLOCK DIAGRAM

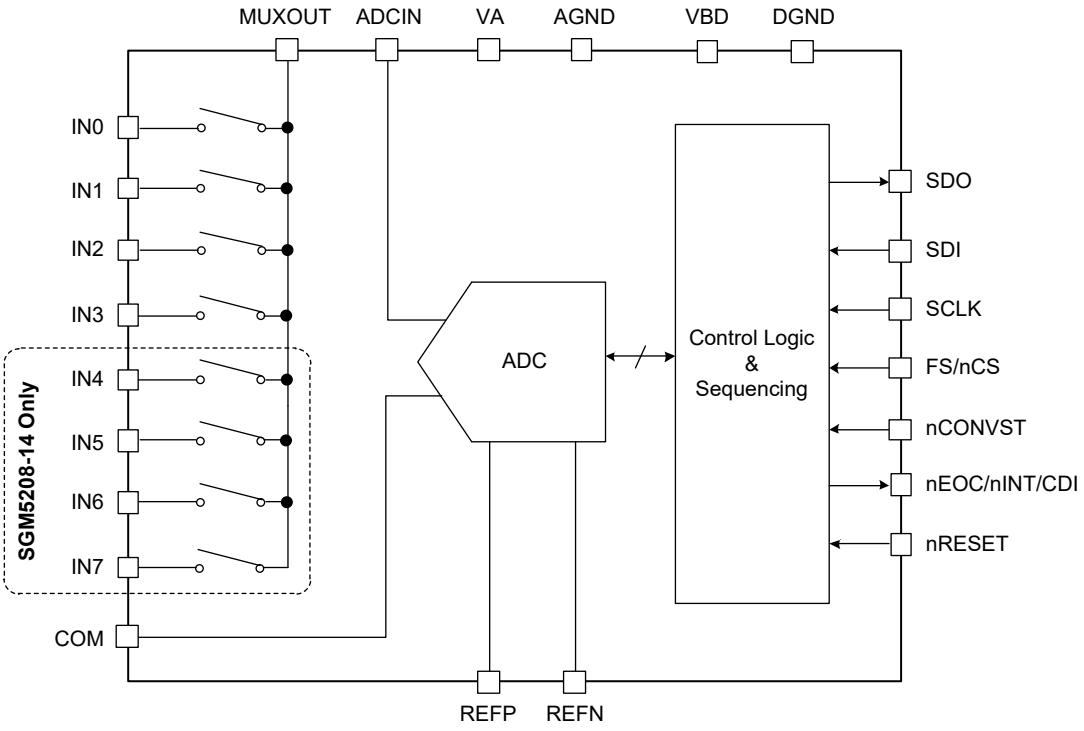


Figure 5. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM5208-14 and SGM5209-14 are low-power, high-speed, successive approximation register (SAR) analog-to-digital converters (ADCs). They need to work with an external voltage reference.

The SGM5208-14 has 8 single-ended input channels, and the SGM5209-14 has 4 single-ended input channels. All inputs share the same common pin (COM pin).

The SGM5208-14 and SGM5209-14 can be driven by either an internal clock, or an external clock (SCLK).

The SGM5208-14 and SGM5209-14 have two working modes, manual channel select mode and auto channel select mode.

Signal Conditioning

For the input signal pre-conditioning, it is recommended to add an amplifier or a PGA (Programmable Gain Amplifier) between the MUXOUT pin and ADCIN pin.

Analog Input

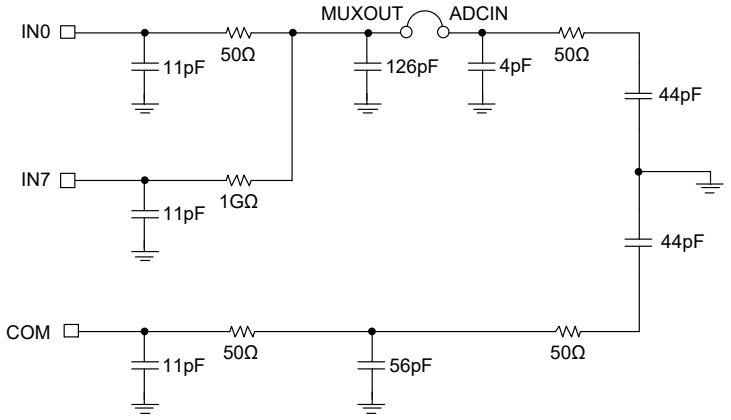
The input signal applied to INx and COM must be limited to the range listed in the Electrical Characteristics table.

The SGM5208-14 and SGM5209-14 are the capacitor array SAR ADCs. During the sampling period, there is an input current flowing into the ADC. The peak input current depends on the sampling rate, reference voltage, input voltage and signal source impedance.

A driver amplifier is usually recommended to buffer the signal source. It makes the analog input source to charge the equivalent input capacitor (48pF) to a 14-bit accuracy level in the acquisition time (240ns). When the input capacitor is fully charged, no further current flows. An equivalent input circuit is shown in Figure 6.

Driver Amplifier Choice

In a demo circuit, the SGM8968-1 is used for the source-follower (unity-gain) configuration, which is shown in Figure 7 with the recommended RC filter values. Low-bandwidth input signals with low-pass filters can be used to minimize noise.



NOTE: IN0 is assumed to be on, and IN7 is assumed to be off.

Figure 6. Equivalent Input Circuit

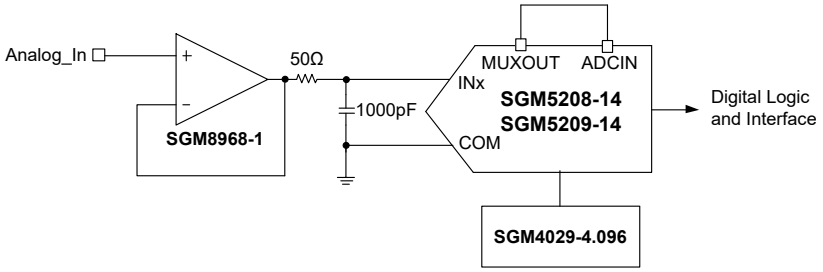


Figure 7. Unipolar Input Drive Configuration

DETAILED DESCRIPTION (continued)

Device Functional Modes

Reference

The SGM5208-14 and SGM5209-14 must be operated with an external voltage reference. The available range is 1.2V to 4.2V. It is recommended to place a 10μF decoupling capacitor between the reference output and the ADC REF input pin.

Converter Operation

The ADC conversion of SGM5208-14/SGM5209-14 is driven by the conversion clock (CCLK) source.

The CCLK source can be selected by software either from an internal oscillator or an external clock (SCLK).

When the CCLK is from the internal oscillator, its minimum frequency is 8.6MHz. The minimum sampling time is 3 CCLK cycles. The minimum conversion time is 18 CCLK cycles.

When the CCLK is from the external clock (SCLK), its maximum frequency is 21MHz. The frequency of SCLK is divided by a factor of two, because the CCLK is toggled on the rising edge of SCLK. In manual-trigger mode, the start of a conversion is triggered by a specific rising edge of SCLK. It will take a minimum 20ns to set up between the falling edge of nCONVST and the rising edge of SCLK. The minimum conversion time is 18 CCLK cycles.

When the SCLK is used to drive ADC conversion, it must meet the minimum high time and low time requirements. The SCLK must meet the minimum rise time, fall time and low jitter to get the best converter performance.

Manual Channel Select Mode

To enter the manual channel select mode, it needs to take two steps. The first step is to set the Configuration register (CFR) to enable the manual channel select mode. The second step is to set the target channel number by configuring the Command register (CMR). Figure 8 shows a demo of the channel switching timing sequence in manual channel select mode.

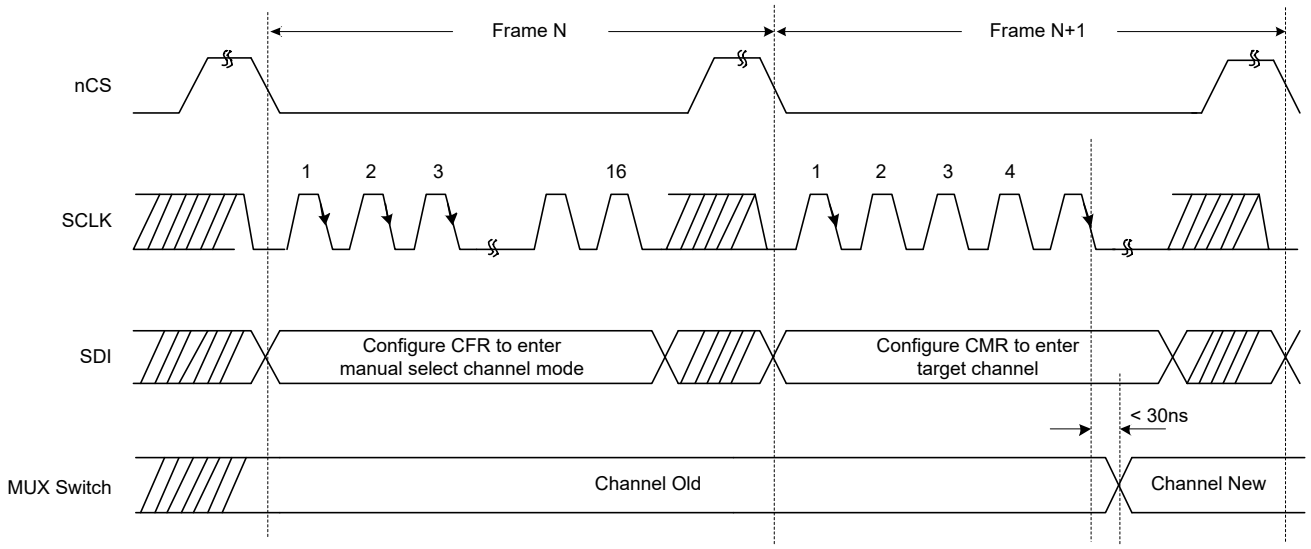


Figure 8. Manual Channel Select Mode Timing

DETAILED DESCRIPTION (continued)

Auto Channel Select Mode

If the chip is configured to work in auto channel select mode, the chip scans all channels in a fixed order and repeats the cycle. The first channel of the cycle scanning starts the channel in manual channel mode. For example, if in manual channel mode, channel 3 is the conversion channel, the auto scanning sequence is 3, 4, 5, 6, 7, 3, and so forth (for the SGM5209-14, the sequence is 3, 4, 3). Figure 9 shows a demo of the channel switching timing sequence in auto channel select mode. The chip quits the scanning cycle after CFR bit D[11] is cleared to 0.

Start of a Conversion

The input signal is sampled on the falling edge of nCONVST, and the pin should be kept low for minimum of 120ns. After the input signal is sampled, the conversion is started at the same time. The conversion time is 18 CCLK cycles. The minimum time between two nCONVST falling pulses is 21 CCLKs. The time between a conversion completed and a new falling edge of nCONVST is the acquisition time.

To allow multiple chips to sample simultaneously, the nCONVST pins of all chips can be controlled by one common logic controller's output (please consider the driving ability of controller's output pin).

A conversion also can be triggered internally without an nCONVST signal. To let the chip work in auto-trigger mode, configure the CFR bit D[9] to 0. Under this auto-trigger mode, when a conversion is completed, it will take 3 more CCLK cycles (if the CFR bit D[8] is set to 0, see Table 4 and Table 5 for details), the next conversion is automatically triggered. Total acquisition time and conversion time are 21 CCLK cycles (if the CFR bit D[8] is set to 0, see Table 4 and Table 5 for details).

The different conversion modes are shown in Table 1.

Note that when the chip is configured to work with manual channel select and auto-trigger mode, it is usually used for a single channel conversion. If there is an input channel switching in this mode, the chip must be set to manual-trigger mode before an input MUX switching. After the channel switching is completed, the chip can be re-configured to work with manual channel select and auto-trigger mode.

Table 1. Different Conversion Types

Mode	Select Channel	Start Conversion
Automatic	**Auto Channel Select** (1)**:** The chip scans the input channels automatically. There is no need to write channel number to CMR. More details refer to Auto Channel Select Mode section	**Auto-Trigger Mode:** Start a conversion with sequenced CCLK automatically
Manual	**Manual Channel Select:** Select the channel number by CMR command	**Manual-Trigger Mode:** Start a conversion with nCONVST

NOTE:
1. It is recommended that auto channel select mode should be worked with auto-trigger mode and TAG bit output enabled.

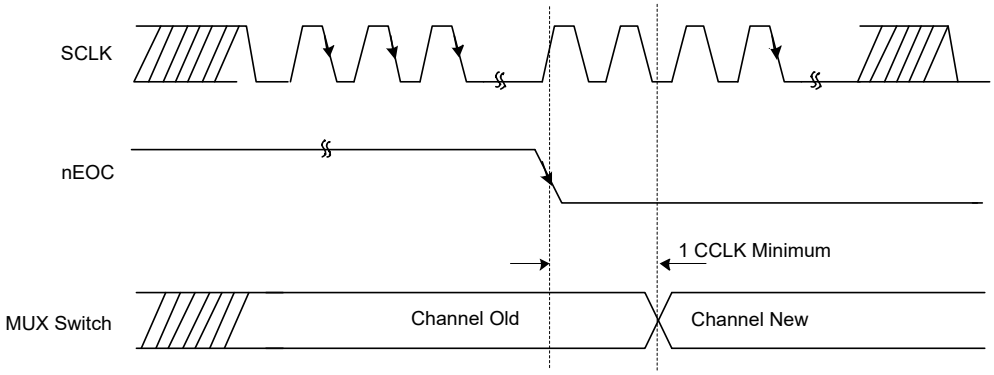


Figure 9. Channel Number Updated in Auto Channel Select Mode Timing

DETAILED DESCRIPTION (continued)

Status Output Pin (nEOC/nINT)

The function of the nEOC/nINT pin is software configurable. When the pin is used as nEOC output and its active polarity is set low, the pin will keep low throughout the conversion and go high if the conversion is completed. In manual-trigger mode, the pin goes low immediately once the nCONVST goes low, the pin will go high once the conversion is completed. In auto-trigger mode, after finishing the previous conversion, the pin goes high, and the pin will keep high for the first 3 CCLK cycles in the next conversion process frame.

If the pin of nEOC/nINT is configured as an interrupt output and active low, it goes low at the end of a conversion, and will go high by the next read cycle.

The function of the pin nEOC/nINT is set by CFR bit D[6]. The output polarity of the pin is set by CFR bit D[7].

Power-Down Modes

The chip has 3 power-down modes, including Nap, Deep, and Auto-Nap. They are all controlled by CFR according bits (refer to Table 5 for details).

Once the Nap power-down mode is enabled, the power consumption will reduce to around 2.6mA in 200ns. There are several ways to call the chip to quit this power-down mode, disable this mode, issue a wake-up command, reset CFR to default value, or reset the chip (software or hardware, see Table 4 and Table 5 for further information). It will take the chip 3 CCLK cycles to wake up from Nap power-down mode.

If the Deep power-down mode is enabled, the chip will be shut down and the power consumption will drop to about 25.2μA in 50ns. The wake-up time from this mode is about 150μs. The methods of calling the chip to wake up are the same as waking from Nap power-down mode.

Once the Auto-Nap power-down mode is enabled, the chip will go to Nap power-down automatically after the next conversion is completed. The power consumption will reduce to around 2.6mA in 200ns. To call the chip to quit Auto-Nap power-down mode, besides the same method as the same as quitting Nap power-down mode, issuing a manual channel select command or starting a conversion also can call the chip to wake up. It will take the chip 3 CCLK cycles to wake up from Auto-Nap power-down mode.

Table 2 shows a comparison of the three power-down modes.

Table 2. Comparison of Power-Down Modes

Power-Down Type	Power Consumption at V_A = 5V	Power-Down by	Power-Down Time	Wake-Up by	Wake-Up Time	Enable
Normal Operation	6.5mA	—	—	—	—	—
Deep Power-Down	25.2μA	Setting CFR bit D[2]	50ns	Wake-up command 1011b	150μs	Set CFR bit D[2]
Nap Power-Down	2.6mA	Setting CFR bit D[3]	200ns	Wake-up command 1011b	3 CCLKs	Set CFR bit D[3]
Auto-Nap Power-Down	2.6mA	nEOC (end of conversion)	200ns	nCONVST, any channel select command, default command 1111b, or wake-up command 1011b	3 CCLKs	Set CFR bit D[4]

DETAILED DESCRIPTION (continued)

Auto-Nap and Acquisition Time

Figure 10 shows the timing diagram for nCONVST, nEOC and Auto-Nap power-down signals in manual-trigger mode. The nCONVST signal triggers the chip to wake up. It will take at least 3 CCLK cycles (3 Conversion Clock Cycles) to wake up and 3 CCLK cycles to acquire input.

The SGM5208-14 and SGM5209-14 support two kinds of sampling rate 500kSPS and 250kSPS in auto-trigger mode. In 500kSPS sampling mode, it works in 21 CCLK cycles per conversion. In 250kSPS sampling mode, it works in 42 CCLK cycles per conversion.

The Nap power-down and Deep power-down are both available in 500kSPS and 250kSPS sampling modes. The Auto-Nap power-down is only available in 250kSPS sampling mode, because there is no time for the core to power down in 500kSPS sampling rate.

Figure 11 shows a timing diagram for the conversion sequence in auto-trigger mode with Auto-Nap power-down signals in 250kSPS sampling rate. For 16-bit word output, two consecutive conversions are 42 CCLK cycles apart. Nap_IN (active high, the signal powers down the ADC core) goes low 6 CCLK cycles ahead of the falling edge of nCONVST_IN (internal signal, active low). Nap_IN calls up the ADC core. It takes 3 CCLK cycles to power up the ADC core, and another 3 CCLK cycles are acquisition time. After the conversion is completed, the chip goes power-down automatically.

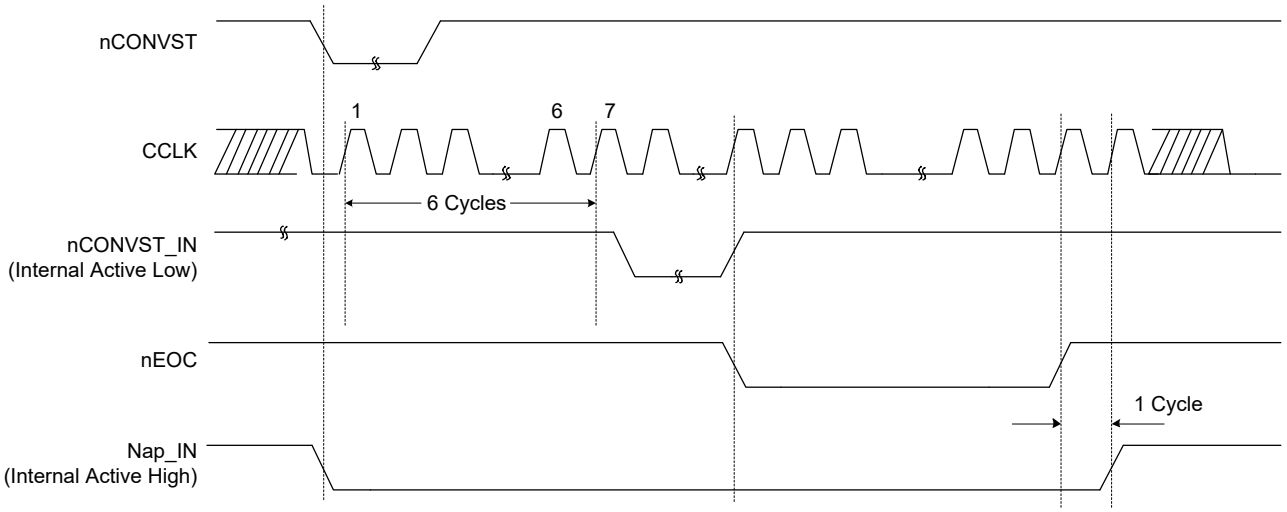


Figure 10. Timing Diagram for nCONVST, nEOC, and Auto-Nap Power-Down Signals in Manual-Trigger Mode (3 CCLKs for Acquisition)

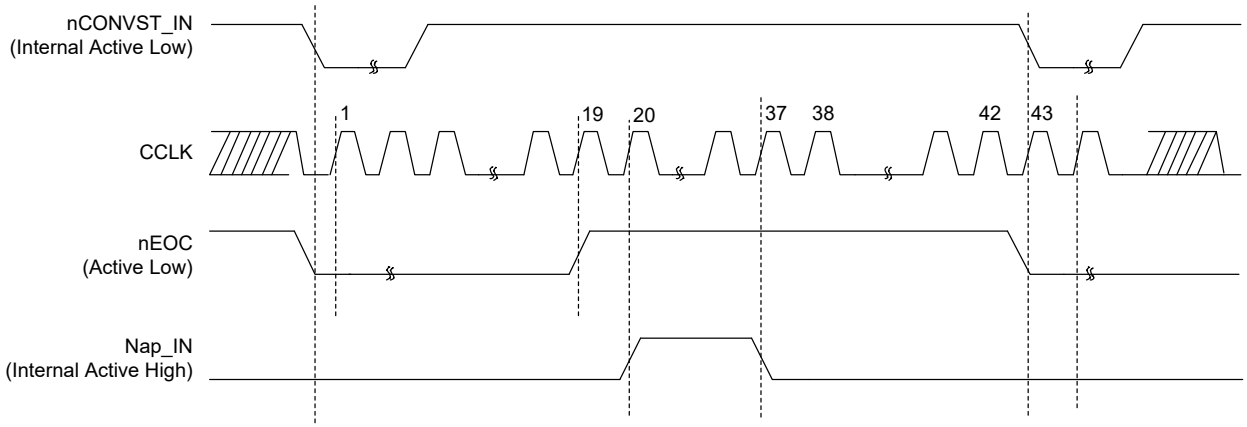


Figure 11. Timing Diagram for Conversion Start and Auto-Nap Power-Down Signals in Auto-Trigger Mode (250kSPS Sampling and 3 CCLKs for Acquisition)

DETAILED DESCRIPTION (continued)

Table 3 lists the total of the acquisition time and conversion time for the different combinations of triggers and power-down modes.

Table 3. Total Acquisition + Conversion Times

Mode	Acquisition + Conversion Time
Auto-Trigger at 500kSPS	= 21 CCLK
Manual-Trigger	≥ 21 CCLK
Manual-Trigger with Deep Power-Down	≥ 4 SCLK + 1μs + 3 CCLK + 18 CCLK + 16 SCLK + 150μs
Manual-Trigger with Nap Power-Down	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 16 SCLK + 200ns
Manual-Trigger with Auto-Nap Power-Down	≥ 4 SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 1 CCLK + 200ns (using wake-up to resume)
	≥ 3 CCLK + 3 CCLK + 18 CCLK + 1 CCLK + 200ns (using nCONVST to resume)

Figure 12 to Figure 14 show the different combinations of various trigger and power-down modes.

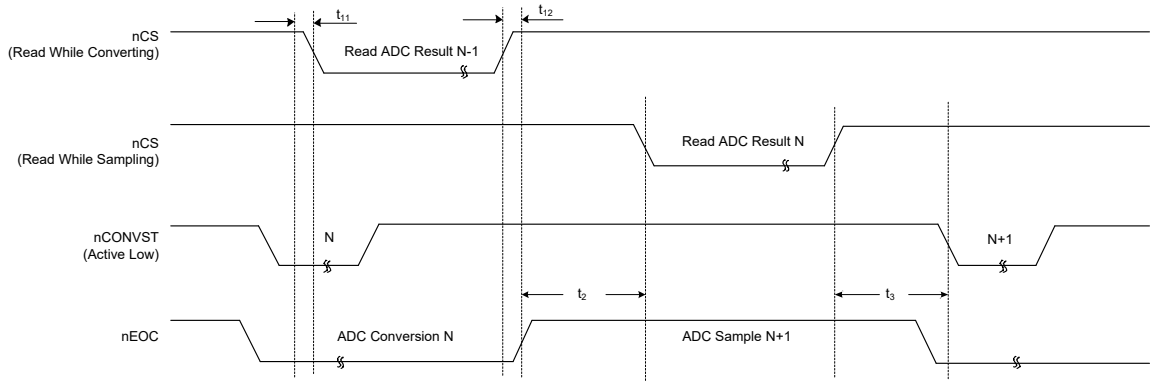
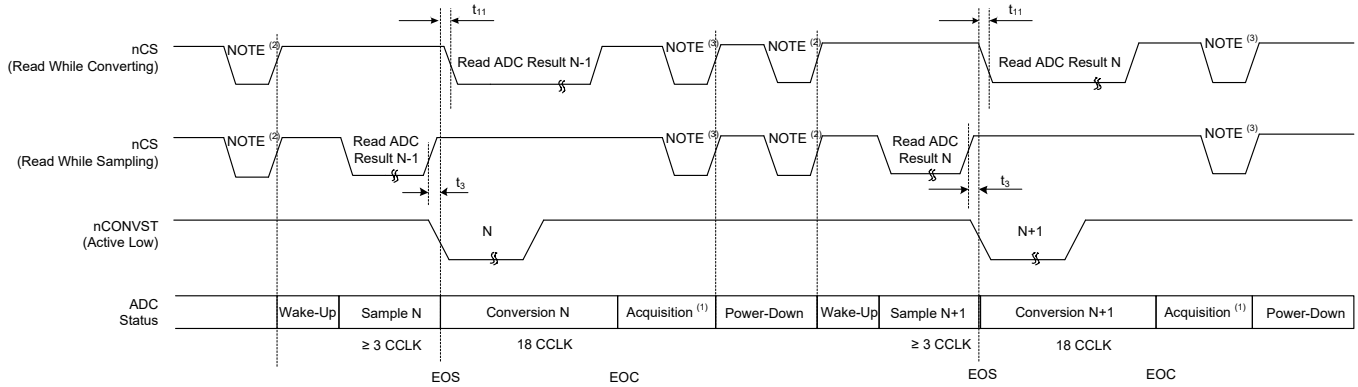


Figure 12. Read While Converting vs. Read While Sampling (Manual-Trigger Mode)

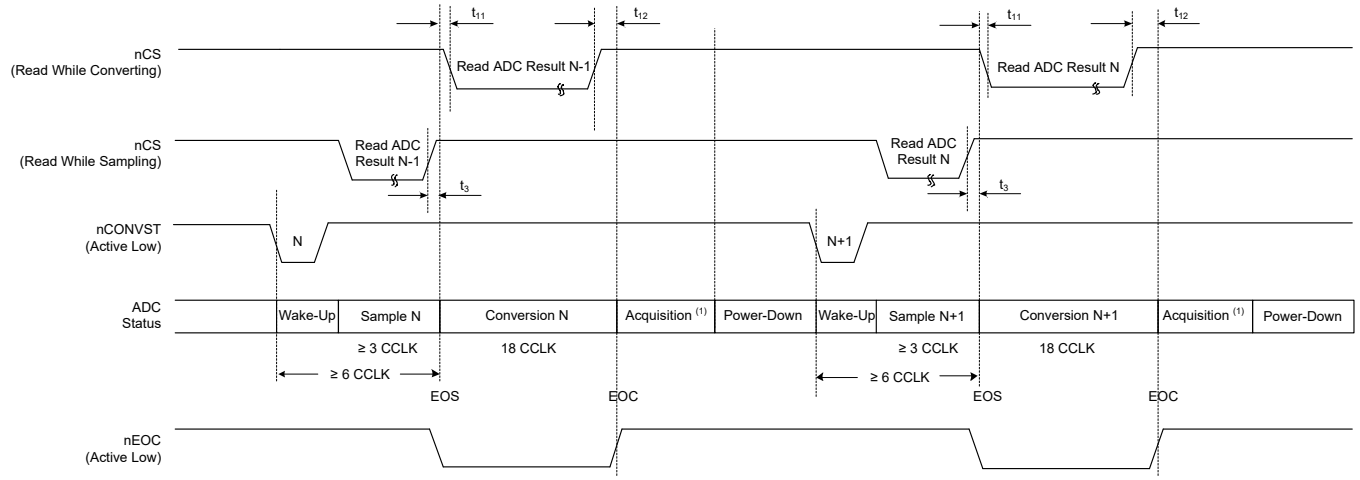


NOTES:
1. The ADC is in acquisition time.
2. Command on SDI pin is minimum 4 SCLK cycles.
3. Command on SDI pin is minimum 16 SCLK cycles to set ADC into Nap or Deep power-down mode.

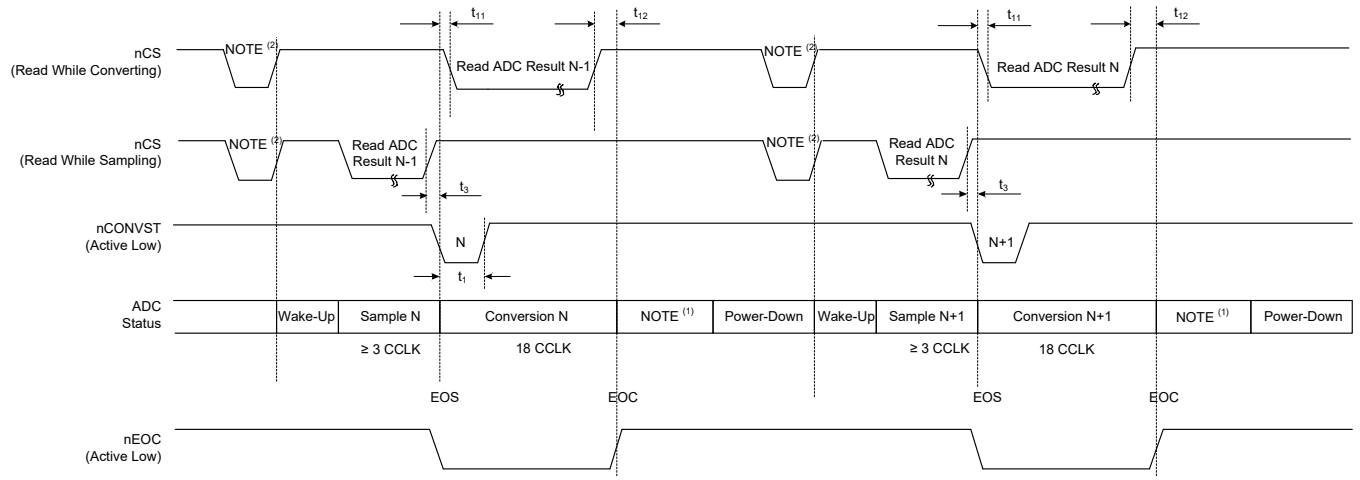
Figure 13. Read While Converting vs. Read While Sampling with Nap or Deep Power-Down (Manual-Trigger Mode)

DETAILED DESCRIPTION (continued)

Manual-Trigger Case 1: Wake-Up Using nCONVST



Manual-Trigger Case 2: Wake-Up Using WAKEUP Command



NOTES:
1. The time between the end of a conversion and Auto-Nap power-down is 1 CCLK cycle.
2. Command on SDI pin is minimum 4 CCLK cycles.

Figure 14. Read While Converting vs. Read While Sampling with Auto-Nap Power-Down

DETAILED DESCRIPTION (continued)

Programming

Digital Interface

The SCLK operation frequency of the interface is up to 25MHz. Each operation frame is started on the falling edge of the FS/nCS. The data input and output are both read on the falling edge of SCLK. The first bit of the output data is the most significant bit (MSB).

One complete serial I/O operation frame starts with the falling edge of FS/nCS, and ends on the 16th falling edge of SCLK. The interface works with the controller typical SPI setting CPOL = 1 (clock polarity) and CPHA = 0 (clock phase). This means that the falling edge of FS/nCS may happens when the SCLK is high. On the rising edge of the FS/nCS, it does not need to consider whether the SCLK is high or low, as long as there are enough SCLK falling edges before the rising edge of FS/nCS.

Internal Register

The internal register is composed of 4 bits of the Command register (CMR) and 12 bits of the Configuration register (CFR).

Writing to the Converter

The chip supports two types of writing to the registers, a 4-bit writing to CMR only and a 16-bit writing to CMR and CFR at the same time. More details refer to Table 4 and Table 5. When there is a 4-bit command, the command will take effect on the 4th falling edge of SCLK. A 16-bit read or write command will be at least 16 SCLK cycles, and in some exceptional cases, it will need more than 16 SCLK cycles (more details refer to Table 7).

Configuring the Converter and Default Mode

A 4-bit command will take effect on the 4th falling edge of SCLK. A 16-bit command will take effect on the 16th falling edge of SCLK.

After a power-on reset, or software reset, or hardware reset, the CFR will be reset to the default value.

The SPI interface of SGM5208-14/SGM5209-14 is full duplex. For all commands, except read CFR, the ADC conversion result is output on the SDO pin.

Table 4. Command Set Defined by Command Register (CMR) (1)

D[15:12]	Hex	Command	D[11:0]	Wake-Up from Auto-Nap	Minimum SCLKs Required	Type
0000b	0h	Select analog input channel 0	Don't care	Y	4	W
0001b	1h	Select analog input channel 1	Don't care	Y	4	W
0010b	2h	Select analog input channel 2	Don't care	Y	4	W
0011b	3h	Select analog input channel 3	Don't care	Y	4	W
0100b	4h	Select analog input channel 4 (2)	Don't care	Y	4	W
0101b	5h	Select analog input channel 5 (2)	Don't care	Y	4	W
0110b	6h	Select analog input channel 6 (2)	Don't care	Y	4	W
0111b	7h	Select analog input channel 7 (2)	Don't care	Y	4	W
1000b	8h	Reserved	Reserved	—	—	—
1001b	9h	Reserved	Reserved	—	—	—
1010b	Ah	Reserved	Reserved	—	—	—
1011b	Bh	Wake-up	Don't care	Y	4	W
1100b	Ch	Read CFR	Don't care	—	16	R
1101b	Dh	Read data	Don't care	—	16	R
1110b	Eh	Write CFR	CFR value	—	16	W
1111b	Fh	Default mode (load CFR with default value)	Don't care	Y	4	W

NOTES:
1. After the falling edge of FS/nCS, the first four bits of SDO are the four MSBs from the previous conversion result. The next 12 bits of SDO are the contents of the CFR.
2. These commands are not available for SGM5209-14.

DETAILED DESCRIPTION (continued)

Reading the Configuration Register

The controller can read back the content of CFR by issuing the read command 1100b. The read-back data is composed of 4-bit (MSBs) previous ADC conversion result plus 12-bit CFR contents. When issuing a read CFR command, nCONVST is not used and regardless of the activity of nEOC/nINT pin.

Table 5. 12-Bit Configuration Register (CFR) Details

BITS	DESCRIPTION	COMMENT
D[11]	Channel Select Mode 0 = Manual channel select mode is enabled. Use CMR command to access a desired channel 1 = Auto channel select mode is enabled. Channels are scanned automatically until the cycle after this bit is cleared to '0'.	
D[10]	Conversion Clock (CCLK) Source Select 0 = Conversion clock (CCLK) = SCLK/2 1 = Conversion clock (CCLK) = internal OSC	
D[9]	Trigger (Conversion Start) Select: Start Conversion at the End of Sampling (EOS) 0 = Auto-trigger mode: conversions are automatically trigged three conversion clocks after EOC at 500kSPS 1 = Manual-trigger mode: conversions are manually trigged on the falling edge of nCONVST	When D[9] = 0 and D[8] = 0, D[4] bit setting is ignored.
D[8]	Sample Rate for Auto-Trigger Mode 0 = 500kSPS (21 CCLKs) 1 = 250kSPS (42 CCLKs)	
D[7]	Pin 10 Polarity Select when Used as an Output (nEOC/nINT) 0 = nEOC/nINT active high 1 = nEOC/nINT active low	
D[6]	Pin 10 Function Select when Used as an Output (nEOC/nINT) 0 = Pin 10 is used as nINT 1 = Pin 10 is used as nEOC	
D[5]	Pin 10 I/O Function Select for Daisy-Chain Mode Operation 0 = Pin 10 is used as CDI input (daisy-chain mode is enabled) 1 = Pin 10 is used as nEOC/nINT output	
D[4]	Auto-Nap Power-Down Enable or Disable 0 = Auto-Nap power-down mode is enabled (not activated) 1 = Auto-Nap power-down mode is disabled	When D[9] = 0 and D[8] = 0, D[4] bit setting is ignored.
D[3]	Nap Power-Down Enable or Disable 0 = Nap power-down is enabled 1 = Nap power-down is disabled (resume normal operation)	The bit is reset to 1 automatically by wake-up command.
D[2]	Deep Power-Down Enable or Disable 0 = Deep power-down is enabled 1 = Deep power-down is disabled (resume normal operation)	The bit is reset to 1 automatically by wake-up command.
D[1]	TAG Bit Output Enable 0 = TAG bit output is disabled 1 = TAG bit output is enabled. TAG bits are attached in tail position after conversion data	
D[0]	Software Reset 0 = System reset, returns to 1 automatically 1 = Normal operation	

NOTE:
1. Default = FFFh.

DETAILED DESCRIPTION (continued)

Reading the Conversion Result

The ADC conversion result is available when the nEOC goes high and it is presented to the output register on the next falling edge of FS/nCS. The host controller can shift out the data on SDO pin at any time except the restricted quiet zone. The quiet zone is defined as 20ns before and 20ns after the end of sampling time (EOS). The EOS is defined as the falling edge of nCONVST in manual-trigger mode. The EOS is defined as the end of 3rd CCLK after nEOC in auto-trigger mode.

The falling edge of FS/nCS should not be set at the moment of the rising edge of nEOC, otherwise the ADC result will be corrupted. If the falling edge of FS/nCS is ahead of the nEOC, the previous result is read out.

The ADC result is in 14-bit strait binary format, as shown in Table 6. In general, at least 14 SCLK cycles is used to read out, and in some exceptional cases, more than 14 SCLK cycles is needed, as shown in Table 7. The data is shifted out by MSB first. If there are more SCLK cycles, 3 TAG bits (if enabled) are attached at the trailing of the ADC data, the others are filled with all 0s.

When FS/nCS is low, SDO is active and goes to 3-state on the rising edge of FS/nCS.

Note that whenever SDO is in output state, the output number of data bits depends on the number of SCLK cycles. For example, if there are 4 SCLK cycles, the first MSBs of data will be shifted out. If any kind of resets happen during the output cycle, the SDO shifts all 1s immediately.

If SCLK is used for the CCLK, it is not possible to shift out the 14-bit ADC data during the sampling time (6 SCLKs) due to the presence of quiet zone. In this case, it is recommended to read the ADC result during the conversion time (36 SCLKs or 48 SCLKs in Auto-Nap mode).

TAG Mode

The SGM5208-14 and SGM5209-14 support TAG features, which is used to indicate ADC result is from which input channel. When the TAG is enabled, at least 19 SCLK cycles (14-bit data + 2-bit 0 + 3-bit TAG) are required to read out all data. The TAG bits are attached the trailing of ADC result. TAG bits are set to '000' for channel 0, '001' for channel 1, and so on. TAG bits are set to '111' for channel 7.

Table 6. Ideal Input Voltages and Output Codes

Description	Analog Value	Digital Output Straight Binary	
		Binary Code	Hex Code
Full-Scale Range	V_{REF}	—	—
Least Significant Bit (LSB)	V_{REF}/16384	—	—
Full-Scale	V_{REF} - 1LSB	11 1111 1111 1111	3FFF
Midscale	V_{REF}/2	10 0000 0000 0000	2000
Midscale - 1LSB	V_{REF}/2 - 1LSB	01 1111 1111 1111	1FFF
Zero	0V	00 0000 0000 0000	0000

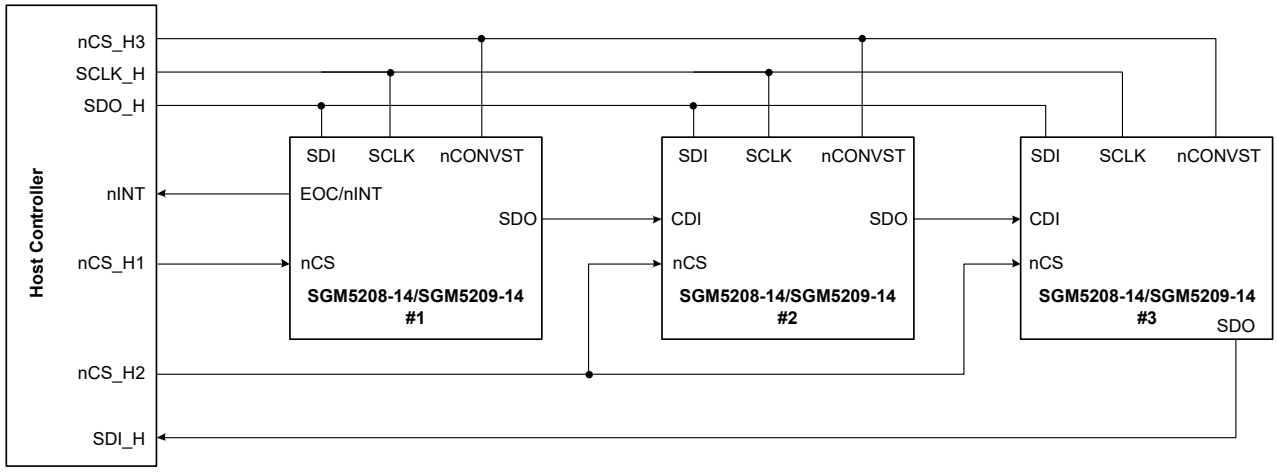
DETAILED DESCRIPTION (continued)

Daisy-Chain Mode

The SGM5208-14 and SGM5209-14 support daisy-chain connection. The CFR bit D[5] can configure the nEOC/nINT pin as the chain data input (CDI) pin. CDI pin is used for a secondary serial data input from an upstream converter.

Figure 15 shows a typical connection of three converters in daisy-chain mode.

Figure 16 shows a timing diagram in a daisy connection, the data in CDI pin goes through the chip to SDO, the serial input passes through each chip with a 16 SCLK cycles delay (TAG is not enabled, see Table 7 for more details about TAG) as long as nCS is active. The 3 chips sample and convert simultaneously in Figure 16.



NOTE:
Device #1 CFR D[5] = 1, Device #2 and Device #3 CFR D[5] = 0.

Figure 15. Connect Multiple Converters in Daisy-Chain Mode

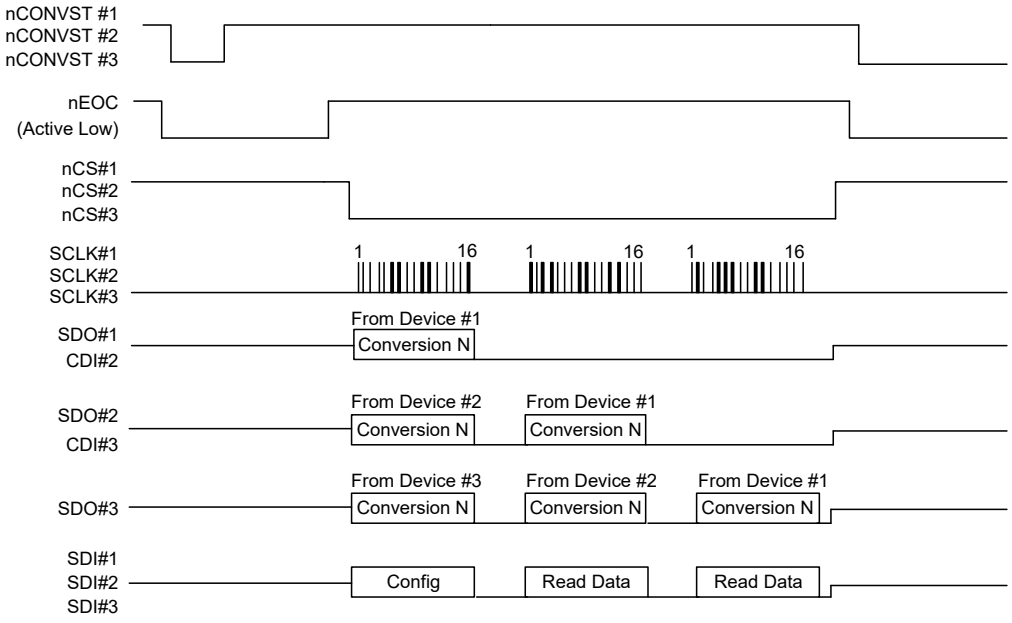


Figure 16. Timing Diagram in Daisy-Chain Mode with Shared nCONVST and Continuous nCS

DETAILED DESCRIPTION (continued)

Note that in the daisy-chain connection, the nCS must be hold low during the entirely data transferring period (in Figure 16, it is 24 SCLK cycles. Assuming TAG is not enabled, see Table 7 for more details about TAG).

If the nCS is toggled during the data transferring in a daisy-chain connection, the data stream cannot go through the daisy-chain, each SDO data always repeats the chip converter data in each nCS frame. An example of this case is shown in Figure 17.

For one chip, the number of SCLK cycles of each read frame is determined by the combination of different read modes.

There are different combination modes of daisy-chain mode, TAG mode, and the manner in which a channel is selected (such as auto channel select mode). Table 7 shows the required numbers of SCLKs for different readout modes.

In a daisy-chain connection, the maximum SCLK frequency may be affected by supply voltage and load when SCLK goes through the connection net of the chips. When the chips are configured in a daisy-chain mode, it is recommended to reduce the SCLK frequency.

Reset Function

There are 3 methods to reset the chip to default status, internal power-on reset (POR), software reset and hardware reset by nRESET pin.

The internal POR circuit will reset the chip to default mode when the chip is initially powered up. The software reset is issued by software command (CFR bit D[0] is set to 0). The software command will be automatically cleared to 1 after the chip is reset. The hardware reset is issued by holding the nRESET pin low at least 10ns. If the hardware reset function is not used, this pin must be tied to VBD.

If a reset function is performed, it will take the chip at least 150μs to be ready to work. During this time, any operation will be corrupted.

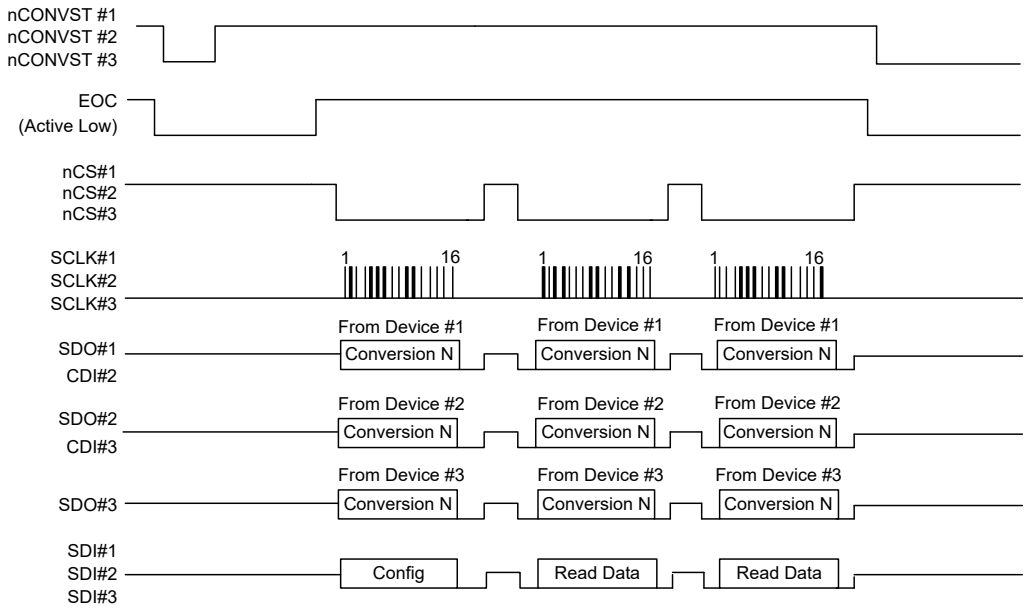


Figure 17. Timing Diagram in Daisy-Chain Mode with Shared nCONVST and Noncontinuous nCS

Table 7. Required SCLKs for Different Readout Mode Combinations

Daisy-Chain Mode CFR D[5]	TAG Mode CFR D[1]	Number of SCLK Cycles per SPI Read	Trailing Bits
1	0	14	None
1	1	≥ 19	TAG bits plus up to 5 zeros
0	0	16	None
0	1	24	TAG bits plus 5 zeros

APPLICATION INFORMATION

A Typical Connection of SGM5208-14/ SGM5209-14

A typical data acquisition circuit for the SGM5208-14/ SGM5209-14 is shown in Figure 18.

Power Supply Recommendations

The SGM5208-14 and SGM5209-14 have analog power supply V_A and digital interface power supply V_{BD}. If the two power supplies are not from a single voltage source, it is recommended to power on V_A firstly and then power on V_{BD}. The supply voltage V_{BD} should not be higher than the supply voltage V_A.

After the V_A and V_{BD} are powered on, it will take the chip at least 2ms to be ready to work. During this time, any operation will be corrupted.

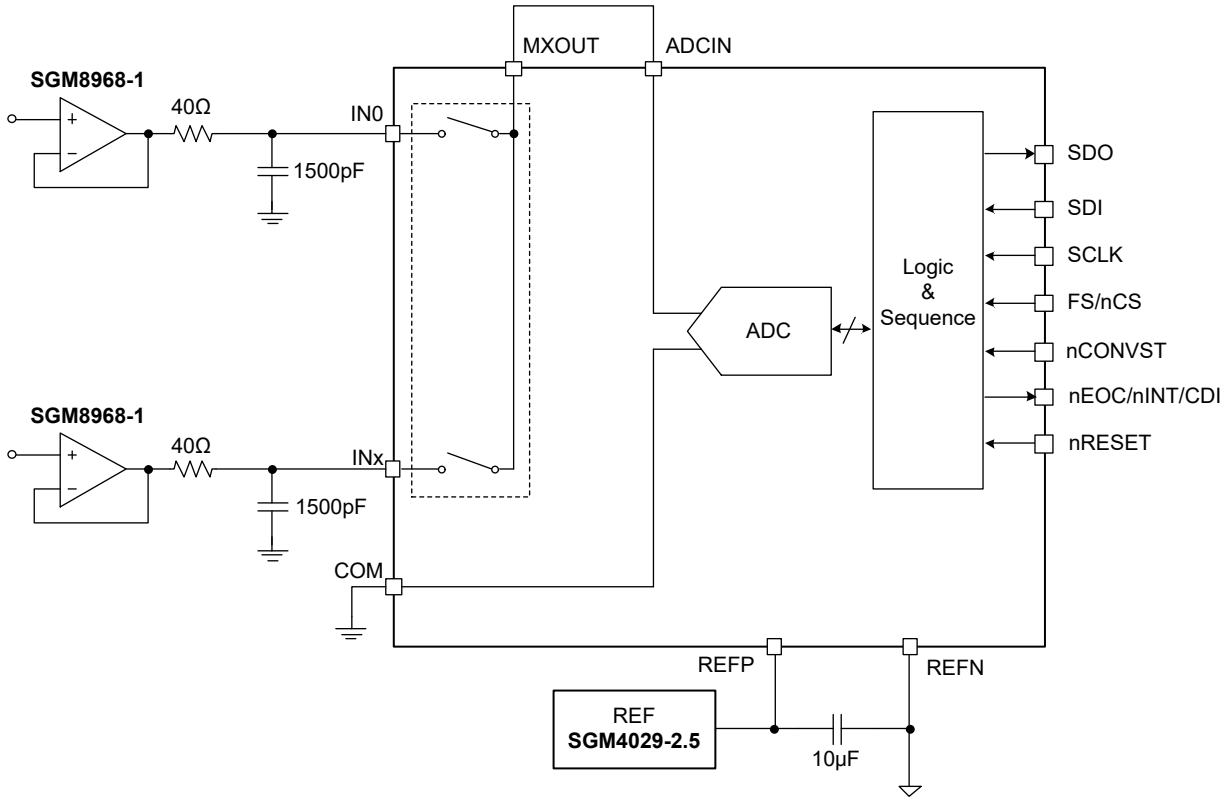


Figure 18. Typical Circuit Configuration

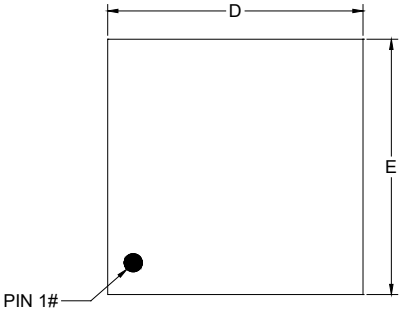
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

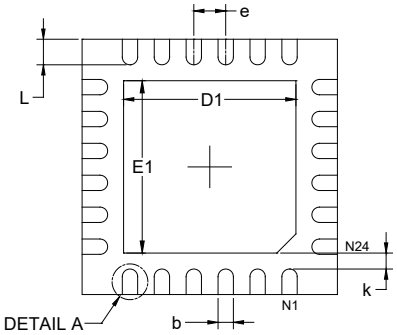
Changes from Original (JUNE 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

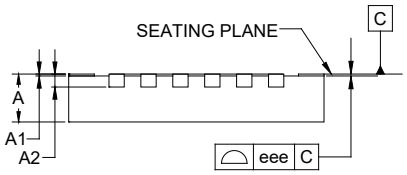
TQFN-4×4-24L



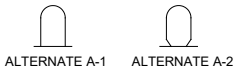
TOP VIEW



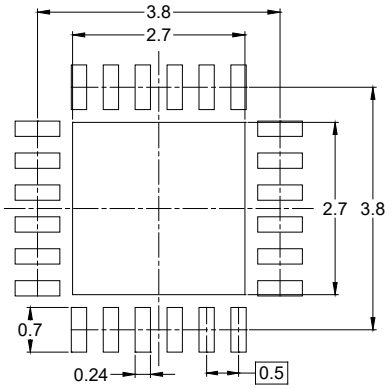
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



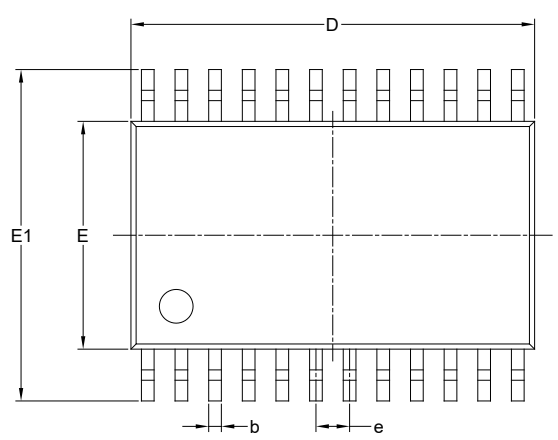
RECOMMENDED LAND PATTERN (Unit: mm)

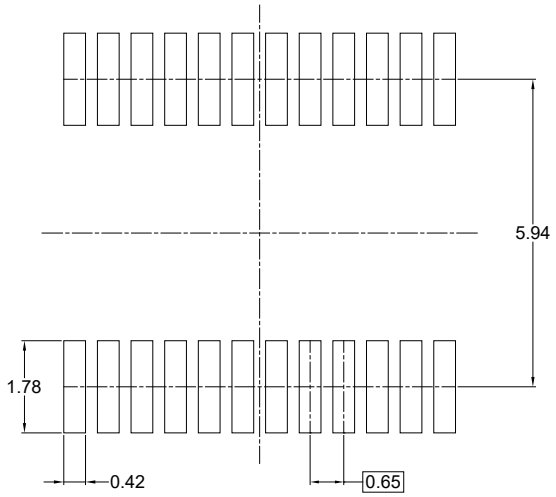
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.180	-	0.300
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.600	-	2.800
E1	2.600	-	2.800
e	0.500 BSC		
k	0.200 MIN		
L	0.300	-	0.500
eee	0.080		

NOTE: This drawing is subject to change without notice.

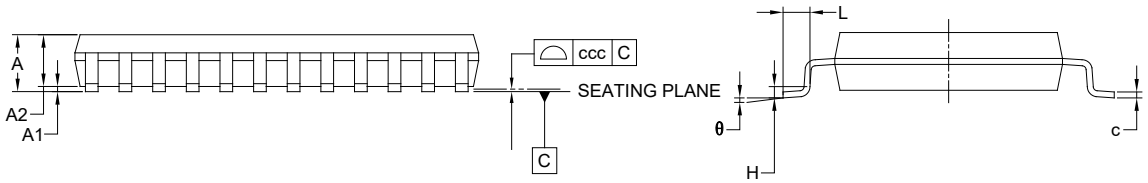
PACKAGE OUTLINE DIMENSIONS

TSSOP-24





RECOMMENDED LAND PATTERN (Unit: mm)

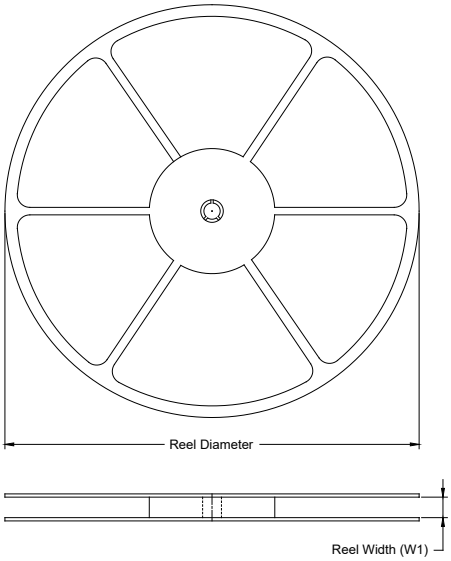


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	7.700	-	7.900
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

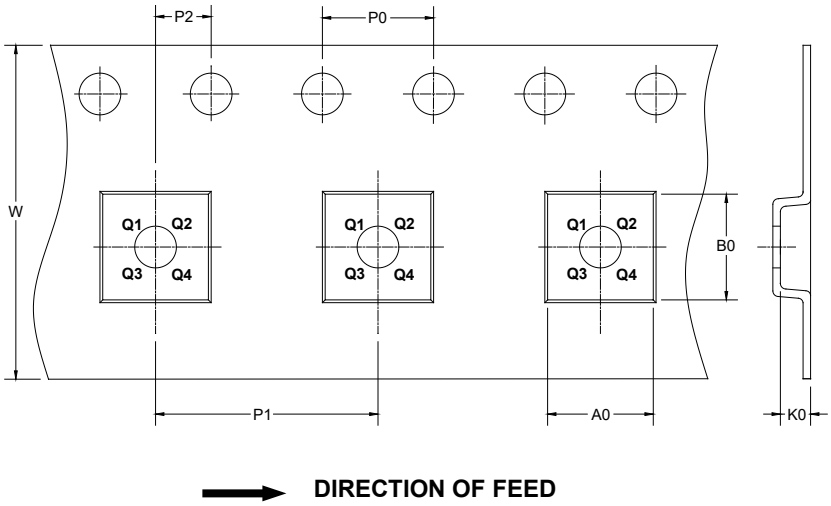
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



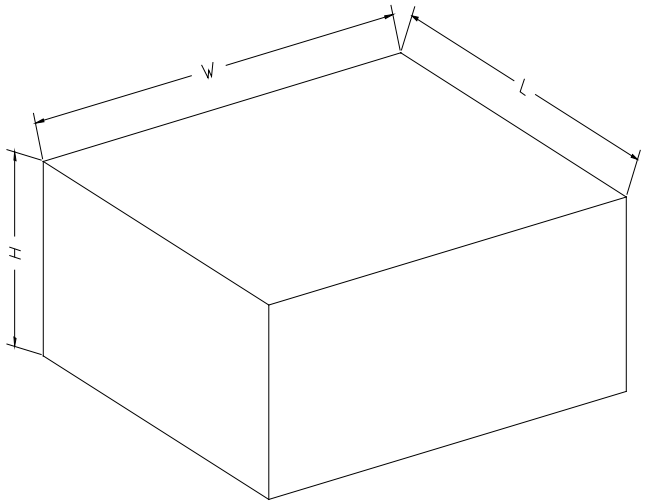
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2
TSSOP-24	13″	16.4	6.80	8.30	1.60	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002