

GENERAL DESCRIPTION

The SGM38042A generates both positive and negative precision regulated voltage power sources with a control scheme for single inductor dual output converter. The positive output is programmable from 2.4V to 6.4V with 100mV per step, and the negative output is programmable from -2V to -3.2V with 50mV per step.

A linear regulator capable of 50mA output current is also integrated. The device is equipped with 1-Wire interface. With input in the range of 2.7V to 5.5V, the device is optimized for loading 100mA in boost-inverter mode and also works in buck-inverter mode.

The SGM38042A is available in a Green WLCSP-1.51×2.10-15B package. It operates over an ambient temperature range of -40°C to +85°C.

FEATURES

- Single Inductor for Triple Outputs
- High Efficiency in Wide Output Loading Range
- 850kHz PWM Mode Control Switching Frequency
- Pulse-Skip Operation in Light Load Condition
- Programmable Outputs with 1-Wire Interface
 $V_{CPO} = 2.4V$ to $6.4V$
 $V_{CNO} = -2V$ to $-3.2V$
- Auxiliary Output Rail: Fixed 3.3V, 2.8V or 1.8V
- 100mA Output Current for V_{CPO} and V_{CNO}
- Configurable Active Discharge
- Internal Soft-Start to limit Inrush Current
- Over-Temperature Protection (OTP)
- Over-Current Protection (OCP)
- Short Circuit Protection (SCP)

SELECTABLE MODEL

Model	Default Outputs
SGM38042A-1	$V_{CPO} = 4.6V/V_{CNO} = -2.4V/V_{CVO} = 1.8V$
SGM38042A-2	$V_{CPO} = 3.3V/V_{CNO} = -3.0V/V_{CVO} = 1.8V$
SGM38042A-3	$V_{CPO} = 4.6V/V_{CNO} = -2.4V/V_{CVO} = 2.8V$
SGM38042A-4	$V_{CPO} = 3.3V/V_{CNO} = -3.0V/V_{CVO} = 2.8V$
SGM38042A-5	$V_{CPO} = 4.6V/V_{CNO} = -2.4V/V_{CVO} = 3.3V$

APPLICATIONS

AMOLED/LCD Smart-Phones/Media-Players
Wearable Device Display

TYPICAL APPLICATION

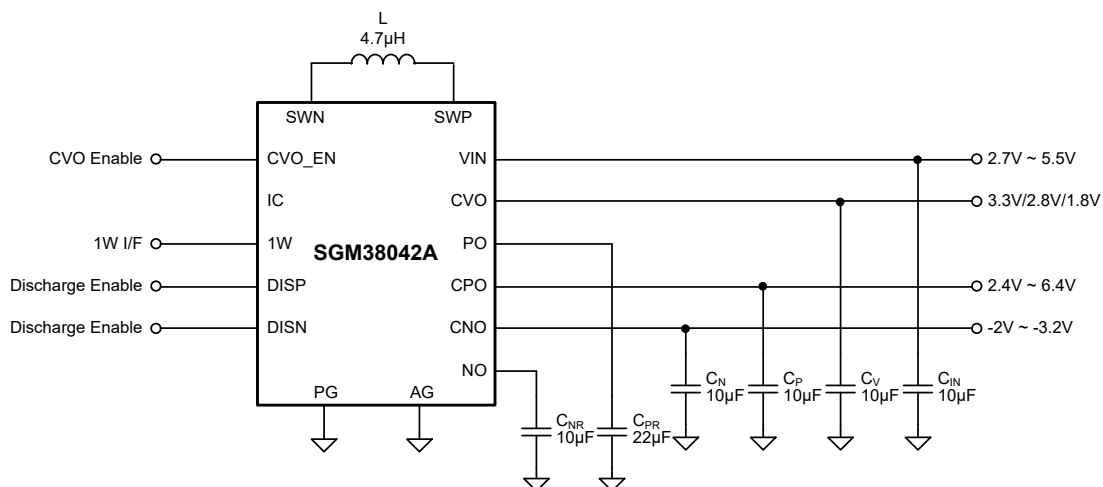


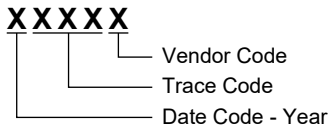
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM38042A-1	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042A-1YG/TR	XXXXX CF1YG	Tape and Reel, 3000
SGM38042A-2	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042A-2YG/TR	XXXXX CF2YG	Tape and Reel, 3000
SGM38042A-3	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042A-3YG/TR	XXXXX CF3YG	Tape and Reel, 3000
SGM38042A-4	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042A-4YG/TR	XXXXX CF4YG	Tape and Reel, 3000
SGM38042A-5	WLCSP-1.51×2.10-15B	-40°C to +85°C	SGM38042A-5YG/TR	XXXXX CMBYG	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, CVO_EN, IC, 1W, DISP, DISN Voltages	-0.3V to 6V
CVO Voltage	-0.3V to VIN + 0.3V
SWN Voltage	-6.7V to 6V
SWN Voltage (Transient: 10ns, 850kHz)	-8V to 8V
NO, CNO Voltages	-6.7V to 0.3V
SWP, PO, CPO Voltages	-0.3V to 6.7V
SWP Voltage (Transient: 10ns, 850kHz)	-2V to 8V
Package Thermal Resistance	
WLCSP-1.51×2.10-15B, θJA	102°C/W
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	4000V
CDM	1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	2.7V to 5.5V
Operating Ambient Temperature Range	-40°C to +85°C
Operating Junction Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

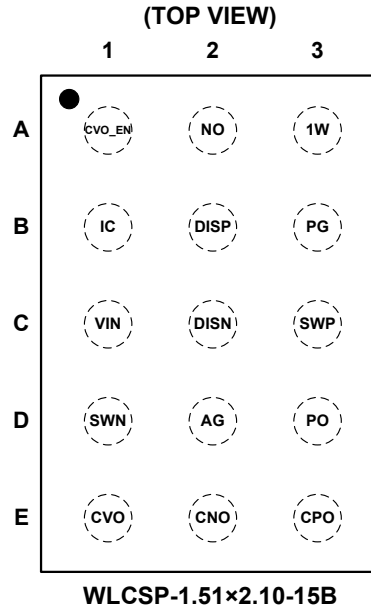
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	CVO_EN	I	Enable for CVO. 0: Disable the LDO; 1: Enable the LDO.
A2	NO	O	Converter Negative Output.
A3	1W	I	1-Wire Interface Input.
B1	IC	I	Internal Connection.
B2	DISP	I	0: Disable Conditioned Positive Output Discharge; 1: Enable Conditioned Positive Output Discharge.
B3	PG	–	Power Ground.
C1	VIN	–	Supply Input.
C2	DISN	I	0: Disable Conditioned Negative Output Discharge; 1: Enable Conditioned Negative Output Discharge.
C3	SWP	O	Switch Node for Powering the Positive-Rail. Connect this pin to one end of power inductor.
D1	SWN	O	Switch Node for Powering the Negative-Rail. Connect this pin to the other end of power inductor.
D2	AG	–	Analog Ground.
D3	PO	O	Converter Positive Output.
E1	CVO	O	Output of the Linear Regulator.
E2	CNO	O	Conditioned Negative Output.
E3	CPO	O	Conditioned Positive Output.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{IN} = 3.7V, CVO_EN = 1W = V_{IN}, Full = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
General Features							
Input Voltage Range	V _{IN}		+25°C	2.7		5.5	V
Under-Voltage Lockout Threshold	V _{UVLO}	V _{IN} falling	+25°C		2.2	2.65	V
Supply Current with No Load	I _Q	V _{IN} = 3.7V, no switching	+25°C		0.5	0.7	mA
Shutdown Current	I _{OFF}	V _{IN} = 3.7V, CVO_EN = 1W = GND	+25°C		0.4	1	μA
Power-On Blanking Time	t _{BLANK}	V _{IN} = 3.7V	+25°C		40		ms
Switching Frequency	f _{SW}	V _{IN} = 3.7V	+25°C		850		kHz
Inductor Peak Current	I _{PEAK}	V _{IN} = 3.7V	+25°C		0.8		A
Conditioned Positive Output Voltage Range	V _{CPO}		+25°C	2.4		6.4	V
Conditioned Positive Output Voltage Accuracy	V _{CPO_ACC_46}	V _{IN} = 3.7V, V _{CPO} = 4.6V	+25°C	-45		+45	mV
Discharge Resistor of Conditioned Positive Output	R _{DP}		+25°C		50		Ω
Discharge Time of Conditioned Positive Output	t _{DISP}		+25°C		10		ms
Conditioned Negative Output Voltage Range	V _{CNO}		+25°C	-3.2		-2	V
Conditioned Negative Output Voltage Accuracy	V _{CNO_ACC_24}	V _{IN} = 3.7V, V _{CNO} = -2.4V	+25°C	-45		+45	mV
Discharge Resistor of Conditioned Negative Output	R _{DN}		+25°C		50		Ω
Discharge Time of Conditioned Negative Output	t _{DISN}		+25°C		10		ms
Linear Regulator Output Voltage Accuracy	V _{CVO_ACC_33}	V _{IN} = 3.7V, V _{CVO} = 3.3V	+25°C		±120		mV
	V _{CVO_ACC_28}	V _{IN} = 3.7V, V _{CVO} = 2.8V	+25°C	-100		+100	mV
	V _{CVO_ACC_18}	V _{IN} = 3.7V, V _{CVO} = 1.8V	+25°C	-45		+45	mV
Linear Regulator Output Dropout Voltage	V _{CVO_DROP}	V _{IN} = 3V, V _{CVO} = 2.8V, I _{LOADCVO} = 100mA	+25°C		290		mV
Logic CVO_EN, 1W							
Low Level Input Voltage	V _{IL}	V _{IN} = 2.7V to 5.5V	Full			0.35	V
High Level Input Voltage	V _{IH}	V _{IN} = 2.7V to 5.5V	Full	1.05			V
CVO_EN and IC Pull-Down Resistors	R _{EN}		+25°C		200		kΩ
Thermal Shutdown							
Thermal Shutdown Threshold	T _{SHDN}				150		°C
Thermal Shutdown Hysteresis	T _{HYS}				15		°C

1-WIRE INTERFACE TIMING CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
1-Wire Initial Time	t_{IH}		0.5		ms
Soft-Start Time by 1-Wire Enable	t_{SS}		2		ms
1-Wire High Level Pulse Time	t_{SH}	2	20	75	μ s
1-Wire Low Level Pulse Time	t_{SL}	2	20	75	μ s
1-Wire Signal Stop Indication Time	t_{STOP}		300	400	μ s
V_{OUT} Turn-Off Delay by 1-Wire	$t_{VO_OFF_DLY}$		10		ms
t_{WAIT} after Data	t_{WAIT}		0		μ s
1-Wire Turn-Off Detection Time	t_{OFF_DLY}		350	450	μ s

1-WIRE PROTOCOL

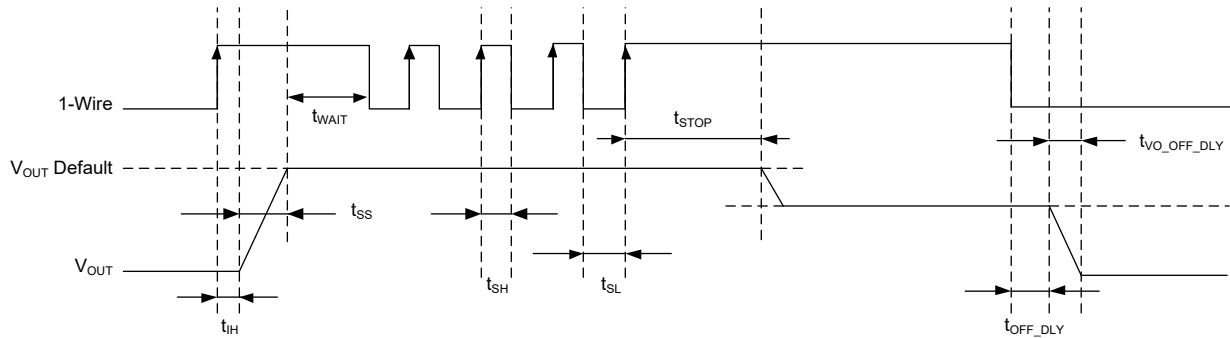


Figure 2. 1-Wire Protocol

1-WIRE PROGRAMMING

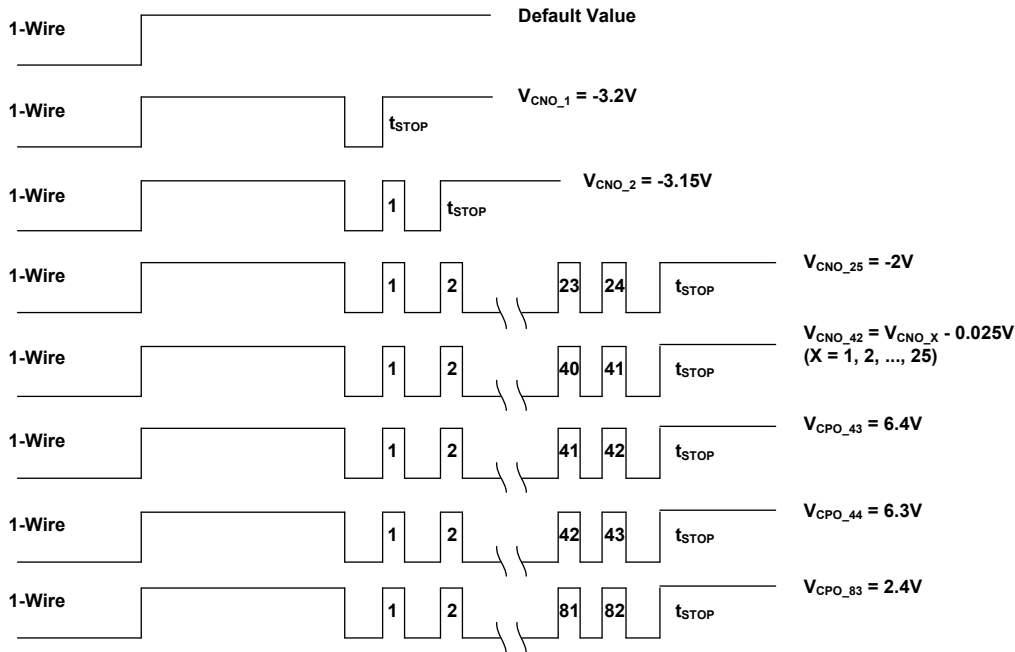


Figure 3. 1-Wire Programming

1-WIRE COUNTS TO VOLTAGE VALUE MAPPING

Counts	V _{CNO} (V)	V _{CPO} (V) ⁽¹⁾	COUNTS	V _{CNO} (V)	V _{CPO} (V)	Counts	V _{CNO} (V)	V _{CPO} (V)
1(43) ⁽¹⁾	-3.2	6.4	15(57)	-2.5	5.0	29(71)	Reserved	3.6
2(44)	-3.15	6.3	16(58)	-2.45	4.9	30(72)	Reserved	3.5
3(45)	-3.1	6.2	17(59)	-2.4	4.8	31(73)	Reserved	3.4
4(46)	-3.05	6.1	18(60)	-2.35	4.7	32(74)	Reserved	3.3
5(47)	-3	6.0	19(61)	-2.3	4.6	33(75)	Reserved	3.2
6(48)	-2.95	5.9	20(62)	-2.25	4.5	34(76)	Reserved	3.1
7(49)	-2.9	5.8	21(63)	-2.2	4.4	35(77)	Reserved	3.0
8(50)	-2.85	5.7	22(64)	-2.15	4.3	36(78)	Reserved	2.9
9(51)	-2.8	5.6	23(65)	-2.1	4.2	37(79)	Reserved	2.8
10(52)	-2.75	5.5	24(66)	-2.05	4.1	38(80)	Reserved	2.7
11(53)	-2.7	5.4	25(67)	-2	4.0	39(81)	Reserved	2.6
12(54)	-2.65	5.3	26(68)	Reserved	3.9	40(82)	Reserved	2.5
13(55)	-2.6	5.2	27(69)	Reserved	3.8	41(83)	Reserved	2.4
14(56)	-2.55	5.1	28(70)	Reserved	3.7	42	V _{CNO_X} - 0.025V	

NOTE: 1. Conditioned negative voltage is programmed with counts 1 ~ 25 and 42. Conditioned positive voltage is programmed with counts 43 ~ 83, which are listed between parentheses.

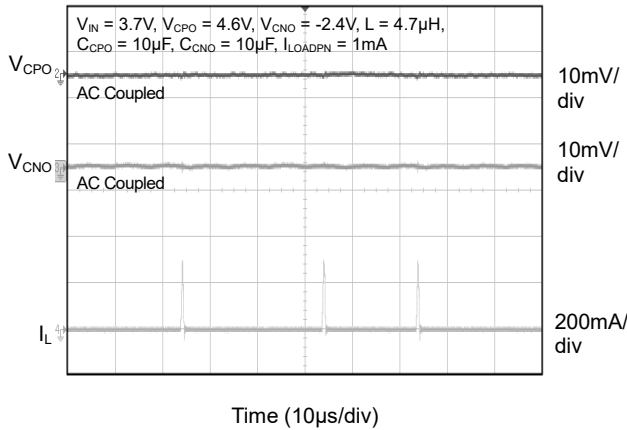
RECOMMENDED COMPONENTS OF TEST CIRCUITS

COMPONENT		COMPONENT	
INDUCTOR	4.7μH/SLF7055T-4R7N3R1-3PF	CAPACITOR	10μF/08055C106KAT2A

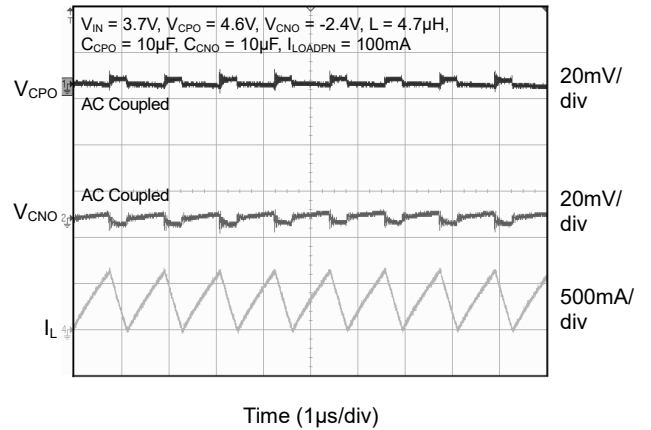
TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.7\text{V}$, $C_{VO_EN} = 1\text{W} = V_{IN}$, unless otherwise noted.

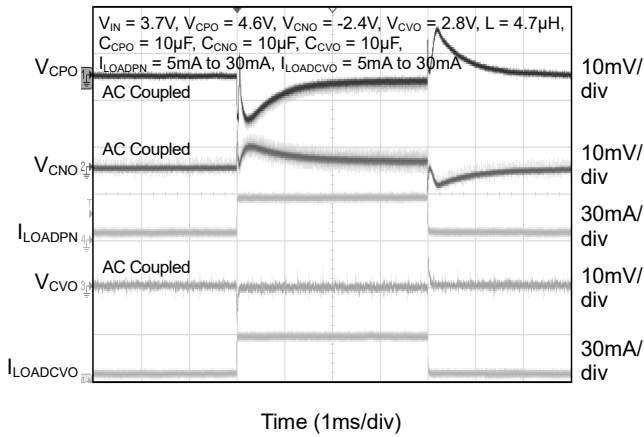
Output Ripple at Light Load



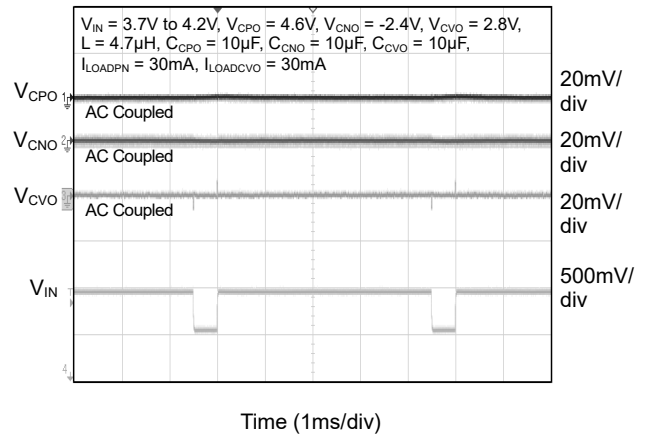
Output Ripple at Full Load



Load Transient Response

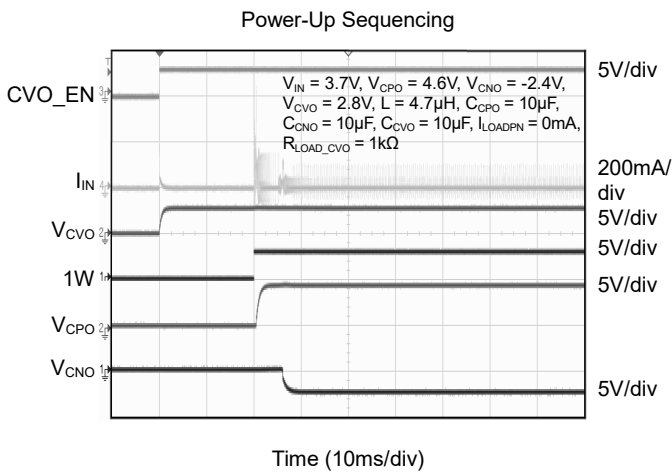
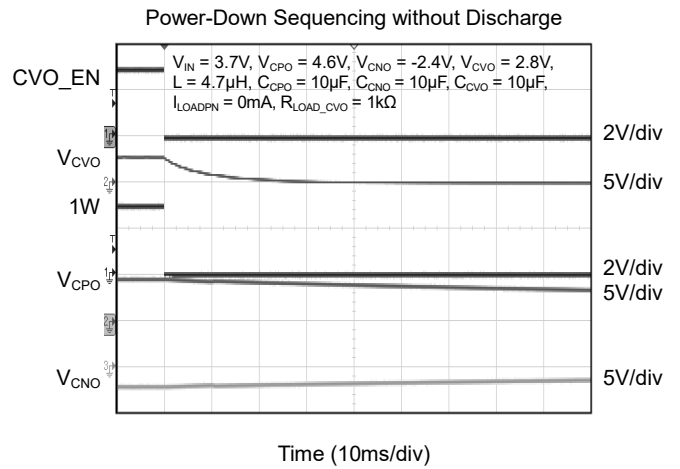
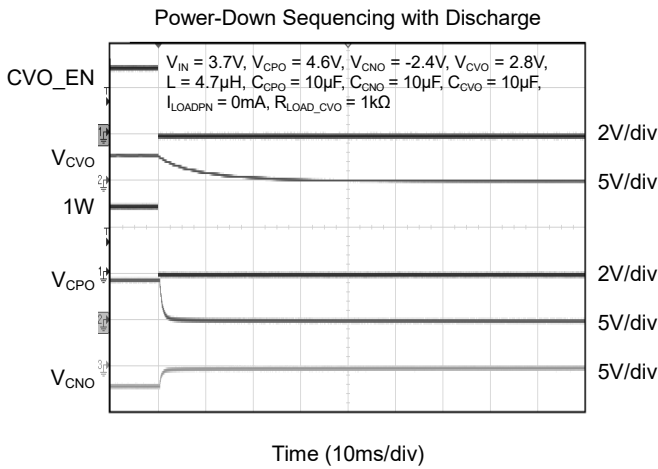


Line Transient Response



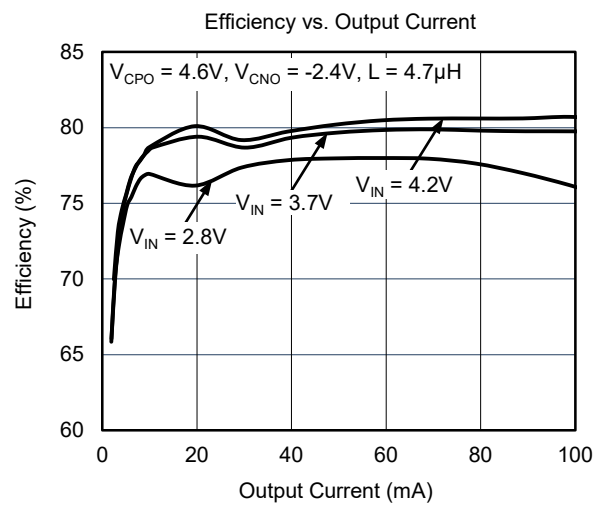
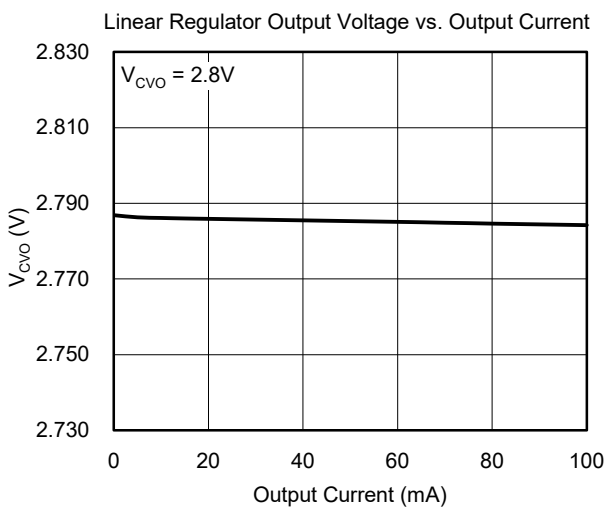
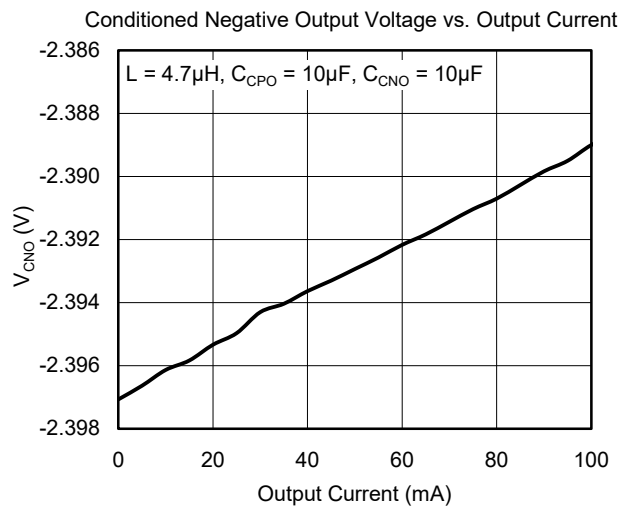
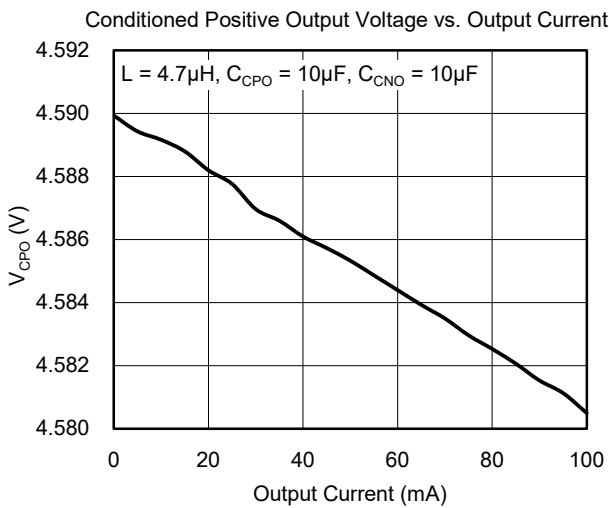
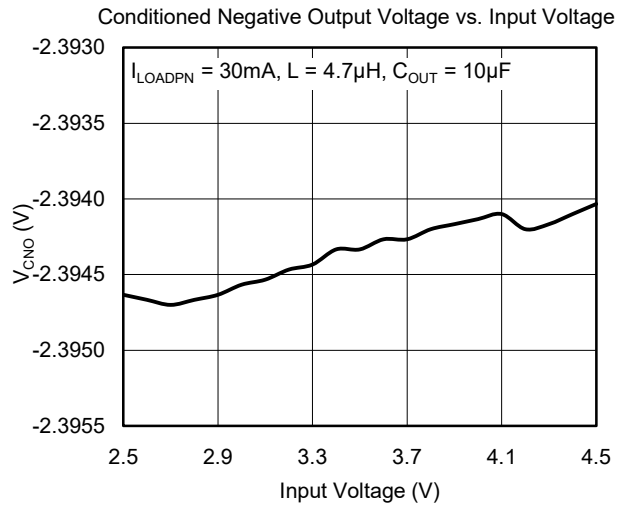
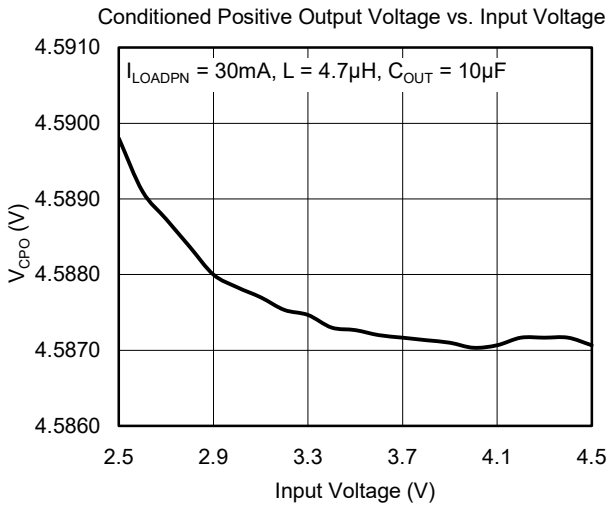
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{IN} = 3.7\text{V}$, $CVO_EN = 1\text{W} = V_{IN}$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{IN} = 3.7\text{V}$, $C_{VO_EN} = 1\text{W} = V_{IN}$, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

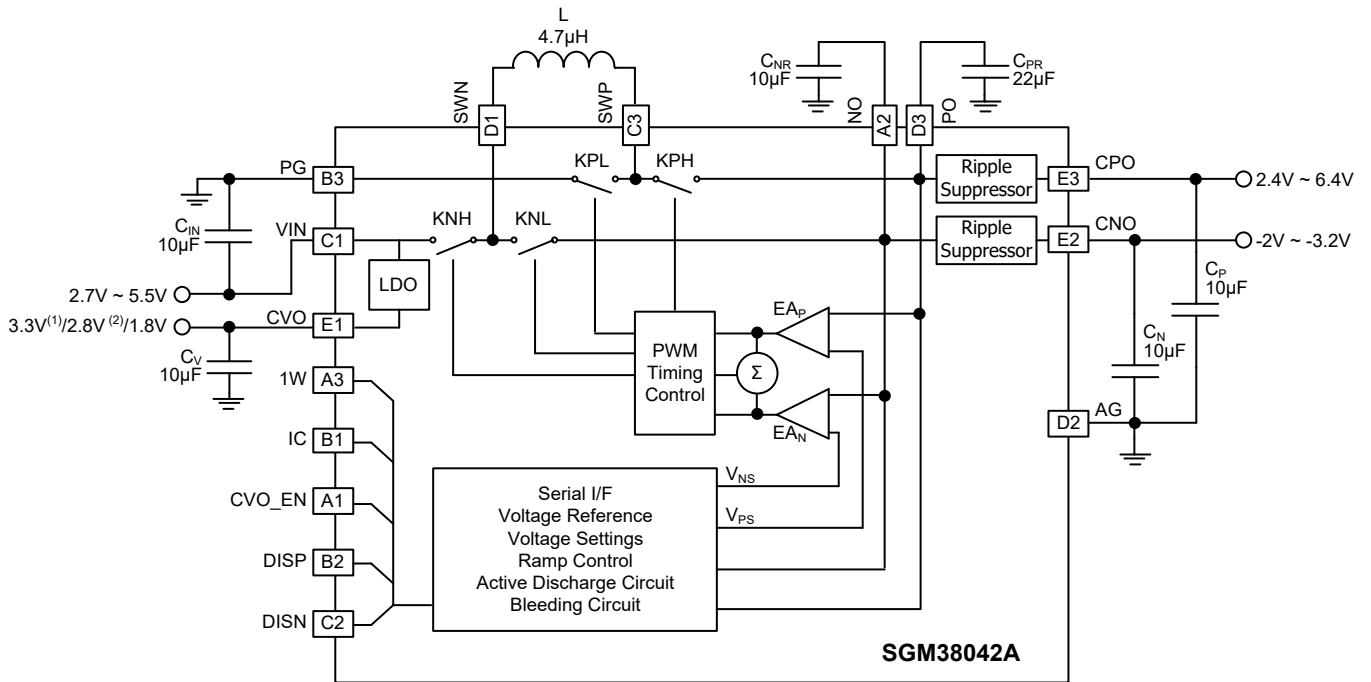


Figure 4. Functional Block Diagram

NOTE:

1. When $V_{IN} \geq 3.5V$, $V_{CVO} = 3.3V$.
2. When $V_{IN} \geq 3.0V$, $V_{CVO} = 2.8V$.

FUNCTION, OPERATION AND APPLICATION

This device is a dedicated approach for providing triple outputs for AMOLED display panels. A unique control scheme is developed for suppressing the loading cross interference between two rails, which is considered as a common drawback when using single inductor to generate two rails. The circuit maintains regulation on both rails without compromising performance in either boost-inverter operation with any loading condition or buck-inverter operation with almost any loading condition. A linear regulator capable of 50mA output current is also integrated.

Soft-Start

The SGM38042A uses an internal soft-start feature to avoid high inrush currents during step-up.

Over-Temperature Protection (OTP)

The SGM38042A includes an OTP feature to prevent excessive power dissipation from overheating the device. The OTP will shut down switching operation when junction temperature exceeds +150°C. Once the junction temperature cools down by approximately 15°C, the converter resumes operation.

Over-Current Protection (OCP)

The SGM38042A includes a current sensing circuitry which monitors the inductor current during each ON period. If the current value becomes greater than the current limit, the switch charging the inductor will turn off, forcing the inductor to discharge.

Short Circuit Protection (SCP)

The SGM38042A has an advanced short circuit protection mechanism which prevents damage to the device from unexpected applications. When the output becomes shorted to ground, the current limit will decrease to 350mA.

Under-Voltage Lockout

The SGM38042A integrates an under-voltage lockout block (UVLO) that enables the device once the voltage on VIN pin exceeds the UVLO rising threshold. No output voltage will however be generated as long as the enable signals are not pulled high. The device will be disabled as soon as the VIN voltage falls below the UVLO falling threshold.

A 40ms delay is starting as soon as the UVLO rising threshold is reached. This delay is implemented to prevent the device from being disabled or enabled by an unwanted VIN voltage spike. Once this delay has passed, the output rails can be enabled or disabled as desired with the enable signals without any delay.

Active Discharge

An active discharge of the conditioned positive output and/or the conditioned negative output can be controlled by DISP and DISN pin. If DISP and/or DISN are/is forced to be high, the discharge will occur at power-down. The discharge switch will be turned off after the 10ms discharge time.

Output Voltage

The output voltages of the converter are automatically adjusted depending on the programmed V_{CPO} and V_{CNO} voltages.

EMI and Acoustic Interference

Switching noise propagating along wire connections commonly dominates the EMI from the device operation, which may degrade receiver sensitivities by injecting interference into its carrier band or interim band through inter-modulation in its down converters. Inserting a ferrite bead into input power path and making short and straightforward path always work well in practice.

The device limits its lowest pulse skip frequency to be higher than audible frequency range for acoustic interference free operation.

Component and Parameter Selection

C_{IN} , C_V , C_{PR} , C_{NR} , C_P and C_N can be any capacitance in the range of 4.7 μ F ~ 47 μ F, and low loss Z5U, X7R and X5R dielectric capacitors are recommended for better performance. A 4.7 μ H inductor is recommended for the best efficiency.

Sequence

When 1W pin is pulled high, the conditioned positive output will start firstly. And then the conditioned negative output will start after a 5ms delay from the rising edge of 1W pin.

FUNCTION, OPERATION AND APPLICATION (continued)

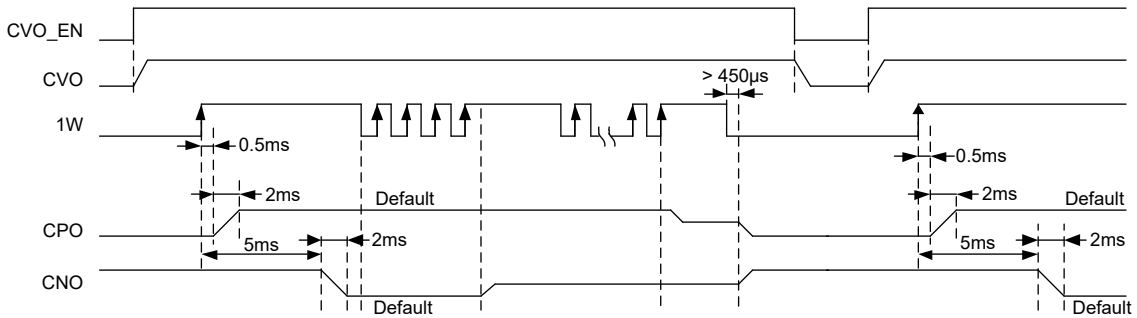


Figure 5. Startup Sequencing

PCB Layout Guidelines

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the SGM38042A the following PCB layout guidelines are recommended.

- Keep the power ground plane on the top layer (all capacitor grounds and PG pins must be connected together with one uninterrupted ground plane).
- AG and PG must be connected together on the same ground plane.
- Always avoid vias when possible. They have high inductance and resistance. If vias are necessary, always use more than one in parallel to decrease parasitics, especially for power lines.

- For high dv/dt signals (switch pin traces): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to a ground plane. Best to route signal and return on same layer.
- For high di/dt signals: keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to help prevent EMI.
- Keep input capacitor close to the IC with low inductance traces.
- Keep trace from switching node pin to inductor short if possible: it reduces EMI emissions and noise that may couple into other portions of the converter.
- Isolate analog signal paths from power paths.

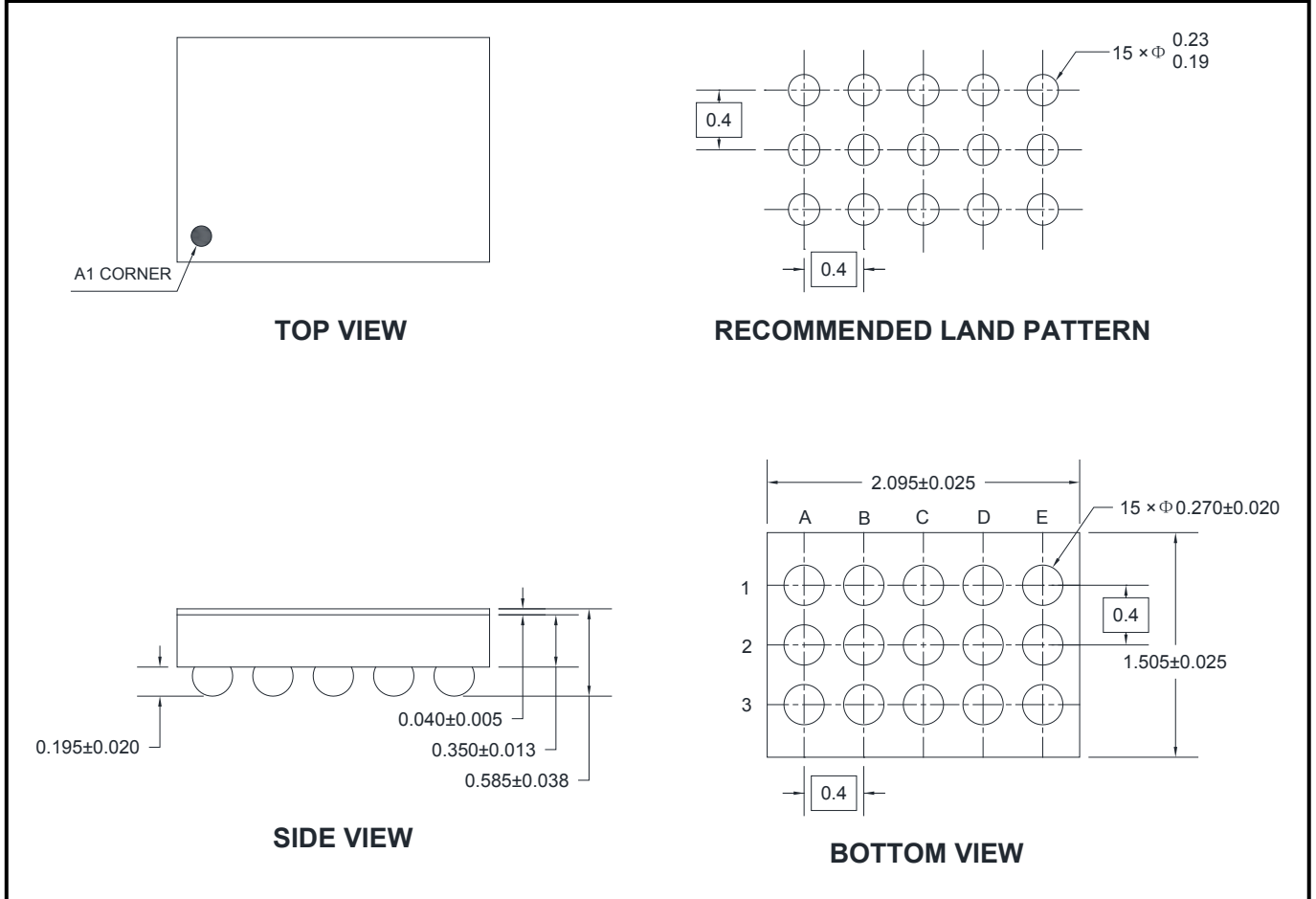
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (FEBRUARY 2021) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

WLCSP-1.51×2.10-15B



NOTE: All linear dimensions are in millimeters.

PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.51×2.10-15B	7"	9.0	1.61	2.21	0.70	4.0	4.0	2.0	8.0	Q1

000001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

DD0002