SGM51613R8
16-Bit, 500kSPS, 8-Channel Low Power, Serial Interface ADC

GENERAL DESCRIPTION

The SGM51613R8 is a 16-bit, 8-channel, successive approximation (SAR) analog-to-digital converter (ADC).

The device is powered by a single unipolar 5V.

Powered by a single-supply 5V, operate and communicate with 1.8V to 5V digital device.

The digital interface is compatible to the traditional SPI protocol.

The SGM51613R8 is available in Green TQFN-4×4-20AL and WLCSP-2.39×2.39-20B packages. It operates over an ambient temperature range of -40℃ to +125℃.

APPLICATIONS

Process Control
Power Line Monitoring
Battery-Powered Equipment
Instrumentation

FEATURES

- **16 Bits, 500kSPS SAR ADC**
- **No Missing Codes**
- **Supported Input Types:**
  - **Single-Ended**
  - **Pseudo Differential (Reference to 1/2V_{REF})**
  - **Pseudo Differential (Reference to GND)**
- **Analog Input Range:**
  0V to V_{REF} with V_{REF} up to V_{DD}
- **Supply Voltage Ranges:**
  - **Analog Supply: 4.5V to 5.5V**
  - **I/O Supply: 1.8V to 5.5V**
- **Integral Nonlinearity (INL): ±1.5LSB (TYP)**
- **Total Harmonic Distortion (THD):**
  - **-99dB (TYP) at 20kHz for TQFN Package**
  - **-98dB (TYP) at 20kHz for WLCSP Package**
- **Signal-to-Noise + Distortion (SINAD):**
  92.4dBFS (TYP) at 20kHz
- **Standby Current: 1μA (TYP)**
- **Multiple Reference Types**
  - **Internal Reference: 4.096V**
  - **External Buffered Reference: Up to V_{DD} - 0.3V**
  - **External Reference: Up to V_{DD}**
- **Support Channel Sequencer**
- **Support Selectable 1-Pole Filter and Busy Indicator**
- **Internal Temperature Sensor**
- **SPI-Compatible Serial Interface**
- **Available in Green TQFN-4×4-20AL and WLCSP-2.39×2.39-20B Packages**

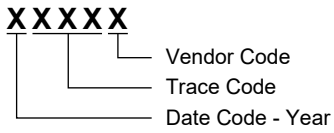
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51613R8	TQFN-4×4-20AL	-40℃ to +125℃	SGM51613R8XTUH20G/TR	51613R8 XTUH20 XXXXX	Tape and Reel, 3000
			SGM51613R8XTUH20SG/TR	51613R8 XTUH20 XXXXX	Tape and Reel, 500
	WLCSP-2.39×2.39-20B	-40℃ to +125℃	SGM51613R8XG/TR	SGM0KJ XXXXX XX#XX	Tape and Reel, 3000

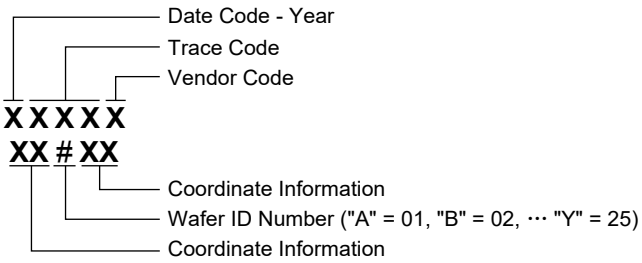
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

TQFN-4×4-20AL



WLCSP-2.39×2.39-20B



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs

INx, COM ..... GND - 0.3V to V_{DD} + 0.3V

REF, REFIN ..... GND - 0.3V to V_{DD} + 0.3V

Supply Voltages

V_{DD}, V_{IO} to GND ..... -0.3V to 6V

V_{DD} to V_{IO} ..... ±6V

DIN, CNV, SCK to GND ..... -0.3V to V_{IO} + 0.3V

SDO to GND ..... -0.3V to V_{IO} + 0.3V

Input Current to Any Pin except Supplies ..... ±10mA

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

Package Thermal Resistance

TQFN-4×4-20AL, θ_{JA} ..... 35.9℃/W

TQFN-4×4-20AL, θ_{JB} ..... 13.1℃/W

TQFN-4×4-20AL, $\theta_{JC\ (TOP)}$ ..... 26.6℃/W

TQFN-4×4-20AL, $\theta_{JC\ (BOT)}$ ..... 1.7℃/W

WLCSP-2.39×2.39-20B, θ_{JA} ..... 59.6℃/W

WLCSP-2.39×2.39-20B, θ_{JB} ..... 15.5℃/W

WLCSP-2.39×2.39-20B, θ_{JC} ..... 12.0℃/W

ESD Susceptibility (1) (2)

HBM ..... ±4000V

CDM ..... ±1000V

NOTES: 1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

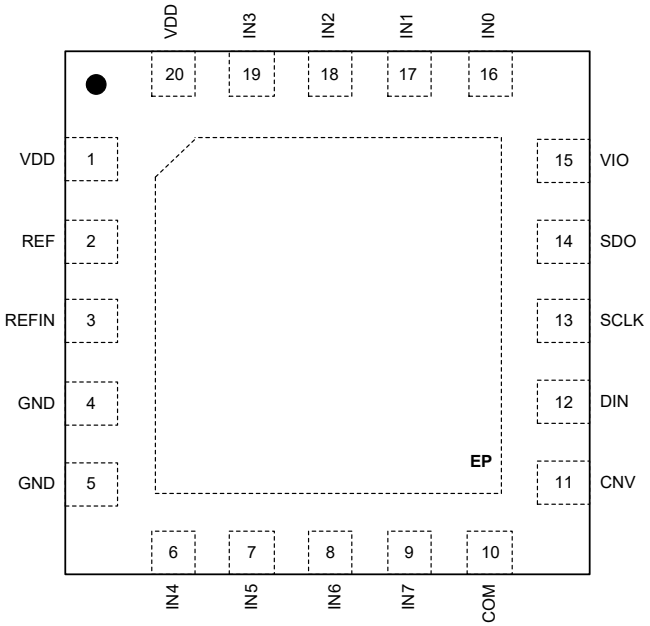
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

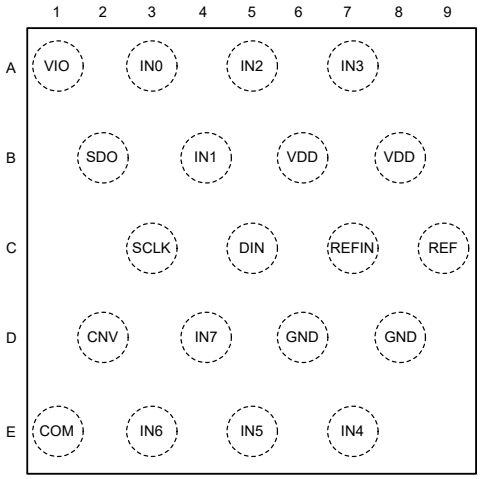
PIN CONFIGURATIONS

(TOP VIEW)



TQFN-4×4-20AL

(TOP VIEW)



WLCSP-2.39×2.39-20B

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
TQFN-4×4-20AL	WLCSP-2.39×2.39-20B			
1, 20	B6, B8	VDD	P	Power Supply Pin. The power supply of this pin must be higher than the voltage potential of reference (internal or external). 10μF and 100nF decoupling capacitors should be connected here.
2	C9	REF	AI/O	Reference Input/Output Pin. This pin needs to be decoupled by 10μF capacitors to GND and the capacitor should be installed as close to REF as possible. There are three working modes for REF pin. Firstly, when working in the internal reference mode, this pin produces 4.096V and no external reference is needed. Secondly, when the internal reference is disabled and the internal buffer is enabled, REF pin can buffer out the voltage presenting on the REFIN pin. Thirdly, a precise reference can be directly connected to REF pin for the best drift effect.
3	C7	REFIN	AI/O	Internal Reference Output/Reference Buffer Input. When the internal reference is used, there is an internal unbuffered reference voltage that requires decoupling with a 1μF capacitor. When the internal reference buffer is used, apply a source between 0.5V and V_{DD} - 0.3V that is buffered to the REF pin.
4, 5	D6, D8	GND	P	Power Supply Ground.
6, 7, 8, 9	E7, E5, E3, D4	IN4 to IN7	AI	Analog Input Pins, Input Channel 4 to Channel 7.
10	E1	COM	AI	Common Input Pin. Common voltage reference of analog input channels. All input channels can be referenced to a common mode point of 0V or V_{REF}/2V.
11	D2	CNV	DI	Conversion Input Pin. It is a digital control pin. The rising edge of CNV signal starts the conversion. During conversion, if CNV is held high long enough, the busy indicator is disabled.

PIN DESCRIPTION (continued)

PIN		NAME	TYPE	FUNCTION
TQFN-4×4-20AL	WLCSP-2.39×2.39-20B			
12	C5	DIN	DI	Data Input Pin. It is the digital pin of serial interface. The 14-bit configuration register can be written by this pin.
13	C3	SCLK	DI	Serial Data Clock Input Pin. It is the digital clock input pin of serial interface.
14	B2	SDO	DO	Serial Data Output Pin. It is the digital data output pin of serial interface. The SDO will synchronize with the above SCLK and output conversion result. When IN- is connected with GND, the conversion results are straight binary. When IN- is connected with $1/2V_{REF}$, the conversion results are two's complement.
15	A1	VIO	P	Input/Output Interface Digital Power Supply Pin. Generally, this pin is powered with the same power source of digital controller.
16, 17, 18, 19	A3, B4, A5, A7	IN0 to IN3	AI	Analog Input Pins, Input Channel 0 to Channel 3.
Exposed Pad	–	EP	–	Exposed pad should be soldered to PCB board and connected to GND.

NOTE: AI = analog input, AI/O = analog input/output, DI = digital input, DO = digital output, P = power.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, V_{DD} = 5V, V_{REF} = 4.096V to V_{DD}, V_{IO} = 3V, all typical values are measured T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution				16			Bits
Analog Input							
Voltage Range	VIN+ - VIN-	Single-ended mode, or differential with COM (INx- = GND), or differential pairs (INx- = GND)		0		$+V_{REF}$	V
		Differential with COM (INx- = $1/2V_{REF}$), or differential pairs (INx- = $1/2V_{REF}$)		$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage		Positive input, unipolar and bipolar modes		-0.1		V_{REF} + 0.1	V
		Negative or COM input, unipolar mode		-0.1		+0.1	
		Negative or COM input, bipolar mode			$V_{REF}/2$		
Analog Input CMRR		f_{IN} = 250kHz			72		dB
Leakage Current at +25℃ Input Impedance (1)		Acquisition phase			18		nA
Throughput							
Conversion Rate		Full bandwidth (2)				500	kSPS
		¼ bandwidth (2)				125	
Transient Response		Full-scale step, full bandwidth				300	ns
		Full-scale step, ¼ bandwidth				1600	
Accuracy							
No Missing Codes					16		Bits
Integral Linearity	INL	TQFN package		-6.5	±1.5	4.5	LSB (3)
		WLCSP package		-12	±1.2	12	
Differential Linearity	DNL	TQFN package		-0.999	±0.6	2.5	LSB
		WLCSP package		-0.999	±0.5	6	
Gain Error (4)	E_G	TQFN package		-14.5	±1	14.5	LSB
		WLCSP package		-18	±1	18	
Gain Error Match		TQFN package		-6	±1	6	LSB
		WLCSP package		-6	±0.5	6	
Offset Error (4)	E_O	INCC[2:0] = 00X	TQFN package	-15	±2	15	LSB
			WLCSP package	-19	±1	19	
		INCC[2:0] = 010	TQFN package	-20	±2.5	20	
			WLCSP package	-21	±0.5	21	
		INCC[2:0] = 10X	TQFN package	-16.5	±1.5	16.5	
			WLCSP package	-19	±0.5	19	
		INCC[2:0] = 110	TQFN package	-14.5	±2	14.5	
			WLCSP package	-12	±0.5	12	
		INCC[2:0] = 111	TQFN package	-13.5	±2.5	13.5	
			WLCSP package	-15.5	±1	15.5	
Offset Error Match		TQFN package		-9.5	±3	9.5	LSB
		WLCSP package		-11	±5	11	
Power Supply Sensitivity		V_{DD} = 5V ± 5%			±1.5		LSB

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, V_{DD} = 5V, V_{REF} = 4.096V to V_{DD}, V_{IO} = 3V, all typical values are measured T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC Accuracy							
Signal-to-Noise Ratio	SNR	f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 00X	TQFN package	88	93.6		dBFS (5)
			WLCSP package	86.5	92.2		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 010	TQFN package	88	93.8		
			WLCSP package	88	92.5		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 10X	TQFN package	87	93.6		
			WLCSP package	86	92.2		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 110	TQFN package	87.5	93.4		
			WLCSP package	87	92.0		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 111	TQFN package	86.5	93.5		
			WLCSP package	86	92.1		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 00X	TQFN package	86.5	92.4		
			WLCSP package	85	91.4		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 010	TQFN package	86.5	92.7		
			WLCSP package	85.5	91.6		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 10X	TQFN package	86	92.8		
			WLCSP package	85	91.8		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 110	TQFN package	86	92.6		
			WLCSP package	86	91.6		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 111	TQFN package	85.5	92.7		
			WLCSP package	85	91.7		
Signal-to-Noise + Distortion	SINAD	f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 00X	TQFN package	87.5	92.4		dBFS (5)
			WLCSP package	86	91.2		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 010	TQFN package	87.5	92.7		
			WLCSP package	87.5	91.4		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 10X	TQFN package	86.5	92.2		
			WLCSP package	85.5	91.1		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 110	TQFN package	87	91.1		
			WLCSP package	86.5	90.5		
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 111	TQFN package	86	92.5		
			WLCSP package	85.5	90.9		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 00X	TQFN package	86	91.0		
			WLCSP package	84.5	90.3		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 010	TQFN package	86	91.1		
			WLCSP package	85	90.4		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 10X	TQFN package	85.5	91.0		
			WLCSP package	84.5	90.5		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 110	TQFN package	85.5	90.0		
			WLCSP package	85.5	89.5		
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 111	TQFN package	85	91.1		
			WLCSP package	84.5	90.4		

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, V_{DD} = 5V, V_{REF} = 4.096V to V_{DD}, V_{IO} = 3V, all typical values are measured T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC Accuracy							
Total Harmonic Distortion	THD	f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 00X, bipolar differential pairs mode	TQFN package		-99	-88.5	dB
			WLCSP package		-98	-87.5	
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 010, bipolar mode	TQFN package		-99	-88.5	
			WLCSP package		-98	-87.5	
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 10X, unipolar differential pairs mode	TQFN package		-99	-90	
			WLCSP package		-98	-89	
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 110, unipolar to COM mode	TQFN package		-99	-90	
			WLCSP package		-98	-88.5	
		f_{IN} = 20kHz, V_{REF} = 5V, INCC[2:0] = 111, unipolar mode	TQFN package		-99	-89	
			WLCSP package		-98	-88.5	
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 00X, bipolar differential pairs mode	TQFN package		-99	-94	
			WLCSP package		-98	-91	
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 010, bipolar mode	TQFN package		-99	-94	
			WLCSP package		-98	-91	
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 10X, unipolar differential pairs mode	TQFN package		-99	-90	
			WLCSP package		-98	-89	
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 110, unipolar to COM mode	TQFN package		-99	-89.5	
			WLCSP package		-98	-89	
		f_{IN} = 20kHz, V_{REF} = 4.096V, INCC[2:0] = 111, unipolar mode	TQFN package		-99	-90	
			WLCSP package		-98	-89	
Spurious Free Dynamic Range	SFDR	f_{IN} = 20kHz			101		dB
Channel-to-Channel Crosstalk		f_{IN} = 100kHz on adjacent channel(s)			-112		dB
Sampling Dynamics							
-3dB Input Bandwidth		Full bandwidth			14		MHz
		¼ bandwidth			3.6		
Internal Reference							
REF Output Voltage		At -40℃ to +125℃		4.083	4.096	4.109	V
REFIN Output Voltage (6)		At +25℃			4.096		V
REF Output Current					±300		μA
Temperature Drift					±10		ppm/℃
Line Regulation		V_{DD} = 5V ± 5%			±15		ppm/V
Long Term Drift		1000 hours			100		ppm

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, V_{DD} = 5V, V_{REF} = 4.096V to V_{DD}, V_{IO} = 3V, all typical values are measured T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
External Reference							
Voltage Range		REF input		0.5	4.096	V_{DD}	V
		REFIN input (buffered)		0.5	4.096	V_{DD} - 0.3	
Temperature Sensor							
Output Voltage (7)		At +25℃			620		mV
Temperature Sensitivity		At +25℃			2		mV/℃
Digital Inputs							
Low Input Voltage	V_{IL}					0.23 × V_{IO}	V
High Input Voltage	V_{IH}			0.7 × V_{IO}			V
Low Input Current	I_{IL}			-1		1	μA
High Input Current	I_{IH}			-1		1	μA
Digital Outputs							
Data Format (8)							
Pipeline Delay (9)							
Low Output Voltage	V_{OL}	I_{SINK} = +500μA				0.4	V
High Output Voltage	V_{OH}	I_{SOURCE} = -500μA		V_{IO} - 0.3			V
Power Requirements							
Analog Supply Voltage	V_{DD}	Specified performance		4.5	5	5.5	V
Digital I/O Supply Voltage	V_{IO}	Specified performance		1.8	3	5.5	V
Standby Current (10) (11)		V_{DD} and V_{IO} = 5V, at +25℃			1		μA
Power Dissipation		V_{DD} = 5V	100kSPS throughput		13.3		mW
			500kSPS throughput		38	70	
			500kSPS throughput with internal reference		48	78	
Temperature Range							
Specified Performance		T_{MIN} to T_{MAX}		-40		125	℃

NOTES:

1. Refer to the Input Structure section for more details.

2. The bandwidth depends on the configuration register settings.

3. LSB = Least Significant Bit. 1LSB = 76.3μV in the 5V input range.

4. These include the full temperature range variation, but exclude the error contribution from the reference.

5. All those parameters are tested with an input signal at -0.5dB for full-scale, unless otherwise specified. The specifications expressed in dBFS are tested with a -0.5dB signal and are recalculated to a full-scale input signal.

6. It is the output from the internal band gap.

7. The output voltage is internal and present on a dedicated multiplexer input.

8. For output data format, please refer to Transfer Functions section.

9. After the conversion is completed, the conversion results are provided immediately.

10. All digital inputs are forced to VIO or GND as required.

11. In the acquisition phase.

TIMING CHARACTERISTICS

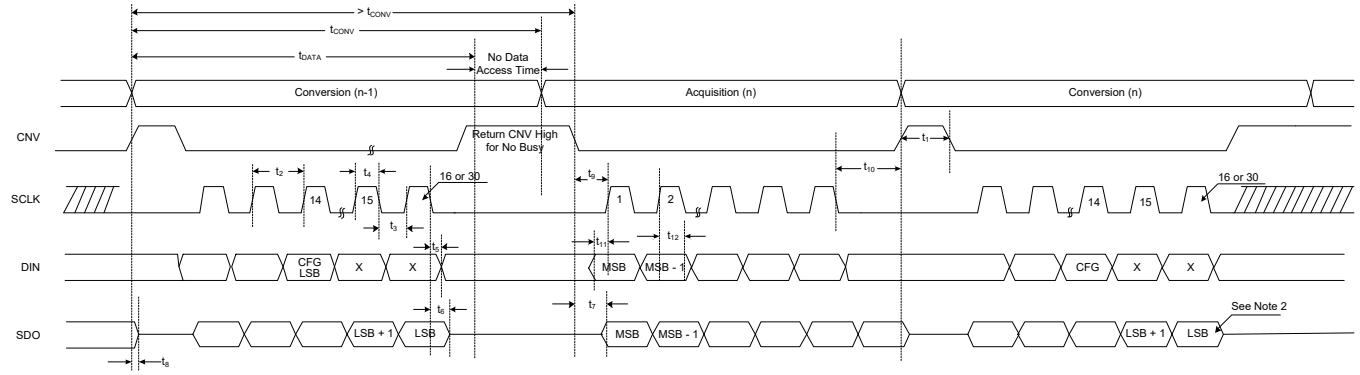
(V_{DD} = 4.5V to 5.5V, V_{REF} = 4.096V to V_{DD}, V_{IO} = 1.8V to V_{DD}, T_A = -40℃ to +125℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}				1.6	μs
Acquisition Time	t_{ACQ}		400			ns
Time between Conversions	t_{CYC}		2			μs
CNV Pulse Width	t_1		10			ns
Data Write/Read during Conversion	t_{DATA}				1.2	μs
SCK Period (2)	t_2		t_6 + 4			ns
SCK Low Time	t_3		11			ns
SCK High Time	t_4		11			ns
SCK Falling Edge to Data Remains Valid	t_5		4			ns
SCK Falling Edge to Data Valid Delay	t_6	V_{IO} = 5V			16	ns
		V_{IO} = 3.3V			17	
		V_{IO} = 1.8V			28	
CNV Low to SDO D15 MSB Valid	t_7	V_{IO} = 5V			15	ns
		V_{IO} = 3.3V			17	
		V_{IO} = 1.8V			25	
CNV High or Last SCK Falling Edge to SDO High Impedance	t_8				32	ns
CNV Low to SCK Rising Edge	t_9		10			ns
Last SCK Falling Edge to CNV Rising Edge Delay	t_{10}		40			ns
DIN Valid Setup Time from SCK Rising Edge	t_{11}		5			ns
DIN Valid Hold Time from SCK Rising Edge	t_{12}		5			ns

NOTES:

1. See Figure 1 and Figure 2.
2. t_2 must be greater than t_3 + t_4.

TIMING DIAGRAMS



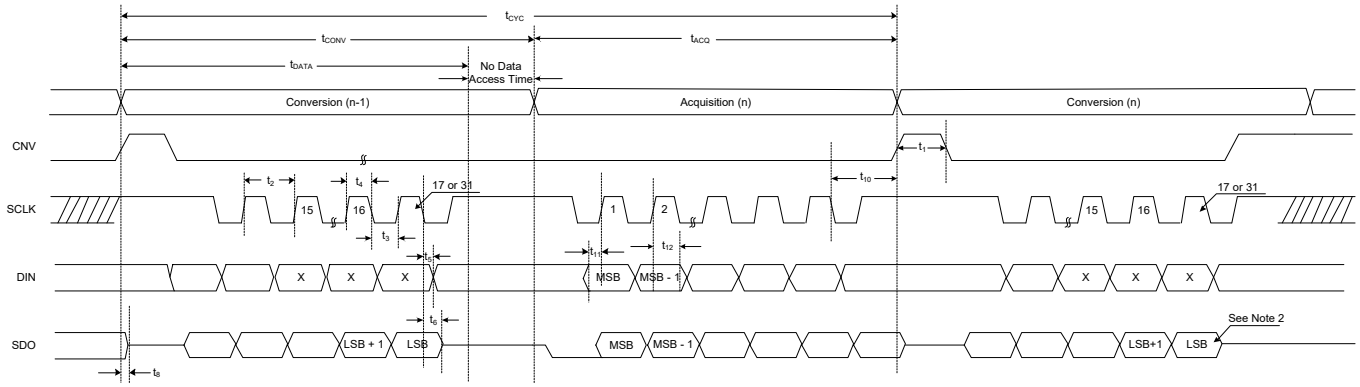
NOTES:

1. No data access time is a time error between t_{CONV} and t_{DATA}.

2. If CFG readback is disabled, 16 SCLKs are needed for the conversion code reading. If CFG readback is enabled, 30 SCLKs are needed for both conversion code and configuration register reading.

3. The CPOL (clock polarity) bit controls the steady state value of the clock when no data is being transferred.

Figure 1. Serial Interface Timing without a Busy Indicator (CPOL = 0)



NOTES:

1. No data access time is a time error between t_{CONV} and t_{DATA}.

2. If CFG readback is disabled, 17 SCLKs are needed for the conversion code reading. If CFG readback is enabled, 31 SCLKs are needed for both conversion code and configuration register reading.

3. The CPOL (clock polarity) bit controls the steady state value of the clock when no data is being transferred.

4. In busy mode, if the busy signal is a needed instruction for reading, then the quantity of SCLK must be sufficient. For example, if CFG[0] = 0, 31 SCLKs must be sent out. If CFG[0] = 1, 17 SCLKs must be sent out. Otherwise, busy signal cannot be released.

Figure 2. Serial Interface Timing with a Busy Indicator (CPOL = 1)

TIMING DIAGRAMS (continued)

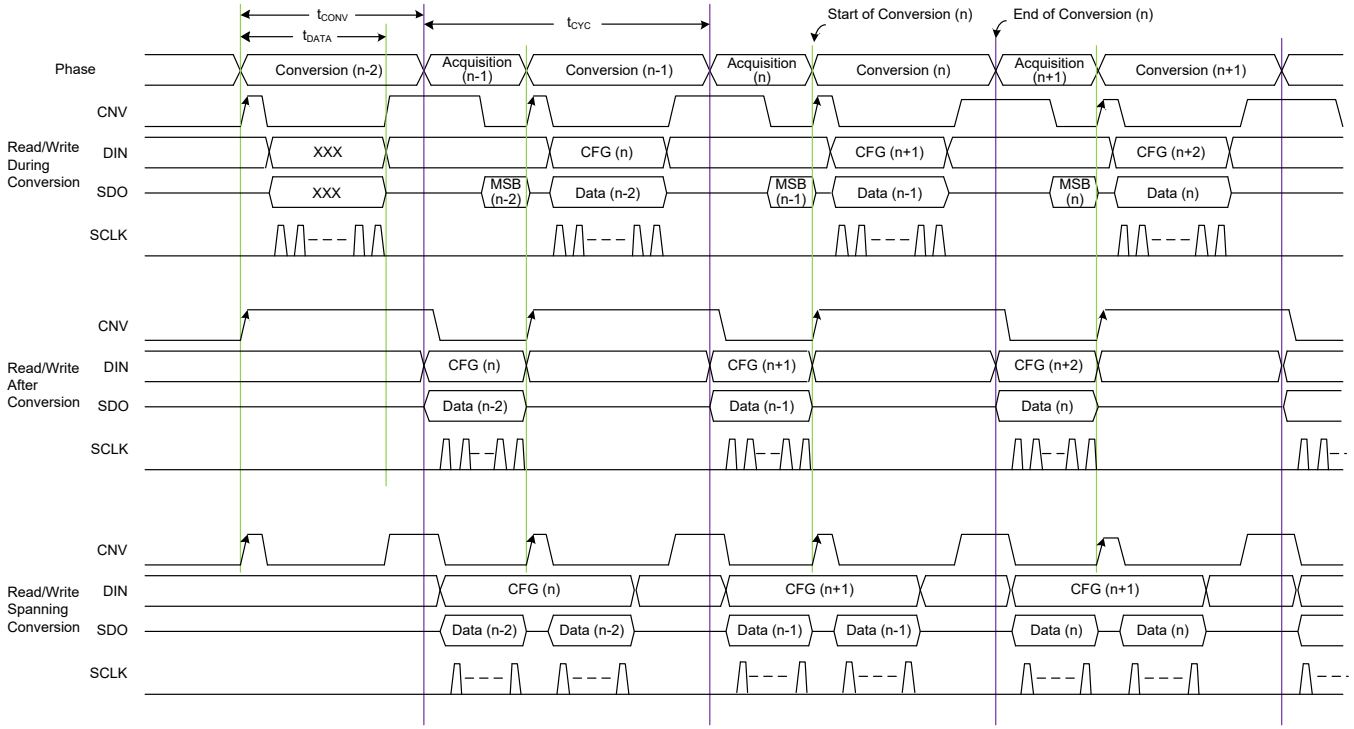


Figure 3. Reading and Writing Sequence without a Busy Indicator (CPOL = 0)

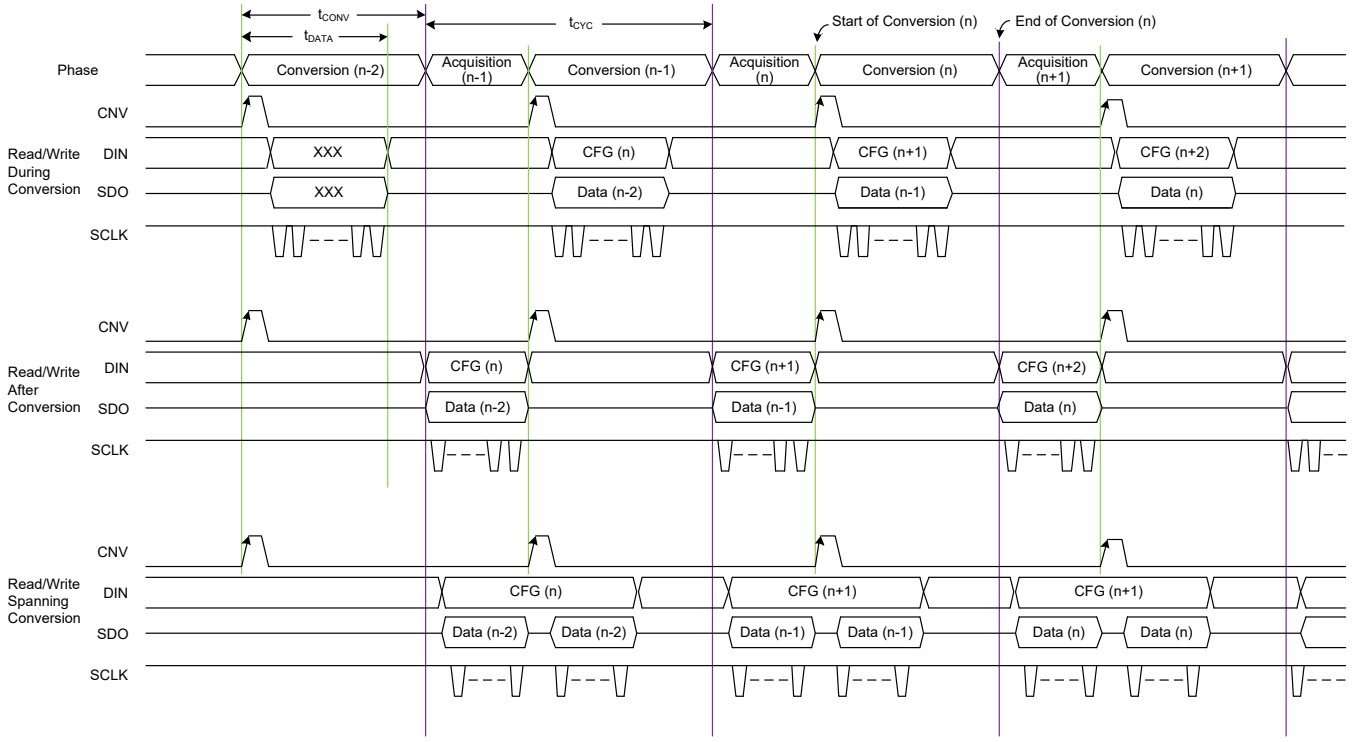
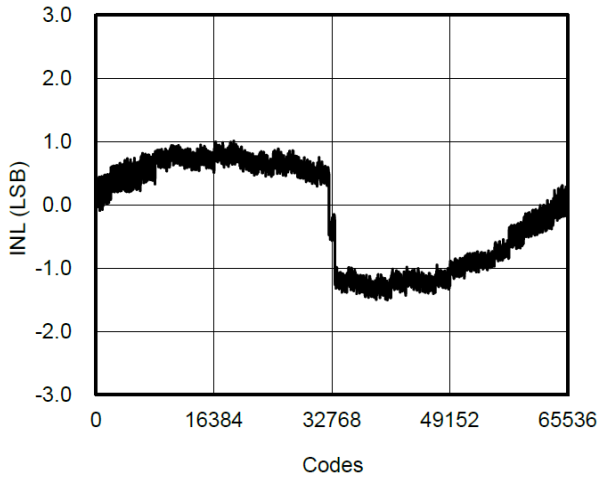


Figure 4. Reading and Writing Sequence with a Busy Indicator (CPOL = 1)

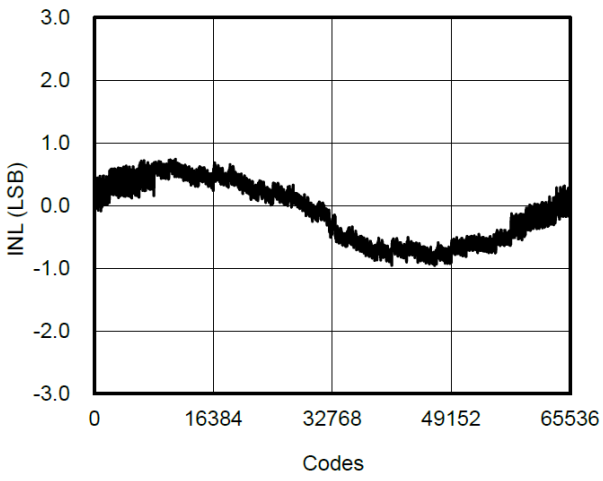
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 5V, V_{IO} = V_{DD}, unless otherwise noted.

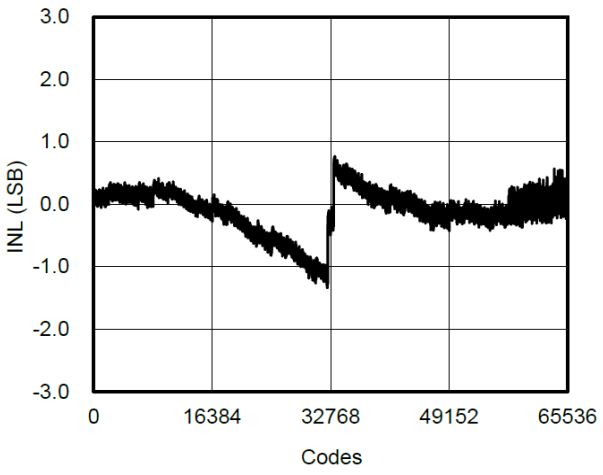
Integral Nonlinearity vs. Code (Bipolar-To-COM)



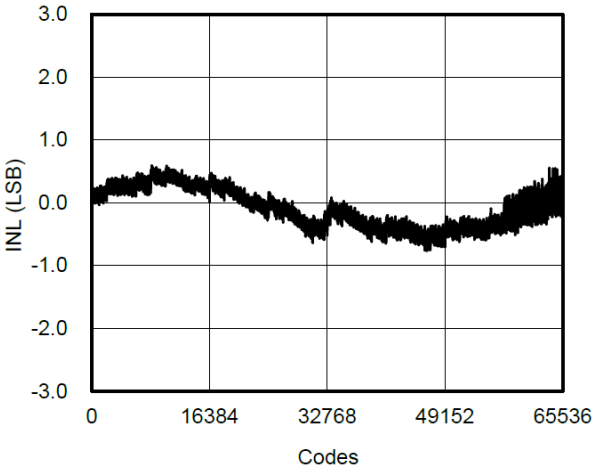
Integral Nonlinearity vs. Code (Bipolar-To-Differential Pairs)



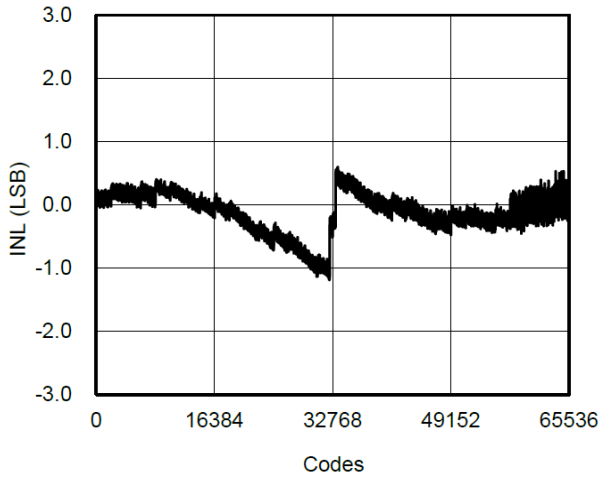
Integral Nonlinearity vs. Code (Unipolar-To-COM)



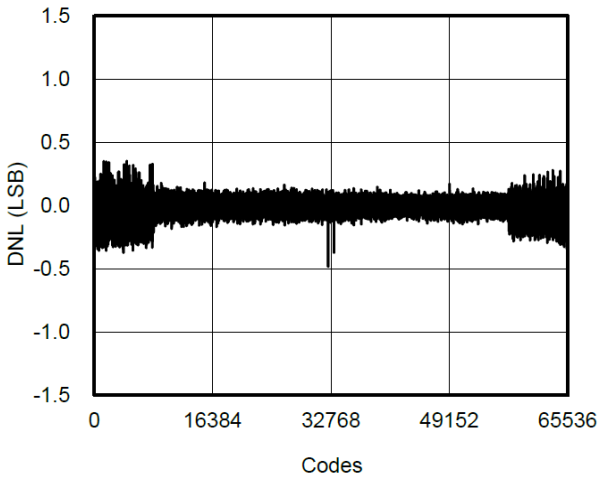
Integral Nonlinearity vs. Code (Unipolar-To-Differential Pairs)



Integral Nonlinearity vs. Code (Signal-To-Ended)



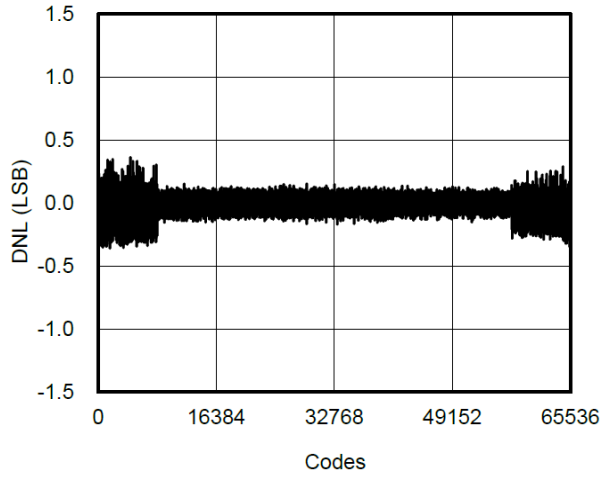
Differential Nonlinearity vs. Code (Bipolar-To-COM)



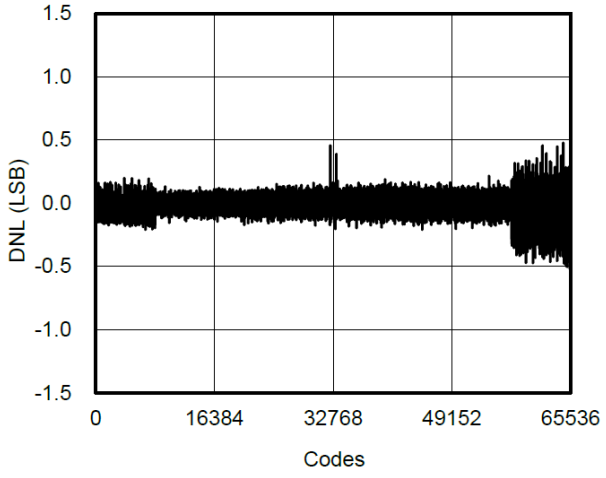
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 5V, V_{REF} = 5V, V_{IO} = V_{DD}, unless otherwise noted.

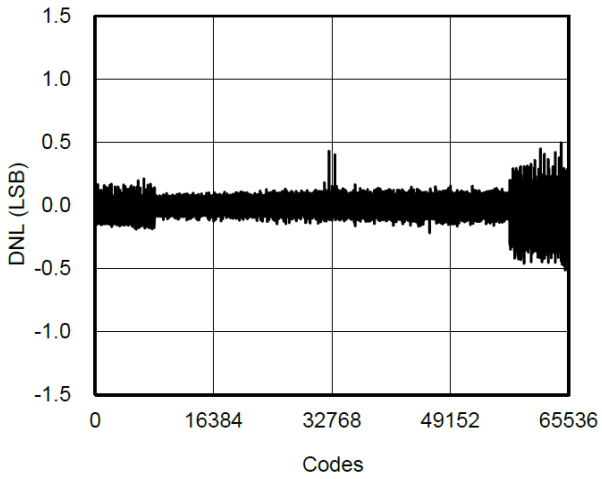
Differential Nonlinearity vs. Code (Bipolar-To-Differential Pairs)



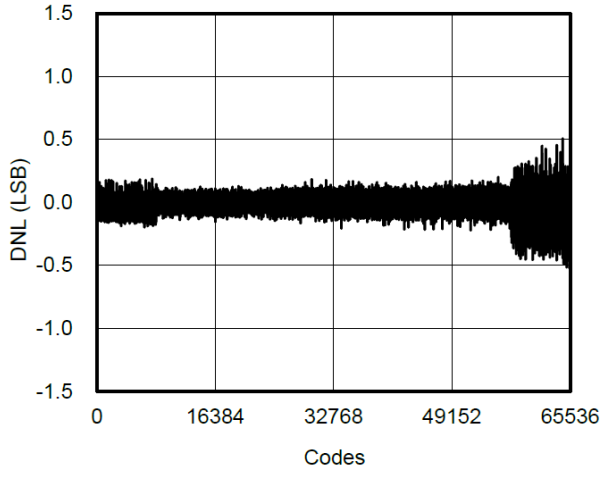
Differential Nonlinearity vs. Code (Unipolar-To-COM)



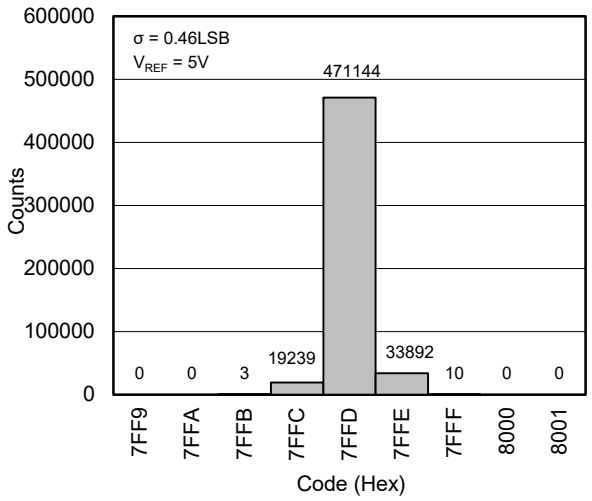
Differential Nonlinearity vs. Code (Signal-To-Ended)



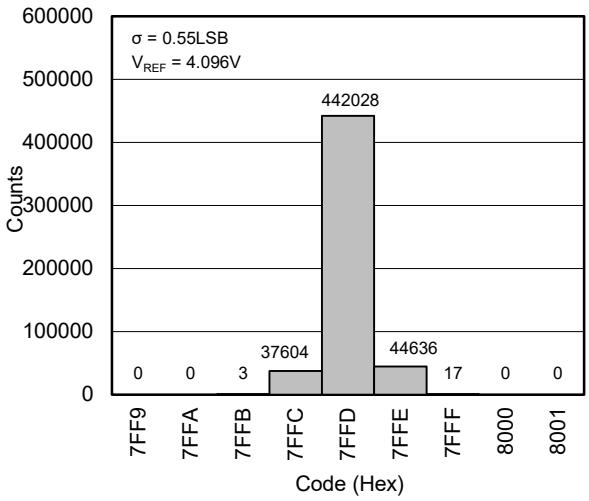
Differential Nonlinearity vs. Code (Unipolar-To-Differential Pairs)



Histogram of a DC Input at Code Center



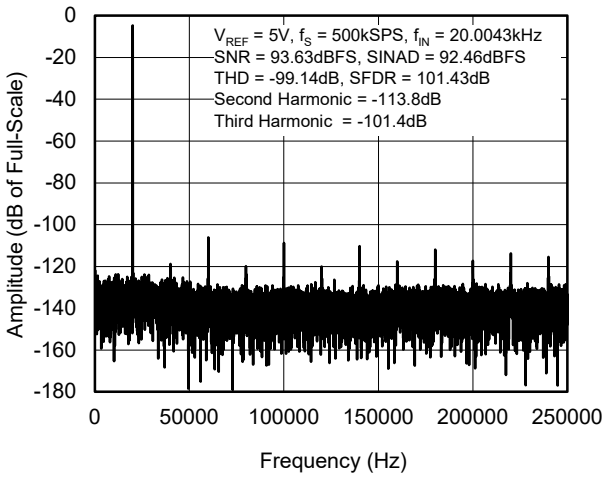
Histogram of a DC Input at Code Center



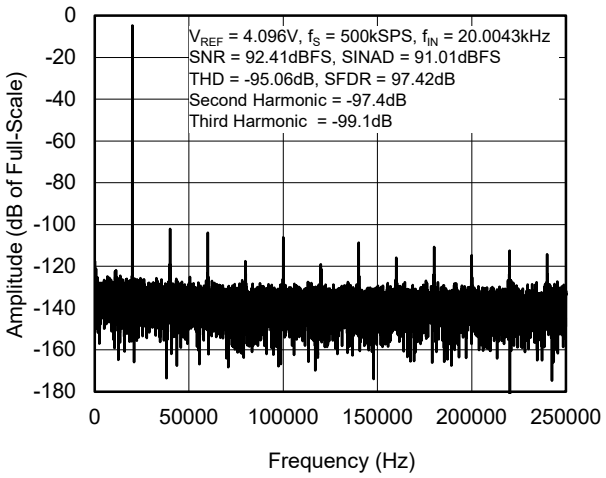
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 5V, V_{REF} = 5V, V_{IO} = V_{DD}, unless otherwise noted.

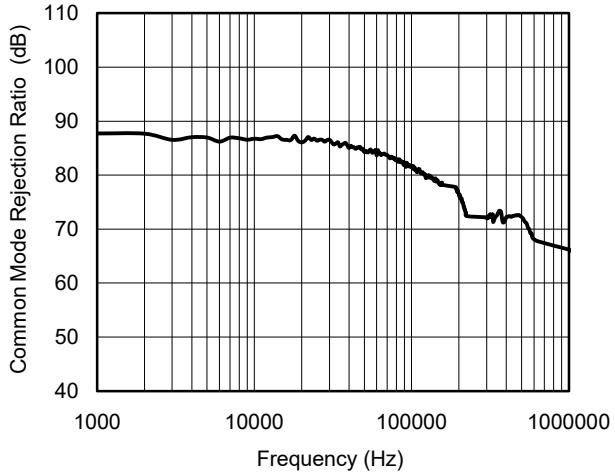
20kHz FFT



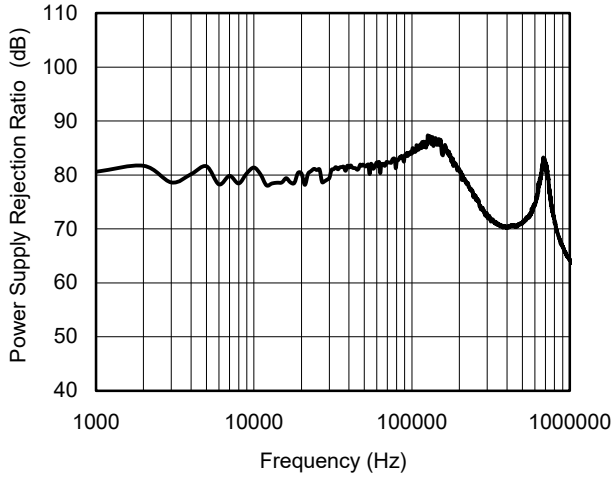
20kHz FFT



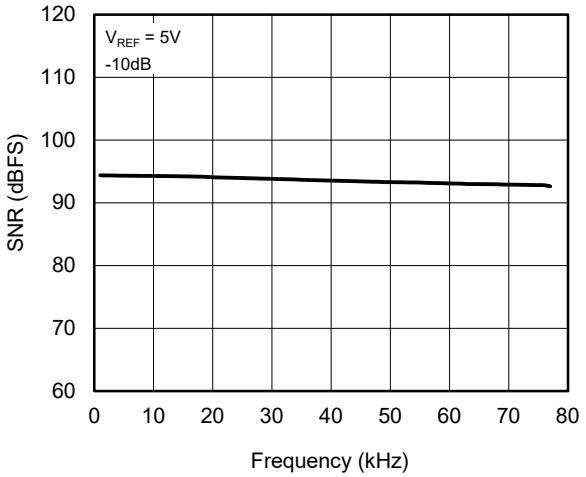
Analog Input CMRR vs. Frequency



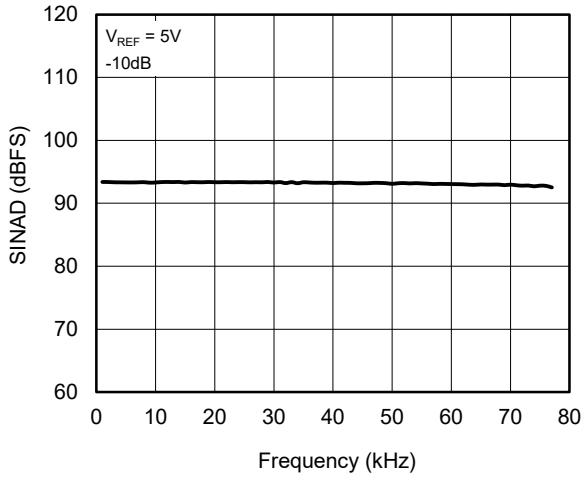
PSRR vs. Frequency



SNR vs. Frequency



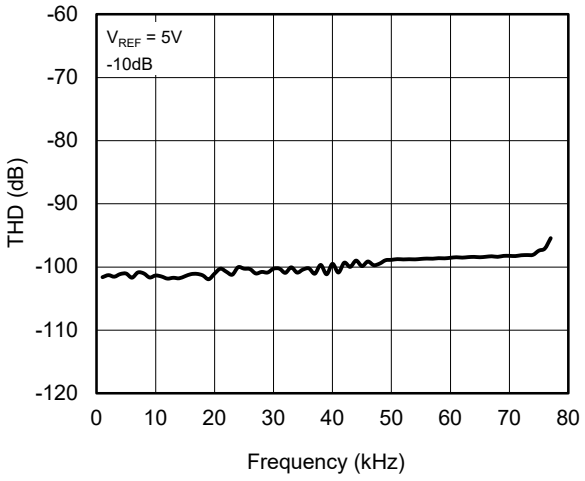
SINAD vs. Frequency



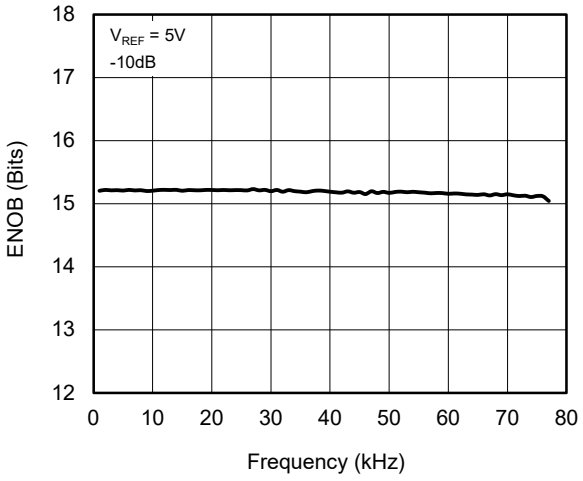
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 5V, V_{REF} = 5V, V_{IO} = V_{DD}, unless otherwise noted.

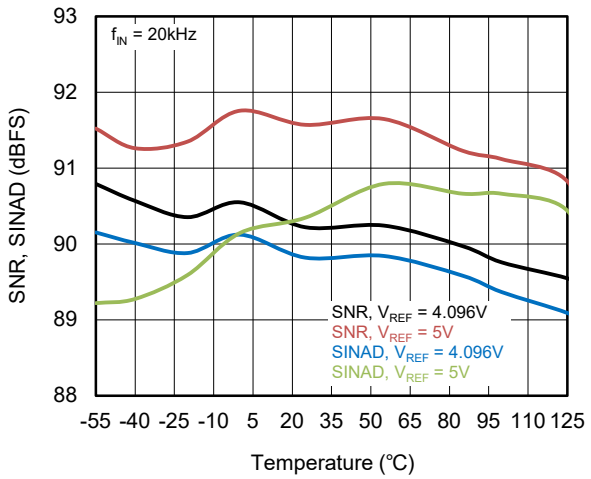
THD vs. Frequency



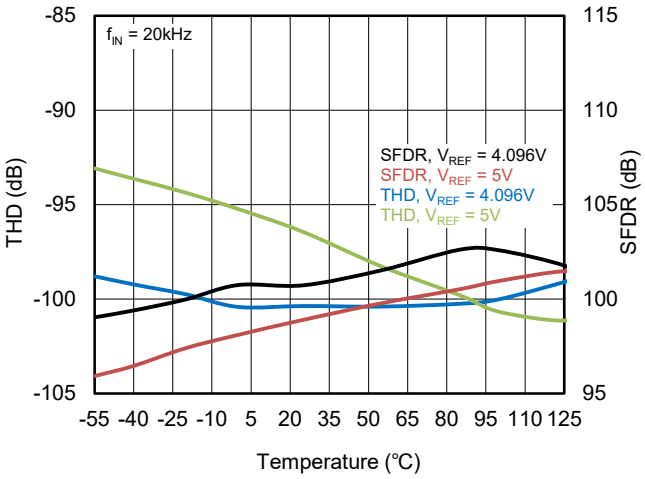
ENOB vs. Frequency



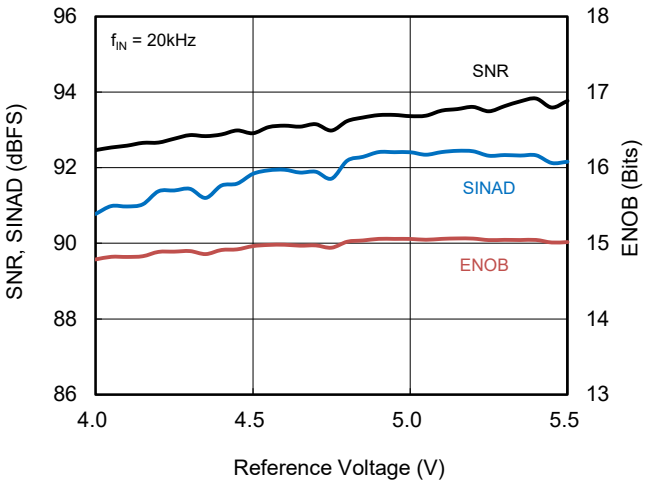
SNR, SINAD vs. Temperature



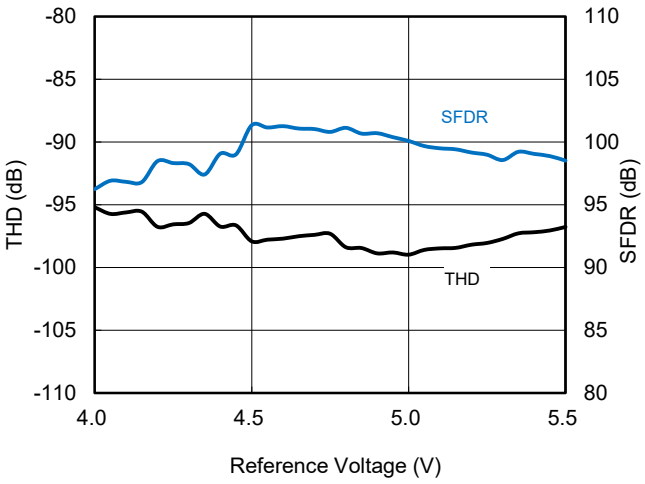
THD, SFDR vs. Temperature



SNR, SINAD, ENOB vs. Reference Voltage



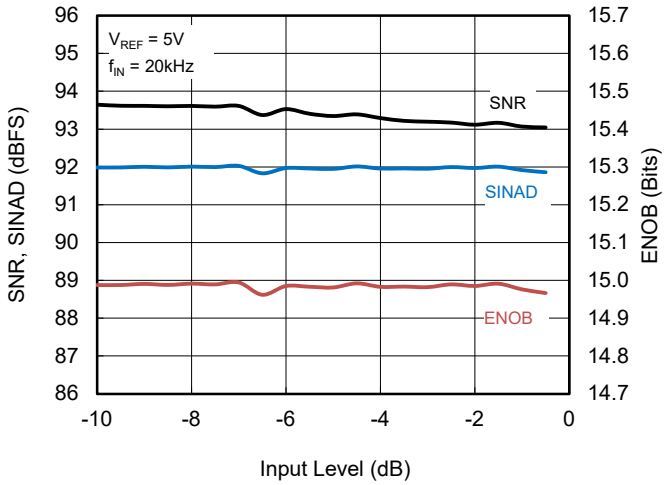
THD, SFDR vs. Reference Voltage



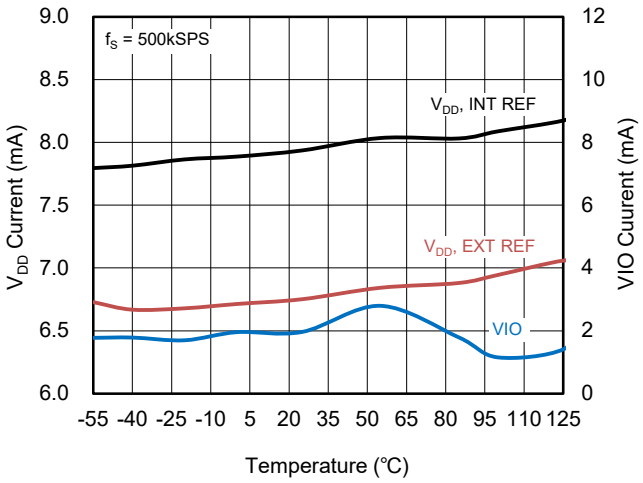
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 5V, V_{REF} = 5V, V_{IO} = V_{DD}, unless otherwise noted.

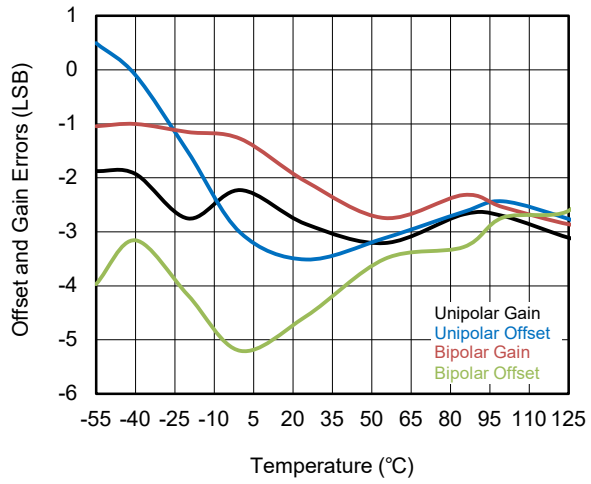
SNR, SINAD, and ENOB vs. Input Level



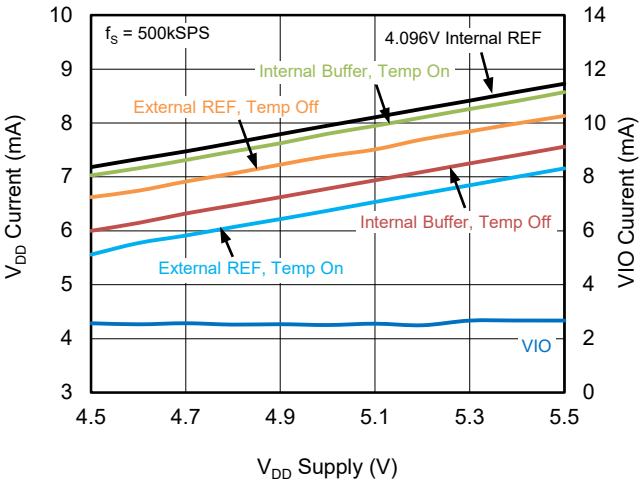
Operating Current vs. Temperature



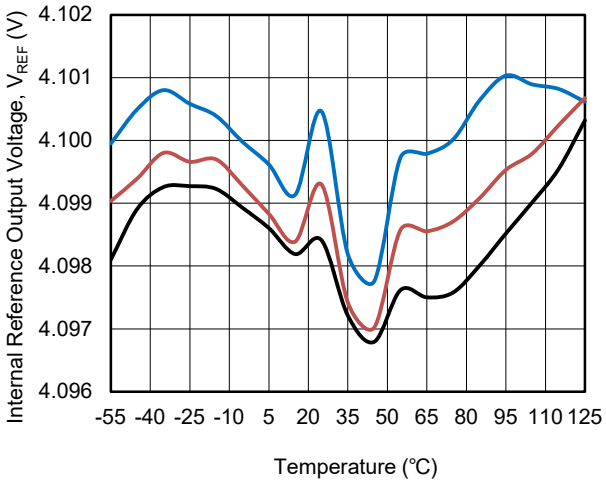
Offset and Gain Errors vs. Temperature, Not Normalized



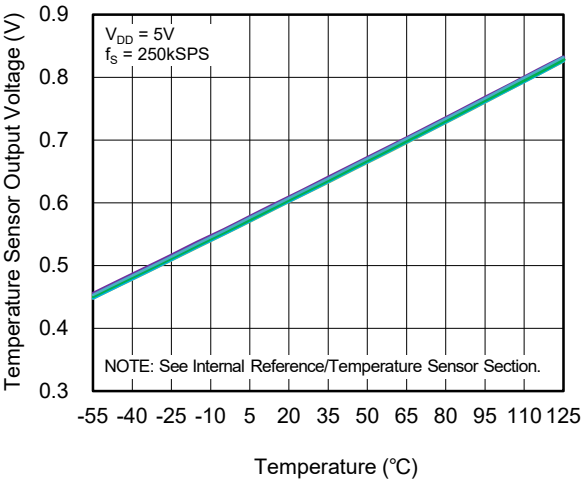
Operating Current vs. Supply



Internal Reference Output Voltage vs. Temperature, Three Devices



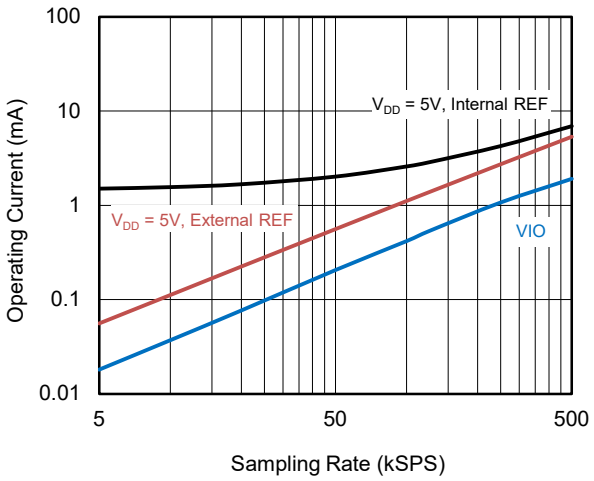
Temperature Sensor Output Voltage vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 5V, V_{REF} = 5V, V_{IO} = V_{DD}, unless otherwise noted.

Operating Current vs. Sampling Rate



FUNCTIONAL BLOCK DIAGRAM

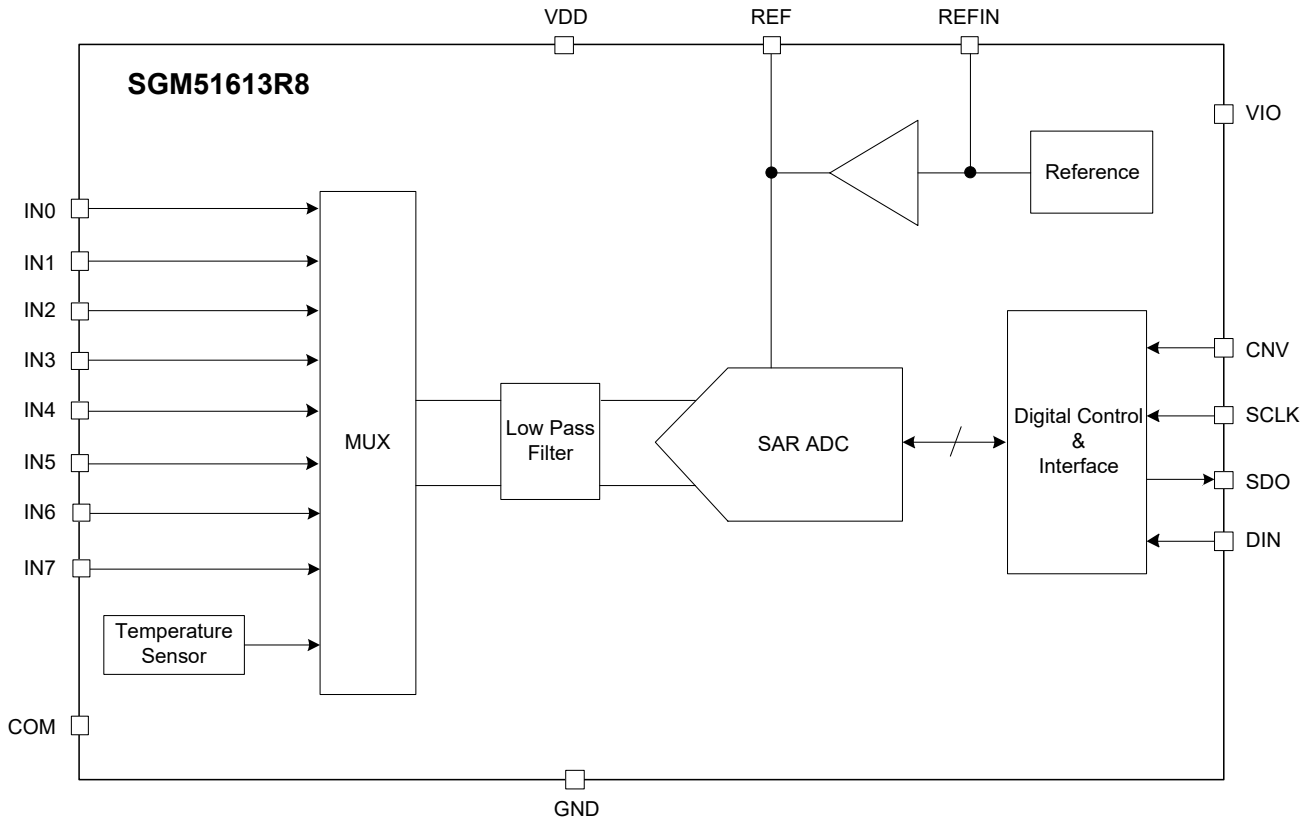


Figure 5. Block Diagram

DETAILED DESCRIPTION

The SGM51613R8 is an 8-channel 16-bit successive approximation ADC, which is based on the switched capacitor array architecture.

The SGM51613R8 has an on-chip internal oscillator which is used to the clock source of internal conversion. The SCLK is not required for the conversion process.

Transfer Functions

The SGM51613R8 supports 5 kinds of input modes, which include single-ended, pseudo differential to COM (referenced to GND or $1/2V_{REF}$) and pseudo differential pairs (referenced to GND or $1/2V_{REF}$). For the first mode, the inputs are configured as single-ended, all eight channels are referenced to GND, and the data output is a straight binary. For the second and third modes, the inputs are configured as pseudo differential to a common reference (COM). If the COM is connected to GND, then the data output is a straight binary, and if the COM is connected to $V_{REF}/2$, then the data output is two's complement. For the fourth and fifth modes, the inputs are configured as pseudo differential pairs of two adjacent channels. If the INx- is connected to GND, then the data output is a straight binary, if the INx- is connected to $V_{REF}/2$, then the data output is two's complement.

Figure 6 shows the ideal transfer characteristic.

Input Configurations

The SGM51613R8 can be configured as single-ended input or pseudo differential input. In both modes, the positive pin input range is 0V to V_{REF}, and the negative input pin must be GND or $V_{REF}/2$. The selectable configurations are shown in the following 4 conditions:

Configuration A: CFG[12:10] = 111, all 8 channels are single-ended input and referenced to GND pin. In this case, each input channel VIN+ is channel0+ to channel7+, each input channel VIN- is GND.

Configuration B: CFG[12:10] = 010, all 8 channels are pseudo differential to COM pin, and COM pin is connected to $V_{REF}/2$. CFG[12:10] = 110, all 8 channels are pseudo differential to COM pin, and COM pin is connected to GND. In this case, each input channel channelx+ is INx+, and the COM pin is INx-.

Configuration C: CFG[12:10] = 00x, two adjacent channels of all inputs are combined as differential pairs, and the channelx- is referenced to $V_{REF}/2$. CFG[12:10] = 10X, two adjacent channels of all inputs are combined as differential pairs, and the channelx- is referenced to GND. In this case, which channel of these adjacent pairs is channelx+ or channelx- is defined by CFG[9:7]. For example, if CFG[9:7] = 000, the positive pin (channel0+) is IN0, and the negative pin (channel0-) is IN1, vice versa.

Configuration D: The chip supports dynamic combined configuration.

More details of input configuration please refer to Figure 7.

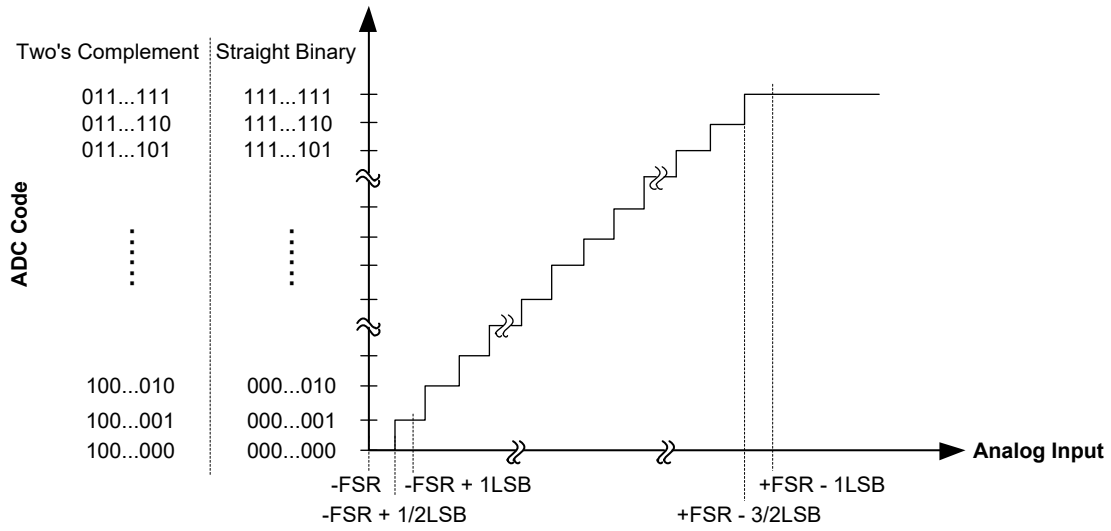


Figure 6. ADC Ideal Transfer Function

DETAILED DESCRIPTION (continued)

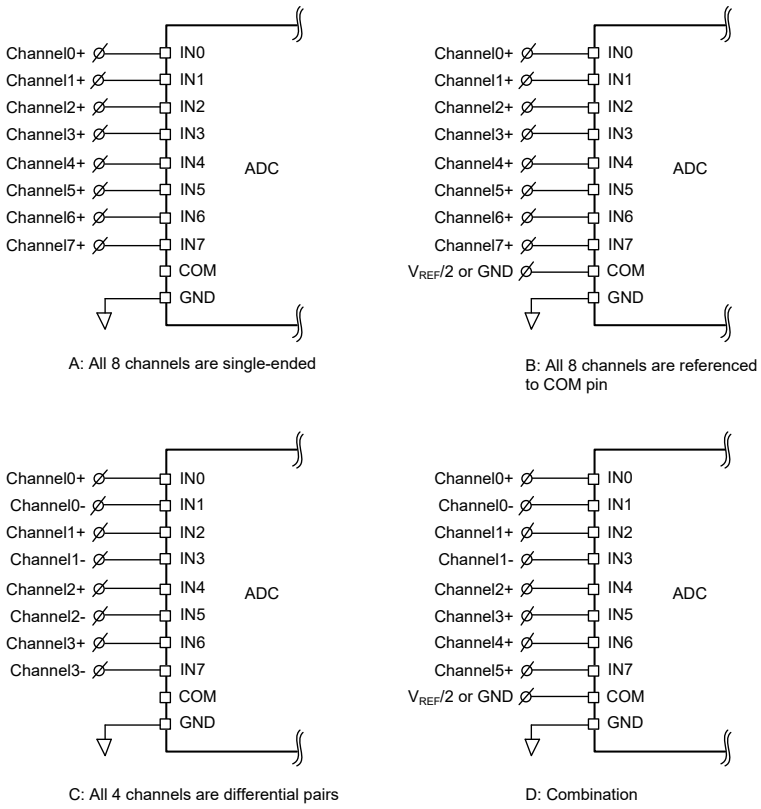


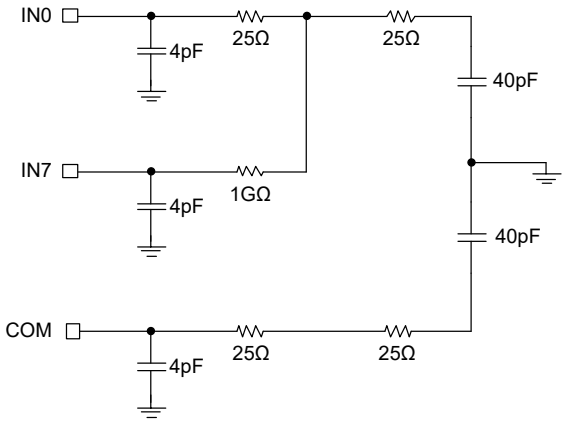
Figure 7. Multiplexed Analog Input Configurations

Input Structure

The input signal applied to INx and COM must be limited in the range that is listed in Electrical Characteristics table.

The SGM51613R8 is a capacitor array SAR ADC. During the sampling period, there is an input current flowing into the ADC. The peak input current depends on sampling rate, reference voltage, input voltage and signal source impedance.

A driver amplifier is usually suggested to buffer the signal source. It makes the analog input source to charge the equivalent input capacitor (44pF) to a 16-bit accuracy level in the acquisition time. When the input capacitor is fully charged, no further current flows. An equivalent input circuit is shown in Figure 8.



NOTE: IN0 is assumed to be on, and IN7 is assumed to be off.

Figure 8. Equivalent Analog Input Circuit

DETAILED DESCRIPTION (continued)

Sequencer

The SGM51613R8 supports automatic channel scanning. The channel configuration can be single-ended or pseudo differential paired. And the temperature sensor also can be configured into the scan sequence, if it is selected, the temperature sensor will be read after the last ADC channel.

In the single-ended mode, the scan sequence starts at IN0 and ends at the channel which is configured by CFG[9:7].

In the differential paired mode, the scan sequence starts at channel0+ (IN0) and channel0- (IN1), and ends at the paired channel set by CFG[9:7]. In the auto scan mode, the positive input is always the even INx and the negative input is always the odd INx, regardless of the setting of CFG[9:7].

The auto scan sequence is initiated by setting the CFG[2:1]. Once the configuration of CFG[13:0] is uploaded to ADC, the DIN must be hold low at least 13 SCLK clocks before the next CFG[13:0] is written to ADC, during these clocks, the ADC data can be read normally.

During the scan sequence, the CFG[13:0] can be updated. Once the CFG[11] or CFG[9:7] is changed, the scan sequence will be restarted from IN0 (or paired with IN1 in pseudo differential mode).

Driver Amplifier Choice

To get the best performance, an input buffer amplifier is recommended. Refer to Figure 9 to Figure 12.

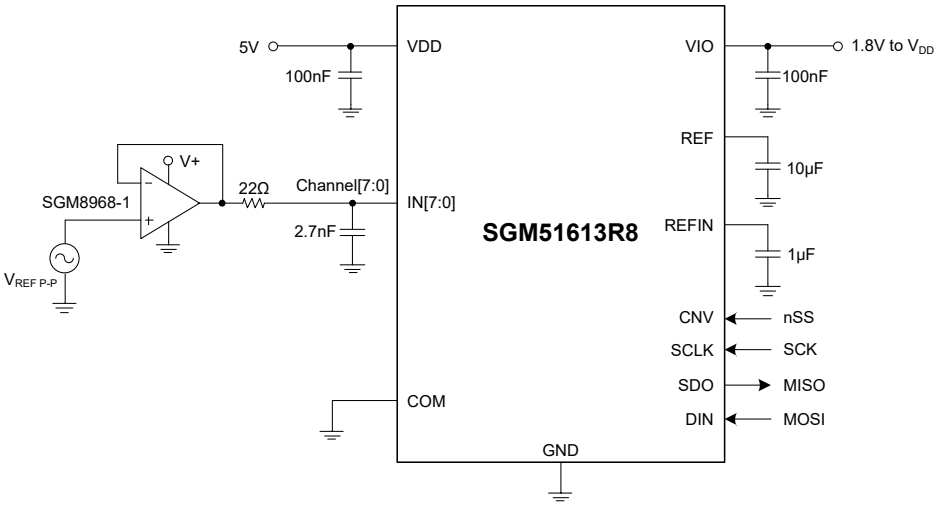


Figure 9. Typical Application with Single-Ended Input or Differential Input to a Common Reference (to GND)

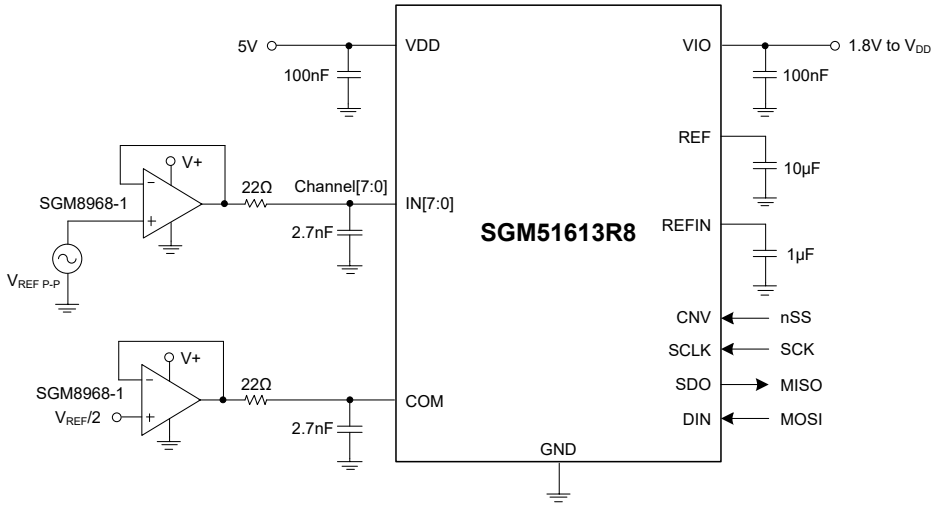


Figure 10. Typical Application with Differential Input to a Common Reference (to 1/2V_{REF})

DETAILED DESCRIPTION (continued)

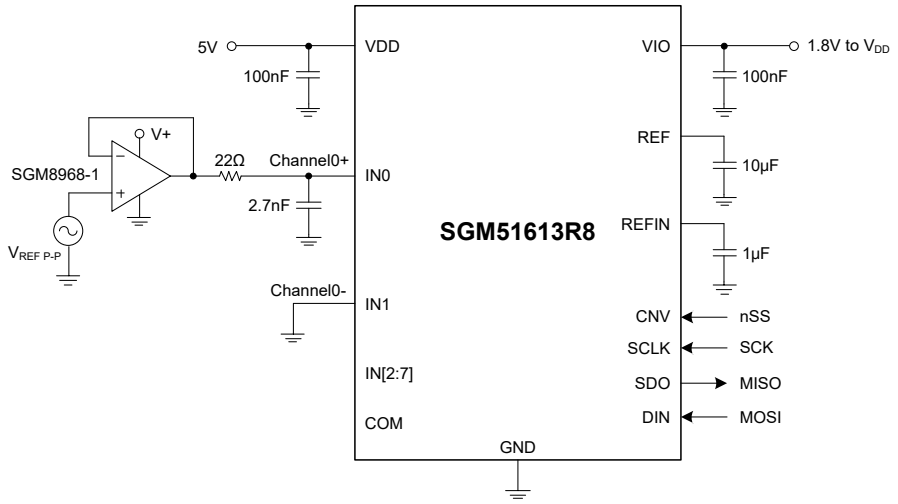


Figure 11. Typical Application with Differential Pairs Input (Reference to GND)

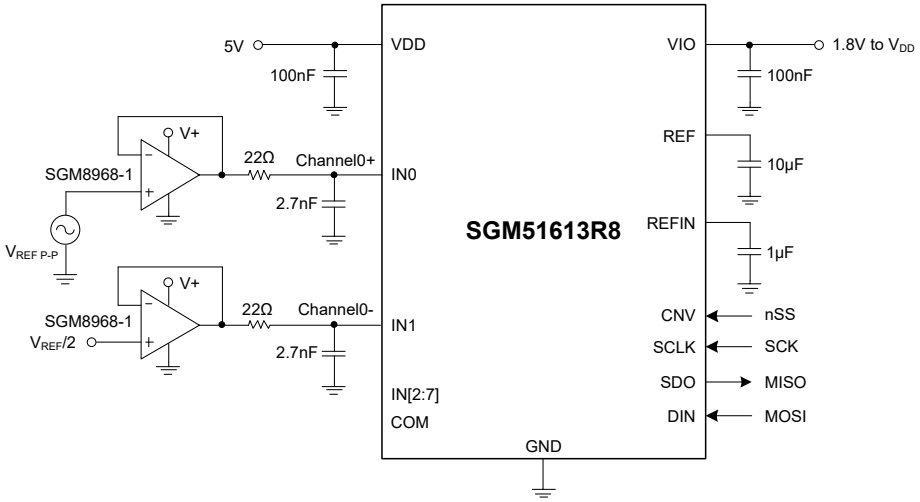


Figure 12. Typical Application with Differential Pairs Input (Reference to 1/2V_{REF})

Voltage Reference

The SGM51613R8 has an on-chip low drift reference. The chip can work with internal reference or external reference. More details are described in Table 1.

If the internal reference is enabled, the voltage is output on the REFIN pin which needs a decoupling capacitor. If the voltage is used for the other circuit, a buffer amplifier is recommended.

If an external reference is used for the better system performance, it can be connected to REFIN pin or REF pin. When it is connected to VREFIN pin, the internal reference buffer must be enabled at the same time. When it is connected to REF pin, an external buffer is optional.

Temperature Sensor

To enable the internal temperature sensor, the internal reference must be active and the internal buffer enabling is not necessary at the same time.

The temperature sensor is a single-ended input to ADC and referenced to GND. Its output is straight binary.

The output code of the temperature sensor can be described as follows:

Temperature Sensor Code = Temperature Sensor Voltage × (Reference Voltage)/(2^{16} - 1)

In which, the voltage of the temperature sensor output is typically 620mV at +25℃. The sensitivity of temperature senor is about 2mV/℃.

DETAILED DESCRIPTION (continued)

Table 1. Configuration Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT
D[13]	CFG	Configuration Update 0 = Keep current configuration settings 1 = Overwrite contents of register	The Meaning of Read Back Value 0 = The last operation is reading CFG 1 = The last operation is writing CFG
D[12:10]	INCC[2:0]	Input Channel Configuration 00X (1) = Bipolar differential pairs, INx- referenced to $V_{REF}/2 \pm 0.1V$ 010 = Bipolar, INx referenced to COM = $V_{REF}/2 \pm 0.1V$ 011 = Temperature sensor 10X (1) = Unipolar differential pairs, INx- referenced to GND ± 0.1V 110 = Unipolar, IN0 to IN7 referenced to COM = GND ± 0.1V (GND sense) 111 = Unipolar, IN0 to IN7 referenced to GND	Selection of pseudo bipolar, pseudo differential, pairs, single-ended, or temperature sensor. Refer to the Input Configurations section.
D[9:7]	INx[2:0]	Input Channel Selection in Binary Fashion 000 = IN0 001 = IN1 010 = IN2 011 = IN3 100 = IN4 101 = IN5 110 = IN6 111 = IN7	
D[6]	BW	Select Bandwidth for Low-Pass Filter 0 = ¼ of BW, uses an additional series resistor to further bandwidth limit the noise. Maximum throughput must also be reduced to ¼ 1 = Full BW	
D[5:3]	REF[2:0] (2)	Reference/Buffer Selection 000 = Do not use 001 = Internal reference and temperature sensor enabled. REF = 4.096V buffered output 010 = Use external reference. Temperature sensor enabled. Internal buffer disabled 011 = Use external reference. Internal buffer and temperature sensor enabled 100 = Do not use 101 = Do not use 110 = Use external reference. Internal reference, internal buffer and temperature sensor disabled 111 = Use external reference. Internal buffer enabled. Internal reference and temperature sensor disabled	Selection of internal, external, and external buffered references, and enabling of the on-chip temperature sensor.
D[2:1]	SEQ[1:0]	Channel Sequencer 00 = Disable sequencer 01 = Update configuration during sequence 10 = Scan IN0 to IN[7:0] (set in CFG[9:7]), then temperature 11 = Scan IN0 to IN[7:0] (set in CFG[9:7])	Allow scanning channels in an IN0 to IN[7:0] fashion. Refer to the Sequencer section.
D[0]	RB	Read Back the CFG Register 0 = Read back current configuration at end of data 1 = Do not read back contents of configuration	

NOTES:

1. X = Don't care.

2. When internal bandgap reference is enabled, the temperature sensor is always enabled.

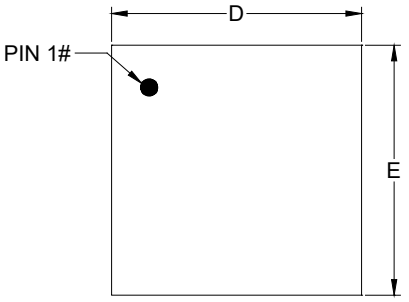
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

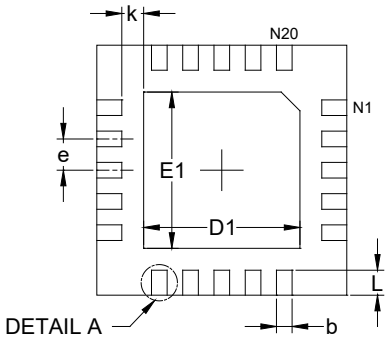
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

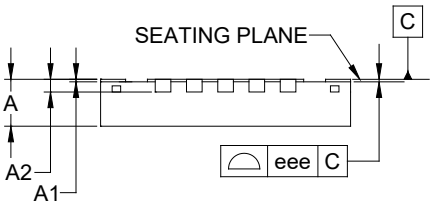
TQFN-4×4-20AL



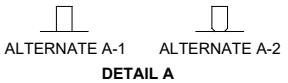
TOP VIEW



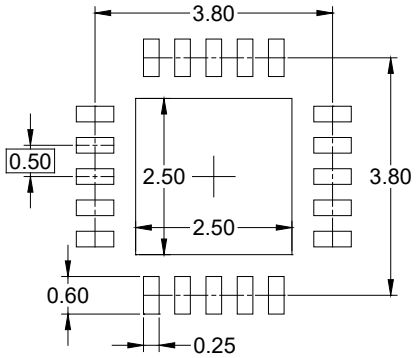
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



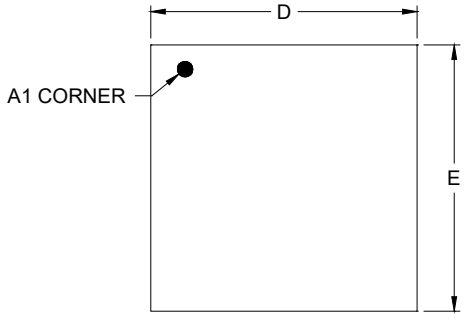
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.400	-	2.600
E1	2.400	-	2.600
e	0.500 BSC		
k	0.350 REF		
L	0.300	-	0.500
eee	0.080		

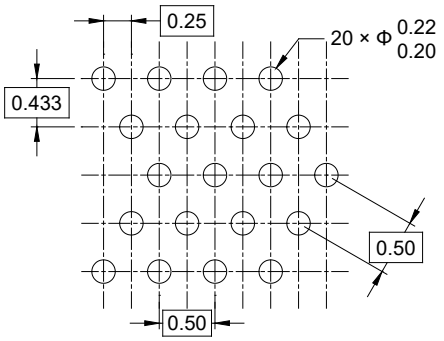
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

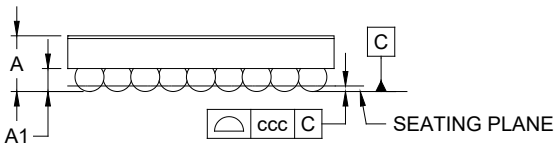
WLCSP-2.39×2.39-20B



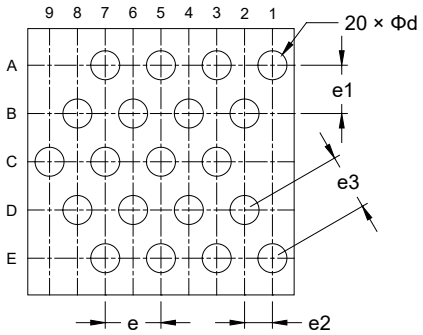
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



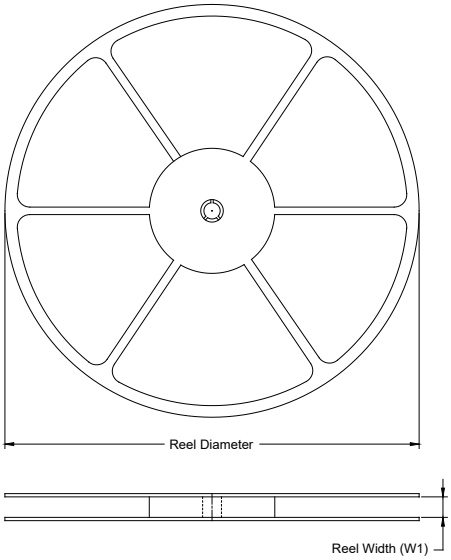
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.538
A1	0.186	-	0.226
D	2.360	-	2.420
E	2.360	-	2.420
d	0.230	-	0.290
e	0.500 BSC		
e1	0.433 BSC		
e2	0.250 BSC		
e3	0.500 BSC		
ccc	0.050		

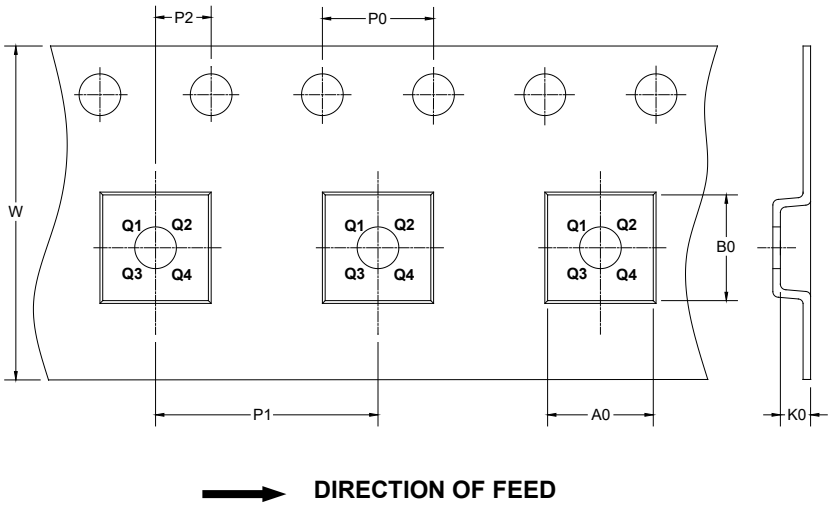
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



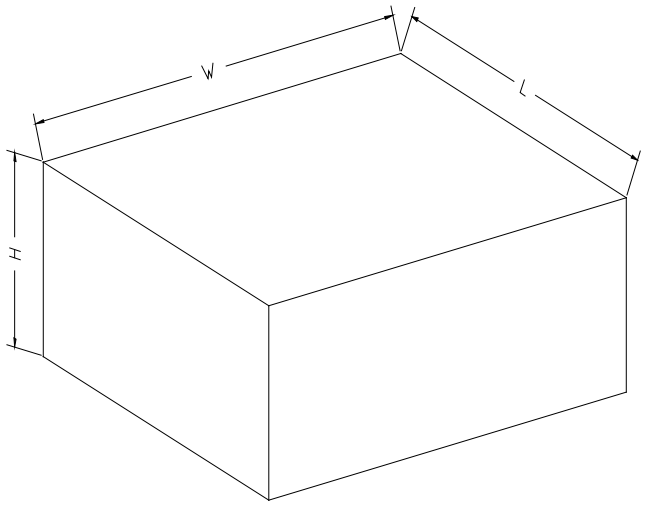
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-20AL	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2
WLCSP-2.39×2.39-20B	7″	9.5	2.52	2.52	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002