SGM71622R8/SGM71622R8A/SGM71622R8B 8-Channel, 16-Bit, SPI, Voltage-Output DAC with Internal Reference

GENERAL DESCRIPTION

The SGM71622R8 family is a 16-bit, low power, 8 channels, buffered voltage-output digital-to-analog converter (DAC).

The SGM71622R8 family has an on-chip 2.5V, 5ppm/℃ internal reference. And it provides the programmable full-scale output voltage ranges of 1.25V (GAIN = ½), 2.5V (GAIN = 1) or 5V (GAIN = 2) with high linearity up to ±0.5LSB (TYP) INL.

The SGM71622R8 family has a flexible serial operation interface which is SPI-compatible. Its operation clock is up to 50MHz.

The SGM71622R8 family contains power-on reset management circuits to make sure that there is a default output voltage. There are two version chips with power-on reset to 0V or mid-scale.

The power consumption is 0.5mA/channel at 5.5V, which is suitable for battery-operated equipment. In power-down mode, it consumes 0.5μA/channel.

The SGM71622R8 family is available in Green TQFN-3.5×3.5-16AL, TQFN-3×3-16DL and WLCSP-2.45×2.45-16B packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Power Supply Range: 2.7V to 5.5V**
- **Integral Nonlinearity (INL):**
  - **SGM71622R8: ±0.5LSB (TYP)**
  - **SGM71622R8A: ±1LSB (TYP)**
  - **SGM71622R8B: ±12LSB (TYP)**
- **Total Unadjusted Error (TUE): ±0.05% of FSR (TYP)**
- **Integrated 2.5V Precision Internal Reference**
  - **Initial Accuracy: ±5mV (MAX)**
  - **Low Drift: 5ppm/℃ (TYP)**
- **Power-On Reset to Zero-Scale or Mid-Scale**
  - **SGM71622R8Z/SGM71622R8ZC/SGM71622R8AZ/ SGM71622R8AZC/SGM71622R8BZ: Power-On Reset to Zero**
  - **SGM71622R8M/SGM71622R8MC/SGM71622R8AM/ SGM71622R8AMC/SGM71622R8BM: Power-On Reset to Mid-Scale**
- **User Selectable GAIN: 2, 1 or ½**
- **Support Clear Output Function**
- **SPI-Compatible Serial Interface: Up to 50MHz**
- **IO Supply Voltage Range: 1.7V to 5.5V**
- **Support Daisy-Chain Operation**
- **Support CRC Error Check**
- **Low Power Consumption: 0.5mA/Channel at 5.5V**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in Green TQFN-3.5×3.5-16AL, TQFN-3×3-16DL and WLCSP-2.45×2.45-16B Packages**

APPLICATIONS

Optical Module
Programmable Logic Controller
Industrial Automation
Lab Instruments

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM71622R8Z	TQFN-3.5×3.5-16AL	-40℃ to +125℃	SGM71622R8ZXTUD16G/TR	SGM08A XTUD16 XXXXX	Tape and Reel, 4000
			SGM71622R8ZXTUD16SG/TR	SGM08A XTUD16 XXXXX	Tape and Reel, 250
	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8ZXTUC16G/TR	0IBUC XXXXX	Tape and Reel, 4000
			SGM71622R8ZXTUC16SG/TR	0IBUC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8ZXG/TR	SGM 088 XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8ZXSG/TR	SGM 088 XXXXX XX#XX	Tape and Reel, 250
SGM71622R8ZC	TQFN-3.5×3.5-16AL	-40℃ to +125℃	SGM71622R8ZCXTUD16G/TR	SGM0PK XTUD16 XXXXX	Tape and Reel, 4000
			SGM71622R8ZCXTUD16SG/TR	SGM0PK XTUD16 XXXXX	Tape and Reel, 250
	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8ZCXTUC16G/TR	0PEUC XXXXX	Tape and Reel, 4000
			SGM71622R8ZCXTUC16SG/TR	0PEUC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8ZCXG/TR	SGM 0PH XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8ZCXSG/TR	SGM 0PH XXXXX XX#XX	Tape and Reel, 250
SGM71622R8M	TQFN-3.5×3.5-16AL	-40℃ to +125℃	SGM71622R8MXTUD16G/TR	SGM0PL XTUD16 XXXXX	Tape and Reel, 4000
			SGM71622R8MXTUD16SG/TR	SGM0PL XTUD16 XXXXX	Tape and Reel, 250
	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8MXTUC16G/TR	0PFUC XXXXX	Tape and Reel, 4000
			SGM71622R8MXTUC16SG/TR	0PFUC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8MXG/TR	SGM 0PI XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8MXSG/TR	SGM 0PI XXXXX XX#XX	Tape and Reel, 250

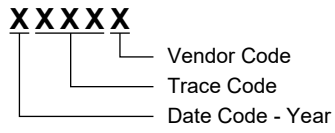
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM71622R8MC	TQFN-3.5×3.5-16AL	-40℃ to +125℃	SGM71622R8MCXTUD16G/TR	SGM0PM XTUD16 XXXXX	Tape and Reel, 4000
			SGM71622R8MCXTUD16SG/TR	SGM0PM XTUD16 XXXXX	Tape and Reel, 250
	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8MCXTUC16G/TR	0PGUC XXXXX	Tape and Reel, 4000
			SGM71622R8MCXTUC16SG/TR	0PGUC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8MCXG/TR	SGM 0PJ XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8MCXSG/TR	SGM 0PJ XXXXX XX#XX	Tape and Reel, 250
SGM71622R8AZ	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8AZXTUC16G/TR	1G2UC XXXXX	Tape and Reel, 4000
			SGM71622R8AZXTUC16SG/TR	1G2UC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8AZXG/TR	SGM 1G8 XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8AZXSG/TR	SGM 1G8 XXXXX XX#XX	Tape and Reel, 250
SGM71622R8AZC	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8AZCXTUC16G/TR	1G3UC XXXXX	Tape and Reel, 4000
			SGM71622R8AZCXTUC16SG/TR	1G3UC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8AZCXG/TR	SGM 1G9 XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8AZCXSG/TR	SGM 1G9 XXXXX XX#XX	Tape and Reel, 250
SGM71622R8AM	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8AMXTUC16G/TR	1G4UC XXXXX	Tape and Reel, 4000
			SGM71622R8AMXTUC16SG/TR	1G4UC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8AMXG/TR	SGM 1GA XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8AMXSG/TR	SGM 1GA XXXXX XX#XX	Tape and Reel, 250

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM71622R8AMC	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8AMCXTUC16G/TR	1G5UC XXXXX	Tape and Reel, 4000
			SGM71622R8AMCXTUC16SG/TR	1G5UC XXXXX	Tape and Reel, 250
	WLCSP-2.45×2.45-16B	-40℃ to +125℃	SGM71622R8AMCXG/TR	SGM 1GB XXXXX XX#XX	Tape and Reel, 5000
			SGM71622R8AMCXSG/TR	SGM 1GB XXXXX XX#XX	Tape and Reel, 250
SGM71622R8BZ	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8BZXTUC16G/TR	1G6UC XXXXX	Tape and Reel, 4000
			SGM71622R8BZXTUC16SG/TR	1G6UC XXXXX	Tape and Reel, 250
SGM71622R8BM	TQFN-3×3-16DL	-40℃ to +125℃	SGM71622R8BMXTUC16G/TR	1G7UC XXXXX	Tape and Reel, 4000
			SGM71622R8BMXTUC16SG/TR	1G7UC XXXXX	Tape and Reel, 250

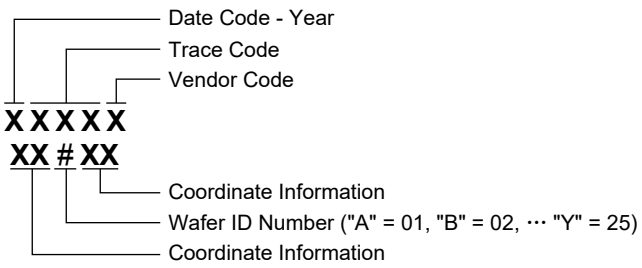
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

TQFN-3.5×3.5-16AL/TQFN-3×3-16DL



WLCSP-2.45×2.45-16B



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range
V_{DD} to GND ..... -0.3V to 6V
V_{IO} to GND ..... -0.3V to 6V
Pin Voltage Range
DAC Outputs to GND ..... -0.3V to V_{DD} + 0.3V
REF to GND ..... -0.3V to V_{DD} + 0.3V
Digital Pins to GND ..... -0.3V to V_{IO} + 0.3V
Input Current to Any Pin except Supply Pins
..... -10mA to 10mA
Package Thermal Resistance
TQFN-3.5×3.5-16AL, θ_{JA} ..... 55.3℃/W
TQFN-3.5×3.5-16AL, θ_{JB} ..... 18.1℃/W
TQFN-3.5×3.5-16AL, $\theta_{JC\ (TOP)}$ ..... 32.3℃/W
TQFN-3.5×3.5-16AL, $\theta_{JC\ (BOT)}$ ..... 16.8℃/W
TQFN-3×3-16DL, θ_{JA} ..... 55.9℃/W
TQFN-3×3-16DL, θ_{JB} ..... 18.2℃/W
TQFN-3×3-16DL, $\theta_{JC\ (TOP)}$ ..... 36.5℃/W
TQFN-3×3-16DL, $\theta_{JC\ (BOT)}$ ..... 17.2℃/W
WLCSP-2.45×2.45-16B, θ_{JA} ..... 70.6℃/W
WLCSP-2.45×2.45-16B, θ_{JB} ..... 20.6℃/W
WLCSP-2.45×2.45-16B, θ_{JC} ..... 17.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage Range, V_{DD} ..... 2.7V to 5.5V
IO Supply Voltage Range, V_{IO} ..... 1.7V to 5.5V
Digital Input Voltage Range ..... 0V to V_{IO}
Reference Input, V_{REFIN}
V_{DD} = 2.7V to 4V (Reference Divider Disabled)
..... 1.2V to (V_{DD} - 0.2V)/2
V_{DD} = 2.7V to 4V (Reference Divider Enabled)
..... 2.4V to (V_{DD} - 0.2V)
V_{DD} = 4V to 5.5V (Reference Divider Disabled)
..... 1.2V to (V_{DD} - 0.2V)/2
V_{DD} = 4V to 5.5V (Reference Divider Enabled)
..... 2.4V to (V_{DD} - 0.2V)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

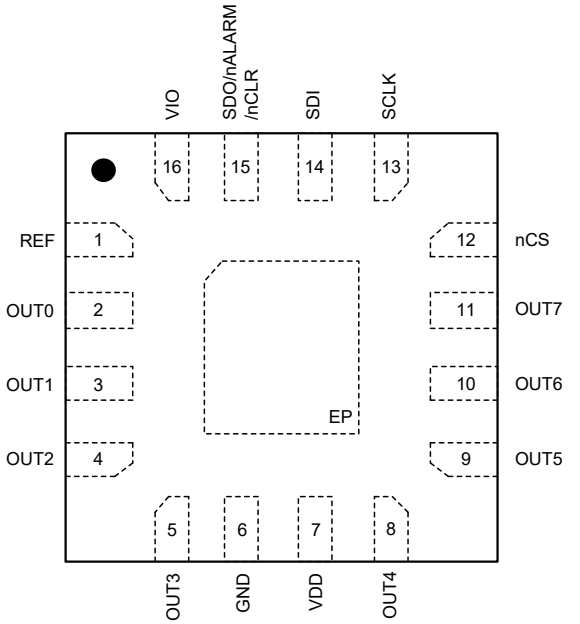
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

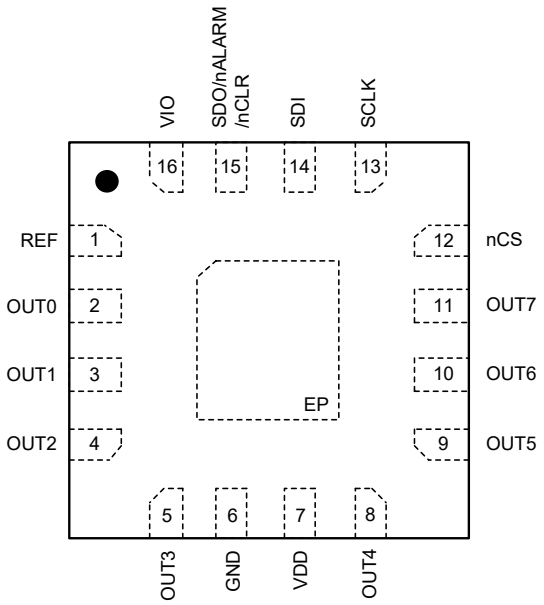
PIN CONFIGURATIONS

SGM71622R8 (TOP VIEW)



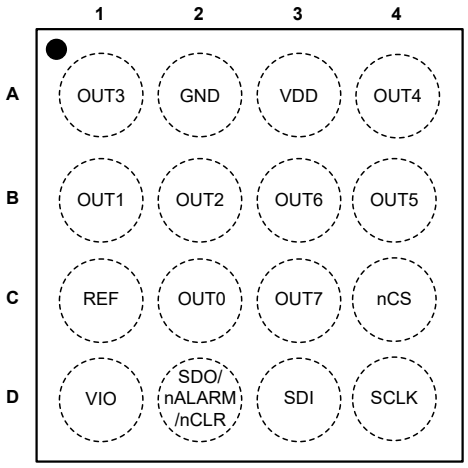
TQFN-3.5×3.5-16AL

SGM71622R8/SGM71622R8A/SGM71622R8B (TOP VIEW)



TQFN-3×3-16DL

SGM71622R8/SGM71622R8A (TOP VIEW)



WLCSP-2.45×2.45-16B

PIN DESCRIPTION

PIN			NAME	TYPE	FUNCTION
TQFN-3.5×3.5-16AL	TQFN-3×3-16DL	WLCSP-2.45×2.45-16B			
1	1	C1	REF	I/O	Reference Output Voltage Pin (Default) or Reference Input Pin.
2	2	C2	OUT0	O	Analog Output DAC 0.
3	3	B1	OUT1	O	Analog Output DAC 1.
4	4	B2	OUT2	O	Analog Output DAC 2.
5	5	A1	OUT3	O	Analog Output DAC 3.
6	6	A2	GND	G	Ground.
7	7	A3	VDD	P	Analog Supply Voltage.
8	8	A4	OUT4	O	Analog Output DAC 4.
9	9	B4	OUT5	O	Analog Output DAC 5.
10	10	B3	OUT6	O	Analog Output DAC 6.
11	11	C3	OUT7	O	Analog Output DAC 7.
12	12	C4	nCS	I	Frame Synchronization Signal Input for the Serial Data. It is active low.
13	13	D4	SCLK	I	Serial Interface Clock Pin.
14	14	D3	SDI	I	Serial Interface Data Input Pin.
15	15	D2	SDO/nALARM	O	For SGM71622R8Z/SGM71622R8AZ/SGM71622R8BZ and SGM71622R8M/SGM71622R8AM/SGM71622R8BM. Serial Interface Data Output (Default). When nCS pin goes high, the SDO pin is in high impedance. The data is clocked out on either rising or falling edges of the SCLK pin configured by the FSDO bit. This pin can be configured as a nALARM pin, under this configuration, it is an open-drain output, and a pull-up resistor to V_{IO} is required.
			nCLR	I	For SGM71622R8ZC/SGM71622R8AZC and SGM71622R8MC/SGM71622R8AMC. Active low. When it is low, chip is cleared to default value zero-scale (SGM71622R8ZC/SGM71622R8AZC) or mid-scale (SGM71622R8MC/SGM71622R8AMC).
16	16	D1	VIO	P	IO Power Supply.
EP	EP	—	Exposed Pad	—	Exposed pad should be soldered to PCB board and connected to GND.

NOTE: I = input, O = output, I/O = input or output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to 5.5V, V_{REFIN} = 1.25V to 5.5V, R_{LOAD} = 2kΩ to GND, C_{LOAD} = 200pF to GND, digital inputs at V_{IO} or GND, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Static Performance (1)							
Resolution				16			Bits
Integral Nonlinearity	INL	SGM71622R8	T_A = +25℃		±0.5	±1	LSB
			T_A = -20℃ to +105℃		±0.5	±1	
			T_A = -40℃ to +125℃		±0.5	±3	
		SGM71622R8A			±1		
		SGM71622R8B			±12		
Differential Nonlinearity	DNL	SGM71622R8	T_A = +25℃		±0.5	±1	LSB
			T_A = -20℃ to +105℃		±0.5	±1	
			T_A = -40℃ to +125℃		±0.5	±3	
		SGM71622R8A			±1		
		SGM71622R8B			±12		
Total Unadjusted Error	TUE	All GAINs			±0.05	±0.2	%FSR
Offset Error	E_O	All GAINs			±0.5	±2	mV
Zero-Code Error		DAC code = zero-scale			0.5	2	mV
Full-Scale Error		GAIN = 2 (BUFFx_GAIN = 1, REFDIV_EN = 0)			±0.05	±0.2	%FSR
		GAIN = 1 (BUFFx_GAIN = 1, REFDIV_EN = 1)			±0.05	±0.2	
		GAIN = ½ (BUFFx_GAIN = 0, REFDIV_EN = 1)			±0.1	±0.2	
Gain Error	E_G	GAIN = 2 (BUFFx_GAIN = 1, REFDIV_EN = 0)			±0.05	±0.2	%FSR
		GAIN = 1 (BUFFx_GAIN = 1, REFDIV_EN = 1)			±0.05	±0.2	
		GAIN = ½ (BUFFx_GAIN = 0, REFDIV_EN = 1)			±0.1	±0.2	
Offset Error Drift					±4		μV/℃
Zero-Code Error Drift					±2		μV/℃
Full-Scale Error Drift					±2		ppm of FSR/℃
Gain Error Drift					±2		ppm of FSR/℃
Output Voltage Drift over Time		T_A = +25℃, DAC code = mid-scale, 1600 hours			30		ppm of FSR
Output Characteristics							
Voltage Range		GAIN = 2 (BUFFx_GAIN = 1, REFDIV_EN = 0)		0		2 × V_{REF}	V
		GAIN = 1 (BUFFx_GAIN = 1, REFDIV_EN = 1)		0		V_{REF}	
		GAIN = ½ (BUFFx_GAIN = 0, REFDIV_EN = 1)		0		½ × V_{REF}	
Output Voltage Headroom		to GND or V_{DD} (unloaded)			0.003		V
		to GND or V_{DD} (-5mA ≤ I_{OUT} ≤ 5mA)		0.2			
		to GND or V_{DD} (-10mA ≤ I_{OUT} ≤ 10mA)		0.4			
		to GND or V_{DD} (-20mA ≤ I_{OUT} ≤ 20mA)		0.6			
Short-Circuit Current (2)		DAC code = full-scale, output shorted to GND			35		mA
		DAC code = zero-scale, output shorted to V_{DD}			35		
Load Regulation		DAC code = mid-scale, -10mA ≤ I_{OUT} ≤ 10mA			75		μV/mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to 5.5V, V_{REFIN} = 1.25V to 5.5V, R_{LOAD} = 2kΩ to GND, C_{LOAD} = 200pF to GND, digital inputs at V_{IO} or GND, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Characteristics							
Maximum Capacitive Load (3)		R_{LOAD} = ∞		0		2	nF
		R_{LOAD} = 2kΩ		0		10	
DC Output Impedance		DAC code = mid-scale			0.08		Ω
		DAC output at GND			10		
		DAC output at V_{DD}			15		
Dynamic Performance							
Output Voltage Settling Time		¼ to ¾ scale and ¾ to ¼ scale settling time to ±2LSB, V_{DD} = 5.5V, V_{REFIN} = 2.5V, GAIN = 2			5		μs
Slew Rate	SR	V_{DD} = 5.5V, V_{REFIN} = 2.5V, GAIN = 2			2		V/μs
Power-Up Time (4)		DACx-PWDWN 1 to 0 transition, DAC code = full-scale, V_{DD} = 5.5V, V_{REFIN} = 2.5V, GAIN = 2			10		μs
Power-Up Glitch Magnitude		DAC code = zero-scale, V_{DD} = 5.5V, V_{REFIN} = 2.5V, GAIN = 2, C_{LOAD} = 50pF			20		mV
Output Noise		0.1Hz to 10Hz, DAC code = mid-scale, V_{DD} = 5.5V, internal reference = 2.5V, GAIN = 2			38		μV_{PP}
Output Noise Density		DAC code = mid-scale, V_{DD} = 5.5V, internal reference = 2.5V, GAIN = 2	1kHz		200		$nV/\sqrt{Hz}$
			10kHz		300		
		DAC code = full-scale, V_{DD} = 5.5V, internal reference = 2.5V, GAIN = 1	1kHz		100		
			10kHz		150		
AC PSRR		DAC code = mid-scale, frequency = 60Hz, amplitude = 200mV_{PP} superimposed on V_{DD}			85		dB
DC PSRR		DAC code = mid-scale, V_{DD} = 5V ± 10%			20		μV/V
Code Change Glitch Impulse		1LSB change around major carrier			2		nV-s
Channel-to-Channel AC Crosstalk		DAC code = mid-scale, code 32 to full-scale swing on adjacent channel			2.5		nV-s
Channel-to-Channel DC Crosstalk		Measured channel at mid-scale, adjacent channel at full-scale			8		μV
		Measured channel at mid-scale, all other channels at full-scale			10		
External Reference Input							
Reference Input Current		V_{REFIN} = 2.5V			25		μA
Reference Input Impedance					100		kΩ
Reference Input Capacitance					5		pF
Internal Reference							
Reference Output Voltage	V_{REFOUT}	T_A = +25℃		2.495	2.5	2.505	V
Reference Output Drift					5	12	ppm/℃
Reference Output Impedance					0.15		Ω
Reference Output Noise		0.1Hz to 10Hz			25		μV_{PP}
Reference Output Noise Density		10kHz, REF_{LOAD} = 10nF			280		$nV/\sqrt{Hz}$
Reference Load Current					±5		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to 5.5V, V_{REFIN} = 1.25V to 5.5V, R_{LOAD} = 2kΩ to GND, C_{LOAD} = 200pF to GND, digital inputs at V_{IO} or GND, T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Inputs							
High-Level Input Voltage	V_{IH}			0.75 × V_{IO}			V
Low-Level Input Voltage	V_{IL}					0.25 × V_{IO}	V
Input Current					5		nA
Input Pin Capacitance					5		pF
Digital Outputs (SDO/nALARM)							
High-Level Output Voltage	V_{OH}	I_{LOAD} = 0.2mA		V_{IO} - 0.2			V
Low-Level Output Voltage	V_{OL}	I_{LOAD} = -0.2mA				0.2	V
Output Pin Capacitance					5		pF
Power Supply Requirements							
V_{DD} Supply Current	I_{DD}	Active mode, GAIN = 1, DAC code = full-scale, outputs unloaded, SPI static	Internal reference enabled		4	5.5	mA
			Internal reference disabled		3.5	4.5	
		Power-down			0.5		μA
V_{IO} Supply Current	I_{IO}				0.35	0.6	μA

NOTES:

1. Specified in all GAIN options, unless otherwise noted. End point fit from code 256 to 65280.
2. Temporary overload condition protection and current limited.
3. Specified by design.
4. Time to get DAC power-up.

TIMING CHARACTERISTICS

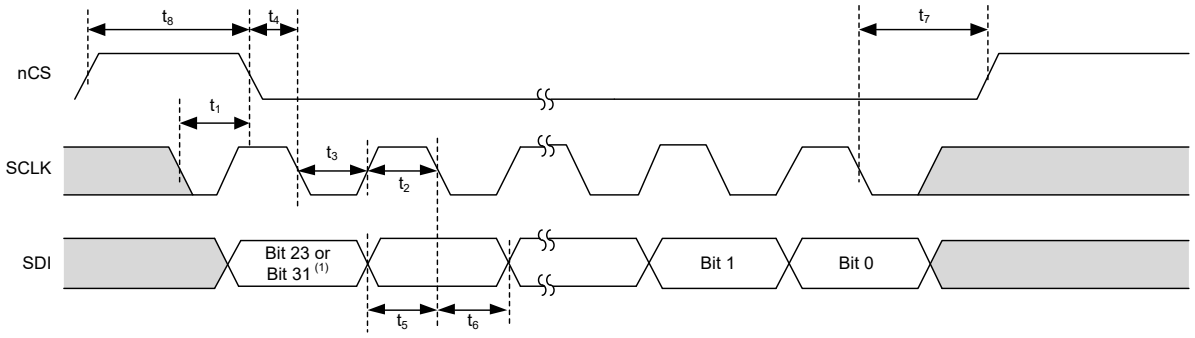
(All input signals are specified with t_R = t_F = 1ns/V (10% to 90% of V_{IO}), timed from a voltage level of (V_{IL} + V_{IH})/2, V_{DD} = 2.7V to 5.5V, V_{IO} = 1.7V to 5.5V, V_{REFIN} = 1.25V to 5.5V, SDO loaded with 20pF, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	V_{IO} = 1.7V to 2.7V			V_{IO} = 2.7V to 5.5V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Serial Interface – Write Operation								
SCLK Frequency	f_{SCLK}			50			50	MHz
SCLK Falling Edge to nCS Ignore	t_1	7			7			ns
SCLK High Time	t_2	9			9			ns
SCLK Low Time	t_3	9			9			ns
nCS to SCLK Falling Edge Setup Time	t_4	13			13			ns
SDI Setup Time	t_5	5			5			ns
SDI Hold Time	t_6	10			10			ns
SCLK Falling Edge to nCS Rising Edge	t_7	10			10			ns
nCS High Time	t_8	15			15			ns
Serial Interface – Read and Daisy-Chain Operation, FSDO = 0								
SCLK Frequency	f_{SCLK}			12			18	MHz
SCLK Falling Edge to nCS Ignore	t_1	7			7			ns
SCLK High Time	t_2	35			25			ns
SCLK Low Time	t_3	35			25			ns
nCS to SCLK Falling Edge Setup Time	t_4	35			25			ns
SDI Setup Time	t_5	5			5			ns
SDI Hold Time	t_6	10			10			ns
SCLK Falling Edge to nCS Rising Edge	t_7	10			10			ns
nCS High Time	t_8	15			15			ns
SDO Output Delay from SCLK Rising Edge	t_9	3.5		33.5	3.5		23	ns
SDO Driven to Tri-State	t_{11}	0		300	0		200	ns
Serial Interface – Read and Daisy-Chain Operation, FSDO = 1								
SCLK Frequency	f_{SCLK}			20			25	MHz
SCLK Falling Edge to nCS Ignore	t_1	7			7			ns
SCLK High Time	t_2	22			18			ns
SCLK Low Time	t_3	22			18			ns
nCS to SCLK Falling Edge Setup Time	t_4	32			20			ns
SDI Setup Time	t_5	5			5			ns
SDI Hold Time	t_6	10			10			ns
SCLK Falling Edge to nCS Rising Edge	t_7	10			10			ns
nCS High Time	t_8	15			15			ns
SDO Output Delay from SCLK Falling Edge	t_{10}	3.5	25	45	3.5	10	32	ns
SDO Driven to Tri-State	t_{11}	0		300	0		200	ns
Digital Logic								
POR Reset Delay	$t_{RSTDLYPOR}$		45			45		μs
Sequential DAC Output Updates	$t_{DACWAIT}$	3			3			μs
nCLR Pulse	t_{CLR}	20			20			ns
nCLR Delay (1)	t_{CLRD}			3			3	μs

NOTE:

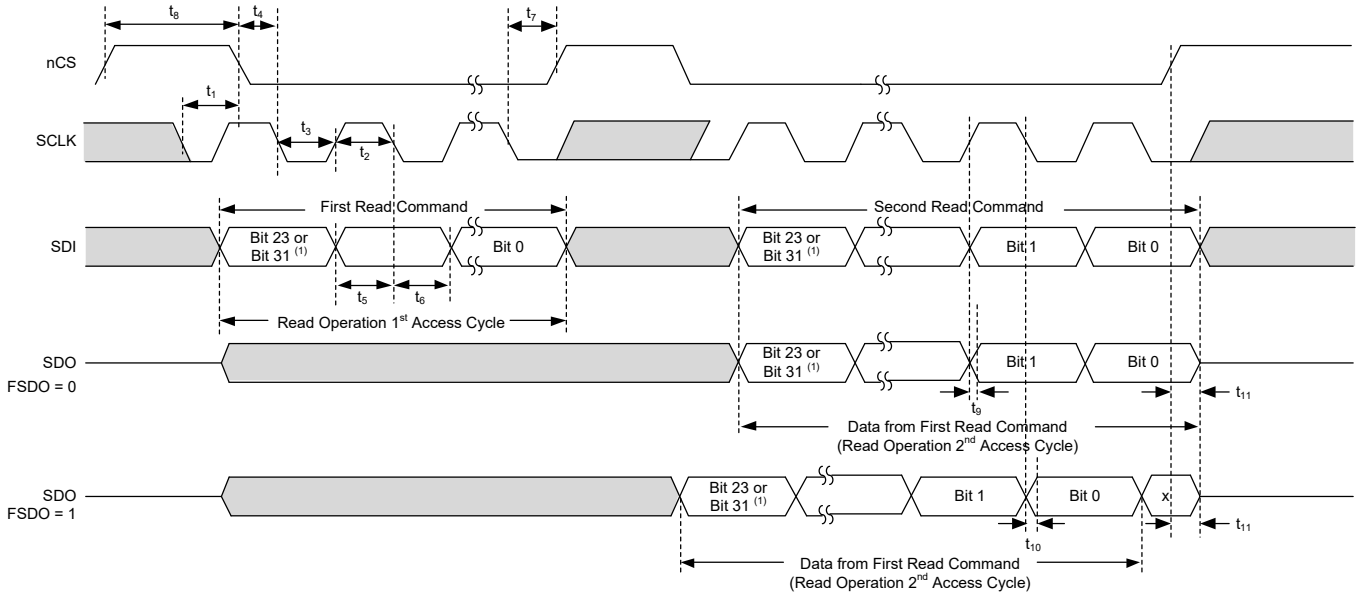
1. Specified from a logic-low on nCLR pin to when the DAC output starts to change. In the special case when the DAC output is at GND or V_{DD}, the nCLR delay may be as long as 3μs.

TIMING DIAGRAMS



NOTE:
1. If CRC is enabled, the data is 32-bit long. If CRC is disabled, the data is 24-bit long (default).

Figure 1. Serial Interface Write Timing Diagram



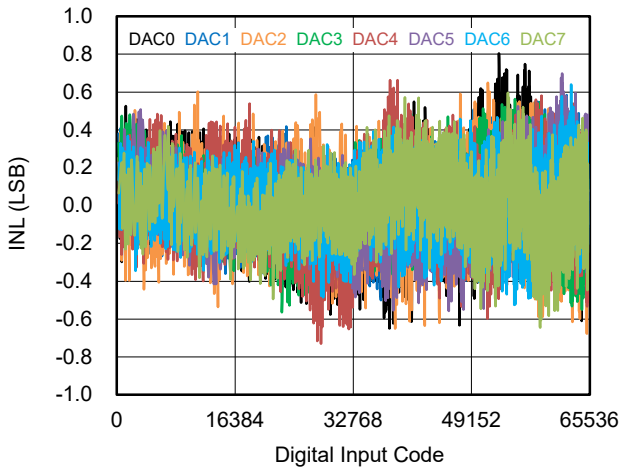
NOTE:
1. If CRC is enabled, the data is 32-bit long. If CRC is disabled, the data is 24-bit long (default).

Figure 2. Serial Interface Read Timing Diagram

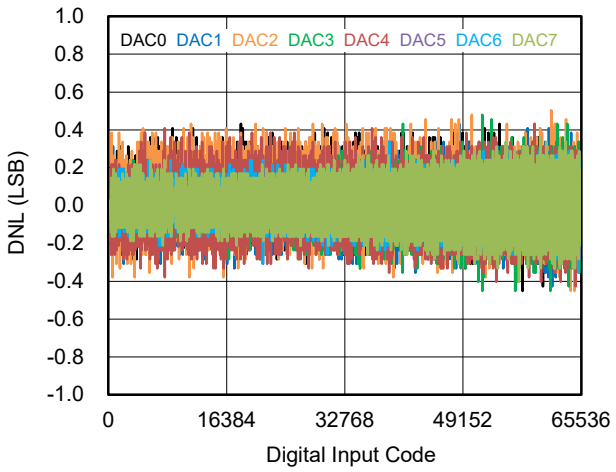
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

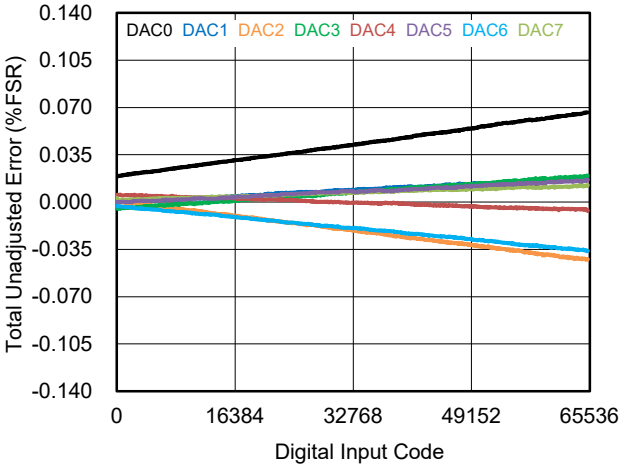
Integral Nonlinearity Error vs. Digital Input Code



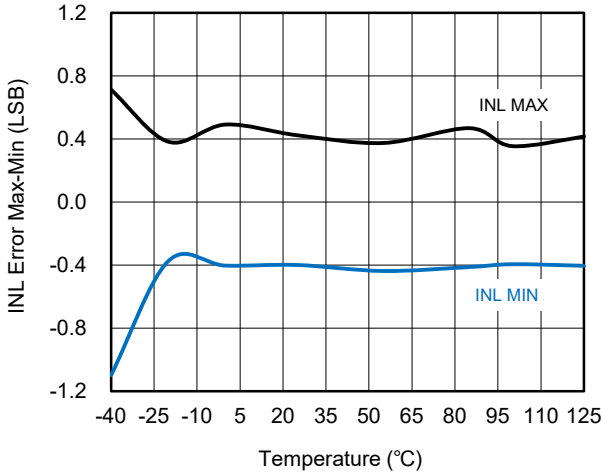
Differential Nonlinearity Error vs. Digital Input Code



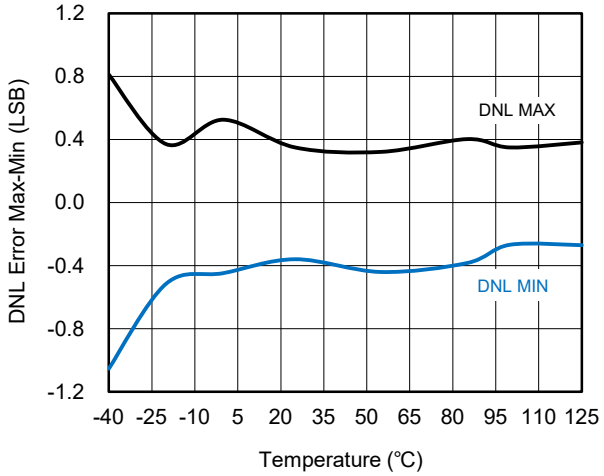
Total Unadjusted Error vs. Digital Input Code



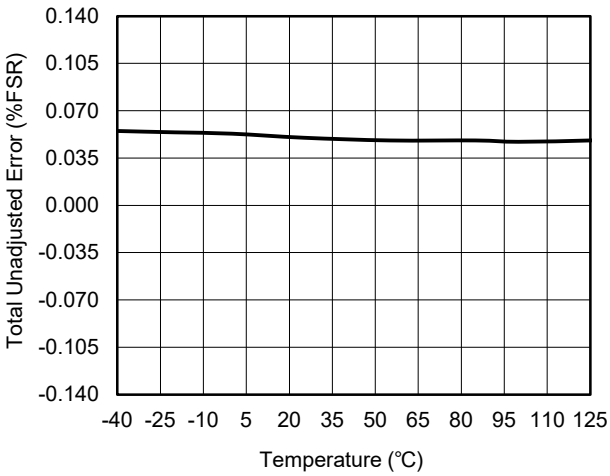
Integral Nonlinearity Error vs. Temperature



Differential Nonlinearity Error vs. Temperature



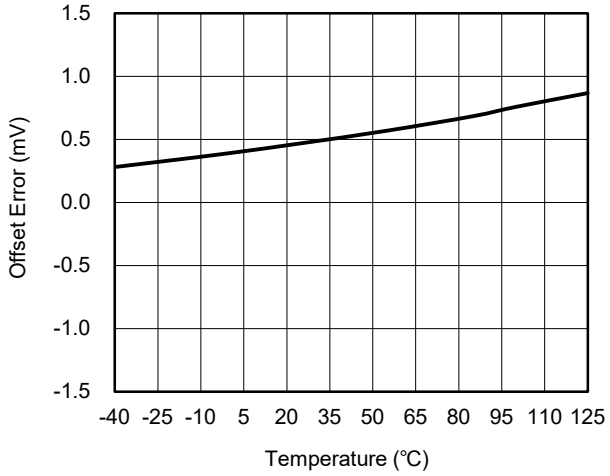
Total Unadjusted Error vs. Temperature



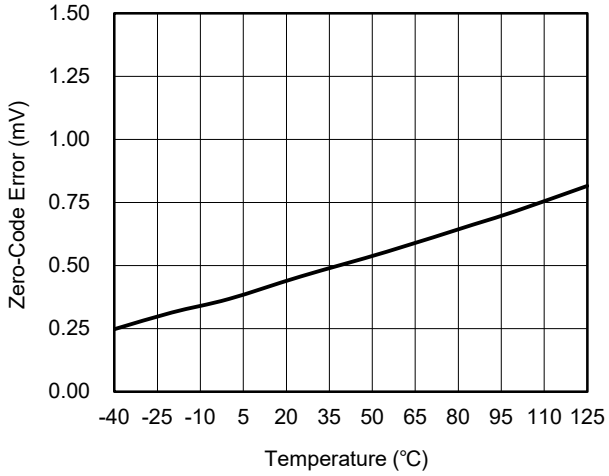
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

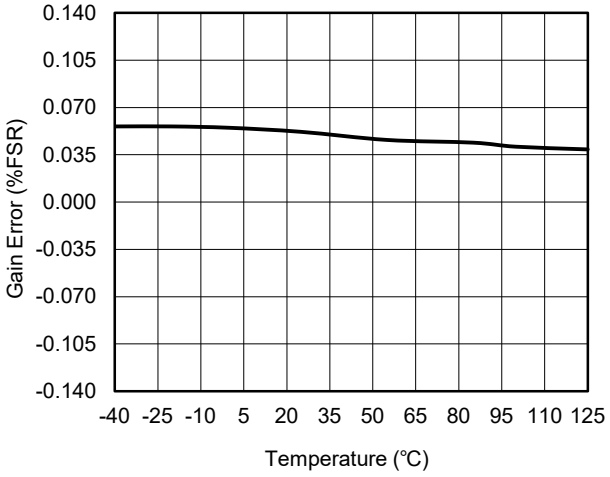
Offset Error vs. Temperature



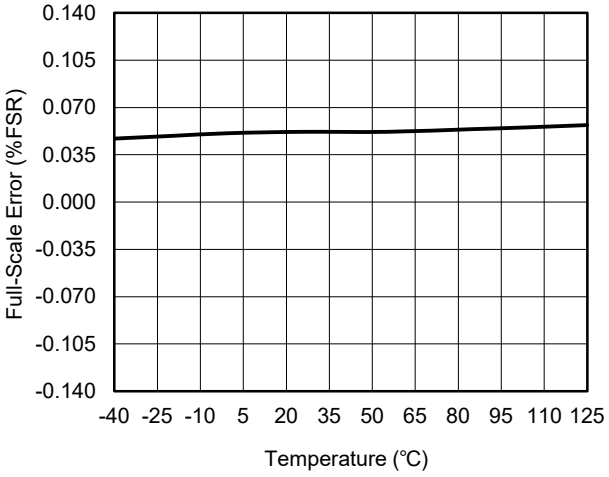
Zero-Code Error vs. Temperature



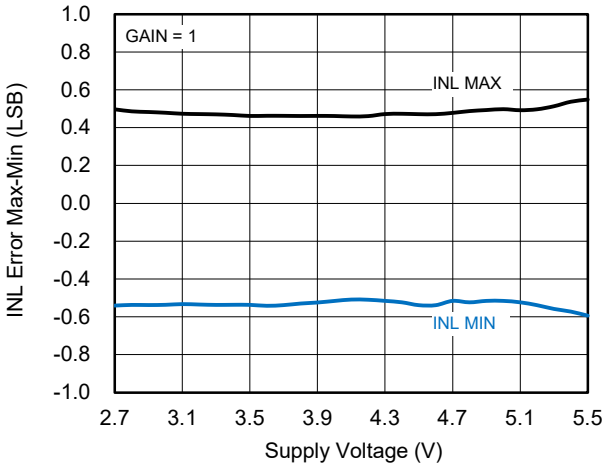
Gain Error vs. Temperature



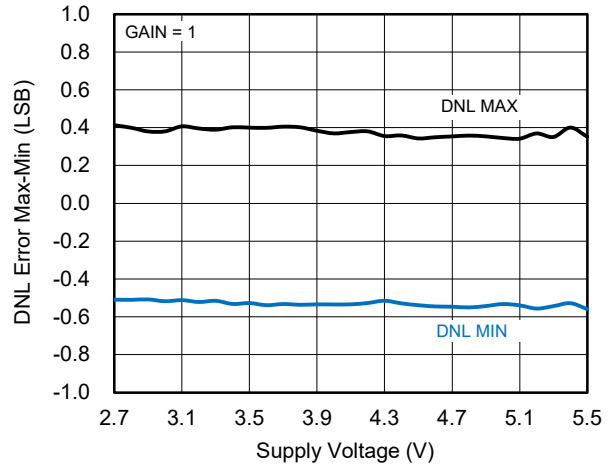
Full-Scale Error vs. Temperature



Integral Nonlinearity Error vs. Supply Voltage



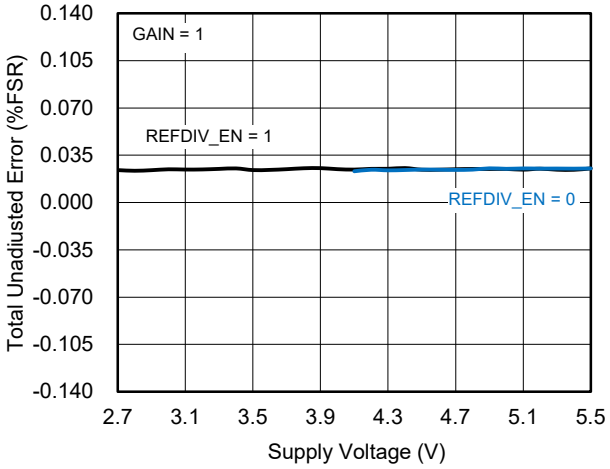
Differential Nonlinearity Error vs. Supply Voltage



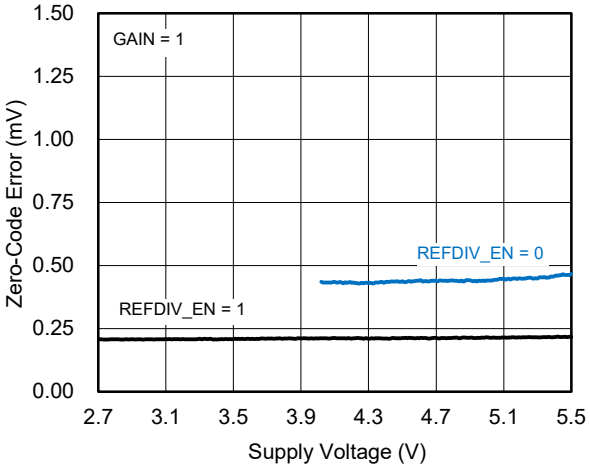
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

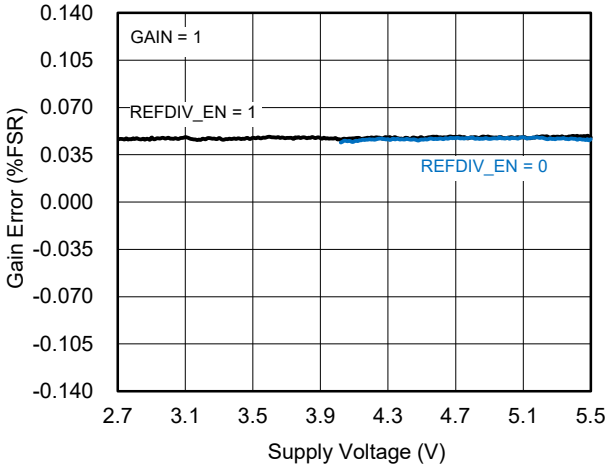
Total Unadjusted Error vs. Supply Voltage



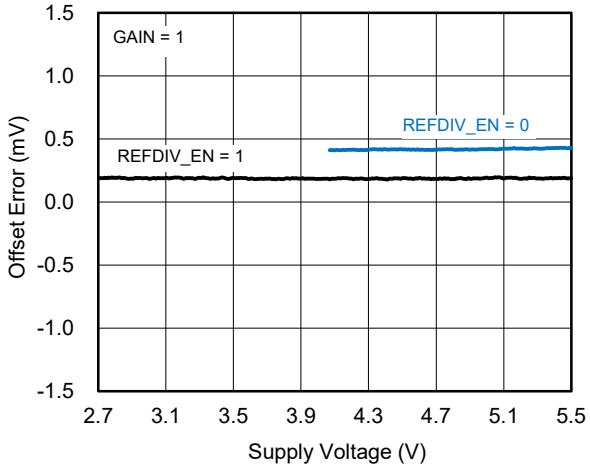
Zero-Code Error vs. Supply Voltage



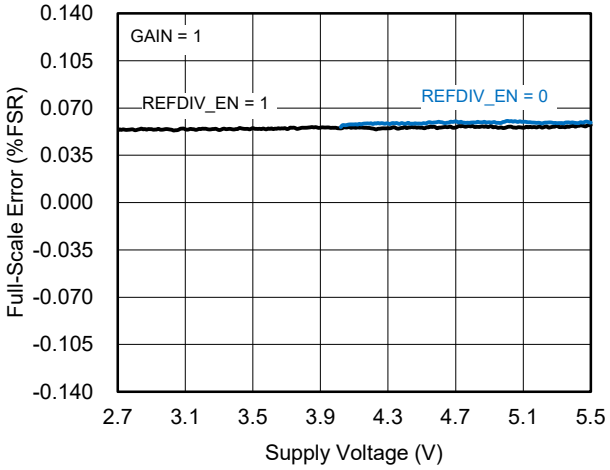
Gain Error vs. Supply Voltage



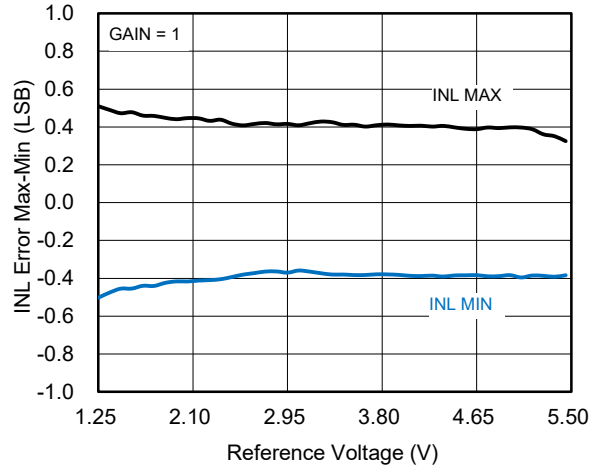
Offset Error vs. Supply Voltage



Full-Scale Error vs. Supply Voltage



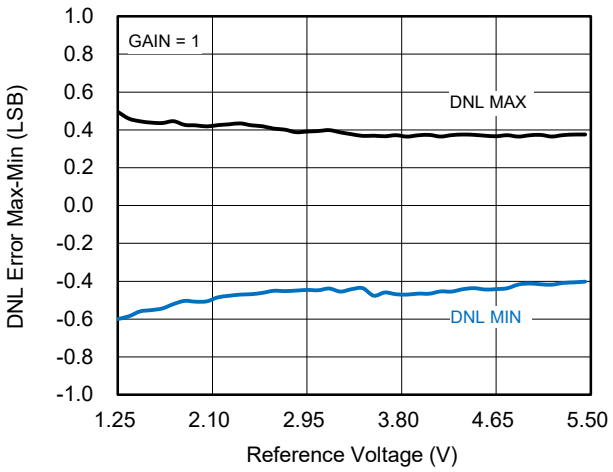
Integral Nonlinearity Error vs. Reference Voltage



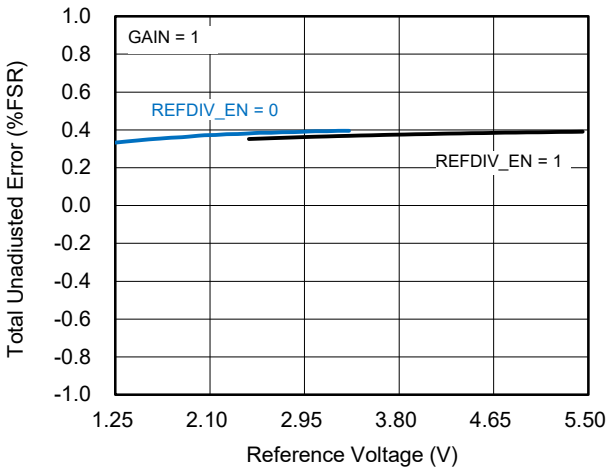
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

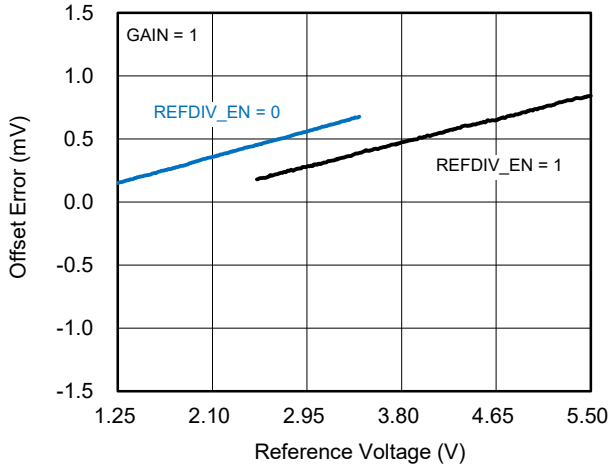
Differential Nonlinearity Error vs. Reference Voltage



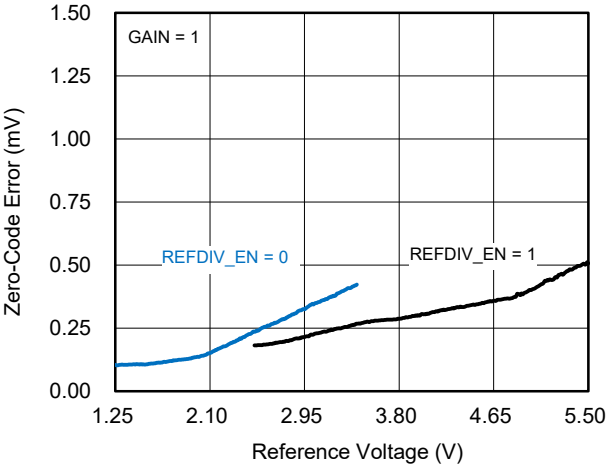
Total Unadjusted Error vs. Reference Voltage



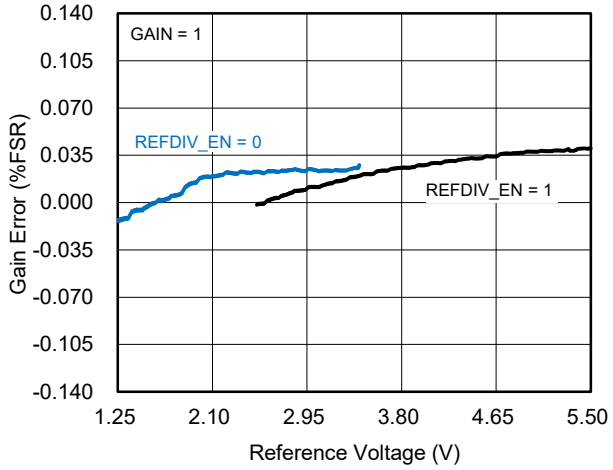
Offset Error vs. Reference Voltage



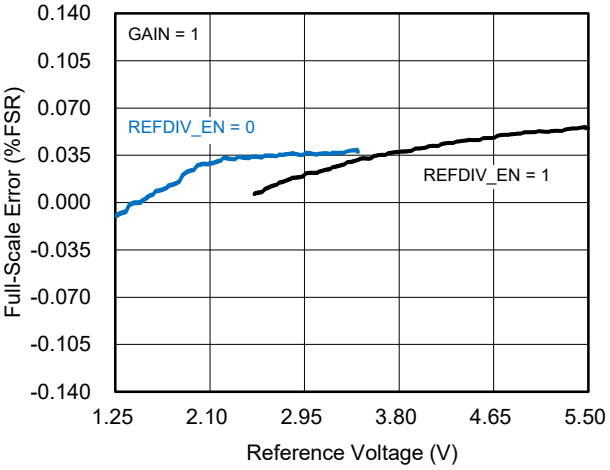
Zero-Code Error vs. Reference Voltage



Gain Error vs. Reference Voltage



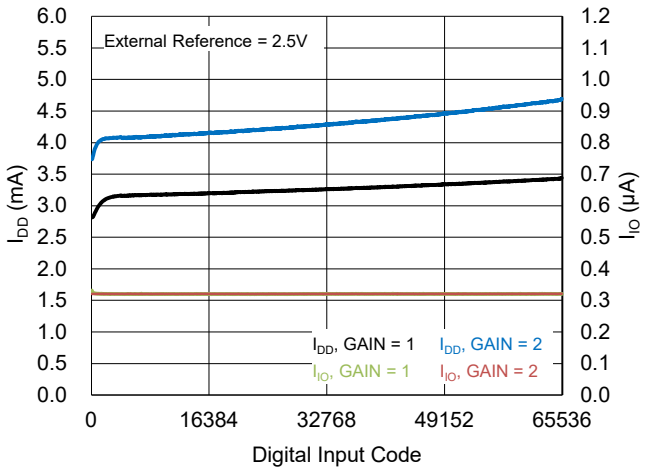
Full-Scale Error vs. Reference Voltage



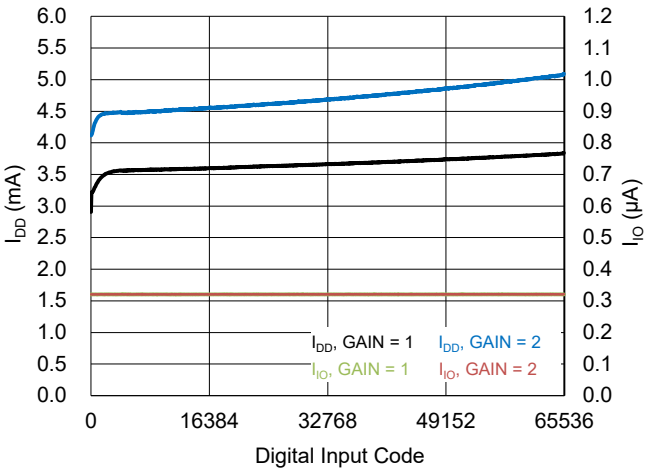
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

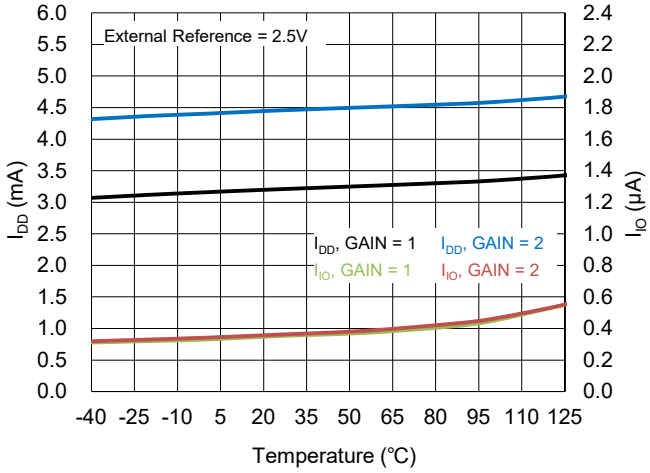
Supply Current with External Reference vs. Digital Input Code



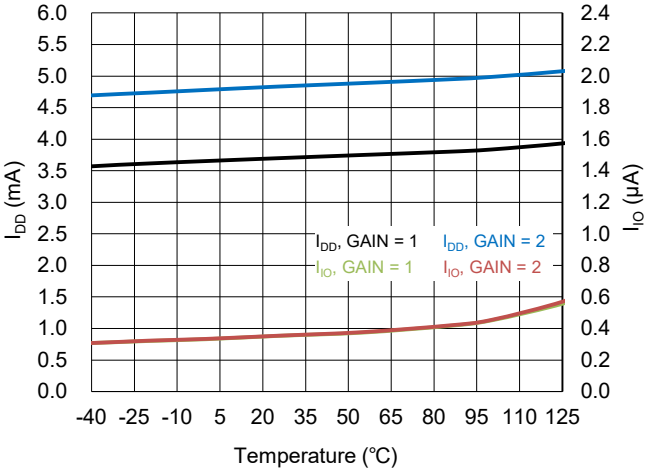
Supply Current with Internal Reference vs. Digital Input Code



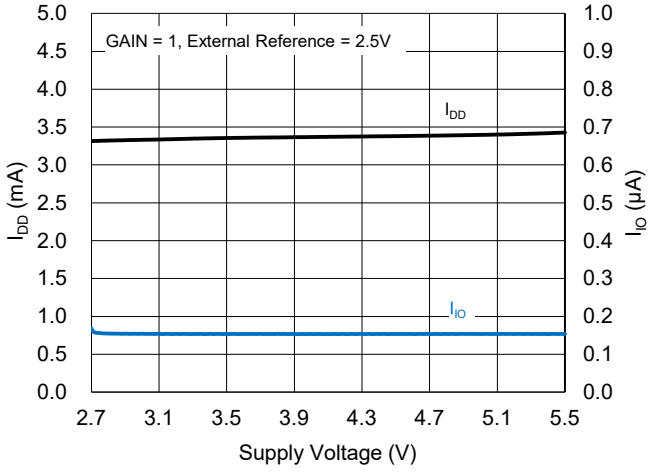
Supply Current with External Reference vs. Temperature



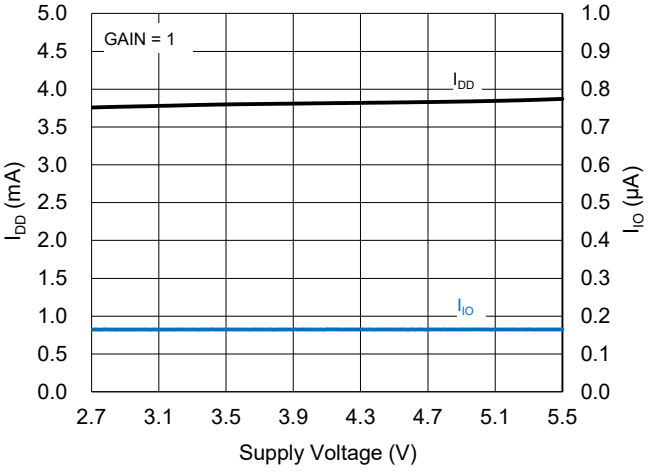
Supply Current with Internal Reference vs. Temperature



Supply Current with External Reference vs. Supply Voltage



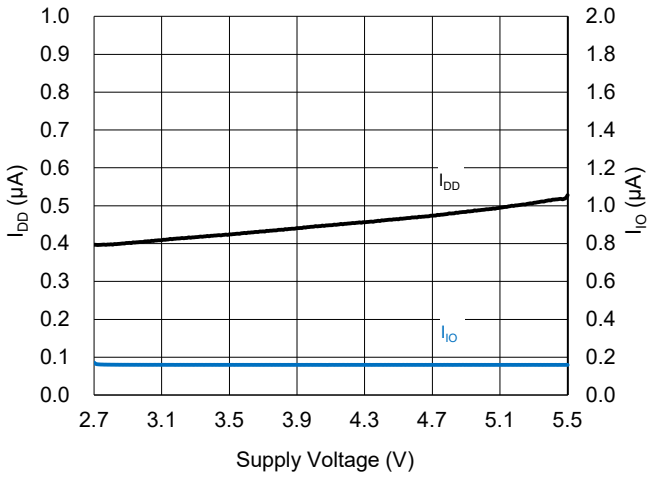
Supply Current with Internal Reference vs. Supply Voltage



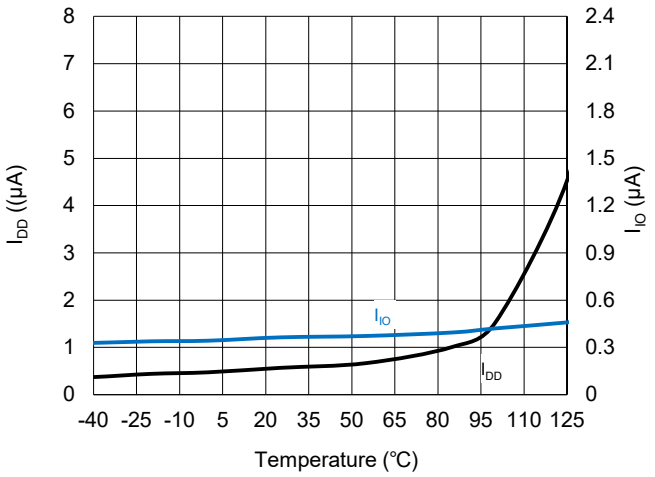
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

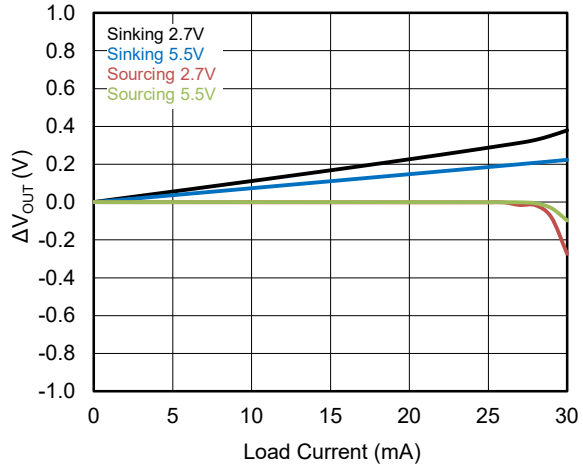
Power-Down Current vs. Supply Voltage



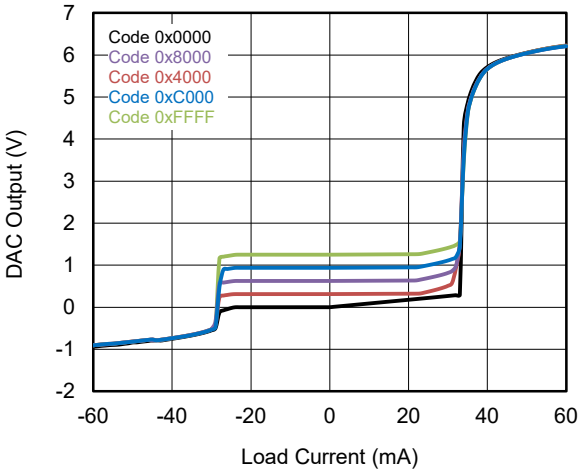
Power-Down Current vs. Temperature



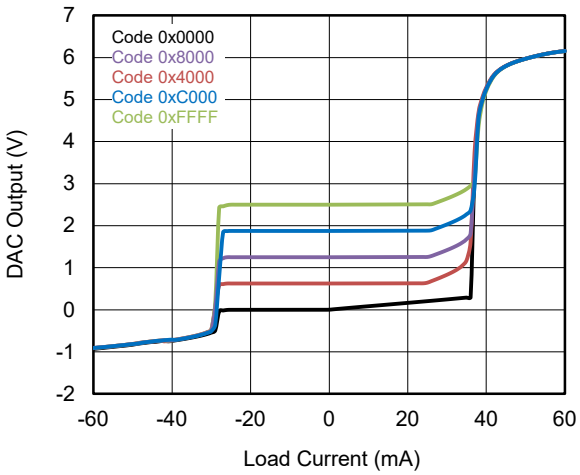
Headroom/Footroom vs. Load Current



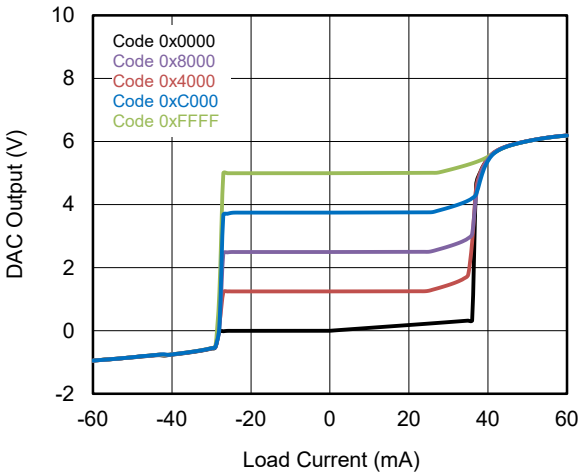
Source and Sink Capability with GAIN = ½



Source and Sink Capability with GAIN = 1



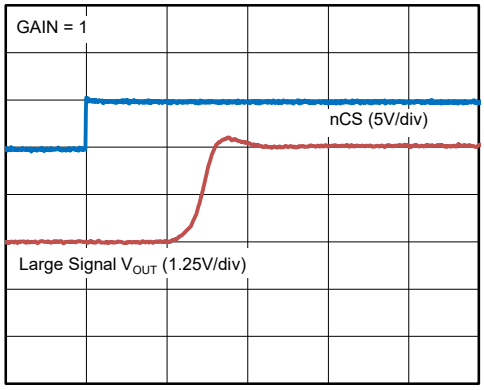
Source and Sink Capability with GAIN = 2



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

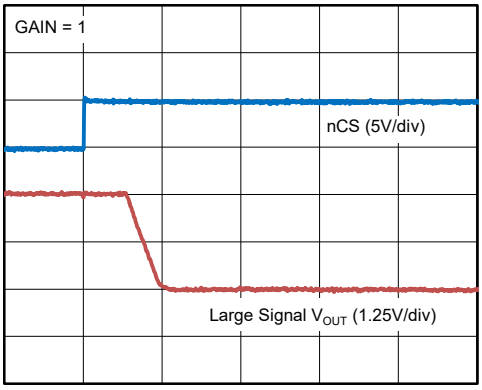
T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

Full-Scale Settling Time, Rising Edge



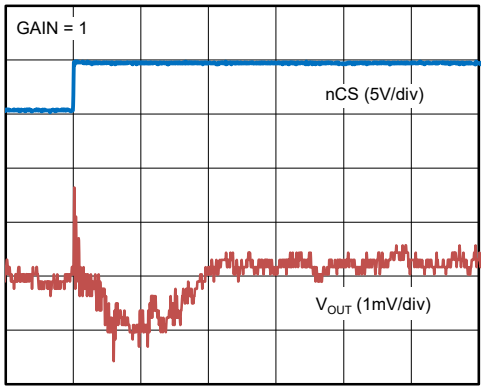
Time (3μs/div)

Full-Scale Settling Time, Falling Edge



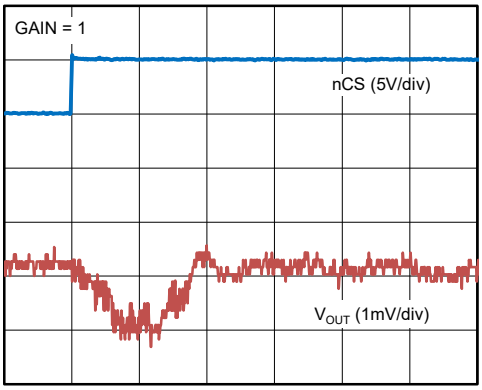
Time (3μs/div)

Glitch Impulse, Rising Edge, 1LSB Step



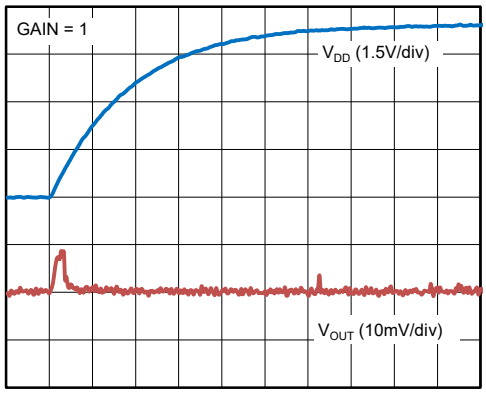
Time (1μs/div)

Glitch Impulse, Falling Edge, 1LSB Step



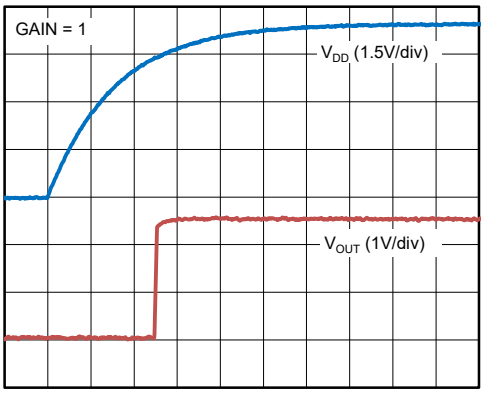
Time (1μs/div)

Power-On, Reset to Zero-Scale



Time (500μs/div)

Power-On, Reset to Mid-Scale

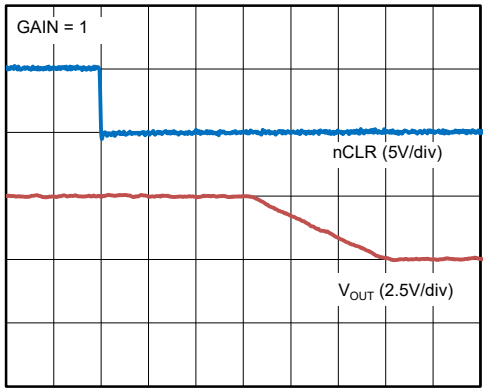


Time (500μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

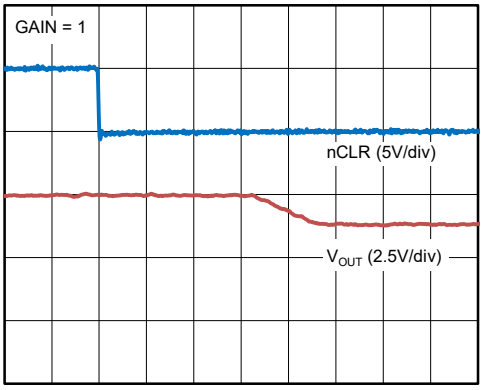
T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

Clear to Zero-Scale (SGM71622R8ZC/SGM71622R8AZC)



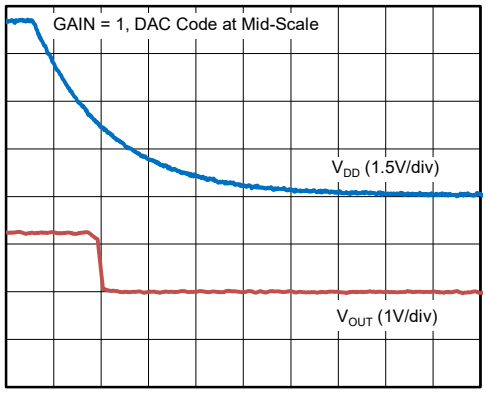
Time (0.5μs/div)

Clear to Mid-Scale (SGM71622R8MC/SGM71622R8AMC)



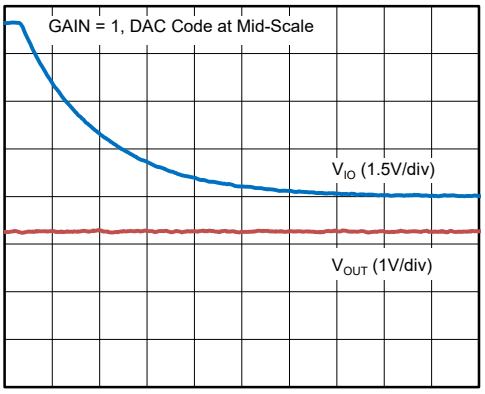
Time (0.5μs/div)

V_{DD} Power-Down



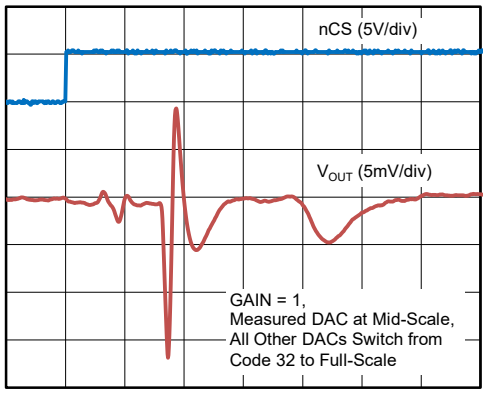
Time (500μs/div)

V_{IO} Power-Down



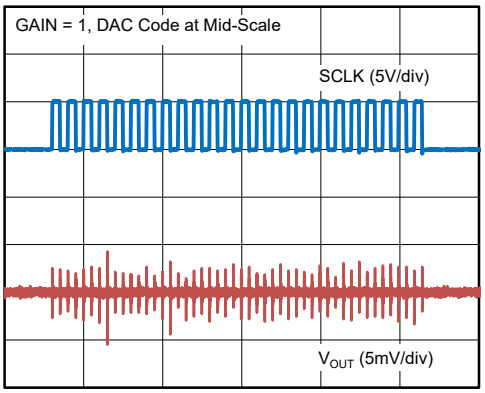
Time (500μs/div)

Channel-to-Channel Crosstalk



Time (1μs/div)

Clock Feedthrough with SCLK = 1MHz

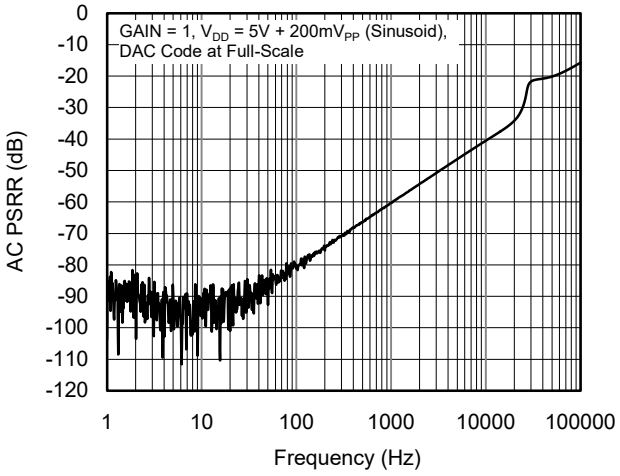


Time (5μs/div)

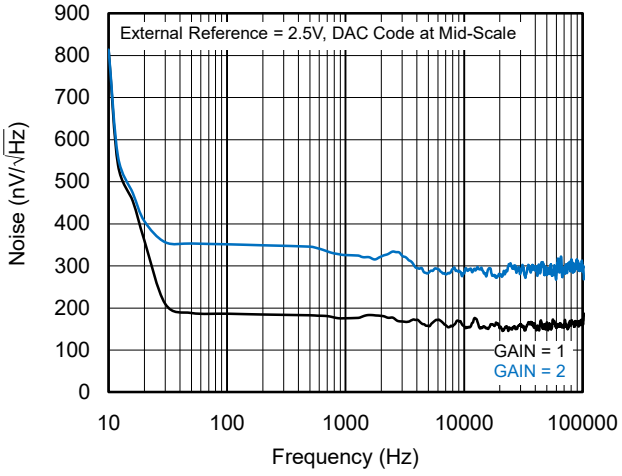
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

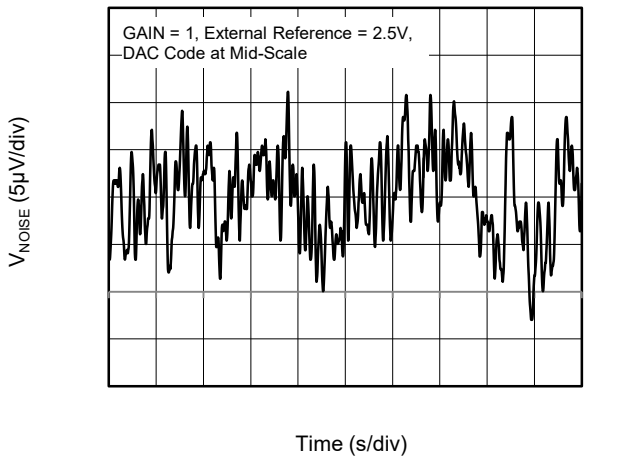
DAC Output AC PSRR vs. Frequency



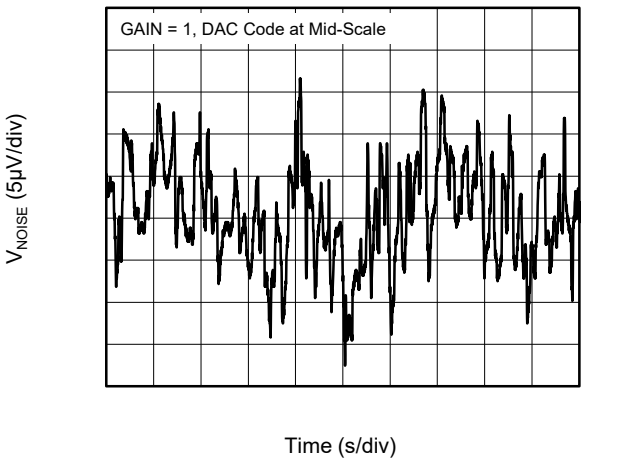
DAC Output Noise Density vs. Frequency



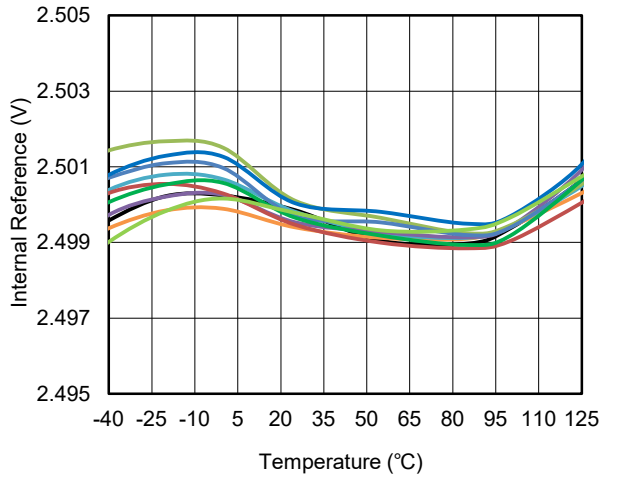
DAC Output Noise with External Reference 0.1Hz to 10Hz



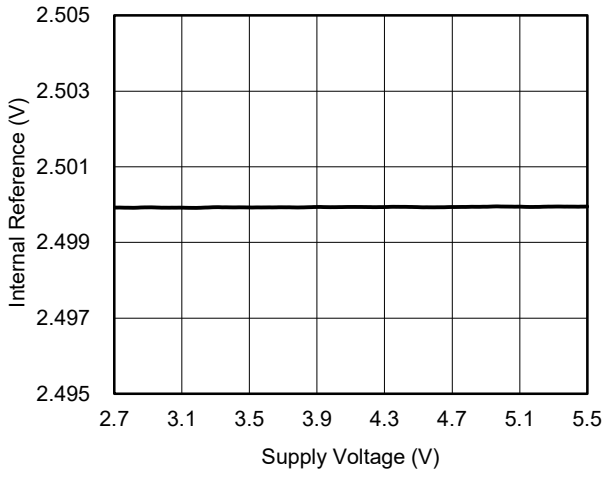
DAC Output Noise with Internal Reference 0.1Hz to 10Hz



Internal Reference Voltage vs. Temperature



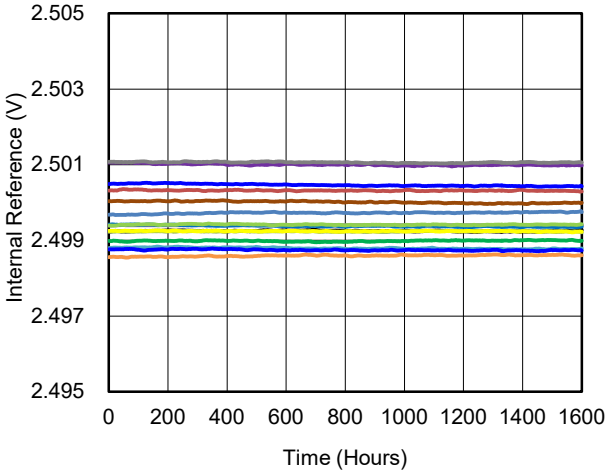
Internal Reference Voltage vs. Supply Voltage



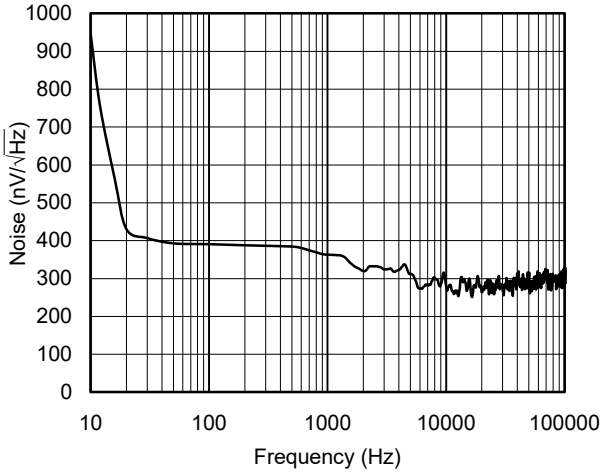
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 5.5V, Internal Reference = 2.5V, DAC outputs unloaded, unless otherwise noted.

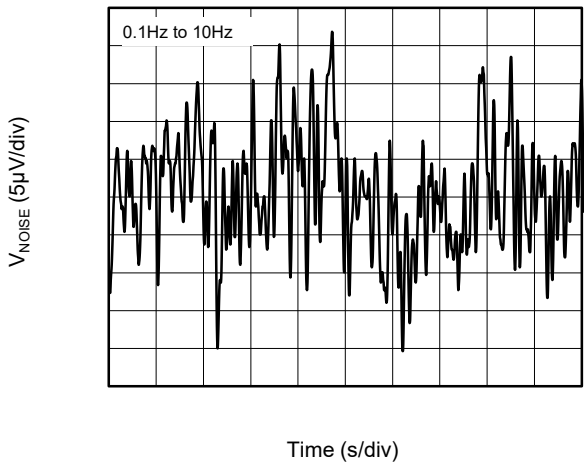
Internal Reference Voltage vs. Time



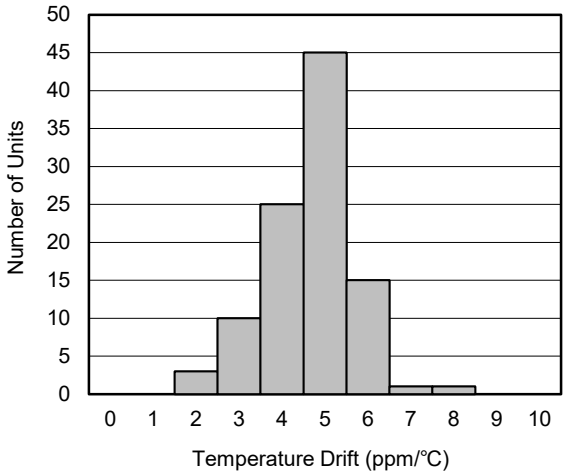
Internal Reference Noise Density vs. Frequency



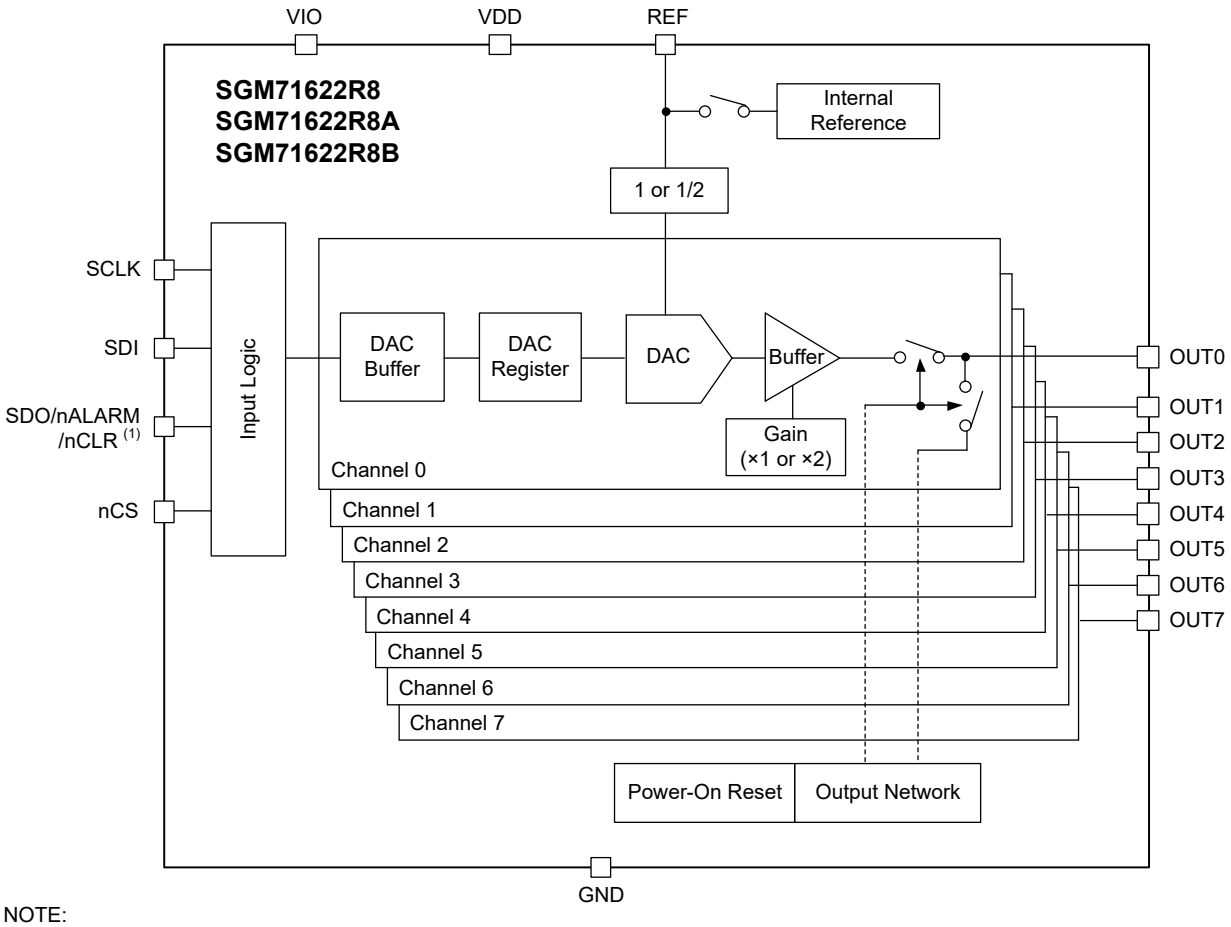
Internal Reference Noise



Internal Reference Temperature Drift Histogram



FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. The SDO/nALARM pin for SGM71622R8Z/SGM71622R8AZ/SGM71622R8BZ and SGM71622R8M/SGM71622R8AM/SGM71622R8BM, and the nCLR pin for SGM71622R8ZC/SGM71622R8AZC and SGM71622R8MC/SGM71622R8AMC.

Figure 3. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM71622R8 family is 16-bit, pin-compatible, low power, 8 channels, buffered voltage-output digital-to-analog converter. The SGM71622R8Z/SGM71622R8AZ/SGM71622R8BZ and SGM71622R8ZC/SGM71622R8AZC are power-on reset to 0V output parts. The SGM71622R8M/SGM71622R8AM/SGM71622R8BM and SGM71622R8MC/SGM71622R8AMC are power-on reset to mid-scale output parts. The SGM71622R8ZC/SGM71622R8AZC and SGM71622R8MC/SGM71622R8AMC have a separate clear pin (pin 15 or pin D2), which can be used to simultaneously reset DAC channels to power-on default value.

DAC Transfer Function

The data to DAC is in straight binary format, so the DAC transfer function is as follows:

$$V_{OUT} = \frac{CODE}{2^n} \times \frac{V_{REF}}{DIV} \times GAIN \quad (1)$$

Where:

CODE = Decimal equivalent of the binary code, which is loaded to the DAC register. It can range from 0 to 65535.

V_{REF} = DAC reference voltage. Voltage reference is an internal 2.5V reference or an external one.

n = Resolution in bits.

DIV = 1 or 2 (configure the REFDIV_EN bit in the GAIN register).

GAIN = 1 or 2 (configure the BUFFx_GAIN bit in the GAIN register).

Output Amplifiers

The full-scale output of each channel is set by V_{REF} (reference voltage), DIV and channel buffer GAIN. The settings for each output channel can be set individually.

Table 1. DAC Output Range Configuration Matrix

DIV Setting	GAIN Setting	DAC Output Range
÷2	×1	0V to ½ × V_{REF}
÷1	×1	Not Recommended
÷2	×2	0V to V_{REF}
÷1	×2	0V to 2 × V_{REF}

DAC Register Synchronous and Asynchronous Updates

In asynchronous mode, a write operation to the DAC data register causes DAC output update immediately on the rising edge of nCS. In synchronous mode, writing to the DAC data register does not cause the DAC output update. The DAC output update is trigged by the LDAC bit setting in the TRIGGER register. It synchronously updates multiple DAC outputs.

In asynchronous mode, for full speed flushing of write command operation, the interval between writing frames (measured from the previous nCS pulse signal's falling edge to the following nCS pulse signal's falling edge) should be longer than 2.5μs to ensure that the output is updated as needed.

Broadcast DAC Register

A single write to DAC broadcast register updates all configured DAC output. Keep unchanged or accept broadcast command can be set individually by the channel in the corresponding DACx_BRDCAST_EN bit (set in SYNC register).

CLEAR Operation (SGM71622R8ZC/SGM71622R8AZC and SGM71622R8MC/SGM71622R8AMC Only)

The logic low on nCLR pin resets multiple DAC channels to their power-on default values. Keeping unaffected or cleared by nCLR can be set by the corresponding CLR_*_MSK bit (DAC channels 0 to 3 and channels 4 to 7 are two individual groups) in GAIN register. The logic high on the nCLR pin sets the device to exit clear mode.

Power-On Reset (POR)

The SGM71622R8 family has a power-on reset function that makes the chip output a default voltage when the system powers on.

Software Reset

The software reset is valid on the rising edge of nCS that is followed at the end of a reset command.

DETAILED DESCRIPTION (continued)

Operation

In an error checking disabled access cycle, the operation is 24-bit long. The bits format is shown in Table 2.

A read operation composed of two 24-bit access cycles, the first one is a read command, and the second one is the requested data, the data format is shown in Table 3.

Daisy-Chain Operation

The SGM71622R8 family supports daisy-chain connection.

Frame Error Checking

This function can be enabled by settling CRC_EN bit in CONFIG register. The CRC check polynomial is 100000111. When the error checking is enabled, the serial interface access cycle is 32-bit long. The write and read operation sequence is as same as stand-alone operation, and the data format is shown in Table 4, Table 5 and Table 6.

The SGM71622R8 family calculates the CRC remainder on nCS rising edges. If no error occurs, the CRC remainder is zero and the data is accepted by the device.

After a write command, a second access can be used to check the error status (CRC_ERROR bit) on the SDO, shown by Table 6. Meanwhile, the SDO/nALARM pin can be configured as CRC alarm pin by setting ALM_EN = 1 and ALM_SEL= 0 in CONFIG register.

For a read operation, it must be followed by the second access to collect the data from the SDO pin, please find more details by Table 5.

Power-Down Mode

The SGM71622R8 family's DAC output amplifiers and internal reference can be powered down individually. All DAC output and internal reference are enabled by default when the chip is powered on. A DAC output is pulled to GND by a 1kΩ resistor internally when the channel is in power-down mode.

Table 2. Serial Interface Access Cycle

BITS	BIT NAME	DESCRIPTION
D[23]	RW	0 = Set a write operation 1 = Set a read operation
D[22:20]	Reserved	Reserved. All zeros.
D[19:16]	A[3:0]	Register Address (to be Read or Write).
D[15:0]	DI[15:0]	Data In a write operation, they are data to be written to the addressed chip register. In a read operation, they are invalid data.

Table 3. SDO Output Access Cycle

BITS	BIT NAME	DESCRIPTION
D[23]	RW	Repeat RW bit from Previous Access Cycle.
D[22:20]	Reserved	Reserved. All zeros.
D[19:16]	A[3:0]	Repeat Address from Previous Access Cycle.
D[15:0]	DO[15:0]	Data from Requested Register.

Table 4. Error Checking Serial Interface Access Cycle

BITS	BIT NAME	DESCRIPTION
D[31]	RW	0 = Set a write operation 1 = Set a read operation
D[30]	CRC_ERROR	Reserved. Set to 0.
D[29:28]	Reserved	Reserved. All zeros.
D[27:24]	A[3:0]	Register Address (to be Read or Write).
D[23:8]	DI[15:0]	Data Cycle In a write operation, they are data to be written to the addressed chip register. In a read operation, they are invalid data.
D[7:0]	CRC	8-Bit CRC Polynomial.

DETAILED DESCRIPTION (continued)

Table 5. Read Operation Error Checking Cycle

BITS	BIT NAME	DESCRIPTION
D[31]	RW	Repeat RW Bit from Previous Access Cycle. (RW = 1)
D[30]	CRC_ERROR	0 = No error 1 = A CRC error is existed
D[29:28]	Reserved	Reserved. All zeros.
D[27:24]	A[3:0]	Repeat Address from Previous Access Cycle.
D[23:8]	DO[15:0]	Data from Requested Register.
D[7:0]	CRC	Calculated CRC Value of Bits [31:8].

Table 6. Write Operation Error Checking Cycle

BITS	BIT NAME	DESCRIPTION
D[31]	RW	Repeat RW Bit from Previous Access Cycle. (RW = 0)
D[30]	CRC_ERROR	0 = No error 1 = A CRC error is existed
D[29:28]	Reserved	Reserved. All zeros.
D[27:24]	A[3:0]	Repeat Address from Previous Access Cycle.
D[23:8]	DO[15:0]	Data from Requested Register.
D[7:0]	CRC	Calculated CRC Value of Bits [31:8].

REGISTER MAPS

Bit Types:
R/W: Read/Write bit(s)
R: Read only bit(s)
W: Write only bit(s)

Table 7. Register Maps

Register	Address Bits				Data Bits																Type	Reset
	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
NOP	0	0	0	0	See Table 8																W	0000h
CHIP_ID	0	0	0	1	See Table 9																R	—
SYNC	0	0	1	0	See Table 10																R/W	FF00h
CONFIG	0	0	1	1	See Table 11																R/W	0000h
GAIN	0	1	0	0	See Table 12																R/W	0000h
TRIGGER	0	1	0	1	See Table 13																W	0000h
BRDCAST	0	1	1	0	BRDCAST_DATA[15:0], See Table 14																R/W	0000h
STATUS	0	1	1	1	See Table 15																R	0000h
DAC0	1	0	0	0	DAC0_DATA[15:0]																R/W	0000h
DAC1	1	0	0	1	DAC1_DATA[15:0]																R/W	0000h
DAC2	1	0	1	0	DAC2_DATA[15:0]																R/W	0000h
DAC3	1	0	1	1	DAC3_DATA[15:0]																R/W	0000h
DAC4	1	1	0	0	DAC4_DATA[15:0]																R/W	0000h
DAC5	1	1	0	1	DAC5_DATA[15:0]																R/W	0000h
DAC6	1	1	1	0	DAC6_DATA[15:0]																R/W	0000h
DAC7	1	1	1	1	DAC7_DATA[15:0]																R/W	0000h
All Others	—	—	—	—	Reserved																—	—

REGISTER MAPS (continued)

REG0x0: NOP Register [Reset = 0x0000]

Table 8. NOP Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	NOP[15:0]	0x0000	W	No Operation Write 0x0000 for proper no-operation command.

REG0x1: CHIP_ID Register [Reset = 0x08X6]

Table 9. CHIP_ID Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	
D[15:2]	CHIPID[13:0]	0	R	D[15]	Reserved.
		000		D[14:12]	Resolution 000 = 16-bit
		1000		D[11:8]	Channels 1000 = 8 channels
		x		D[7]	Reset 0 = SGM71622R8Z/SGM71622R8AZ/SGM71622R8BZ and SGM71622R8ZC/SGM71622R8AZC: reset to zero 1 = SGM71622R8M/SGM71622R8AM/SGM71622R8BM and SGM71622R8MC/SGM71622R8AMC: reset to mid-scale
		0 0101		D[6:2]	Reserved.
D[1:0]	VERSIONID[1:0]	10	R	Version ID Subject to change.	

REG0x2: SYNC Register [Reset = 0xFF00]

Table 10. SYNC Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	DAC7_BRDCAST_EN	1	R/W	0 = No response to broadcast command and keep unchanged 1 = Accept broadcast command
D[14]	DAC6_BRDCAST_EN	1	R/W	
D[13]	DAC5_BRDCAST_EN	1	R/W	
D[12]	DAC4_BRDCAST_EN	1	R/W	
D[11]	DAC3_BRDCAST_EN	1	R/W	
D[10]	DAC2_BRDCAST_EN	1	R/W	
D[9]	DAC1_BRDCAST_EN	1	R/W	
D[8]	DAC0_BRDCAST_EN	1	R/W	
D[7]	DAC7_SYNC_EN	0	R/W	0 = Asynchronous update mode, update at nCS rising edge 1 = Synchronous update mode, update at an LDAC trigger
D[6]	DAC6_SYNC_EN	0	R/W	
D[5]	DAC5_SYNC_EN	0	R/W	
D[4]	DAC4_SYNC_EN	0	R/W	
D[3]	DAC3_SYNC_EN	0	R/W	
D[2]	DAC2_SYNC_EN	0	R/W	
D[1]	DAC1_SYNC_EN	0	R/W	
D[0]	DAC0_SYNC_EN	0	R/W	

REGISTER MAPS (continued)

REG0x3: CONFIG Register [Reset = 0x0000]

Table 11. CONFIG Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:14]	Reserved	00		Reserved for factory use.
D[13]	ALM_SEL	0	R/W	ALARM Select 0 = nALARM pin is CRC_ERROR 1 = nALARM pin is REF_ALARM
D[12]	ALM_EN	0	R/W	Configure SDO/nALARM Pin 0 = Configure SDO/nALARM pin as a SDO pin 1 = Configure SDO/nALARM pin as an alarm pin
D[11]	CRC_EN	0	R/W	CRC Enable Bit 0 = Disable 1 = Enable CRC
D[10]	FSDO	0	R/W	Fast SDO Bit (Half-Cycle Speedup) 0 = SDO updates on an SCLK rising edge 1 = SDO updates a half-cycle earlier, during an SCLK falling edge
D[9]	DSDO	0	R/W	Disable SDO Bit 0 = SDO is driven while nCS is low, and tri-stated while nCS is high 1 = SDO is always tri-stated
D[8]	REF_PWDWN	0	R/W	0 = Enable internal reference 1 = Disable internal reference
D[7]	DAC7_PWDWN	0	R/W	0 = No power-down 1 = DAC channel is power-down
D[6]	DAC6_PWDWN	0	R/W	
D[5]	DAC5_PWDWN	0	R/W	
D[4]	DAC4_PWDWN	0	R/W	
D[3]	DAC3_PWDWN	0	R/W	
D[2]	DAC2_PWDWN	0	R/W	
D[1]	DAC1_PWDWN	0	R/W	
D[0]	DAC0_PWDWN	0	R/W	

REGISTER MAPS (continued)

REG0x4: GAIN Register [Reset = 0x0XXX]

Table 12. GAIN Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:11]	Reserved	0 0000		Reserved.
D[10]	Reserved/ CLR_4TO7_MSK (1)	0	R/W	SGM71622R8Z/SGM71622R8AZ/SGM71622R8BZ and SGM71622R8M/ SGM71622R8AM/SGM71622R8BM: Reserved. SGM71622R8ZC/SGM71622R8AZC and SGM71622R8MC/SGM71622R8AMC: 0 = Enable response to nCLR pin operation 1 = Disable response to nCLR pin operation
D[9]	Reserved/ CLR_0TO3_MSK (1)	0	R/W	SGM71622R8Z/SGM71622R8AZ/SGM71622R8BZ and SGM71622R8M/ SGM71622R8AM/SGM71622R8BM: Reserved. SGM71622R8ZC/SGM71622R8AZC and SGM71622R8MC/SGM71622R8AMC: 0 = Enable response to nCLR pin operation 1 = Disable response to nCLR pin operation
D[8]	REFDIV_EN	0/1	R/W	0 = Reference voltage is unaffected 1 = Reference voltage is internally divided by a factor of 2
D[7]	BUFF7_GAIN	0/1	R/W	0 = The buffer amplifier for corresponding DAC has a GAIN of 1 1 = The buffer amplifier for corresponding DAC has a GAIN of 2 (Default value for the SGM71622R8M/SGM71622R8AM/SGM71622R8BM devices is 1, and default value for the SGM71622R8Z/SGM71622R8AZ/SGM71622R8BZ devices is 0.)
D[6]	BUFF6_GAIN	0/1	R/W	
D[5]	BUFF5_GAIN	0/1	R/W	
D[4]	BUFF4_GAIN	0/1	R/W	
D[3]	BUFF3_GAIN	0/1	R/W	
D[2]	BUFF2_GAIN	0/1	R/W	
D[1]	BUFF1_GAIN	0/1	R/W	
D[0]	BUFF0_GAIN	0/1	R/W	

NOTE:

1. SGM71622R8ZC/SGM71622R8AZC and SGM71622R8MC/SGM71622R8AMC only. Reserved bits in SGM71622R8Z/ SGM71622R8AZ/SGM71622R8BZ and SGM71622R8M/SGM71622R8AM/SGM71622R8BM.

REG0x5: TRIGGER Register [Reset = 0x0000]

Table 13. TRIGGER Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:5]	Reserved	000 0000 0000		Reserved.
D[4]	LDAC	0	W	0 = Otherwise 1 = Synchronously load DAC
D[3:0]	SOFT_RESET[3:0]	0000	W	1010 = Reset chip to default state Others = Otherwise

REG0x6: BRDCAST Register [Reset = 0x0000]

Table 14. BRDCAST Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	BRDCAST_DATA[15:0]	0x0000	R/W	Broadcast Data Writing to this register issues a broadcast command. Data format is straight binary format. MSB is Data[15].

REGISTER MAPS (continued)

REG0x7: STATUS Register [Reset = 0x0000]

Table 15. STATUS Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:1]	Reserved	000 0000 0000 0000		Reserved.
D[0]	REF_ALM	0	R	Reference Alarm Bit 0 = Otherwise 1 = V_{DD} - V_{REF}/DIV < required minimum threshold

REG0x8 ~ REG0xF: DACx Register [Reset = 0x0000 or 0x8000]

Table 16. DACx Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:0]	DACx_DATA[15:0]	0x0000 (SGM71622R8Z/ SGM71622R8AZ//SGM71622R8BZ) or 0x8000 (SGM71622R8M/ SGM71622R8AM/SGM71622R8BM)	R/W	DACx Data Register Data format is straight binary format. MSB is Data[15].

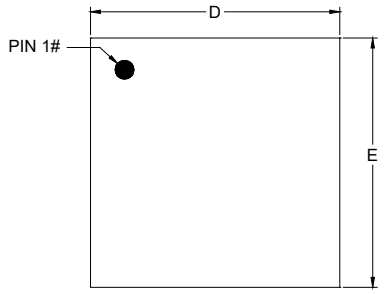
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

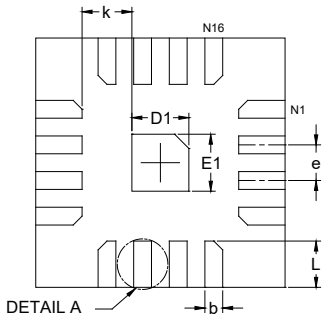
Changes from Original (JULY 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

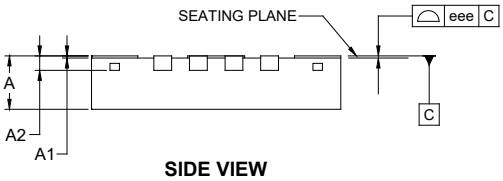
TQFN-3.5×3.5-16AL



TOP VIEW

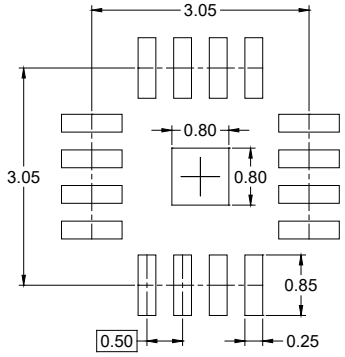


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



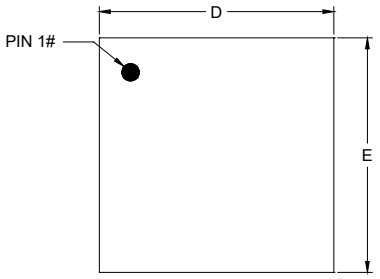
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	3.400	-	3.600
E	3.400	-	3.600
D1	0.700	-	0.900
E1	0.700	-	0.900
e	0.500 BSC		
k	0.700 REF		
L	0.550	-	0.750
eee	0.080		

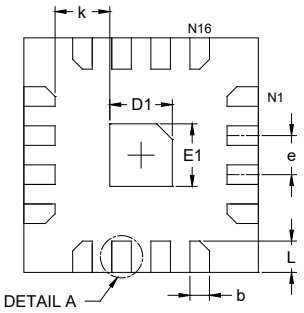
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

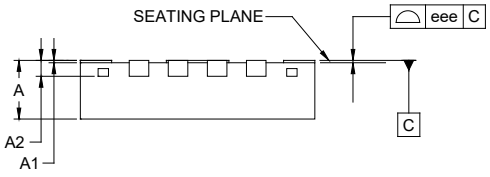
TQFN-3×3-16DL



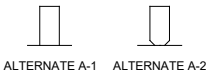
TOP VIEW



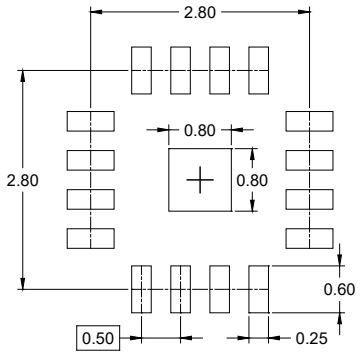
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



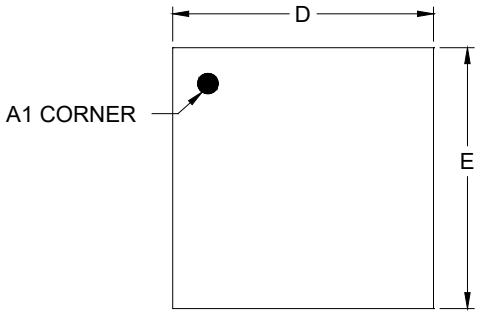
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	2.900	-	3.100
E	2.900	-	3.100
D1	0.700	-	0.900
E1	0.700	-	0.900
e		0.500 BSC	
k		0.700 REF	
L	0.300	-	0.500
eee		0.080	

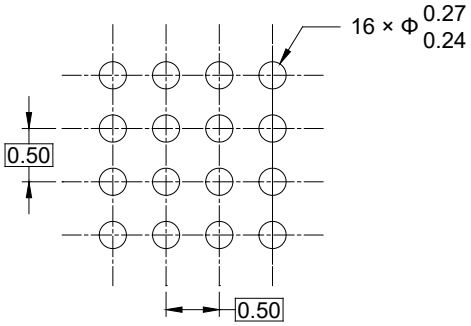
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

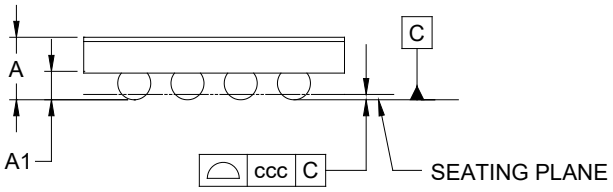
WLCSP-2.45×2.45-16B



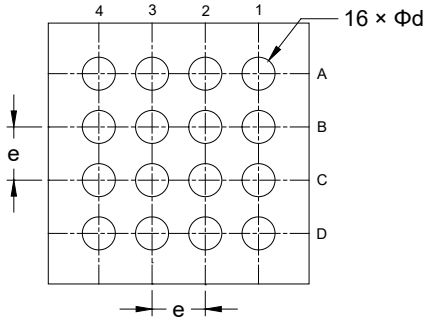
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



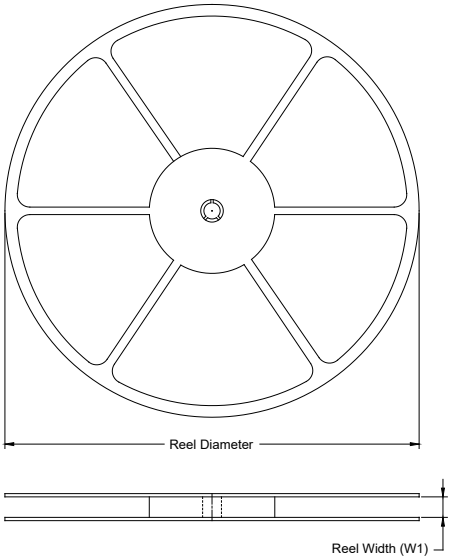
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.625
A1	0.231	-	0.271
D	2.420	-	2.480
E	2.420	-	2.480
d	0.280	-	0.340
e	0.500 BSC		
ccc	0.050		

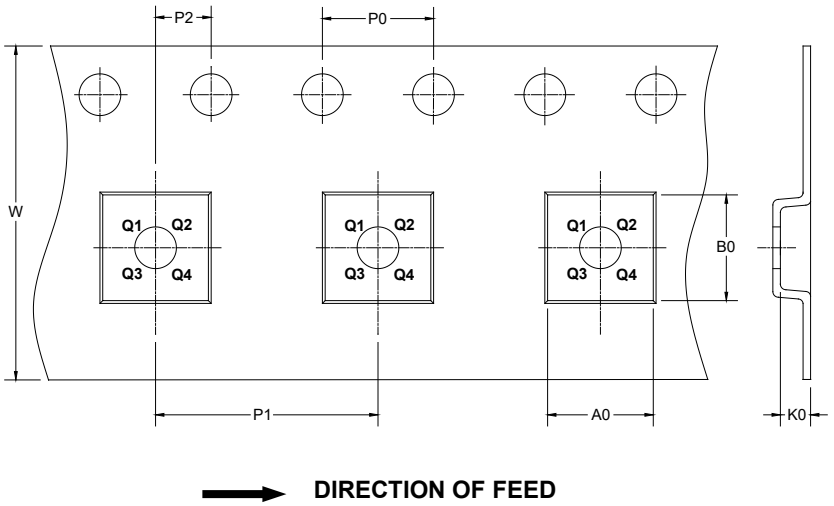
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



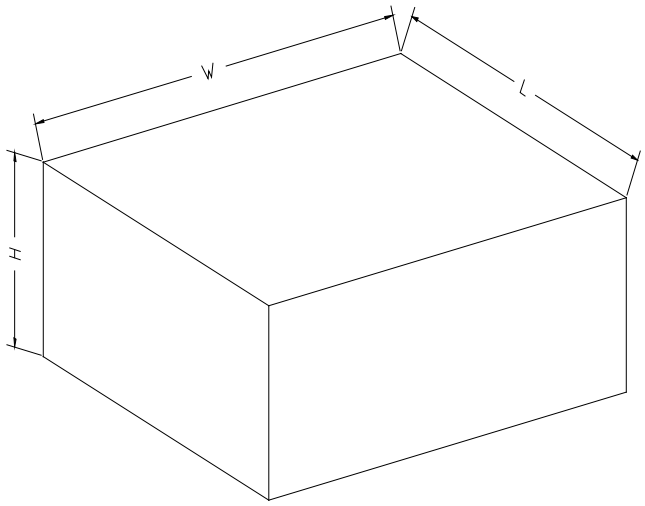
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3.5×3.5-16AL	13″	12.4	3.80	3.80	1.00	4.0	8.0	2.0	12.0	Q2
TQFN-3×3-16DL	13″	12.4	3.30	3.30	1.05	4.0	8.0	2.0	12.0	Q2
WLCSP-2.45×2.45-16B	13″	12.4	2.72	2.72	0.73	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002