# SGM41543/SGM41543D
# High Input Voltage, 3.78A Single-Cell Battery Charger with NVDC Power Path Management

## FEATURES

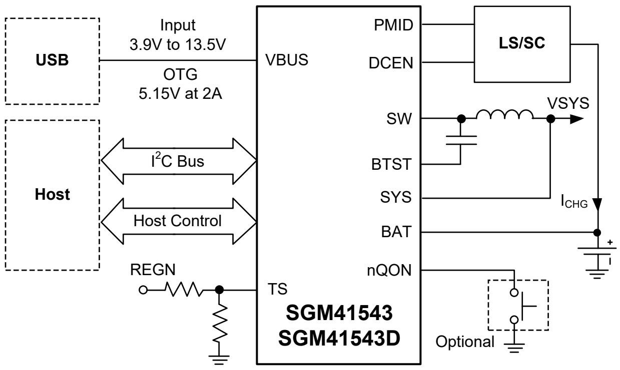
- High Efficiency, 1.5MHz, Synchronous Buck Charger
  - 94% Charge Efficiency at 1A from 5V Input
  - 91% Charge Efficiency at 2A from 9V Input
  - Optimized for USB Voltage Input (5V)
  - Selectable PFM Mode for Light Load Efficiency
- USB On-The-Go (OTG) Support (Boost Mode)
  - Boost Converter with up to 2A Output
  - Boost Efficiency of 94.8% at 0.5A and 94.5% at 1A
  - Accurate Hiccup Mode Over-Current Protection
  - Output Short Circuit Protection
  - Selectable PFM Mode for Light Load Operations
- Single Input for USB or High Voltage Adaptors
  - 3.9V to 13.5V Operating Input Voltage Range
  - 22V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit and Dynamic Power Management (IINDPM, 100mA to 3.1A with 100mA Resolution & 3.8A) to Support USB 2.0 and USB 3.0 Standards and High Voltage Adaptors
  - Maximum Power Tracking by Programmable Input Voltage Limit (VINDPM) with Selectable Offset
  - VINDPM Tracking of Battery Voltage
  - Auto Detect USB BC1.2, SDP, CDP, DCP and Non-Standard Adaptors
- High Battery Discharge Efficiency with 16mΩ Switch
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with No or Highly Depleted Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Ship Mode, Wake-Up and Full System Reset Capability by Battery FET Control
- Flexible Autonomous and $I^2C$ Operation Modes for Optimal System Performance
- Fully Integrated Switches, Current Sense and Compensation
- External Direct Charging Path Enable Output
- 8μA Ship Mode Low Battery Leakage Current
- High Accuracy
  - ±0.5% Charge Voltage Regulation (8mV/Step)
  - ±5% Charge Current Regulation at 1.5A
  - ±10% Input Current Regulation at 0.9A
- Safety
  - Battery Temperature Sensing (Charge/Boost Modes)
  - Thermal Regulation and Thermal Shutdown
  - Input Under-Voltage Lockout (UVLO)
  - Input Over-Voltage (ACOV) Protection

## APPLICATIONS

Smart Phones, EPOS

Portable Internet Devices and Accessory

## SIMPLIFIED SCHEMATIC



## GENERAL DESCRIPTION

The SGM41543/SGM41543D are battery chargers and system power path management devices with integrated converter and power switches for using with single-cell Li-Ion or Li-polymer batteries. This highly integrated 3.78A device is capable of fast charging and supports a wide input voltage range suitable for smart phones, tablets and portable systems. $I^2C$ programming makes it a very flexible powering and charger design solution.

The devices include four main power switches: input reverse blocking FET (RBFET, Q1), high-side switching FET for Buck or Boost mode (HSFET, Q2), low-side switching FET for Buck or Boost mode (LSFET, Q3) and battery FET that controls the interconnection of the system and battery (BATFET, Q4). The bootstrap diode for the high-side gate driving is also integrated. The internal power path has a very low impedance that reduces the charging time and maximizes the battery discharge efficiency. Moreover, the input voltage and current regulations provide maximum charging power delivery to the battery with various types of input sources.

A wide range of input sources are supported, including standard USB hosts, charging ports and USB compliant high voltage adaptors. The default input current limit is automatically selected based on the built-in USB interface. This limit is determined by the detection circuit in the system (e.g. USB PHY). SGM41543/SGM41543D are USB 2.0 and USB 3.0 power specifications compliant with input current and voltage regulation. It also meets USB On-The-Go (OTG) power rating specification and is capable of boosting the battery voltage to supply 5.15V on VBUS with 2A (or 1.2A) current limit.

The system voltage is regulated slightly above the battery voltage by the power path management circuit and is kept above the programmable minimum system voltage (3.5V by default). Therefore, system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the power path management provides the deficit from battery by discharging battery to the system until the system power demand is fulfilled. This is called supplement mode, which prevents the input source from overloading.

Starting and termination of a charging cycle can be accomplished without software control. The sensed battery voltage is used to decide for starting phase of charging in one of the three phases of charging cycle: pre-conditioning, constant current or constant voltage. When the charge current falls below a preset limit and the battery voltage is above recharge threshold, the charger function will automatically terminate and end the charging cycle. If the voltage of a charged battery falls below the recharge threshold, the charger begins another charging cycle.

Several safety features are provided in the SGM41543/ SGM41543D such as over-voltage and over-current protections, battery temperature monitoring, charging safety timing, thermal shutdown and input UVLO. TS pin is connected to an NTC thermistor for battery temperature monitoring and protection in both charge and Boost modes according to JEITA profile. This device also features thermal regulation in which the charge current is reduced, if the junction temperature exceeds 80℃ or 120℃ (selectable).

Charging status is reported by the STAT output and fault/status bits. A negative pulse is sent to the nINT output pin as soon as a fault occurs to notify the host. BATFET reset control is provided by nQON pin to exit ship mode or for a full system reset.

The devices supply a DCEN signal to control an external P-MOSFET or load switch as a direct charging path for low voltage PMID, or to control a 2:1 switching capacitor divider for high voltage PMID.

The SGM41543/SGM41543D are available in a Green TQFN-4×4-24L package.

## PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM41543 | TQFN-4×4-24L | -40℃ to +85℃ | SGM41543YTQF24G/TR | SGM41543<br>YTQF24<br>XXXXX | Tape and Reel, 3000 |
| SGM41543D | TQFN-4×4-24L | -40℃ to +85℃ | SGM41543DYTQF24G/TR | SGMMCC<br>YTQF24<br>XXXXX | Tape and Reel, 3000 |

### MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

**X X X X X**

- Vendor Code
- Trace Code
- Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VAC, VBUS (Converter Not Switching)............-2V to 22V [1]
- BTST, PMID (Converter Not Switching)........... -0.3V to 22V
- SW ...................................................................... -2V to 16V
- SW (Peak for 10ns Duration).............................. -3V to 16V
- BTST to SW ....................................................... -0.3V to 6V
- D+, D- ............................................................... -0.3V to 6V
- REGN, TS, nCE, BAT, SYS (Converter Not Switching) ........................................................................... -0.3V to 6V
- SDA, SCL, nINT, nQON, STAT, DCEN ............. -0.3V to 6V

Output Sink Current
- STAT.............................................................................6mA
- nINT ..............................................................................6mA

Package Thermal Resistance
- TQFN-4×4-24L, $\theta_{JA}$ .................................................. 35℃/W
- TQFN-4×4-24L, $\theta_{JB}$ .................................................. 10℃/W
- TQFN-4×4-24L, $\theta_{JC}$ .................................................. 16℃/W

Junction Temperature................................................+150℃
Storage Temperature Range ........................-65℃ to +150℃
Lead Temperature (Soldering, 10s)............................+260℃
ESD Susceptibility
HBM.............................................................................2000V
CDM ............................................................................1000V

NOTE: 1. Maximum 28V for 10 seconds.

## RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, $V_{VBUS}$.............................. 3.9V to 13.5V
Input Current (VBUS), $I_{IN}$.................................... 3.8A (MAX)
Output DC Current (SW), $I_{SWOP}$ ............................. 5A (MAX)
Battery Voltage, $V_{BATOP}$ .................................. 4.624V (MAX)
Fast Charging Current, $I_{CHGOP}$ .......................... 3.78A (MAX)
Discharging Current (Continuous), $I_{BATOP}$............... 6A (MAX)
Ambient Temperature Range ......................... -40℃ to +85℃
Junction Temperature Range....................... -40℃ to +125℃

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

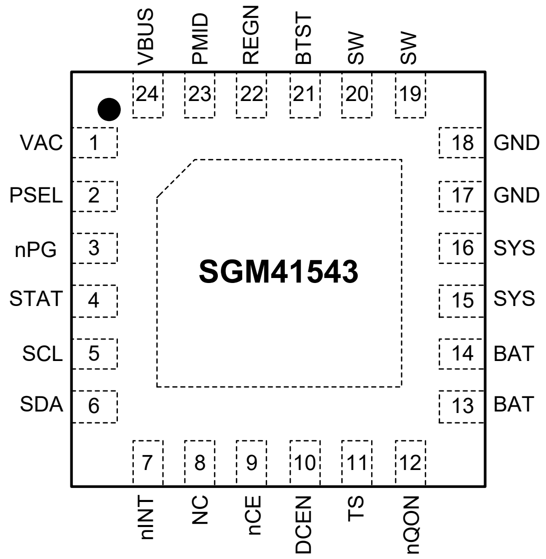
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

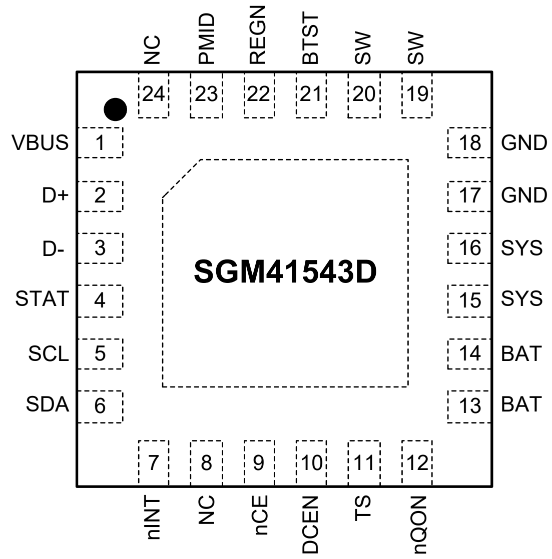
# PIN CONFIGURATIONS

**SGM41543 (TOP VIEW)**




**TQFN-4×4-24L**

**SGM41543D (TOP VIEW)**




**TQFN-4×4-24L**

# PIN DESCRIPTION

| PIN | | NAME | TYPE [1] | FUNCTION |
|---|---|---|---|---|
| SGM 41543 | SGM 41543D | | | |
| 1 | — | VAC | AI | Sense Input for DC Input Voltage (Typically from an AC/DC Adaptor). It must be connected to VBUS pin. (SGM41543 only) |
| 2 | — | PSEL | DI | Power Source Selection Input. If PSEL is pulled high, the input current limit is set to 500mA (USB 2.0) and if it is pulled low, the limit is set to 2.4A (adaptor). When the $I^2C$ link to the host is established, the host can program a different input current limit value by writing to the IINDPM[4:0] register. (SGM41543 only) |
| — | 2 | D+ | AIO | Positive USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DP_VSET[1:0]. (SGM41543D only) |
| 3 | — | nPG | DO | Open-Drain Active Low Input Power Good Indicator. Use a 10kΩ pull-up to the logic high rail. A low state indicates a good input ($V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$, $V_{VBUS}$ is above sleep mode threshold, and $V_{VBUS} > V_{VBUSMIN}$ when $I_{BAD\_SRC}$ = 25mA). (SGM41543 only) |
| — | 3 | D- | AIO | Negative USB Data Line. D+/D- based USB device protocol detection and voltage of this pin can be set by DM_VSET[1:0]. (SGM41543D only) |
| 4 | 4 | STAT | DO | Open-Drain Charge Status Output. Use a 10kΩ pull-up to the logic high rail (or an LED + a resistor). The STAT pin acts as follows:<br>During charge: low (LED ON).<br>Charge completed or charger in sleep mode: high (LED OFF).<br>Charge suspended (in response to a fault): 1Hz, 50% duty cycle pulses (LED BLINKS).<br>The function can be disabled via EN_ICHG_MON[1:0] register. |
| 5 | 5 | SCL | DI | $I^2C$ Clock Signal. Use a 10kΩ pull-up to the logic high rail. |
| 6 | 6 | SDA | DIO | $I^2C$ Data Signal. Use a 10kΩ pull-up to the logic high rail. |
| 7 | 7 | nINT | DO | Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform host about a new charger status update or a fault. |
| 8 | 8, 24 | NC | — | Do Not Connect and Leave This Pin Floating. |

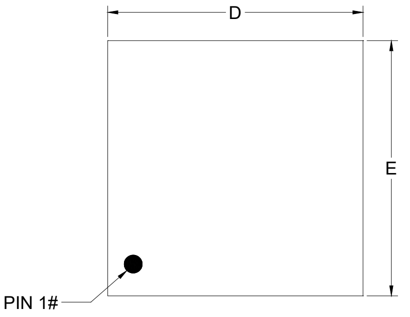
# PIN DESCRIPTION (continued)

| PIN | | NAME | TYPE [1] | FUNCTION |
|---|---|---|---|---|
| SGM 41543 | SGM 41543D | | | |
| 9 | 9 | nCE | DI | Charge Enable Input Pin (Active Low). Battery charging is enabled when CHG_CONFIG bit is 1 and nCE pin is pulled low. |
| 10 | 10 | DCEN | — | External Direct Charge Enable Pin. This pin can be set high to enable an external direct charging device. |
| 11 | 11 | TS | AI | Temperature Sense Input Pin. Connect to the battery NTC thermistor that is grounded on the other side. To program operating temperature window, it can be biased by a resistor divider between REGN and GND. Charge suspends if TS voltage goes out of the programmed range. It is recommended to use a 103AT-2 type thermistor.<br>If NTC or TS pin function is not needed, use a 10kΩ/10kΩ pair for the resistor divider. |
| 12 | 12 | nQON | DI | BATFET On/Off Control Input. Use an internal pull-up to a small voltage for maintaining the default high logic (whenever a source or battery is available). In the ship mode, the BATFET is off. To exit ship mode and turn BATFET on, a logic low pulse with a duration of $t_{SHIPMODE}$ (1s TYP) can be applied to nQON. When VBUS source is not connected, a logic low pulse with a duration of $t_{QON\_RST}$ (10s TYP) resets the system power (SYS) by turning BATFET off for $t_{BATFET\_RST}$ (320ms TYP) and then goes back to provide a full power reset for system. |
| 13, 14 | 13, 14 | BAT | P | Battery Positive Terminal Pin. Use a 10μF capacitor between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability. |
| 15, 16 | 15, 16 | SYS | P | Connection Point to Converter Output. SYS is connected to the converter LC filter output that powers the system. BAT to SYS internal current (power from battery to system) is sensed. Connect a 20μF capacitor between SYS pin and GND close to the device. |
| 17, 18 | 17, 18 | GND | — | Ground Pin of the Device. |
| 19, 20 | 19, 20 | SW | P | Switching Node Output. Connect SW pin to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BTST pin. |
| 21 | 21 | BTST | P | High-side Driver Positive Supply. It is internally connected to the boost-strap diode cathode. Use a 47nF ceramic capacitor from SW pin to BTST pin. |
| 22 | 22 | REGN | P | LDO Output that Powers LSFET Driver and Internal Circuits. Internally, the REGN pin is connected to the anode of the bootstrap diode. Place a 4.7μF (10V rating) ceramic capacitor between REGN pin and GND. It is recommended to place the capacitor close to the REGN pin. |
| 23 | 23 | PMID | P | PMID Pin. PMID is the actual higher voltage port of converter (Buck or Boost) and is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect a 22μF ceramic capacitor from PMID pin to GND. It is the proper point for decoupling of high frequency switching currents. |
| 24 | 1 | VBUS | P | Charger Input ($V_{IN}$). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS pin to GND close to the device. For SGM41543, this pin senses the input voltage. |
| Exposed Pad | Exposed Pad | — | P | Thermal Pad and Ground Reference. It is the ground reference for the device and also the thermal pad to conduct heat from the device (not suitable for high current return). Tie it externally to the PCB ground plane (GND). Thermal vias under the pad are needed to conduct the heat to the PCB ground planes. |

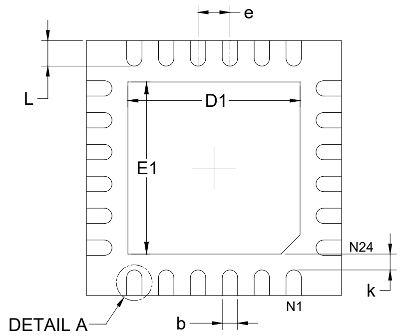
NOTE:
1. AI = Analog Input, AO = Analog Output, AIO = Analog Input and Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input and Output, P = Power.

# PACKAGE OUTLINE DIMENSIONS

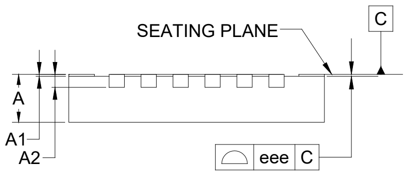
## TQFN-4×4-24L



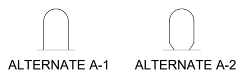

**TOP VIEW**



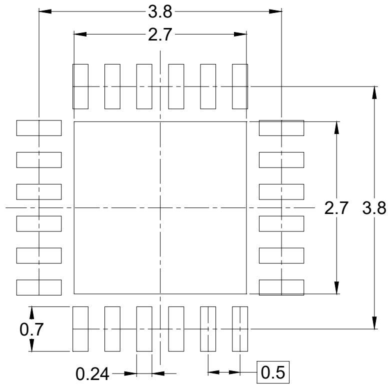

**BOTTOM VIEW**




**SIDE VIEW**




**DETAIL A**
ALTERNATE TERMINAL
CONSTRUCTION



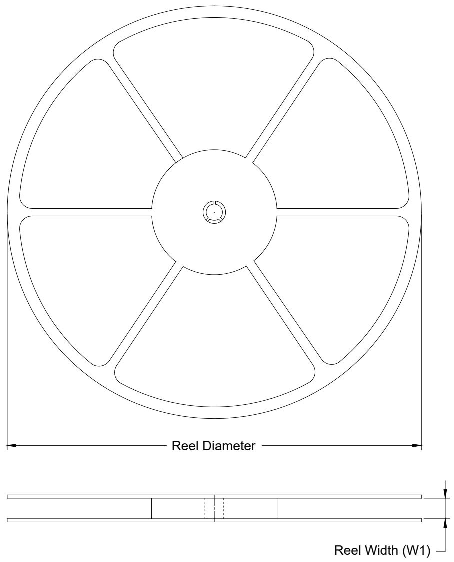

**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | **MIN** | **MOD** | **MAX** |
| A | 0.700 | - | 0.800 |
| A1 | 0.000 | - | 0.050 |
| A2 | 0.203 REF | | |
| b | 0.180 | - | 0.300 |
| D | 3.900 | - | 4.100 |
| E | 3.900 | - | 4.100 |
| D1 | 2.600 | - | 2.800 |
| E1 | 2.600 | - | 2.800 |
| e | 0.500 BSC | | |
| k | 0.200 MIN | | |
| L | 0.300 | - | 0.500 |
| eee | 0.080 | | |

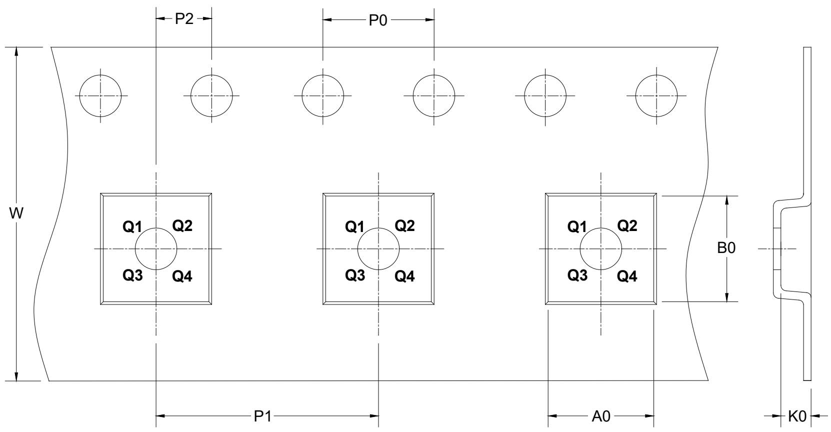
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS




**DIRECTION OF FEED**

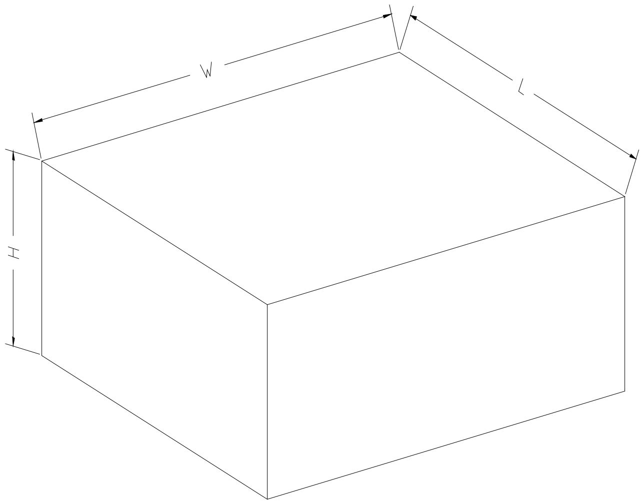
NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| TQFN-4×4-24L | 13″ | 12.4 | 4.30 | 4.30 | 1.10 | 4.0 | 8.0 | 2.0 | 12.0 | Q2 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002