SGM12213A
SP3T MIPI RFFE High Power Switch

GENERAL DESCRIPTION

The SGM12213A is a single-pole/three-throw (SP3T) switch, which supports a wide operating frequency from 0.4GHz to 5.8GHz. The device provides low insertion loss and high isolation performance. These specifications make the device appropriate for 2G/3G/4G/5G applications, which need high power processing and high linearity.

No external DC blocking capacitors are required on the RF paths as long as no external DC voltage is applied, which can save PCB area and cost.

The SGM12213A is available in a Green ULGA-1.1×1.1-9L package.

APPLICATIONS

2G/3G/4G/5G Applications

FEATURES

- **Operating Frequency Range: 0.4GHz to 5.8GHz**
- **Low Insertion Loss**
- **High Isolation**
- **MIPI RFFE V2.1 Interface Compatible**
- **Input 0.1dB Compression Point: 40dBm**
- **Capable of 1.8V Operation**
- **No External DC Blocking Capacitors Required**
- **The ID Pin to Control Two Devices on the Same RFFE Bus with Separate Product ID's**
- **Available in a Green ULGA-1.1×1.1-9L Package**

BLOCK DIAGRAM

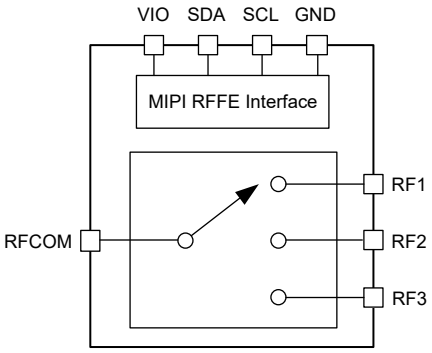


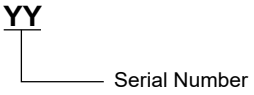
Figure 1. SGM12213A Block Diagram

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM12213A	ULGA-1.1×1.1-9L	-40℃ to +85℃	SGM12213AYULA9G/TR	2R	Tape and Reel, 3000

MARKING INFORMATION

NOTE: Fixed character for 2R.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{IO} 2.5V
SDA, SCL Control Voltage 2.5V
Maximum Power Handling .....
..... 40dBm (1:1 VSWR, +90℃, 25% DC)
Junction Temperature ..... +150℃
Storage Temperature Range ..... -55℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 2000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃
Supply Voltage, V_{IO} ..... 1.65V to 1.95V
SDA Logic Output Low Voltage ..... 0V to (0.2 × V_{IO})
SDA Logic Output High Voltage..... (0.8 × V_{IO}) to V_{IO}
SDA, SCL Logic High Current..... 0.1μA to 5μA

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

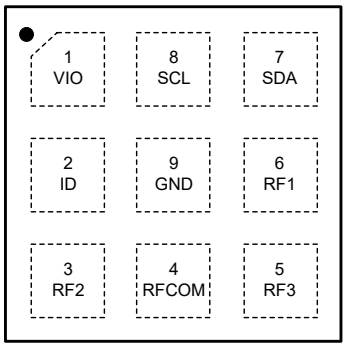
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



ULGA-1.1×1.1-9L

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	VIO	Supply Voltage.
2	ID	Product ID.
3	RF2	RF Port 2.
4	RFCOM	RF Common Port.
5	RF3	RF Port 3.
6	RF1	RF Port 1.
7	SDA	RFFE Data Signal.
8	SCL	RFFE Clock Signal.
9	GND	Ground.

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{IO} = 1.65V to 1.95V, typical values are at V_{IO} = 1.8V, input and output resistance = 50Ω, SDA/SCL = 1.8V/0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Characteristics						
Supply Voltage	V_{IO}		1.65	1.8	1.95	V
Supply Current	I_{VIO}	Active mode		60	100	μA
		Low power mode		5	10	
Turn-On Time	t_{ON}	50% V_{DD} to 90% RF			30	μs
RF Path Switching Time	t_{SW}	Switching CMD 50% SCL to 90%/10% RF		1	2	μs
Wake Up Time	t_{WK}	End of low power state 50% SCL to 90% RF		10	15	μs
VIO Reset Time	t_{RST}	VIO off to it starts to re-power up	10			μs
RF Characteristics						
Insertion Loss (RF1/RF2/RF3 to RFCOM)	IL	f_0 = 0.4GHz to 1.0GHz		0.34	0.52	dB
		f_0 = 1.0GHz to 2.0GHz		0.40	0.64	
		f_0 = 2.0GHz to 2.7GHz		0.48	0.73	
		f_0 = 3.0GHz to 3.8GHz		0.51	0.81	
		f_0 = 4.8GHz to 5.8GHz		0.64	1.09	
Isolation (RF1/RF2/RF3 to RFCOM)	ISO	f_0 = 0.4GHz to 1.0GHz	32	42		dB
		f_0 = 1.0GHz to 2.0GHz	25	35		
		f_0 = 2.0GHz to 2.7GHz	22	30		
		f_0 = 3.0GHz to 3.8GHz	17	25		
		f_0 = 4.8GHz to 5.8GHz	15	23		
2nd Harmonics (RF1/RF2/RF3 to RFCOM)	$2f_0$	f_0 = 900MHz, P_{IN} = 26dBm		-101	-95	dBc
		f_0 = 900MHz, P_{IN} = 35dBm		-90	-86	
		f_0 = 1900MHz, P_{IN} = 32dBm		-93	-80	
3rd Harmonics (RF1/RF2/RF3 to RFCOM)	$3f_0$	f_0 = 900MHz, P_{IN} = 26dBm		-96	-94	dBc
		f_0 = 900MHz, P_{IN} = 35dBm		-80	-75	
		f_0 = 1900MHz, P_{IN} = 32dBm		-93	-85	
Input Return Loss (RFCOM to RF1/RF2/RF3)	RL	f_0 = 0.4GHz to 2.7GHz		22		dB
		f_0 = 2.7GHz to 5.8GHz		17		
Input 0.1dB Compression Point (RFCOM to RF1/RF2/RF3)	$P_{0.1dB}$	f_0 = 0.4GHz to 2.7GHz, CW		40		dBm
		f_0 = 3.0GHz to 5.8GHz, CW		38		
2nd Order Intermodulation	IMD2	f_0 = 836.5MHz, P_{IN} = 20dBm f_1 = 1718MHz, P_{IN} = 20dBm		90		dBc
3rd Order Intermodulation	IMD3	f_0 = 836.5MHz, P_{IN} = 20dBm f_1 = 791.5MHz, P_{IN} = 20dBm		88		dBc
		f_0 = 1760MHz, P_{IN} = 20dBm f_1 = 1950MHz, P_{IN} = 20dBm		88		
		f_0 = 2535MHz, P_{IN} = 20dBm f_1 = 2415MHz, P_{IN} = 20dBm		86		

MIPI RFFE READ AND WRITE TIMING

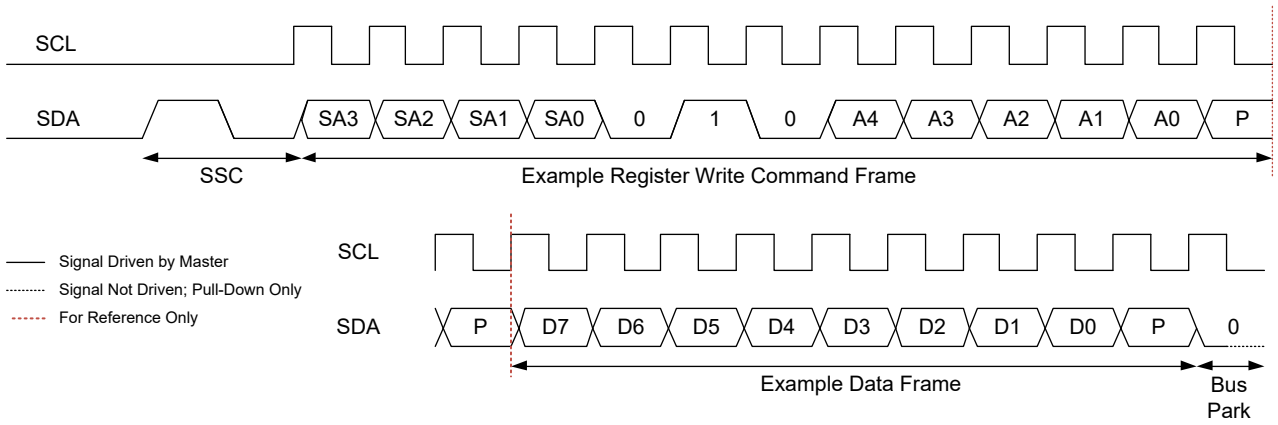


Figure 2. Register Write Command Timing Diagram

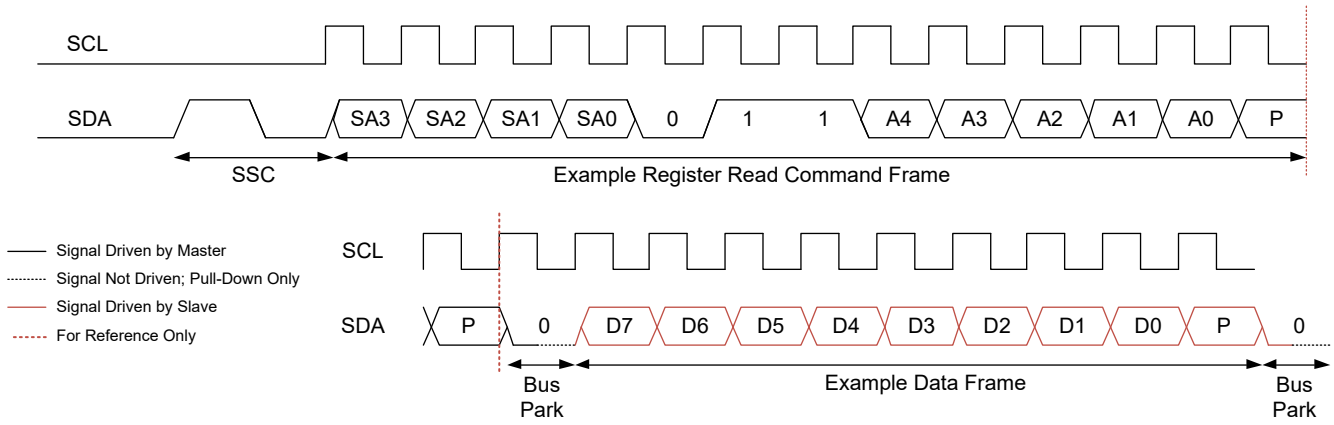


Figure 3. Register Read Command Timing Diagram

COMMAND SEQUENCE BIT DEFINITIONS

Type	SSC	Command Frame Bits					Parity Bits	Bus Park Cycle	Extended Operation					
		C[11:8]	C[7]	C[6:5]	C[4]	C[3:0]			Data Frame Bits	Parity Bits	Bus Park Cycle	Data Frame Bits	Parity Bits	Bus Park Cycle
Reg Write	Y	SA[3:0]	0	10	A[4]	A[3:0]	Y	-	D[7:0]	Y	Y	-	-	-
Reg Read	Y	SA[3:0]	0	11	A[4]	A[3:0]	Y	Y	D[7:0]	Y	Y	-	-	-
Reg0 Write	Y	SA[3:0]	1	D[6:5]	D[4]	D[3:0]	Y	Y	-	-	-	-	-	-

Legends:

SSC = Sequence Start Command

SA = Slave Address

A = Register Address

D = Data Bit

REGISTER MAPS

SW_CTRL0

Register Address: 0x00; R/W

Table 1. SW_CTRL0 Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:4]	Reserved	Reserved.	0000	R/W	No	0, 1, 2
D[3:0]	SW_CTRL	0000: Isolation 0001: RF1 - RFCOM 0100: RF3 - RFCOM 1000: RF2 - RFCOM	0000	R/W	No	0, 1, 2

SPARE

Register Address: 0x01; R/W

Table 2. SPARE Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	Reserved	Reserved.	00000000	R/W	No	0, 1, 2

RFFE_STATUS

Register Address: 0x1A; R/W

Table 3. RFFE_STATUS Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7]	UDR_RST	0: Normal 1: Software reset During software reset, this register and all configurable registers are set to their default values except for reserved registers.	0	R/W	No	No
D[6]	COMMAND_FRAME_ PARITY_ERR	Command frame parity error.	0	R/W	No	No
D[5]	COMMAND_LENGTH_ERR	Command length error.	0	R/W	No	No
D[4]	ADDRESS_FRAME_ PARITY_ERR	Address frame parity error.	0	R/W	No	No
D[3]	DATA_FRAME_PARITY_ ERR	Data frame parity error.	0	R/W	No	No
D[2]	RD_IVD_ADD	Read command to an invalid address.	0	R/W	No	No
D[1]	WR_IVD_ADD	Write command to an invalid address.	0	R/W	No	No
D[0]	BID_GID_ERR	Read command with a BROADCAST_ID or GSID. When this register is read, it will be reset.	0	R/W	No	No

GROUP_SID

Register Address: 0x1B; R and R/W

Table 4. GROUP_SID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:4]	Reserved	Reserved.	0000	R	No	No
D[3:0]	GSID	Group slave ID.	0000	R/W	No	No

REGISTER MAPS (continued)

PM_TRIG

Register Address: 0x1C; R/W and W

Table 5. PM_TRIG Register Details

Bits	Bit Name	Description		Default	Type	B/G	Trig
D[7:6]	PWR_MODE[1:0]	00: Active - Normal 01: Startup - All registers are set to the default value 10: Active - Low power condition - All ports in isolation 11: Startup - All registers are set to the default value		00	R/W	Yes	No
D[5]	TRIGGER_MASK_2	0: TRIGGER_2 enabled 1: TRIGGER_2 disabled	If any one of the three TRIGGER_MASK_x is set to logic '1', the corresponding trigger is disabled, in that case data written to a register associated with the trigger goes directly to the destination register. Otherwise, if the TRIGGER_MASK_x is set to logic '0', incoming data is written to the shadow register, and the destination register is unchanged until its corresponding trigger is asserted.	0	R/W	No	No
D[4]	TRIGGER_MASK_1	0: TRIGGER_1 enabled 1: TRIGGER_1 disabled		0	R/W	No	No
D[3]	TRIGGER_MASK_0	0: TRIGGER_0 enabled 1: TRIGGER_0 disabled		0	R/W	No	No
D[2]	TRIGGER_2	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_2 is set to logic '0'		0	W	Yes	No
D[1]	TRIGGER_1	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_1 is set to logic '0'		0	W	Yes	No
D[0]	TRIGGER_0	0: Keep its associated destination registers unchanged 1: Load its associated destination registers with the data in the parallel shadow register, provided TRIGGER_MASK_0 is set to logic '0'		0	W	Yes	No

PRODUCT_ID

Register Address: 0x1D; R

Table 6. PRODUCT_ID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	PRODUCT_ID	Product number. This value will be defined when the bias voltage of the ID pin changes. GND to set to 00000110, VIO voltage for 00000111.	00000111 or 00000110	R	No	No

MANUFACTURER_ID

Register Address: 0x1E; R

Table 7. MANUFACTURER_ID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:0]	MANUFACTURER_ID[7:0]	Lower eight bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	01001010	R	No	No

MAN_USID

Register Address: 0x1F; R and R/W

Table 8. MAN_USID Register Details

Bits	Bit Name	Description	Default	Type	B/G	Trig
D[7:6]	Reserved	Reserved.	00	R	No	No
D[5:4]	MANUFACTURER_ID[9:8]	Upper two bits of Manufacturer ID. Read-only. Note that during USID programming, the write command sequence is executed on the register, but the value does not change.	00	R	No	No
D[3:0]	USID	Unique slave identifier.	1011	R/W	No	No

POWER ON AND OFF SEQUENCE

Once the VIO voltage drops to 0V, the VIO waits at least 10μs before repowering (see Figure 4).

In order to ensure the correct data transmission, SDA/SCL must be sent after VIO has been applied at least 120ns. There must be at least 15μs to apply RF power after VIO has been applied. Wait a minimum of typically 10μs after RFFE bus is idle to apply an RF signal (see Figure 5).

Do not apply RF power during switching. To ensure this, the RF power needs to be removed before the register write operation that changes the switching mode is completed (see Figure 6).

When the low power mode is used, a delay time of 10μs is required to exit the low power mode (see Figure 7).

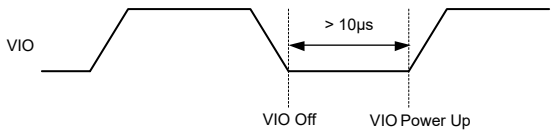


Figure 4. Digital Supply Detail

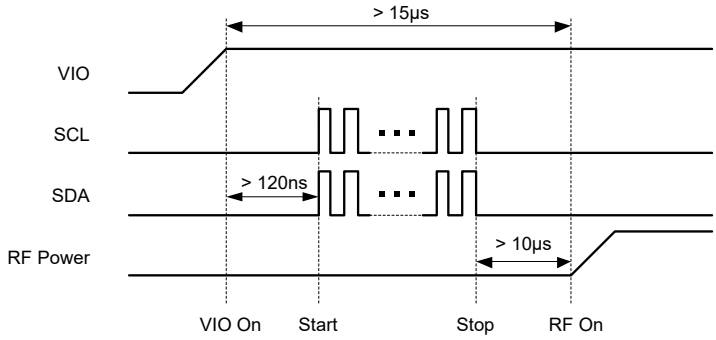


Figure 5. Digital Signal/RF Power-On Detail

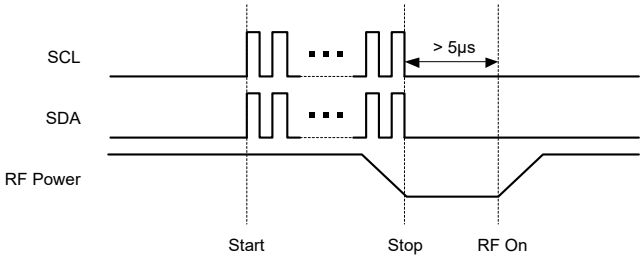


Figure 6. Switch Event Timing

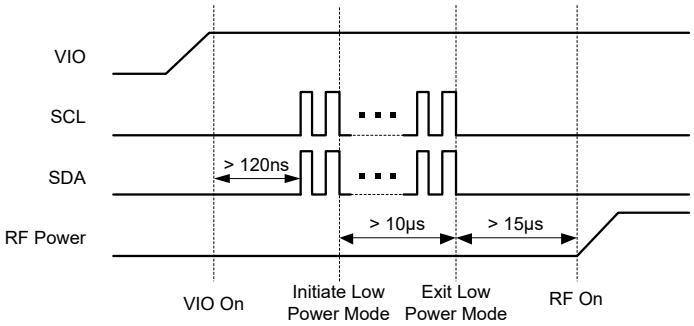
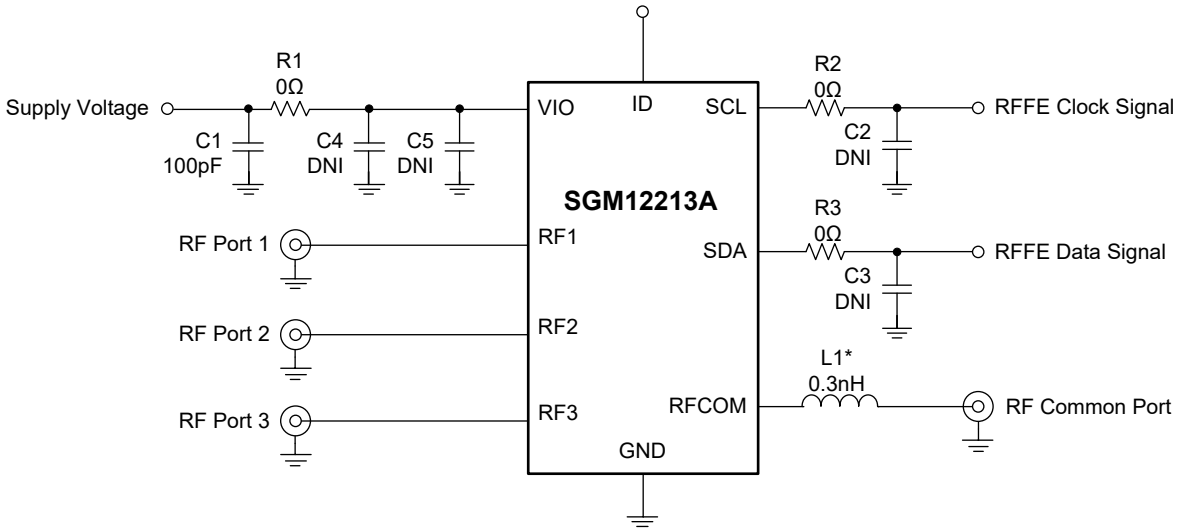


Figure 7. Low Power Mode Exit Timing

TYPICAL APPLICATION CIRCUIT



NOTE: * Matching for optimized RF performance, it may be changed according to different applications.

Figure 8. SGM12213A Typical Application Circuit

EVALUATION BOARD LAYOUT

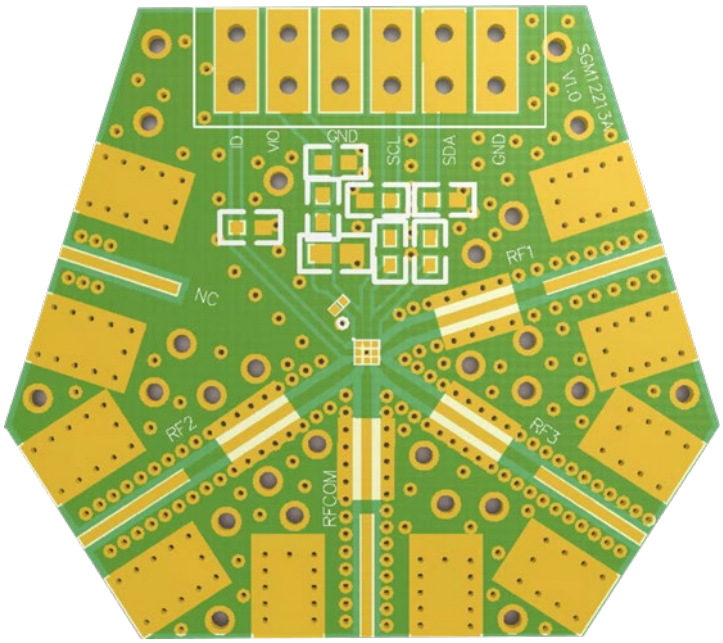


Figure 9. SGM12213A Evaluation Board Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

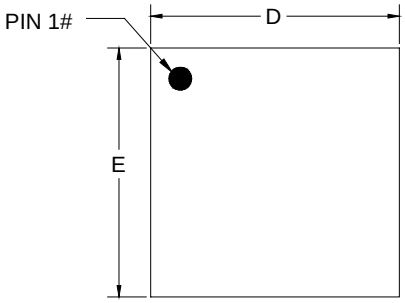
APRIL 2024 – REV.A.1 to REV.A.2	Page
Updated ESD Susceptibility	2

DECEMBER 2022 – REV.A to REV.A.1	Page
Updated Electrical Characteristics	4

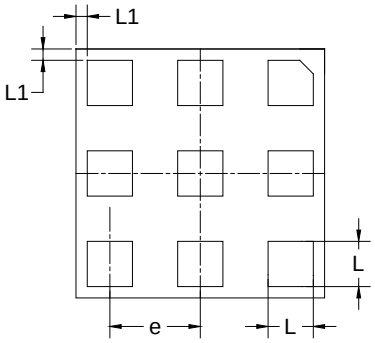
Changes from Original (JUNE 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

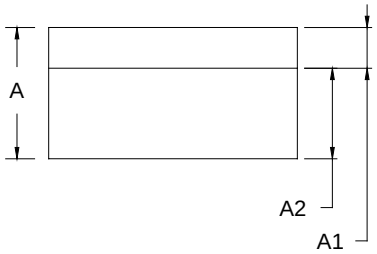
ULGA-1.1×1.1-9L



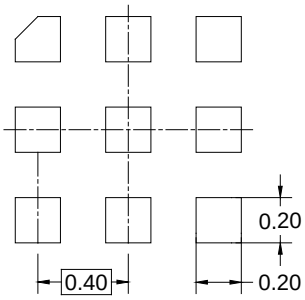
TOP VIEW



BOTTOM VIEW



SIDE VIEW



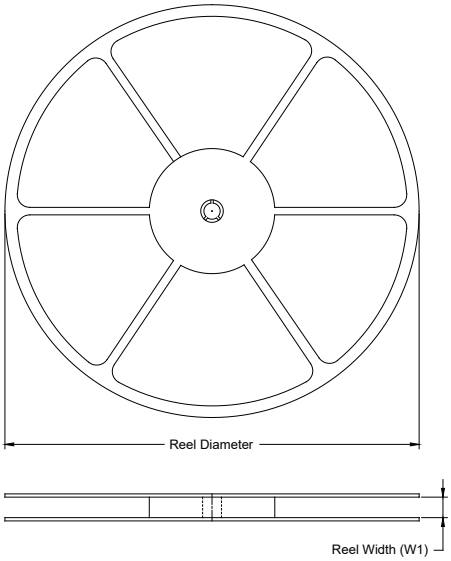
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.530	0.580	0.630
A1	0.150	0.180	0.210
A2	0.400 BSC		
D	1.000	1.100	1.200
E	1.000	1.100	1.200
e	0.400 BSC		
L	0.150	0.200	0.250
L1	0.050 REF		

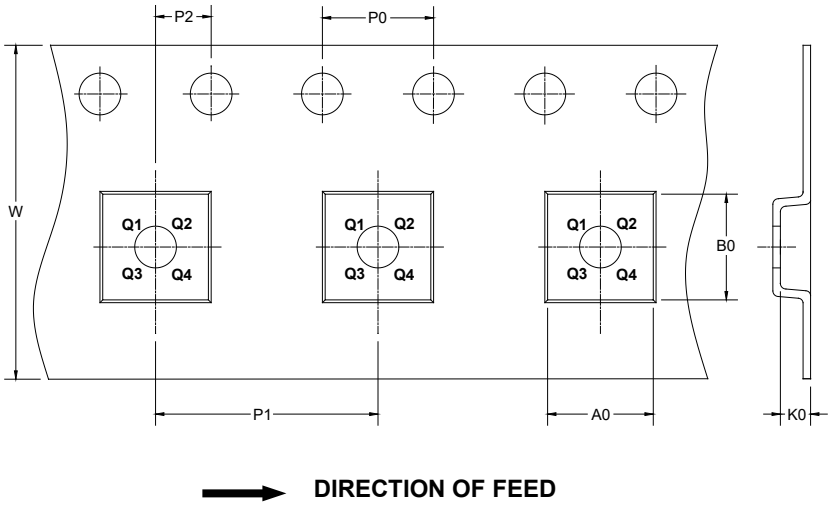
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



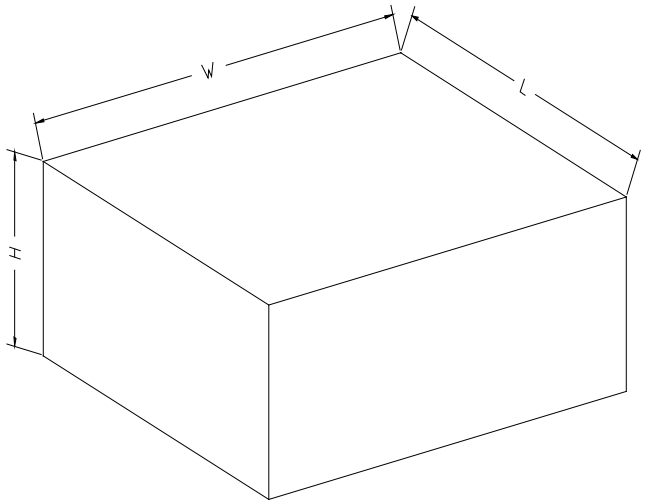
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
ULGA-1.1×1.1-9L	7″	8.6	1.26	1.26	0.72	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002