SGM40657/SGM40658
High-Current Over-Voltage Protector

GENERAL DESCRIPTION

The SGM40657/8 over-voltage protection devices feature a low 20mΩ (TYP) R_{ON} internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +120V. When the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected downstream components.

The over-voltage protection threshold can be adjusted with optional external resistors to any voltage between 4V and 20V. If the OVLO input is below the external OVLO select voltage, the SGM40657/8 automatically choose the internal trip thresholds. The internal over-voltage thresholds (V_{IN_OVLO}) are preset to be 6.82V/5.95V typical (SGM40657/8). The devices feature an open-drain $\overline{ACOK}$ output indicating a stable supply between minimum supply voltage and V_{OVLO}. The SGM40657/8 are also protected against over-current events by an internal thermal shutdown.

The SGM40657/8 are available in Green 12-Ball CSP package and operate over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Protect High-Power Portable Devices**
  - **Wide Operating Input Voltage Protection from 2.5V to 28V**
  - **Integrated 20mΩ (TYP) N-Channel MOSFET Switch**
- **Flexible Over-Voltage Protection Design**
  - **Adjustable Over-Voltage Protection Trip Level**
  - **Wide Adjustable OVLO Threshold Range from 4V to 20V**
  - **Internal Preset OVLO Thresholds:**
    6.82V (SGM40657)
    5.95V (SGM40658)
- **Additional Protection Features Increase System Reliability**
  - **Surge Immunity up to +120V**
  - **Soft-Start to Minimize In-Rush Current**
  - **Internal 15ms Startup Debounce**
  - **Thermal Shutdown Protection**
- **Enable Function**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green WLCSP-1.31×1.84-12B Package**

APPLICATIONS

Smart Phones
Tablet PCs
Mobile Internet Devices

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40657	WLCSP-1.31×1.84-12B	-40℃ to +85℃	SGM40657YG/TR	XXXXX GM3YG	Tape and Reel, 3000
SGM40658	WLCSP-1.31×1.84-12B	-40℃ to +85℃	SGM40658YG/TR	XXXXX GM4YG	Tape and Reel, 3000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN (with respect to GND)..... -0.3V to 28V (1)
IN (with respect to GND)..... +120V, 1.2/50μs, 2Ω surge (2) (3)
OUT (with respect to GND)..... -0.3V to V_{IN} + 0.3V
OVLO..... -0.3V to 26.4V
$\overline{ACOK}$, $\overline{EN}$ (with respect to GND)..... -0.3V to 6V
Continuous IN, OUT Current (4)..... 6A
Peak IN, OUT Current (10ms)..... 8A
Junction Temperature..... +150℃
Storage Temperature Range..... -65℃ to +150℃
Lead Temperature (Soldering 10 sec)..... +260℃
ESD Susceptibility
HBM..... 7kV
MM..... 400V
CDM..... 1kV
Air Gap Discharge on IN Pin (IEC61000-4-2)..... 20kV
Contact Discharge on IN Pin (IEC61000-4-2)..... 12kV

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range..... 2.5V to 28V (5)
Operating Temperature Range..... -40℃ to +85℃

NOTES:
1. Non-frequent repeat peak voltage during input surge transient and ESD transient is not subject to this rating value, which may go higher than 35V during the surge test.
2. Surge test in compliance with IEC61000-4-5 specification.
3. Survives burst pulse up to +120V with 2Ω series resistance.
4. Continuous current limit may vary with the circuit board thermal dissipation condition.
5. If protection discharging triggered, the discharging keeps until the supply falls below the hysteresis range. Continuously force driving during discharging with a voltage in the hysteresis range would cause overstress or even damage the device. Supply voltage within the hysteresis range is not recommended. A 1kΩ resistor should be inserted in supply path for clamp voltage evaluation to avoid overstress damage by unintended triggering.

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DISCLAIMER

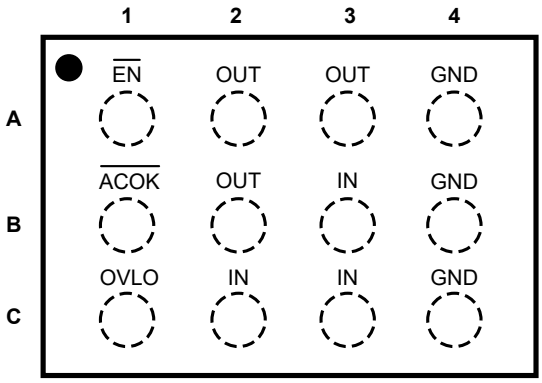
SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

SGM40657/8 (TOP VIEW)



WLCSP-1.31×1.84-12B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	$\overline{EN}$	Enable Control. When $\overline{EN}$ = "Low", chip is enabled; when $\overline{EN}$ = "High", chip is in disable status.
A4, B4, C4	GND	Ground. Connect GND pins together for proper operation.
A2, A3, B2	OUT	Output Voltage. Output of internal switch. Connect OUT pins together for proper operation.
B1	$\overline{ACOK}$	Open-Drain Flag Output. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pull-up resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.
B3, C2, C3	IN	Input Voltage. Bypass IN with a 0.1μF ceramic capacitor as close as possible to the device. Connect IN pins together for proper operation.
C1	OVLO	External OVLO Adjustment. Connect OVLO to GND when using the internal threshold. Connect a resistor-divider to OVLO to set a different OVLO threshold; this external resistor-divider is completely independent of the internal threshold.

ELECTRICAL CHARACTERISTICS

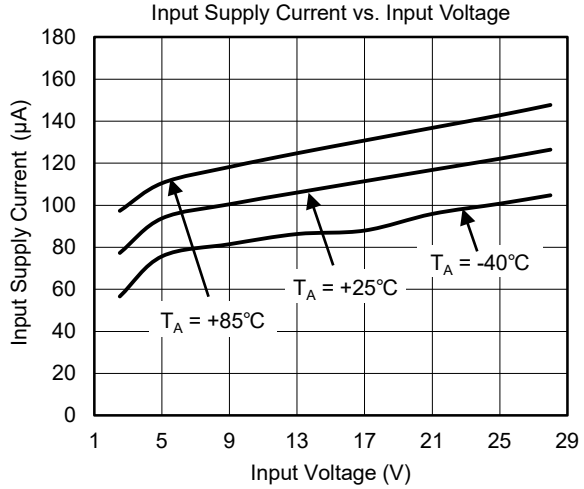
(V_{IN} = 2.5V to 28V, $\overline{EN}$ = 0V, C_{IN} = 0.1μF, T_A = -40℃ to +85℃, typical values are at V_{IN} = 5V, I_{IN} ≤ 3A, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			2.5		28	V
Input Clamp Triggering Voltage	V_{IN_CLAMP}	I_{IN} = 10mA limited, T_A = +25℃			28.8		V
Input Clamp Hysteresis	V_{HYS}				0.75		V
Input Supply Current	I_{IN}	V_{IN} = 5V			95	155	μA
OVLO Supply Current	I_{IN_Q}	V_{OVLO} = 3V, V_{IN} = 5V, V_{OUT} = 0V			95	155	μA
Shutdown Current	I_{Q_OFF}	V_{IN} = 5V, $\overline{EN}$ = 2V				2	μA
Internal Over-Voltage Trip Level	V_{IN_OVLO}	V_{IN} rising	SGM40657	6.61	6.82	7.06	V
			SGM40658	5.73	5.95	6.18	
		V_{IN} falling	SGM40657	6.07	6.53		
			SGM40658	5.15	5.63		
V_{BG} Reference	V_{BG}			1.180	1.216	1.255	V
Adjustable OVLO Threshold Range				4		20	V
External OVLO Select Threshold	V_{OVLO_SELECT}			0.23	0.26	0.30	V
Switch On-Resistance	R_{ON}	V_{IN} = 5V, I_{OUT} = 0.5A, T_A = +25℃			20	35	mΩ
OUT Load Capacitance	C_{OUT}	V_{IN} = 5V				1000	μF
OVLO Input Leakage Current	I_{OVLO}	V_{OVLO} = 1.3V		-100		100	nA
IN Leakage Voltage by OVLO	V_{IN_LEAK}	V_{OVLO} = 20V, V_{IN} = unconnected, R_{OVLO} = 1MΩ				0.2	V
Thermal Shutdown					150		℃
Thermal Shutdown Hysteresis					30		℃
DIGITAL SIGNAL ($\overline{ACOK}$)							
$\overline{ACOK}$ Output Low Voltage	V_{OL}	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA, See Figure 1			0.26	0.32	V
$\overline{ACOK}$ Leakage Current	I_{ACOK_LEAK}	$V_{I/O}$ = 3.3V, $\overline{ACOK}$ deasserted, See Figure 1				1	μA
TIMING CHARACTERISTICS							
Debounce Time	t_{DEB}	Time from V_{IN} > 2.5V to the time V_{OUT} starts rising			15		ms
Soft-Start Time	t_{SS}	Time from V_{IN} > 2.5V to soft-start off			30		ms
Switch Turn-On Time	t_{ON}	V_{IN} = 5V, R_L = 100Ω, C_{LOAD} = 100μF, V_{OUT} from 10%, V_{IN} to 90% V_{IN}			1.5		ms
Switch Turn-Off Time	t_{OFF}	V_{IN} > V_{IN_OVLO} to V_{OUT} = 80% of V_{IN}, R_L = 100Ω, with 20% over drive, for the case of using the internal threshold.			50		ns
Switch Turn-Off Propagation Delay	t_{DELAY}	OVLO > V_{BG} with 20% over drive to output falling 10%, R_L = 100Ω. For the case of using external threshold.			80		ns
$\overline{EN}$ LOGIC LEVELS							
Logic LOW Input Voltage	V_{IL}					0.4	V
Logic HIGH Input Voltage	V_{IH}			1.6			V
$\overline{EN}$ Leakage Current	I_{EN_LEAK}	V_{IN} = 5V				1	μA

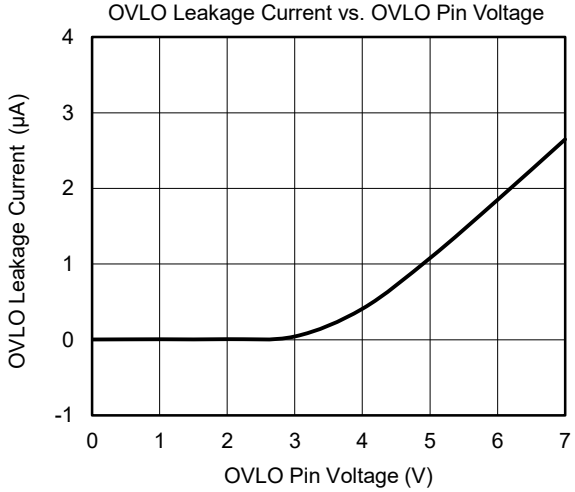
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, T_A = +25℃, unless otherwise noted.

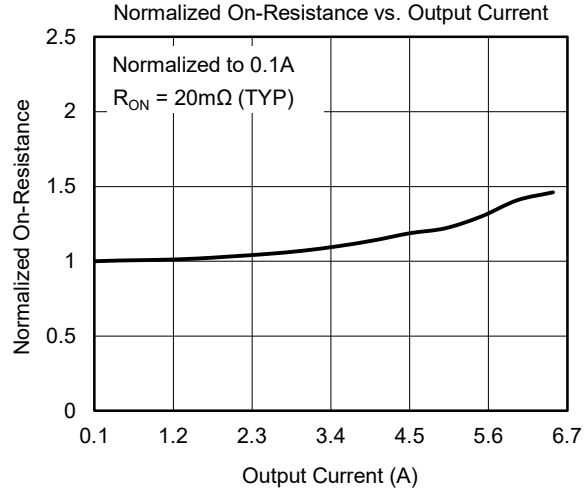
Input Supply Current vs. Input Voltage



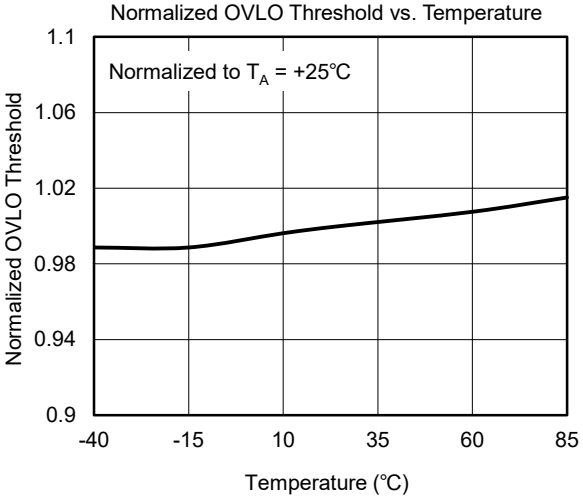
OVLO Leakage Current vs. OVLO Pin Voltage



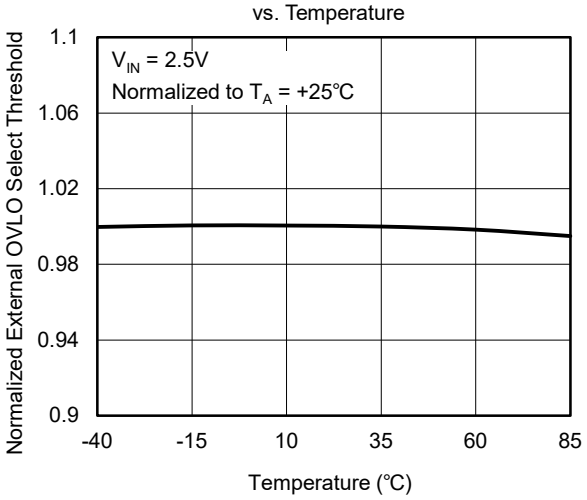
Normalized On-Resistance vs. Output Current



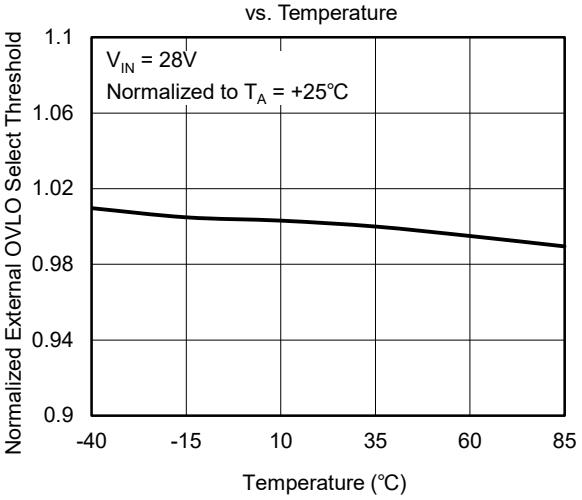
Normalized OVLO Threshold vs. Temperature



Normalized External OVLO Select Threshold vs. Temperature



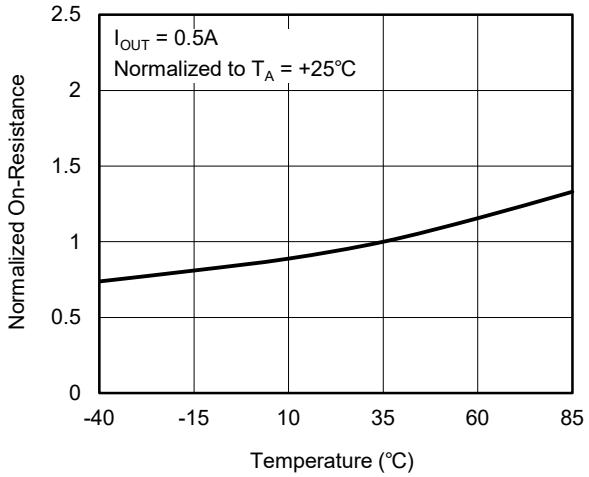
Normalized External OVLO Select Threshold vs. Temperature



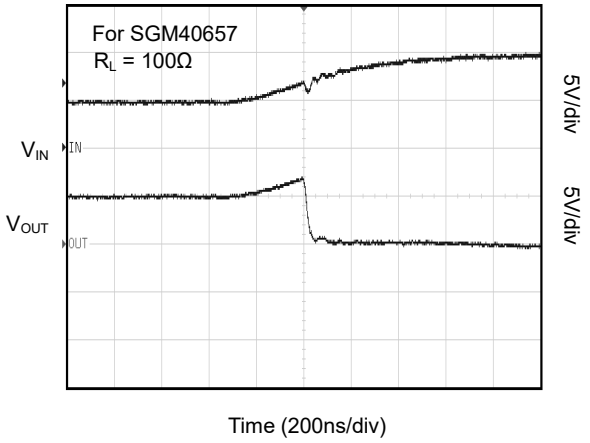
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, T_A = +25℃, unless otherwise noted.

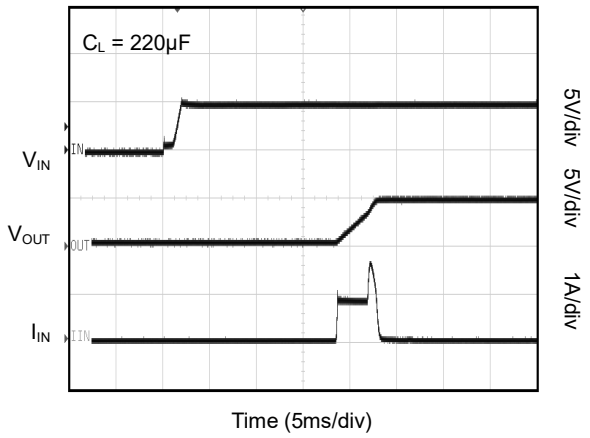
Normalized On-Resistance vs. Temperature



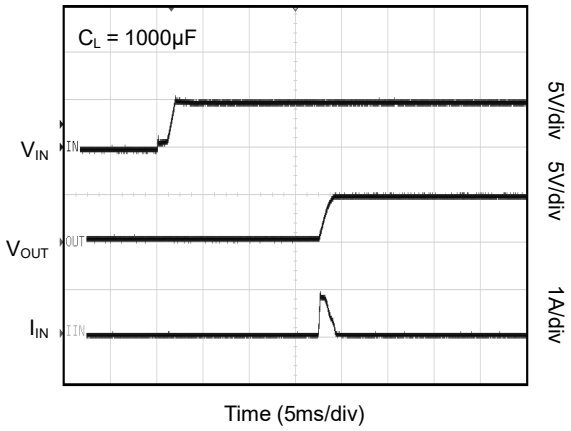
Over-Voltage Fault Response



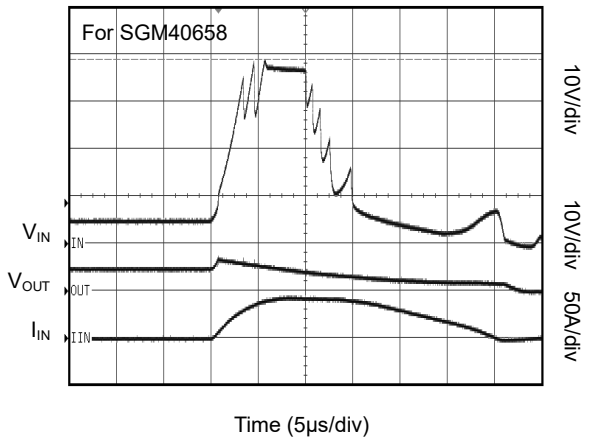
Power-Up Response



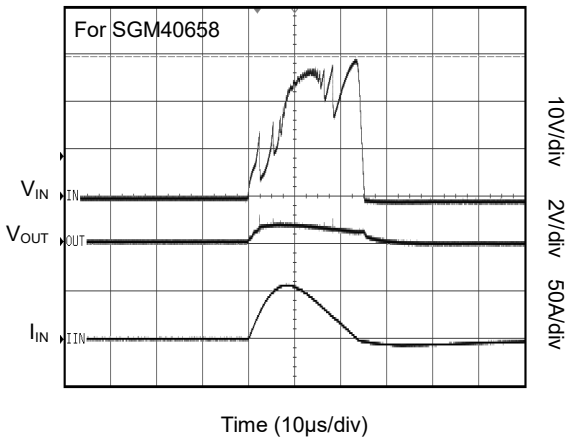
Power-Up Response



IN-GND 120V Surge Discharge Waveforms (On-State)



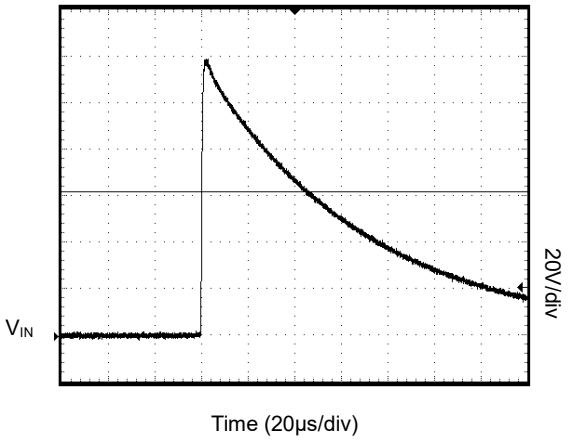
IN-GND 120V Surge Discharge Waveforms (Off-State)



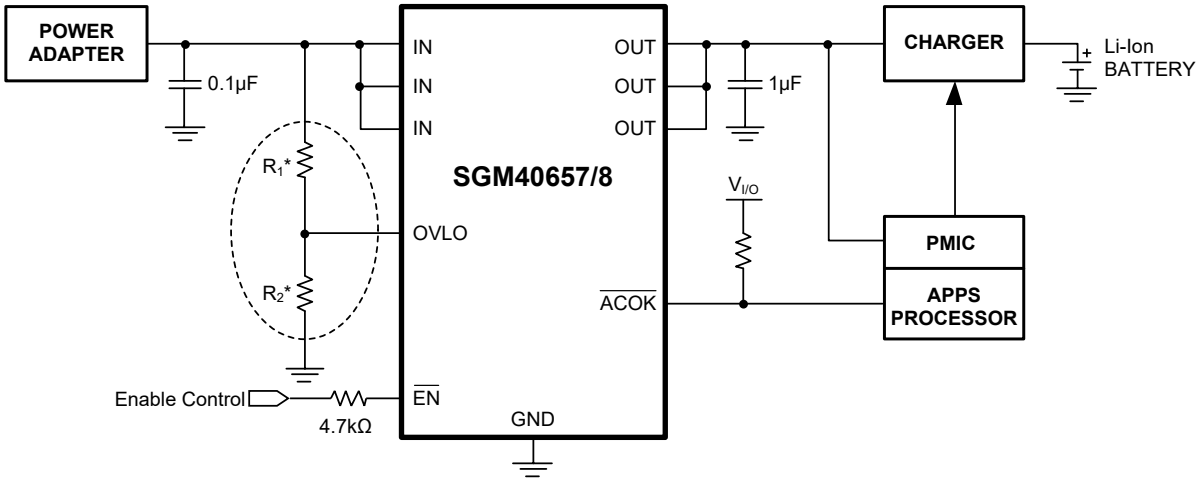
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 5V, $\overline{EN}$ = 0V, C_{IN} = 0.1μF, C_{OUT} = 1μF, T_A = +25℃, unless otherwise noted.

Open Circuit Voltage Waveform without SGM40657/8, +120V, 1.2/50μs Surge



TYPICAL APPLICATION



*** R_1 and R_2 are only required for adjustable OVLO; otherwise, connect OVLO to GND.**

Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

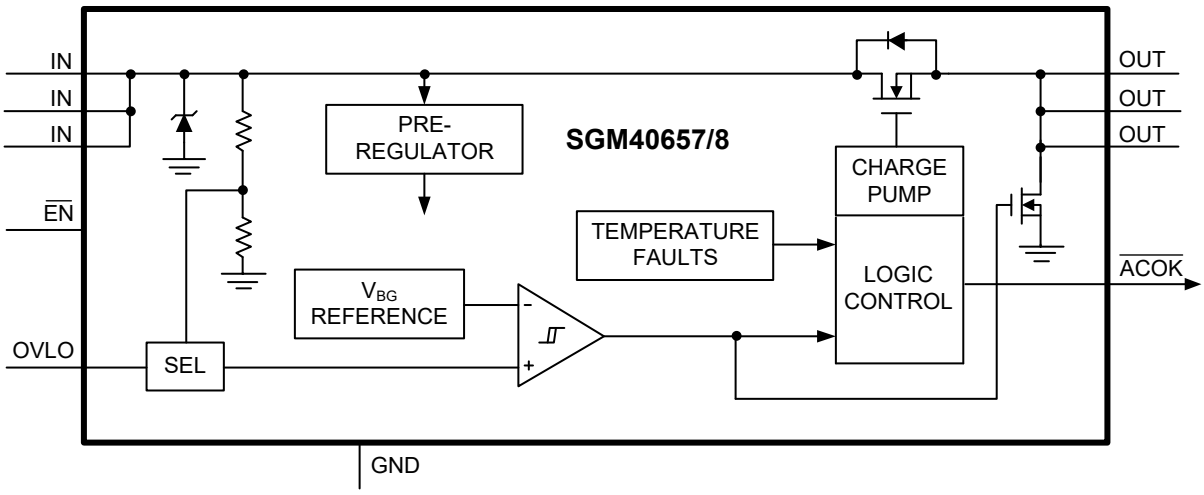
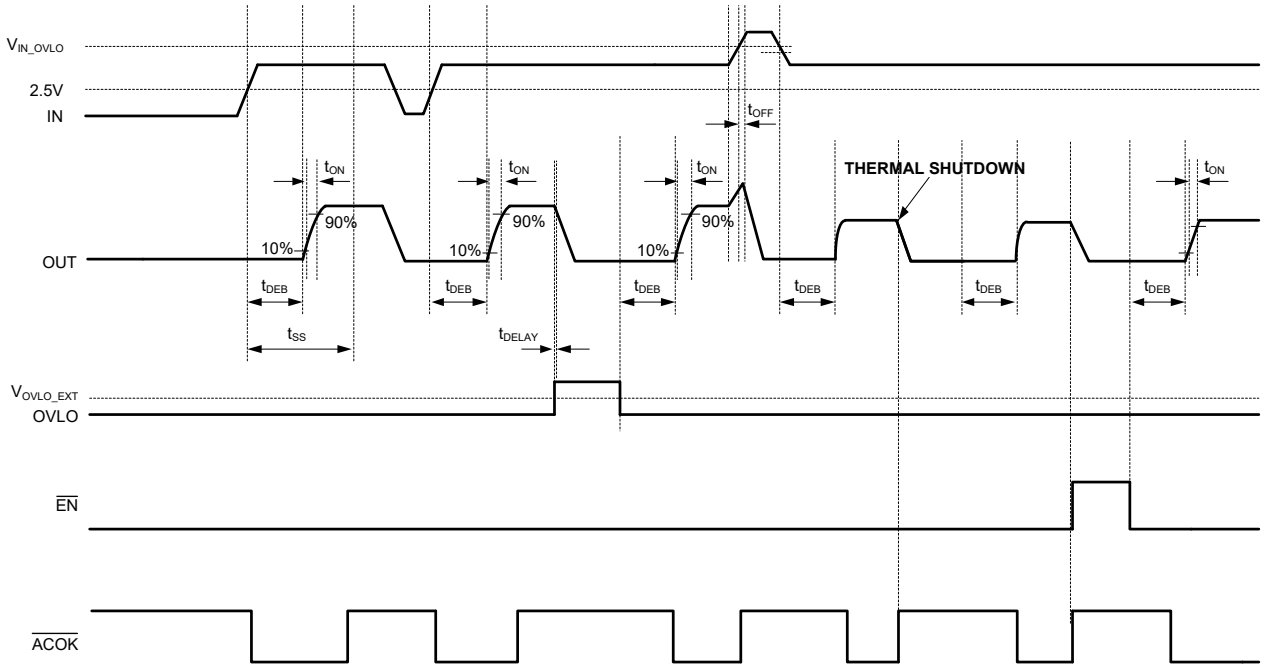


Figure 2. Block Diagram

TIMING DIAGRAM



NOTE: Waveforms are not to scale.

Figure 3. Timing Diagram

SURGE UP TEST CIRCUIT

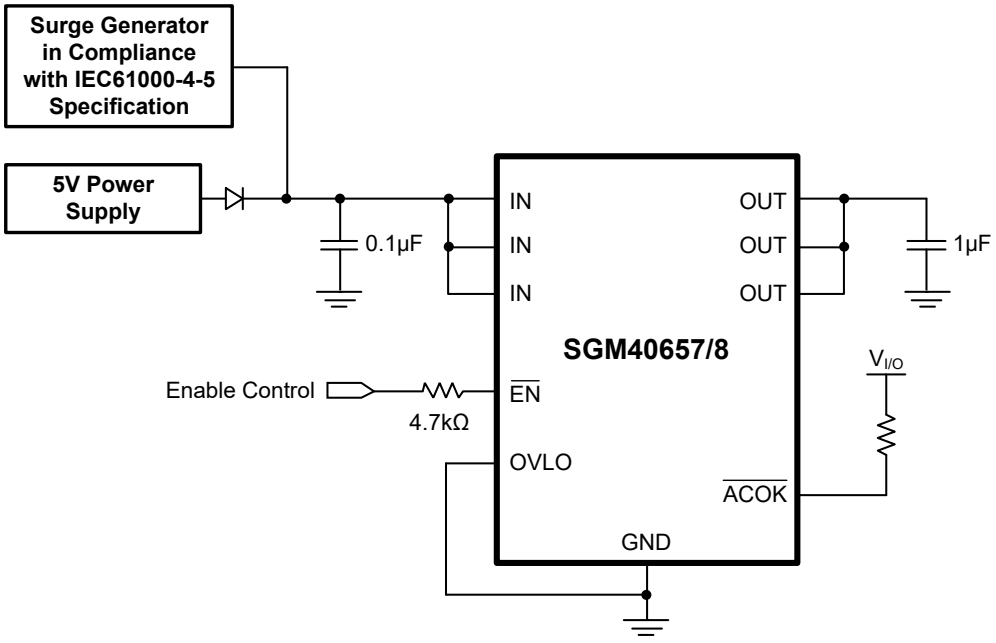


Figure 4. Surge Up Test Circuit

DETAILED DESCRIPTION

The SGM40657/8 over-voltage protection devices feature a low on-resistance (R_{ON}) internal FET and protect low-voltage systems against voltage faults up to +28V_{DC}. An internal clamp also protects the devices from surges up to +120V. Surge up tests are operated according to the test circuit in Figure 4. If the input voltage exceeds the over-voltage threshold, the internal FET is turned off to prevent damage to the protected components. A 15ms (TYP) debounce time built into the device prevents false turn-on of the internal FET during startup.

Device Operation

The devices contain timing logic that controls the turn-on of the internal FET. The internal charge pump is enabled when V_{IN} < V_{IN_OVLO}, if internal trip thresholds are used or when V_{OVLO} < V_{OVLO_EXT} if external trip thresholds are used. The charge-pump after a 15ms (TYP) debounce delay, turns the internal FET on (see Figure 2). After the debounce time, soft-start limits the FET inrush current for 15ms (TYP). At any time, if V_{IN} rises above V_{OVLO_THRESH}, OUT is disconnected from IN.

Enable Function

The IC has an enable pin which is used to enable or disable the device. Connect the $\overline{EN}$ pin high to turn off the internal pass FET. Connect the $\overline{EN}$ pin low to turn on the internal pass FET and enter the start-up routine.

Internal Switch

The SGM40657/8 incorporate an internal FET with a 20mΩ (TYP) R_{ON}. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

Over-Voltage Lockout (OVLO)

The SGM40657/8 have 6.82V/5.95V (TYP) over-voltage threshold (OVLO) respectively.

Thermal Shutdown Protection

The SGM40657/8 feature thermal shutdown circuitry. The internal FET turns off when the junction temperature exceeds +150℃ (TYP). The device exits thermal shutdown after the junction temperature cools by 30℃ (TYP).

$\overline{ACOK}$ Output

An open-drain $\overline{ACOK}$ output gives the SGM40657/8 the ability to communicate a stable power source to the host system. $\overline{ACOK}$ is driven low after input voltage is stable between minimum V_{IN} and V_{OVLO} after debounce. Connect a pull-up resistor from $\overline{ACOK}$ to the logic I/O voltage of the host system. $\overline{ACOK}$ is high impedance after thermal shutdown.

USB OTG Support

When used in an OTG application the SGM40657/8 can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward-bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. Once the voltage at IN exceeds the minimum input voltage of 2.5V and the debounce time has elapsed, the main power switch will turn fully on, significantly reducing the voltage drop from OUT to IN. In this mode，the part is able to supply a continuous current up to 3.5A to the OTG load.

APPLICATION INFORMATION

Bypass Capacitor

For most applications, bypass IN to GND with a 0.1μF ceramic capacitor as close as possible to the device. If the power source has significant inductance due to long lead length, the device clamps the overshoot due to LC tank circuit.

Output Capacitor

The slow turn-on time provides a soft-start function that allows the SGM40657/8 to charge an output capacitor up to 1000μF without turning off due to an over-current condition.

Enhancing Surge Absorbability

When the input voltage ramps higher than the V_{IN_CLAMP}, it triggers an active path in the device to discharge the input quickly until the input voltage falls V_{HYS} below the V_{IN_CLAMP}. Input rising and discharging may repeat until the surge source energy is discharged. A voltage pulse with saw shape top is clamped between the V_{IN_CLAMP} and the active path's resumable breaking voltage, which protects components which are connected to the device's input or output.

As the active path tries to pull in more energy upon triggering, only those absorption components with similar triggering voltage and similar residual voltage could share their capability for enhancing surge absorption. Both the trigger voltage and the residual voltage should be evaluated for selection matched companion absorption components. As a rule of thumb, a TVS with triggering voltage lower than the V_{IN_CLAMP} is recommended.

External OVLO Adjustment Functionality

The device detects voltage at the OVLO pin to check if an external divider exists. If OVLO is connected to ground, the internally set OVLO value will be applied.

If an external resistor-divider is connected to OVLO and V_{OVLO} exceeds the OVLO select voltage, V_{OVLO_SELECT}, then this external resistor divider determines the $V_{IN\_OVLO\_EXT}$. R_1 = 1MΩ is a good starting value for minimum current consumption. Since $V_{IN\_OVLO\_EXT}$, V_{BG}, and R_1 are known, R_2 can be calculated from the following formula:

$$V_{IN\_OVLO\_EXT} = V_{BG} \times \left[1 + \frac{R_1}{R_2}\right]$$

This external resistor-divider is completely independent from the internal resistor-divider.

REVISION HISTORY

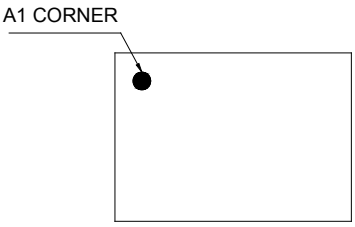
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2017) to REV.A

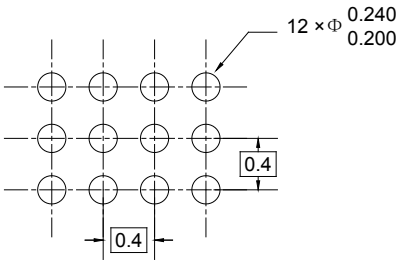
Changed from product preview to production data ..... AI

PACKAGE OUTLINE DIMENSIONS

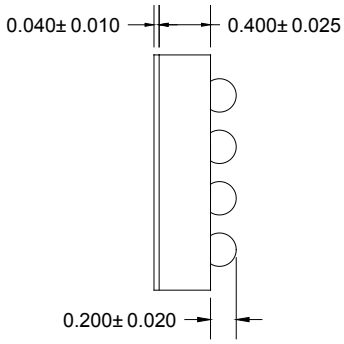
WLCSP-1.31×1.84-12B



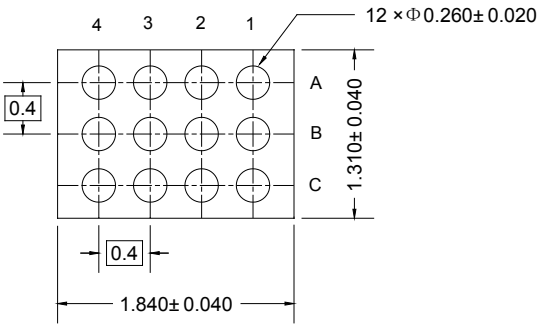
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

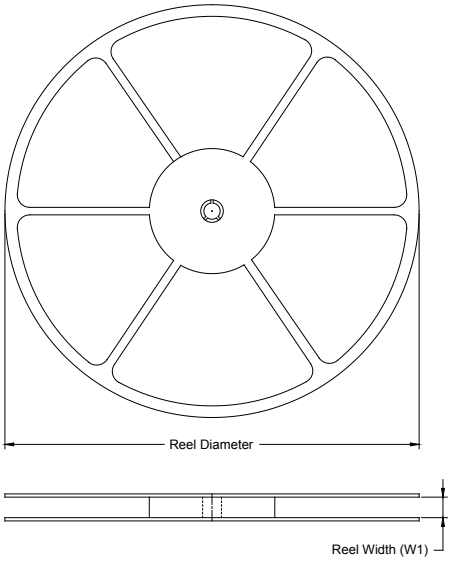


BOTTOM VIEW

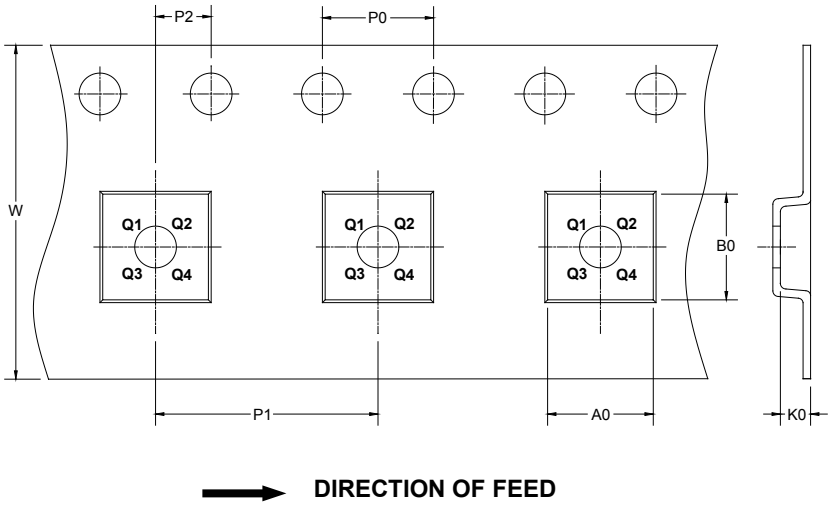
NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



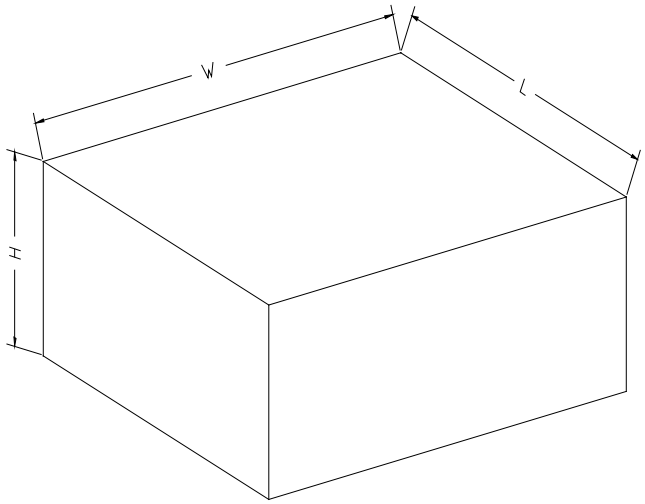
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.31×1.84-12B	7″	9.2	1.40	2.00	0.80	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002