SGM61630
60V, 3A Buck Converter with 50μA I_Q

GENERAL DESCRIPTION

The SGM61630 is a current mode controlled Buck regulator with 4.3V to 60V input range and 3A continuous output current. The device suits various applications of industry, which demands power conditioning from unregulated sources. A 140mΩ R_{DSON} MOSFET is integrated as high-side switch. The ultra-low 50μA (TYP) quiescent current and low shutdown current of only 2μA (TYP) make it a suitable choice for battery-powered applications. Switching frequency can be selected over a wide range (200kHz to 2500kHz) to allow desired tradeoff between efficiency and component sizes. There is also the internal loop compensation that simplifies compensation network design, and requires less external components, saving user design time and cost. With precision enable input, regulator control is simplified, as well as system power sequencing. Protection against over-voltage transient is provided to limit the startup or other transient overshoots. Secure operation in overload conditions is ensured by thermal shutdown protection and cycle-by-cycle current limit.

The SGM61630 is available in a Green SOIC-8 (Exposed Pad) package.

FEATURES

- **4.3V to 60V Input Range**
- **3A Continuous Output Current**
- **50μA (TYP) Ultra-Low Operating Quiescent Current**
- **140mΩ High-side MOSFET**
- **Minimum Switching-On Time: 100ns**
- **Current Mode Control**
  - **SGM61630A: Soft-Start Version**
  - **SGM61630B: Power-Good Version**
- **Adjustable Switching Frequency from 200kHz to 2500kHz**
- **Frequency Synchronization to External Clock**
- **Easy-to-Use Internal Compensation**
- **Support High Duty Cycle Operation**
- **Precision Enable Input**
- **2μA (TYP) Shutdown Current**
- **Thermal, Over-Voltage and Short Protection**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Industrial Power Supplies
Telecom and Datacom Systems
General Purpose Wide Input Voltage Regulation

TYPICAL APPLICATION

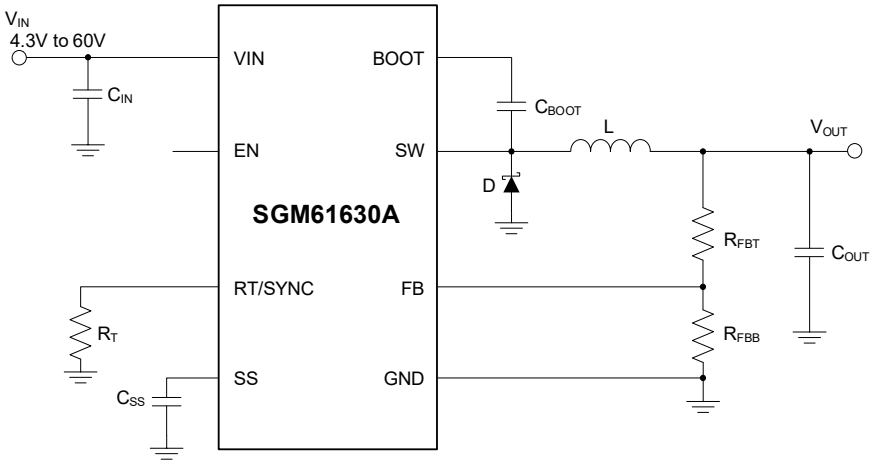


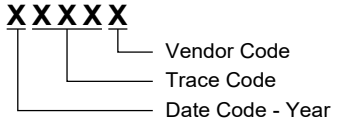
Figure 1. SGM61630A Typical Application

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61630A	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61630AXPS8G/TR	SGM MCLXPS8 XXXXX	Tape and Reel, 4000
SGM61630B	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61630BXPS8G/TR	SGM MCMXPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltages
- VIN, EN to GND ..... -0.3V to 65V
- BOOT to GND ..... -0.3V to 71V
- SS (SGM61630A) to GND..... -0.3V to 5V
- PGOOD (SGM61630B) to GND ..... -0.3V to 5V
- FB to GND..... -0.3V to 6.5V
- RT/SYNC to GND ..... -0.3V to 6.5V

Output Voltages
- BOOT to SW 6.5V
- SW to GND ..... -1.5V to 65V
- SW to GND (10ns Transient) ..... -5V to 65V

Package Thermal Resistance
- SOIC-8 (Exposed Pad), θ_{JA} ..... 41℃/W

Junction Temperature.....150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Buck Regulator
- VIN .....4.3V to 60V
- BOOT .....65V (MAX)
- FB .....0V to 5V

Control
- EN .....0V to 60V
- RT/SYNC .....0V to 5V
- SS (SGM61630A) to GND.....0V to 5V
- PGOOD (SGM61630B) to GND .....0V to 5V

Switching Frequency Range
- RT Mode ..... 200kHz to 2500kHz
- SYNC Mode ..... 210kHz to 2400kHz

Operating Junction Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

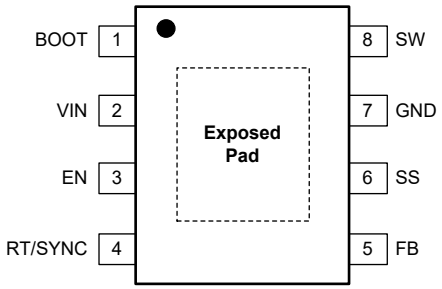
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

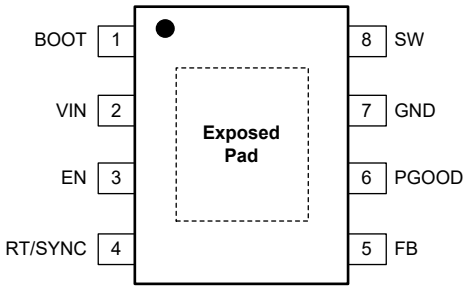
PIN CONFIGURATIONS

SGM61630A (TOP VIEW)



SOIC-8 (Exposed Pad)

SGM61630B (TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN		NAME	I/O	DESCRIPTION
SGM61630A	SGM61630B			
1	1	BOOT	I	Bootstrap Input (for N-MOSFET Gate Driver Supply Voltage). Connect this pin to SW pin with a 0.1μF ceramic capacitor. The MOSFET will be turned off if the BOOT capacitor voltage drops below its BOOT-UVLO level to get the capacitor voltage refreshed.
2	2	VIN	P	Supply Input. Connect VIN to a power source with 4.3V to 60V output voltage range. Decouple VIN to GND as close as possible to the catch diode anode and the device with a high frequency, and low ESR ceramic capacitor (X5R or higher grade is recommended).
3	3	EN	I	Active High Enable Input. Float or pull up to VIN pin to enable, or pull down below 1.12V to disable the device. Input UVLO threshold can be programmed through using a resistor divider from VIN pin.
4	4	RT/SYNC	I	Resistor Timing and External Clock. Setting frequency by the external RT resistor or external SYNC clock, refer to Synchronization to RT/SYNC Pin for more details.
5	5	FB	I	Feedback Pin for Setting the Output Voltage. The SGM61630 regulates the FB pin to 0.75V. Connect a feedback resistor divider tap to this pin.
6	—	SS	O	SS Pin for Soft-Start Version. Connect an external capacitor (C_{SS}) between this pin and the GND to set the soft-start time.
—	6	PGOOD		PGOOD Pin for Power-Good Version. Open drain output for power-good flag, use a 10kΩ to 100kΩ pull-up resistor to logic rail or other DC voltage no higher than 5V.
7	7	GND	G	Ground Pin.
8	8	SW	P	Switching Node of the Converter (Source of the Internal MOSFET). Connect it to the cathode of the external power diode (catch diode), the bootstrap capacitor and the inductor.
—	—	Exposed Pad	G	Exposed Pad. It helps cooling the device junction and must be connected to GND pin for proper operation.

NOTE: I = input, O = output, G = ground, P = power.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{IN} = 4.3V to 60V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply (VIN Pin)						
Operation Input Voltage	V_{IN}		4.3		60	V
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	3.6	3.85	4.1	V
Under-Voltage Lockout Threshold Hysteresis	V_{UVLO_HYS}			300		mV
Shutdown Supply Current	I_{SHDN}	T_A = +25℃, V_{EN} = 0V, V_{IN} = 24V		2	3	μA
Operating Quiescent Current (Non-Switching)	I_Q	T_A = +25℃, V_{FB} = 1.0V, V_{IN} = 24V		50		μA
Enable (EN Pin)						
EN Threshold Voltage	V_{ENH}		1.08	1.17	1.26	V
	V_{ENL}		1.03	1.12	1.20	V
EN Pin Current	I_{EN_PIN}	Enable threshold +50mV		-4.7		μA
		Enable threshold -50mV		-1.0		
EN Hysteresis Current	I_{EN_HYS}			-3.7		μA
Soft-Start						
SS Pin Current	I_{SS}	T_A = +25℃, for SGM61630A only		3		μA
Internal Soft-Start Time	t_{SS}	For SGM61630B only		4		ms
Power-Good (SGM61630B Only)						
PGOOD Flag Under-Voltage Tripping Threshold	V_{PG_UV}	Power-good (% of V_{FB})		95		%
		Power-bad (% of V_{FB})		92		%
PGOOD Flag Over-Voltage Tripping Threshold	V_{PG_OV}	Power-bad (% of V_{FB})		110		%
		Power-good (% of V_{FB})		107		%
PGOOD Flag Recovery Hysteresis	V_{PG_HYS}	% of V_{FB}		3		%
PGOOD Leakage Current at High Level Output	I_{PG}	$V_{Pull\text{-}Up}$ = 5V		100		nA
PGOOD Voltage at Low Level Output	V_{PG_LOW}	$I_{Pull\text{-}Up}$ = 1mA		0.1		V
VIN for Valid PGOOD Output at a Minimum	$V_{IN\_PG\_MIN}$	$V_{Pull\text{-}Up}$ < 5V at $I_{Pull\text{-}Up}$ = 100μA		1		V
Voltage Reference (FB Pin)						
Feedback Voltage	V_{FB}	T_J = +25℃	0.745	0.750	0.763	V
		T_J = -40℃ to +125℃	0.741	0.750	0.765	V
High-side MOSFET						
On-Resistance	R_{DSON}	V_{IN} = 12V, V_{BOOT} - V_{SW} = 5V		140	255	mΩ
High-side MOSFET Current Limit						
Current Limit	I_{LIMT}	V_{IN} = 12V, open-Loop	3.5	4.8	6.0	A
Thermal Performance						
Thermal Shutdown Threshold	T_{SHDN}			170		℃
Hysteresis	T_{HYS}			20		℃

ELECTRICAL CHARACTERISTICS (continued)

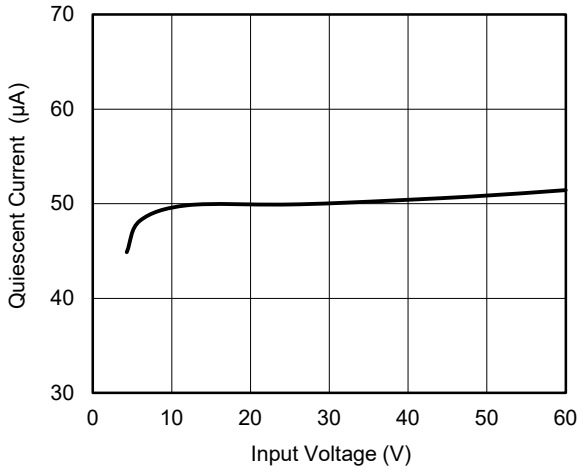
(T_J = -40℃ to +125℃, V_{IN} = 4.3V to 60V, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Characteristics						
Switching Frequency	f_{SW}	R_T = 11.5kΩ	1666	1940	2209	kHz
Switching Frequency Range at SYNC Mode	f_{SYNC}		210		2400	kHz
SYNC Input Clock High Level	V_{SYNC_R}		2.0			V
SYNC Input Clock Low Level	V_{SYNC_F}				0.3	V
Minimum SYNC Input Pulse Width	t_{SYNC_MIN}	Measured at 500kHz		30		ns
PLL Lock In Time	t_{LOCK_IN}	Measured at 500kHz		100		μs
Minimum Controllable On Time	t_{ON-MIN}			100		ns
Maximum Duty Cycle	D_{MAX}	f_{SW} = 200kHz		98		%

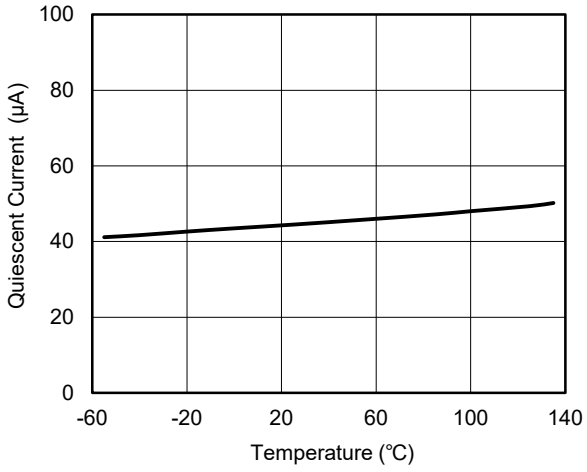
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 10μH and C_{OUT} = 2 × 47μF, unless otherwise noted.

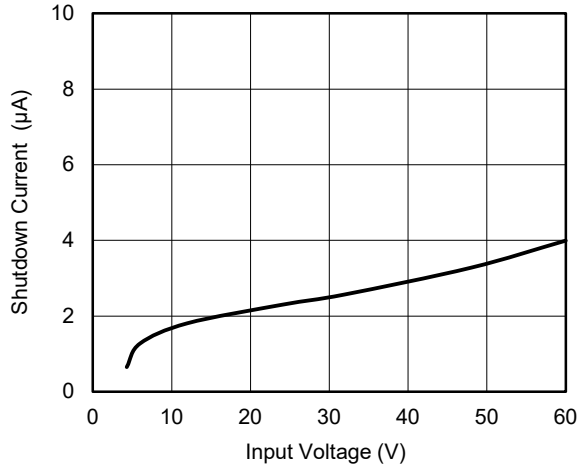
Quiescent Current vs. Input Voltage



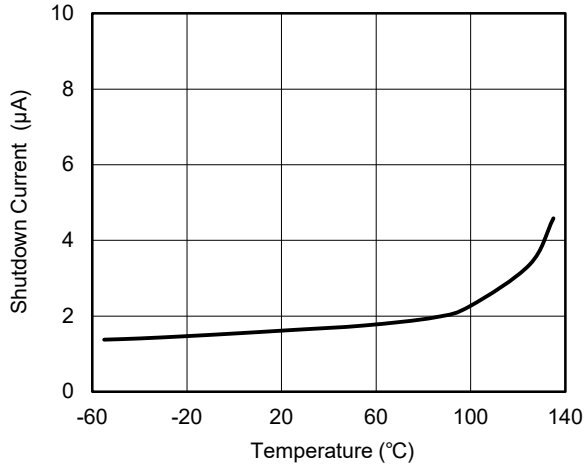
Quiescent Current vs. Temperature



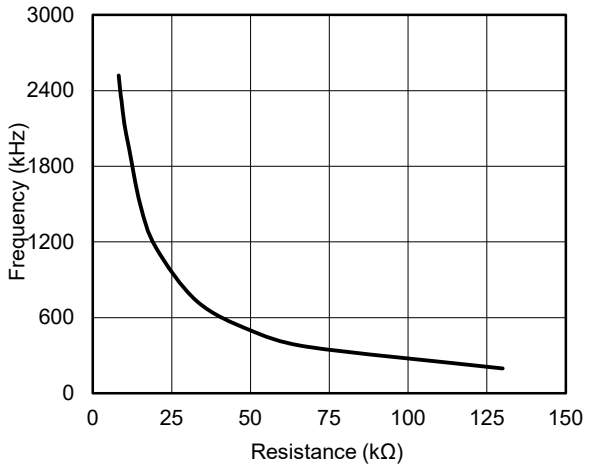
Shutdown Current vs. Input Voltage



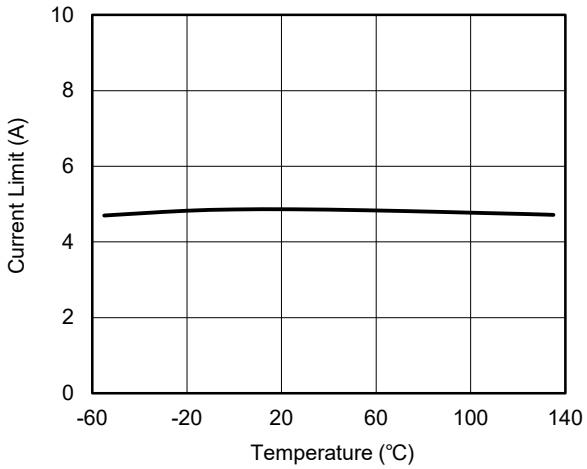
Shutdown Current vs. Temperature



Frequency vs. Resistance



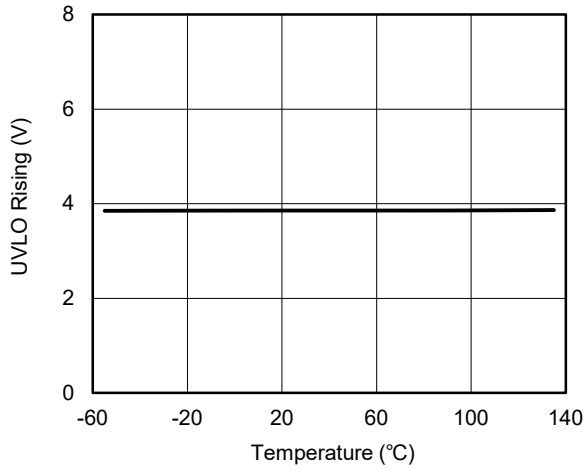
Current Limit vs. Temperature



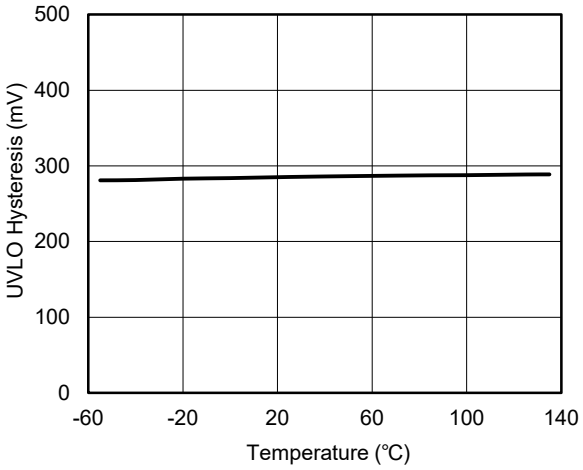
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 10μH and C_{OUT} = 2 × 47μF, unless otherwise noted.

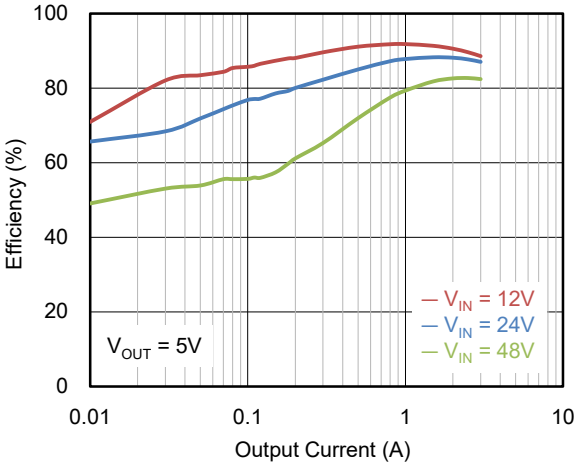
UVLO Rising vs. Temperature



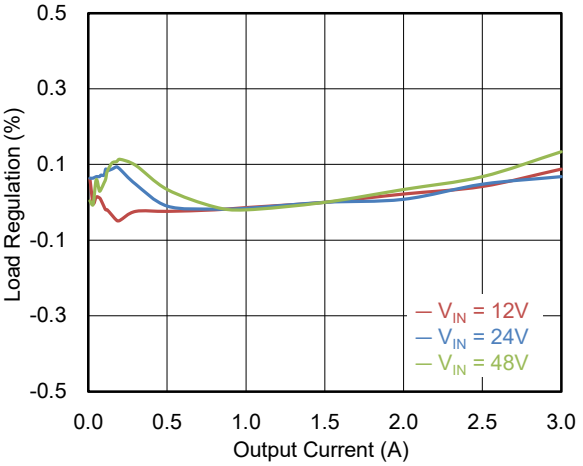
UVLO Hysteresis vs. Temperature



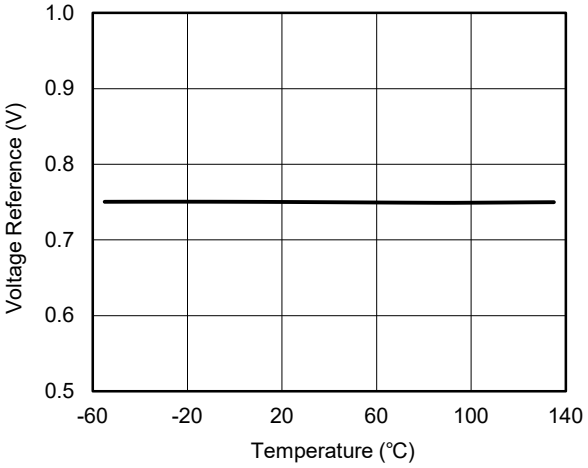
Efficiency vs. Output Current



Load Regulation



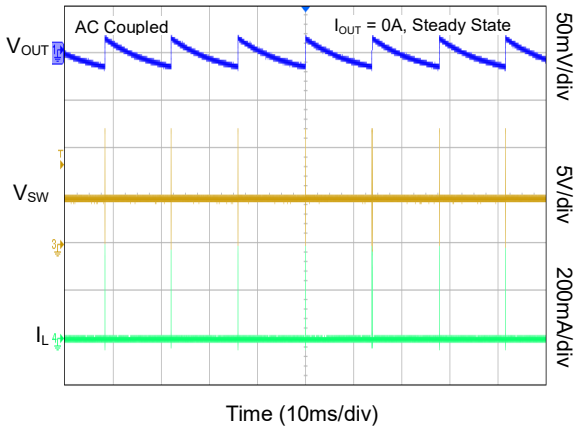
Voltage Reference vs. Temperature



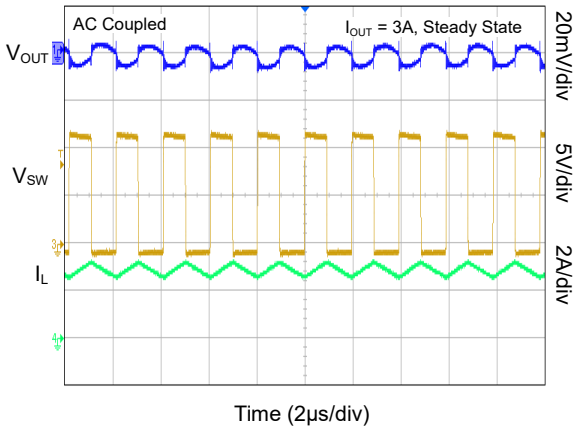
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 10μH and C_{OUT} = 2 × 47μF for SGM61630A version, unless otherwise noted.

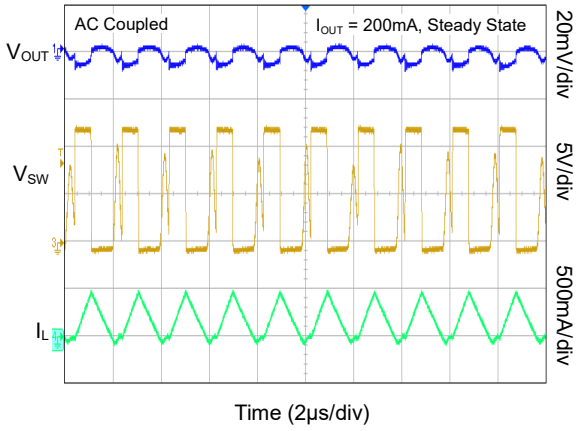
PSM Mode



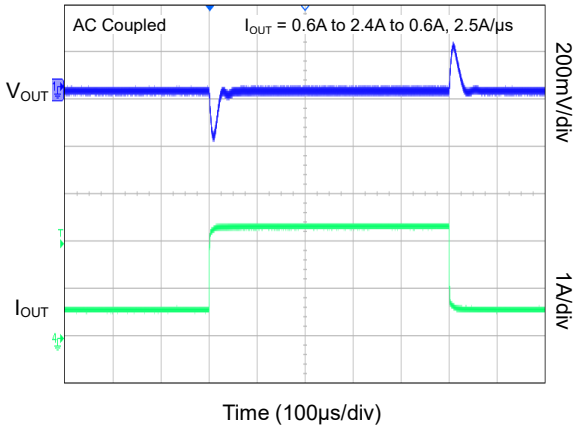
CCM Mode



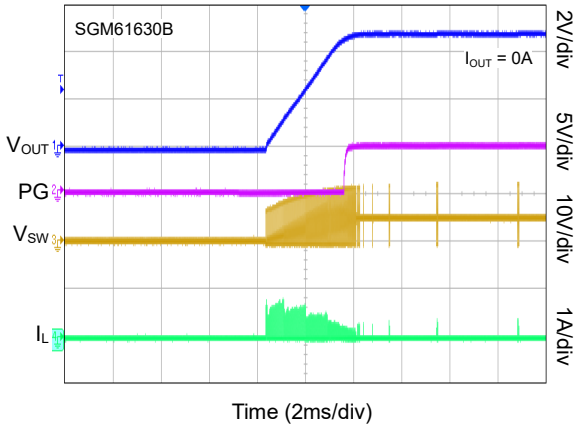
DCM Mode



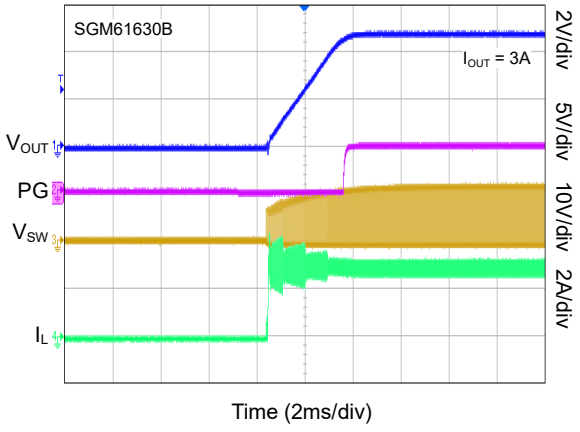
Load Transient



Startup by VIN



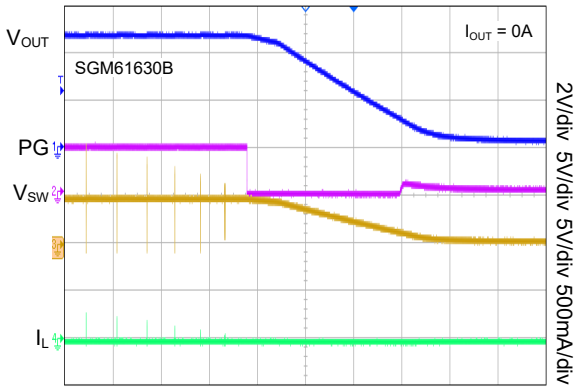
Startup by VIN



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

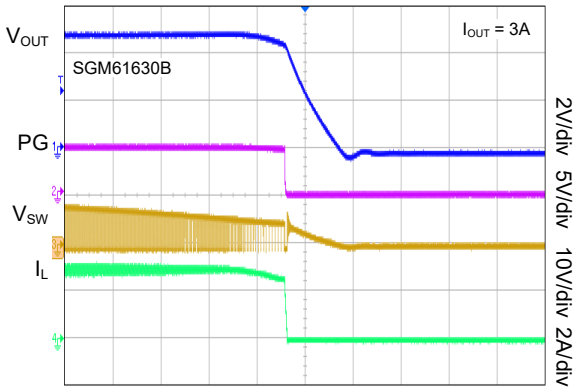
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 10μH and C_{OUT} = 2 × 47μF for SGM61630A version, unless otherwise noted.

Shutdown by VIN



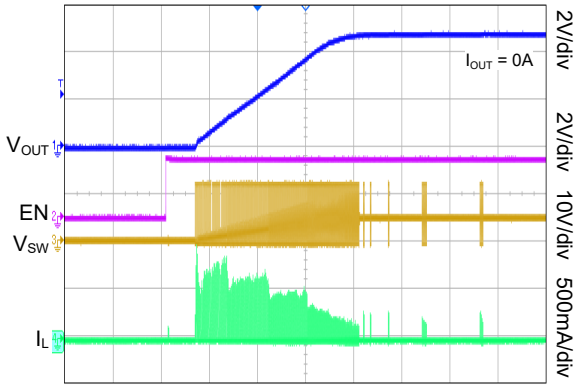
Time (20ms/div)

Shutdown by VIN



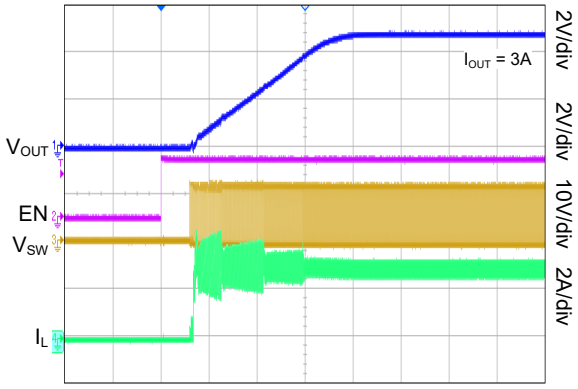
Time (100μs/div)

Startup by EN



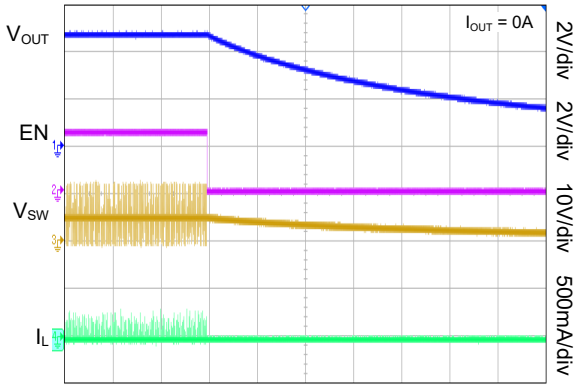
Time (1ms/div)

Startup by EN



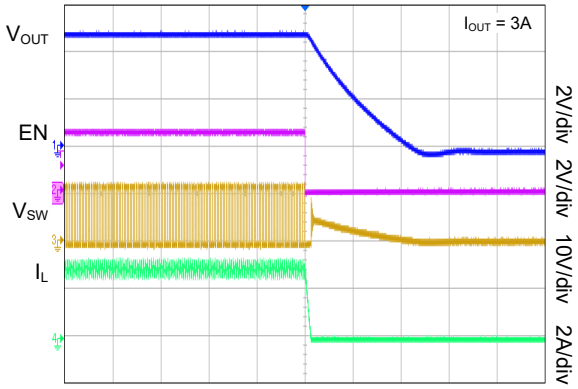
Time (1ms/div)

Shutdown by EN



Time (500ms/div)

Shutdown by EN

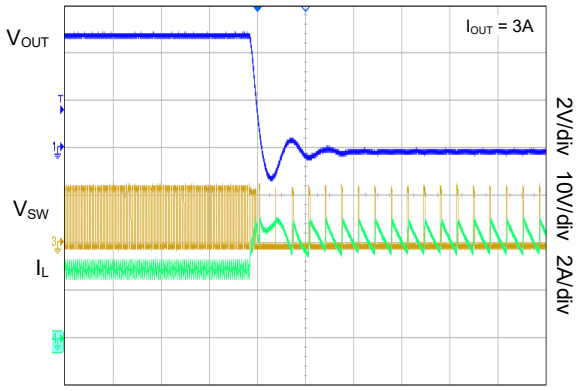


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

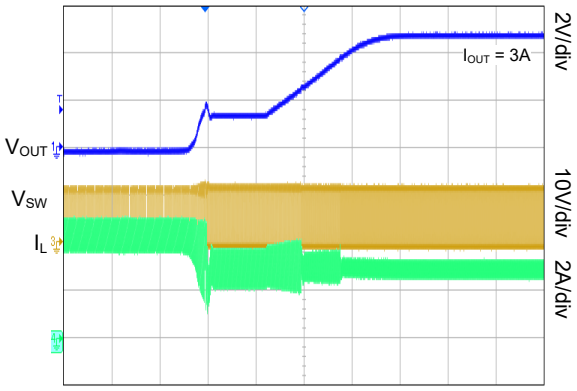
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 10μH and C_{OUT} = 2 × 47μF for SGM61630A version, unless otherwise noted.

SCP Entry



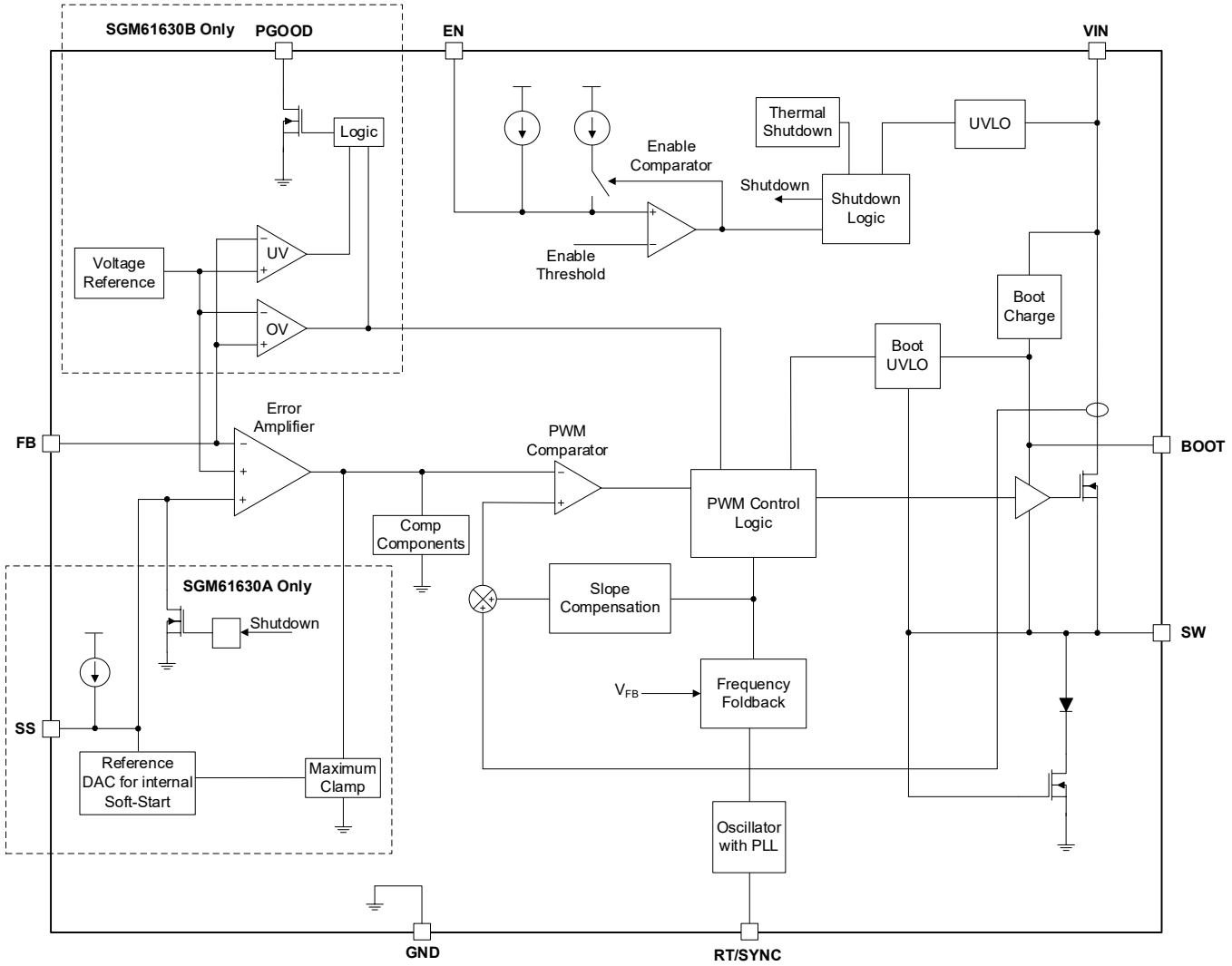
Time (50μs/div)

SCP Recovery



Time (1ms/div)

FUNCTIONAL BLOCK DIAGRAM



NOTE: SS pin is for the SGM61630A version and PGOOD pin is for the SGM61630B version.

Figure 2. SGM61630 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61630 is a 60V Buck converter with integrated high-side N-MOSFET (140mΩ) power switch and 3A continuous output current capability. The minimum operating input voltage of the device is 4.3V. The quiescent current is 50μA (TYP). When the device is disabled, the shutdown current reduces to 2μA.

The SGM61630 uses peak current mode control with power-save mode at light loads to achieve high efficiency. The device is internally compensated, which reduces design time.

The EN pin is internally pulled up by a current source that can keep the device enable if EN pin is floating. It can also be used to increase the input UVLO threshold using a resistor divider.

The bootstrap diode is integrated and only a small capacitor between BOOT and SW pins (C_{BOOT}) is needed for the N-MOSFET gate driving bias. A separate UVLO circuit monitors C_{BOOT} voltage and turns the high-side switch off if this voltage falls below a preset threshold.

The switching frequency is adjusted using a resistor to ground connected to the RT/SYNC pin. It is also can be synchronized to an external clock signal with 210kHz to 2400kHz.

Over-voltage protection (OVP) circuit is designed to minimum the output over-voltage transients. When this comparator detects an OVP (V_{FB} > 110% × V_{REF}), the switch is kept off until the V_{FB} falls below 107% of the V_{REF}. The SS pin internal current source allows soft-start time adjustments with a small external capacitor. During startup and over-current, the frequency is reduced (frequency fold-back) to allow easy maintenance of low inductor current. The thermal shutdown provides an additional protection in fault conditions.

Minimum Input Voltage (4.3V) and UVLO

The recommended minimum operating input voltage is 4.3V. It may operate with lower voltages that are above the V_{IN} rising UVLO threshold (3.85V TYP). If V_{IN} falls below its falling UVLO threshold, the device will stop switching.

Enable Input and UVLO Adjustment

An internal current source pull-up keeps the EN pin voltage at high state by default. The device will enable if the EN pin voltage exceeds the enable threshold of 1.17V and V_{IN} exceeds its UVLO threshold. The device will disable if the EN voltage is externally pulled low or the VIN pin voltage falls below its UVLO threshold.

If an application requires a higher V_{IN} UVLO threshold, an external V_{IN} UVLO adjustment circuit is recommended in Figure 3. Figure 3 shows how UVLO and hysteresis are increased using R_{EN1} and R_{EN2}. A 3.7μA additional current is injected to the divider when EN pin voltage exceeds V_{ENH} (1.17V TYP) to provide hysteresis and it will be removed when EN pin voltage is below V_{ENL} (1.12V TYP). Use Equations 1 and 2 to calculate these resistors. V_{START} is the input start (turn-on) threshold voltage and V_{STOP} is the input stop (turn-off) threshold voltage.

$$R_{EN1}=\frac{(V_{START}-V_{STOP})-V_{EN\_HYS}\times\frac{V_{START}}{V_{ENH}}}{3.7\mu A+V_{EN\_HYS}\times\frac{1\mu A}{V_{ENH}}} \quad (1)$$

$$R_{EN2}=\frac{V_{ENH}}{\frac{V_{START}-V_{ENH}}{R_{EN1}}+1\mu A} \quad (2)$$

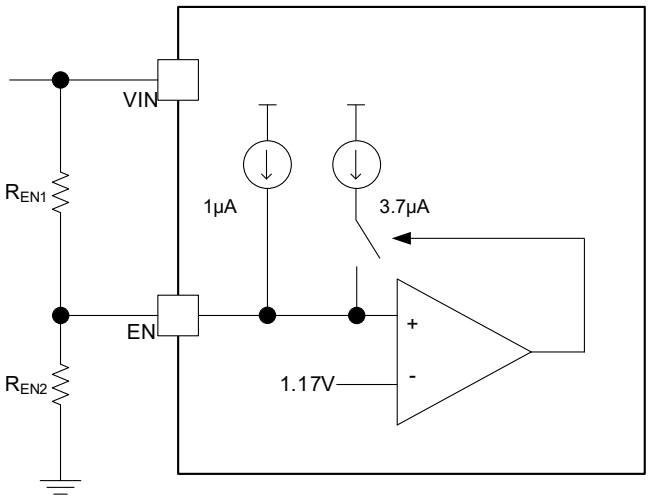


Figure 3. V_{IN} UVLO Adjustment Circuit

DETAILED DESCRIPTION (continued)

Switching Frequency and Timing Resistor (RT/SYNC Pin)

The switching frequency can be set from 200kHz to 2500kHz by a timing resistor (R_T) placed between the RT/SYNC and GND pins. There is an internal bias voltage (0.5V TYP) on the RT/SYNC pin during the RT mode and must have a resistor to ground to set the switching frequency. Use Equation 3 to find the R_T resistance for any desired switching frequency (f_{SW}).

$$f_{SW}\,(kHz)=17700\times R_T\,(k\Omega)^{-0.918} \quad (3)$$

Synchronization to RT/SYNC Pin

The internal oscillator also can synchronize to an external logic clock applied to the RT/SYNC pin (see Figure 4) in the 210kHz to 2400kHz range. The SW rising edge (switch turn-on) is synchronized with the SYNC falling edge. The SYNC low and high levels must be less than 0.3V and more than 2.0V and have a pulse width larger than 30ns. So when the SYNC source is removed, the DC resistance seen between the RT/SYNC and GND pins determines the default switching frequency (f_{SYNC}).

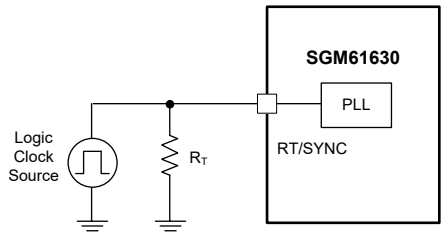


Figure 4. Synchronization to External Clock

Low Dropout Operation and Bootstrap Gate Driving (BOOT Pin)

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. X5R or better dielectric types are recommended. The capacitor must have a 10V or higher voltage rating. The BOOT capacitor is refreshed when the high-side switch is off and the external low-side diode conducts.

The SGM61630 operates at maximum duty cycle when input voltage is closed to output voltage if the bootstrap voltage (V_{BOOT} - V_{SW}) is greater than its UVLO threshold. When the bootstrap voltage falls below the UVLO threshold, the high-side switch is turned off, and the integrated low-side switch is turned on to recharge the BOOT capacitor. After the recharge, the high-side switch is turned on again to regulate the output.

External Soft-Start Adjustment (SGM61630A Only)

The SGM61630A has an external soft-start (SS) pin for adjustable startup time. It is recommended to add a soft-start capacitor (C_{SS}) between the SS and GND pins to set the soft-start time. The internal I_{SS} = 3μA current charges C_{SS} and provides a linear voltage ramp on the SS pin. Use Equation 4 to calculate the soft-start time.

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF)\times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \quad (4)$$

Power-Good (SGM61630B Only)

The SGM61630B has a power-good (PGOOD) pin for indicate whether the output voltage in the desired level. The PGOOD pin is open-drain output that requires 10kΩ to 100kΩ resistor pulled up to an DC voltage(not exceeds 5V).

As shown in Figure 5, when the FB voltage is within the power-good range, the PGOOD switch is turned off and the PGOOD pin is pulled up to high. When the FB voltage is outside the power-good range, the PGOOD switch is turned on and the PGOOD pin is pulled down to low.

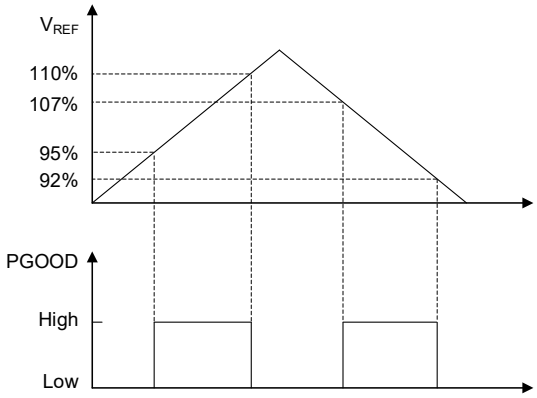


Figure 5. Power-Good Flag

DETAILED DESCRIPTION (continued)

Slope Compensation

Without implementing some slope compensation, the PWM pulse widths will be unstable and oscillatory at duty cycles above 50%. To avoid sub-harmonic oscillations in this device, an internal compensation ramp is added to the measured switch current before comparing it with the control signal by the PWM comparator.

Power-Save Mode

At light loads the SGM61630 enters Pulse-Skipping Mode (PSM) to keep its high efficiency by lowering the number of switching pulses. When the peak inductor current is below PSM current threshold, the corresponding internal COMP voltage (V_{COMP}) will be lower than 410mV. The device will enter PSM in such conditions. In PSM mode, V_{COMP} is internally clamped at 350mV that inhibits the high-side MOSFET switching, the device draws only 50μA (TYP) input quiescent current. The device can exit PSM if V_{COMP} rises above 410mV.

Over-Current Protection and Frequency Fold-back

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the HS current sensing starts a short time (blanking time) after the HS switch is turned on. The sensed HS switch current is continuously compared with the current limit threshold and when the HS current reaches to that threshold, the HS switch is turned off. If the output is overloaded, V_{OUT} drops and V_{COMP} is increases by EA to compensate that. However, the EA output (V_{COMP}) is clamped to a maximum value.

The natural OCP of the peak current mode control may not be able to provide a complete protection when an output short-circuit occurs and an extra protection mechanism for short-circuit is needed. During an output short, inductor current may runaway above over-current limits because of the high input voltage and the minimum controllable on-time. During the output short, the inductor current decreases slowly because a small negative diode forward voltage appears across the inductor during the off-time, as a result the inductor current cannot be reset. In these conditions, current can saturate the inductor and the current may even increase higher until the device is damaged. In the SGM61630, this problem is effectively solved by increasing the off-time during short-circuit by reducing the switching frequency (frequency fold-back). As the output voltage drops and the FB pin voltage falls from 0.75V to 0V, the frequency will be divided by 1, 2, 4 and 8.

Over-Voltage Transient Protection

When an overload or an output fault condition is removed, large overshoots may occur on the output. The SGM61630 includes OVP circuit to reduce such over-voltage transients. If V_{FB} voltage exceeds 110% of the V_{REF} threshold, the high-side switch is turned off. When it returns below 107% of the V_{REF}, the switch is released again.

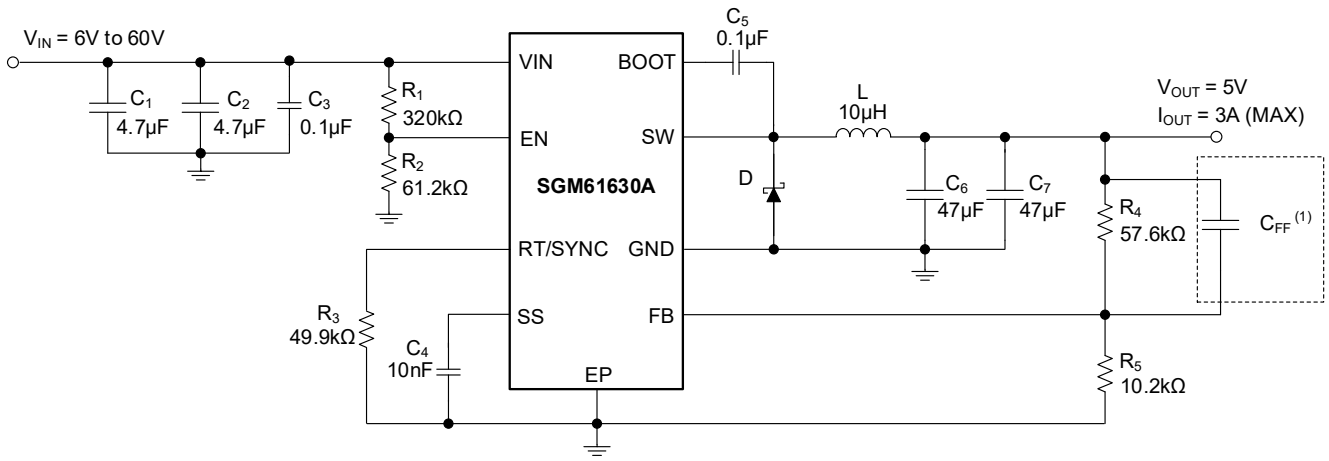
Thermal Shutdown (TSD)

If the junction temperature (T_J) exceeds +170℃, the TSD protection circuit will stop switching to protect the device from overheating. The device will automatically restart with a power up sequence when the junction temperature drops below +150℃.

APPLICATION INFORMATION

A typical application circuit for the SGM61630A as a Buck converter is shown in Figure 6. It is used for converting a 6V to 60V supply voltage to a lower voltage level supply voltage (5V) suitable for the system.

Typical Application



NOTE: 1. In low input voltage condition, C_{FF} = 33pF is recommended.

Figure 6. 5V Output SGM61630A Design Example

Design Requirements

The design parameters given in Table 1 are used for this design example.

Table 1. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP). 6V to 60V
Start Input Voltage (Rising V_{IN})	7V
Stop Input Voltage (Falling V_{IN})	5.5V
Input Ripple Voltage	360mV, 3% of V_{IN_TYP}
Output Voltage	5V
Output Voltage Ripple	50mV, 1% of V_{OUT}
Output Current Rating	3A
Transient Response 1.5A to 3A Load Step	250mV, 5% of V_{OUT}
Operation Frequency	500kHz

Switching Frequency Selection

Several parameters such as losses, inductor and capacitors sizes and response time are considered in selection of the switching frequency. Higher frequency increases the switching and gate charge losses and lower frequency requires larger inductance and capacitances and results in larger overall physical size and higher cost. Therefore, a tradeoff is needed between losses and component size. If the application is noise-sensitive to a frequency range, the frequency should be selected out of that range.

For this design, a lower switching frequency of 500kHz is chosen and a 49.9kΩ resistor can be chosen for R_3 according to Equation 3.

APPLICATION INFORMATION (continued)

Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61630. At least 3μF of effective capacitance (after derating) is needed on the VIN input. In some applications additional bulk capacitance may also be required for the V_{IN} input, for example, when the SGM61630 is more than 5cm away from the input source. The V_{IN} capacitor ripple current rating must also be greater than the maximum input current ripple. The input current ripple can be calculated using Equation 5 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 3A, yields an RMS input ripple current of 1.5A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For this design, a ceramic capacitor with at least 100V voltage rating is required to support the maximum input voltage. So, two 4.7μF/100V capacitors in parallel are selected for V_{IN} to cover all DC bias, thermal and aging deratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 6. In this example, the total effective capacitance of the two 4.7μF/100V capacitors is around 8μF at 12V input, and the input voltage ripple is 200mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (6)$$

It recommended to place an additional small size 0.1μF ceramic capacitor right beside the VIN and GND pins (anode of the diode) for high frequency filtering.

Inductor Design

Equation 7 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions especially if a hard-saturation core type inductor (such as ferrite) is chosen. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 20% to 40% ripple is selected (K_{IND} = 0.2 ~ 0.4). Choosing a higher K_{IND} value reduces the selected inductance, but a too high K_{IND} factor may result in insufficient slope compensation.

$$L = \frac{V_{IN} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (7)$$

In this example, the calculated inductance will be 10.18μH with K_{IND} = 0.3, so the nearest larger inductance of 10μH is selected. The ripple, RMS and peak inductors current calculations are summarized in Equations 8, 9 and 10 respectively.

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (8)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (9)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (10)$$

Note that during startup, load transients or fault conditions the peak inductor current may exceed the calculated I_{L_PEAK}. Therefore, it is always safer to choose the inductor saturation current higher than the current limit.

APPLICATION INFORMATION (continued)

External Diode

An external power diode between the SW and GND pins is needed for the SGM61630 to complete the converter. This diode must tolerate the application's absolute maximum ratings. The reverse blocking voltage must be higher than V_{IN_MAX} and its peak current must be above the maximum inductor current. Choose a diode with small forward voltage drop for higher efficiency. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 60V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SGM61630.

Output Capacitor

Three primary criteria must be considered for design of the output capacitor (C_{OUT}):

1. The converter pole location.
2. The output voltage ripple.
3. The transient response to a large change in load current.

The selected output capacitor value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 11 can be used to calculate the minimum output capacitance that is needed to supply a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (11)$$

where:

ΔI_{OUT} is the change in output current.
ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient from 1.5A to 3A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V and ΔI_{OUT} = 1.5A, the minimum required capacitance will be 24μF. Note that the impact of output capacitor ESR on the transient is not considered in Equation 11. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient. However, for aluminum electrolytic and tantalum capacitors, or high current power supplies, the ESR contribution to ΔV_{OUT} must be considered.

When the load steps down, the excess inductor current will charge the capacitor and the output voltage will overshoot. The catch diode current cannot discharge C_{OUT}, so C_{OUT} must be large enough as given in Equation 12 to absorb the excess inductor energy with limited over-voltage. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 12 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^2} \quad (12)$$

where:

I_{OUT_H} is the high level of the current step.
I_{OUT_L} is the low level of the current step.

APPLICATION INFORMATION (continued)

For example, if the acceptable transient from 3A to 1.5A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V, the minimum required capacitance will be 26.3μF.

Equation 13 can be used for the output ripple criteria and finding the minimum output capacitance needed.

V_{OUT_RIPPLE} is the maximum acceptable ripple. In this example, the allowed ripple is 50mV that results in minimum capacitance of 4.5μF.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (13)$$

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 13. For a specific output capacitance value, use Equation 14 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (14)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a 2 × 47μF/25V X5R ceramic capacitor with 1.5mΩ of ESR is used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 15 calculates the RMS current that the output capacitor must support.

$$I_{COUT\_RMS} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L \times f_{SW}} \quad (15)$$

Bootstrap Capacitor Selection

It is recommended to use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_5).

UVLO Setting

The V_{IN} UVLO can be programmed using an external voltage divider on the EN pin of the SGM61630. In this design R_1 is connected between the VIN and EN pins and R_2 is connected between EN and GND (see Figure 6). The UVLO has two thresholds (Hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 7V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input voltage falls below 5.5V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 320kΩ and R_2 = 61.2kΩ.

Feedback Resistors Setting

Use resistor dividers (R_4 and R_5) to set the output voltage using Equation 16.

$$R_4 = R_5 \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}} \right) \quad (16)$$

For this example, 57.6kΩ was selected for R_4 and 10.2kΩ was selected for R_5.

APPLICATION INFORMATION (continued)

Layout Considerations

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast raising/falling voltages that can couple through stray capacitances to other signal paths, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. Following the guidelines provided here are necessary to design a good layout:

- Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R or X7R or better dielectric) placed as close as possible to VIN pin and the catch diode anode pin.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections, SW pin and the catch diode.
- Connect the device GND pin directly to the thermal pad copper area under the IC device.
- Stitch the thermal pad to the internal ground planes and the back side of the PCB directly under the IC using multiple thermal vias.
- Use a short and wide path for routing the SW pin to the cathode of the catch diode on the same layer and to the output inductor.
- Keep the SW area minimal and away from sensitive signals like FB input and divider resistors or RT/SYNC to avoid capacitive noise coupling.
- Top side GND plane that is connected to the thermal pad provides the best heat removal path for the IC. It should be large enough for designs that operate with full rated loads. Thicker copper planes can improve heat dissipation.
- Place the RT resistor (R_3) as close as possible to the RT/SYNC pin with short routes.

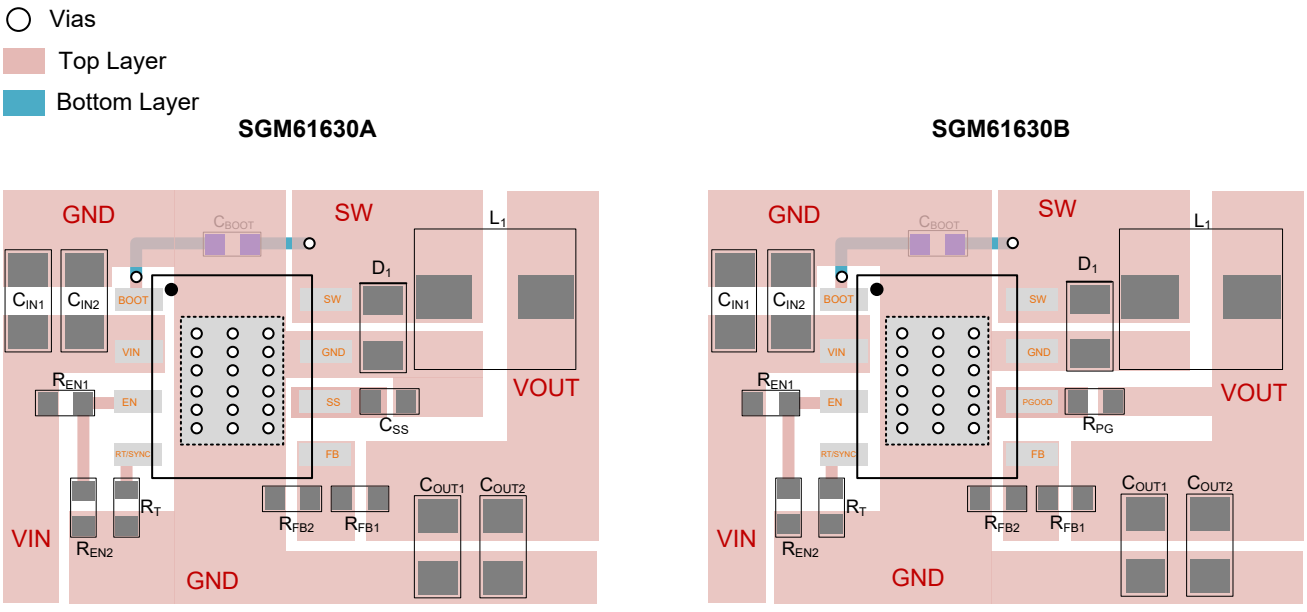


Figure 7. Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DECEMBER 2023 - REV.A.2 to REV.A.3	Page
Updated Application Information	15, 16, 18

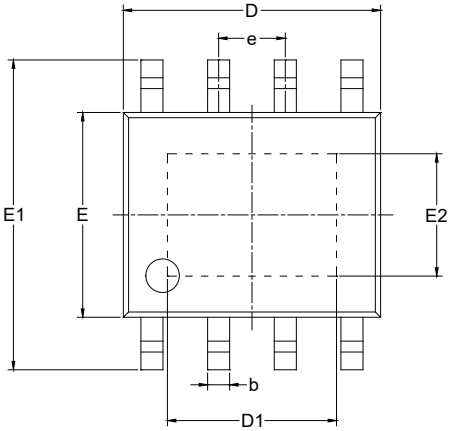
JUNE 2023 - REV.A.1 to REV.A.2	Page
Updated Absolute Maximum Ratings	2

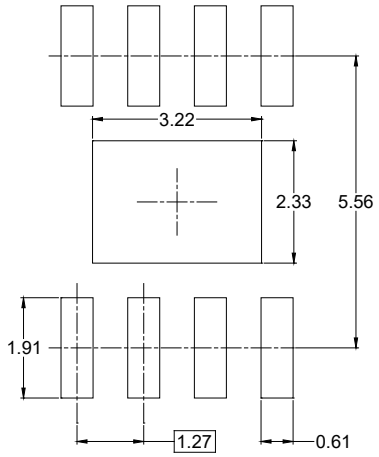
MARCH 2023 - REV.A to REV.A.1	Page
Changed Layout	19

Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

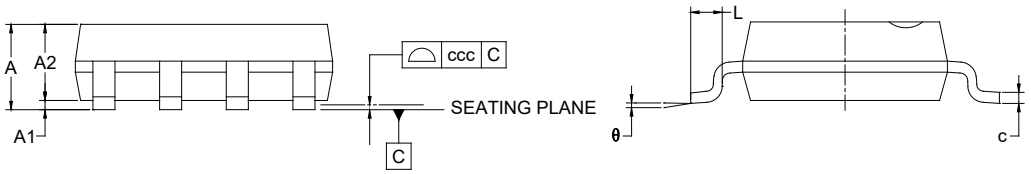
PACKAGE OUTLINE DIMENSIONS

SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

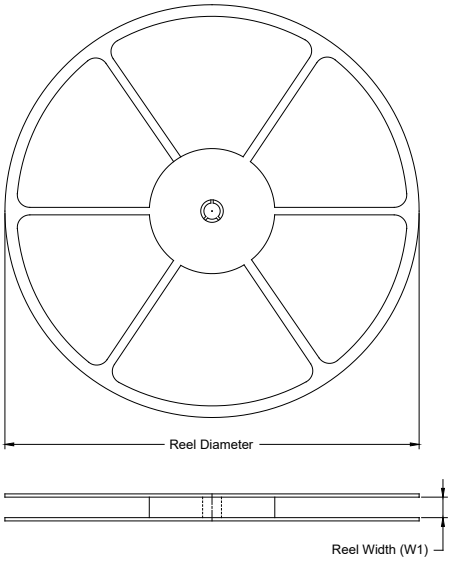


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

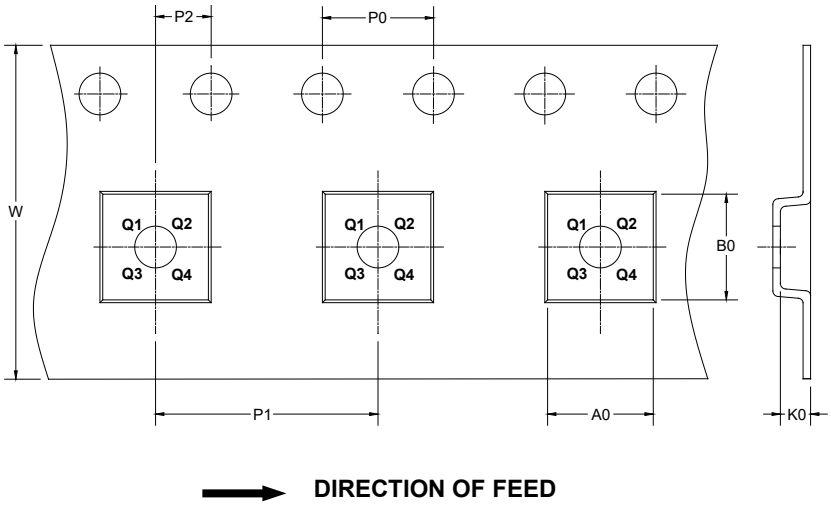
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



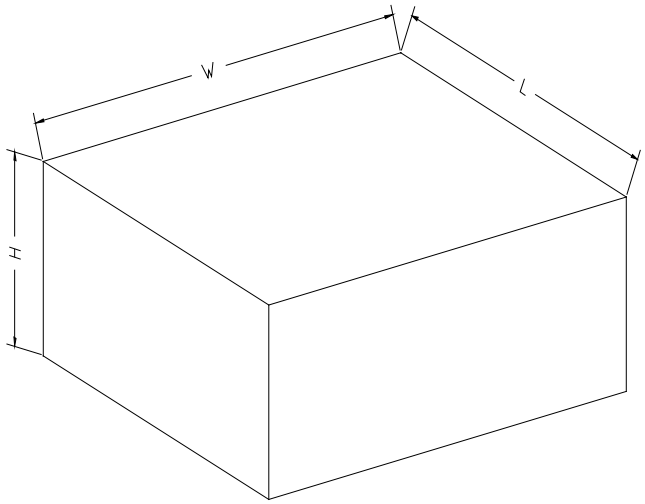
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002