74HC373
Octal D-Type Transparent Latch with 3-State Outputs

GENERAL DESCRIPTION

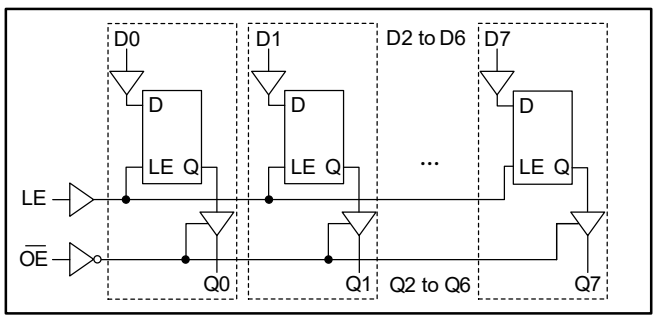
The 74HC373 is an 8-bit D-type transparent latch with 3-state outputs that is designed for 2.0V to 5.5V V_{CC} operation.

The device is provided with a latch enable (LE) input and an output enable ($\overline{OE}$) input. When LE is set high, data at the inputs gets access to the latches and the latches are transparent, the latch outputs will vary with corresponding data inputs. When LE is set low, the latches store data that appeared on the inputs for a setup time before the high-to-low transition of LE. When $\overline{OE}$ is high, all outputs are in high-impedance state. $\overline{OE}$ has no influence on the state of the latches.

The clamp diodes of inputs allow the use of current limiting resistors to connect inputs to the voltage exceeding supply voltage.

The 74HC373 is available in Green SOIC-20 and TSSOP-20 packages. It operates over an ambient temperature range of -40℃ to +125℃.

LOGIC DIAGRAM



FEATURES

- **Wide Operating Voltage Range: 2.0V to 5.5V**
- **+7.8mA/-7.8mA Output Current**
- **CMOS Low Power Consumption**
- **3-State Non-Inverting Outputs Suitable for Bus-Oriented Applications**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-20 and TSSOP-20 Packages**

FUNCTION TABLE

CONTROL INPUT		INPUT	INTERNAL LATCHES	OUTPUT
$\overline{OE}$	LE	Dn		Qn
L	H	L	L	L
L	H	H	H	H
L	L	I	L	L
L	L	h	H	H
H	*X*	*X*	*X*	Z

H = High voltage level.

h = High voltage level one setup time before the high-to-low transition of LE.

L = Low voltage level.

I = Low voltage level one setup time before the high-to-low transition of LE.

Z = High-impedance state.

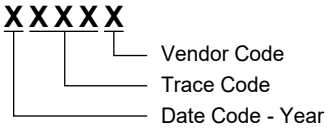
X = Don't care.

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74HC373	SOIC-20	-40℃ to +125℃	74HC373XS20G/TR	74HC373XS20 XXXXX	Tape and Reel, 1500
	TSSOP-20	-40℃ to +125℃	74HC373XTS20G/TR	0MDXTS20 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CC} ..... -0.5V to 7.0V
Input Voltage Range, V_I (2) .... -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Output Voltage Range, V_O (2) -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Input Clamp Current, I_{IK} (V_I < 0V or V_I > V_{CC})..... ±20mA
Output Clamp Current, I_{OK} (V_O < 0V or V_O > V_{CC}) ..... ±20mA
Continuous Output Current, I_O (V_O = 0V to V_{CC}) ..... ±35mA
Continuous Current through V_{CC} or GND..... ±70mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} .....2.0V to 5.5V
Input Voltage Range, V_I..... 0V to V_{CC}
Output Voltage Range, V_O..... 0V to V_{CC}
Output Current, I_O ..... ±7.8mA
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 2.0V..... 625ns/V (MAX)
V_{CC} = 4.5V..... 139ns/V (MAX)
V_{CC} = 5.5V..... 83ns/V (MAX)
Operating Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

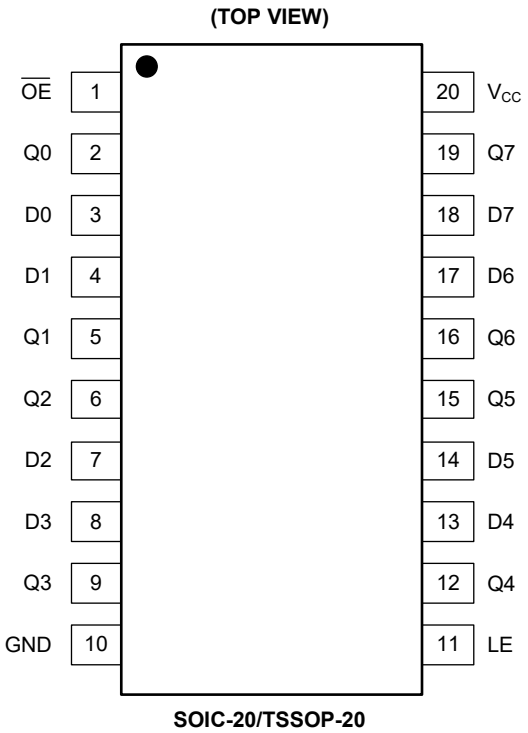
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$\overline{OE}$	Output Enable Input (Active-Low).
2, 5, 6, 9, 12, 15, 16, 19	Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	Outputs.
3, 4, 7, 8, 13, 14, 17, 18	D0, D1, D2, D3, D4, D5, D6, D7	Data Inputs.
10	GND	Ground.
11	LE	Latch Enable Input (Active-High).
20	V_{CC}	Power Supply.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V	Full	1.50			V
		V_{CC} = 4.5V	Full	3.15			
		V_{CC} = 5.5V	Full	3.85			
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V	Full			0.50	V
		V_{CC} = 4.5V	Full			1.35	
		V_{CC} = 5.5V	Full			1.65	
High-Level Output Voltage	V_{OH}	V_{CC} = 2.0V, I_O = -20μA	Full	1.95	1.995		V
		V_{CC} = 4.5V, I_O = -20μA	Full	4.45	4.495		
		V_{CC} = 5.5V, I_O = -20μA	Full	5.45	5.495		
		V_{CC} = 4.5V, I_O = -6mA	Full	3.85	4.300		
		V_{CC} = 5.5V, I_O = -7.8mA	Full	4.80	5.270		
Low-Level Output Voltage	V_{OL}	V_{CC} = 2.0V, I_O = 20μA	Full		0.005	0.05	V
		V_{CC} = 4.5V, I_O = 20μA	Full		0.005	0.05	
		V_{CC} = 5.5V, I_O = 20μA	Full		0.005	0.05	
		V_{CC} = 4.5V, I_O = 6mA	Full		0.170	0.40	
		V_{CC} = 5.5V, I_O = 7.8mA	Full		0.210	0.40	
Input Leakage Current	I_I	V_{CC} = 5.5V, V_I = V_{CC} or GND	Full		±0.1	±1	μA
Off-State Output Current	I_{OZ}	V_{CC} = 5.5V, V_I = V_{IH} or V_{IL}, V_O = V_{CC} or GND	Full		±0.1	±5	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A	Full		0.1	5	μA
Input Capacitance	C_I		+25℃		3.5		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, C_L = 50pF, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	Dn to Qn, see Figure 2	V_{CC} = 2.0V	Full	1	40	110	ns
			V_{CC} = 4.5V	Full	1	12	35	
			V_{CC} = 5.5V	Full	1	9	30	
		LE to Qn, see Figure 3	V_{CC} = 2.0V	Full	1	38	100	ns
			V_{CC} = 4.5V	Full	1	13	35	
			V_{CC} = 5.5V	Full	1	10	30	
Enable Time (2)	t_{EN}	$\overline{OE}$ to Qn, see Figure 4	V_{CC} = 2.0V	Full	1	31	100	ns
			V_{CC} = 4.5V	Full	1	9	35	
			V_{CC} = 5.5V	Full	1	7	30	
Disable Time (2)	t_{DIS}	$\overline{OE}$ to Qn, see Figure 4	V_{CC} = 2.0V	Full	1	15	30	ns
			V_{CC} = 4.5V	Full	1	8	25	
			V_{CC} = 5.5V	Full	1	8	25	
Transition Time (2)	t_T	Qn, see Figure 2 and Figure 3	V_{CC} = 2.0V	Full	1	25	80	ns
			V_{CC} = 4.5V	Full	1	7	18	
			V_{CC} = 5.5V	Full	1	6	15	
Pulse Width	t_w	LE high, see Figure 3	V_{CC} = 2.0V	Full	80			ns
			V_{CC} = 4.5V	Full	16			
			V_{CC} = 5.5V	Full	14			
Setup Time	t_{SU}	Dn to LE, see Figure 5	V_{CC} = 2.0V	Full	40			ns
			V_{CC} = 4.5V	Full	18			
			V_{CC} = 5.5V	Full	15			
Hold Time	t_H	Dn to LE, see Figure 5	V_{CC} = 2.0V	Full	5			ns
			V_{CC} = 4.5V	Full	5			
			V_{CC} = 5.5V	Full	5			
Power Dissipation Capacitance (3)	C_{PD}	Per latch, V_I = GND to V_{CC}		+25℃		8.5		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. t_{PD} is the same as t_{PLH} and t_{PHL}. t_{DIS} is the same as t_{PLZ} and t_{PHZ}. t_{EN} is the same as t_{PZL} and t_{PZH}. t_T is the same as t_{THL} and t_{TLH}.
3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = Input frequency in MHz.

   f_o = Output frequency in MHz.

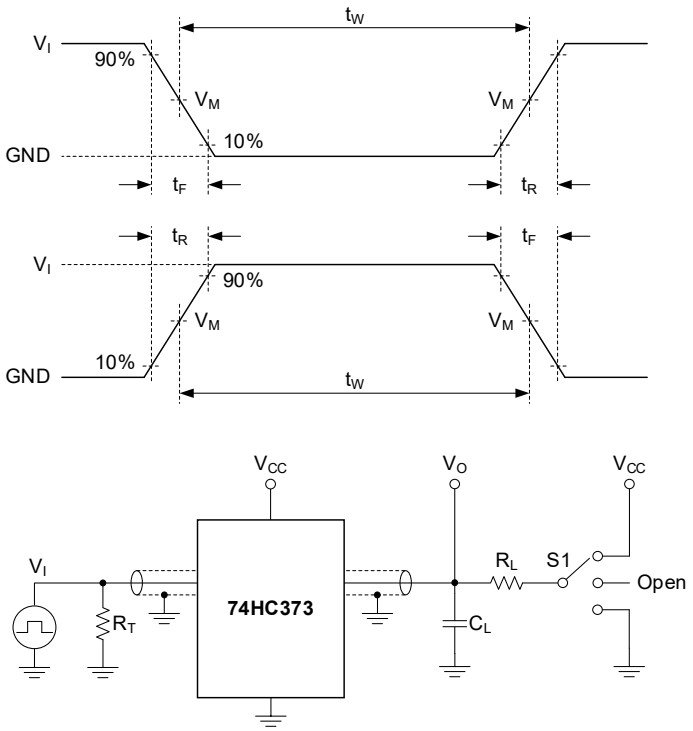
   C_L = Output load capacitance in pF.

   V_{CC} = Supply voltage in Volts.

   N = Number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

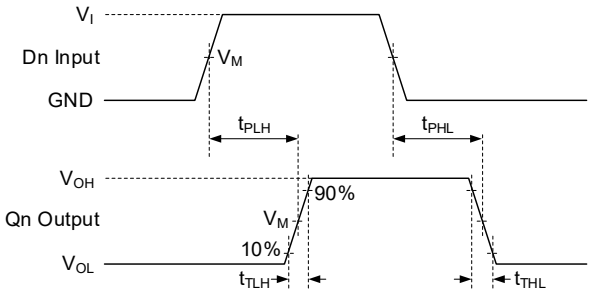
S1: Test selection switch.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

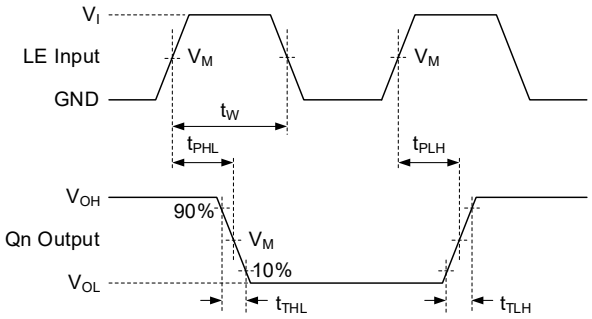
SUPPLY VOLTAGE	INPUT		LOAD		S1 POSITION		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.0V to 5.5V	V_{CC}	≤ 6.0ns	50pF	1kΩ	Open	V_{CC}	GND

WAVEFORMS



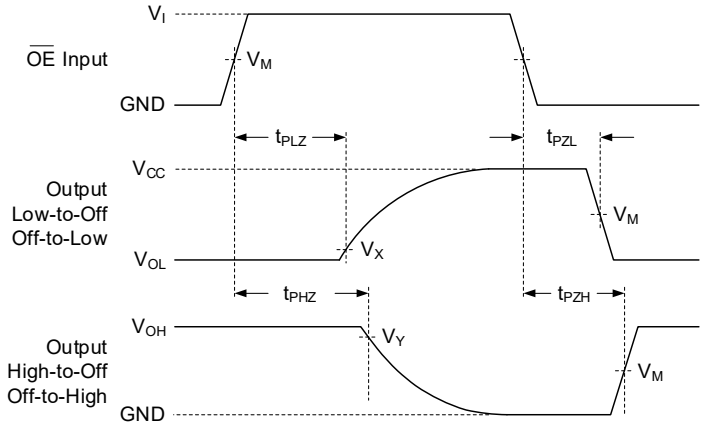
Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Data Input Dn to Output Qn Propagation Delays and Transition Times



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

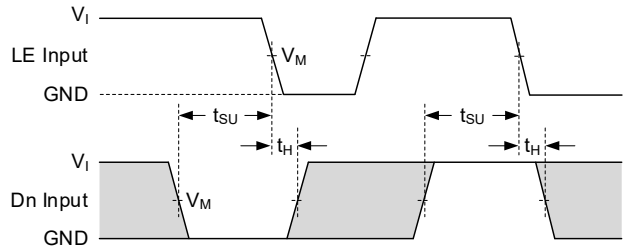
Figure 3. Latch Enable Input LE to Output Qn Propagation Delays, Pulse Width and Transition Times



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 4. Enable and Disable Times

WAVEFORMS (continued)



Test conditions are given in Table 1.

Measurement points are given in Table 2.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5. Data Setup Times and Hold Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT		
V_{CC}	V_I	V_M (1)	V_M	V_X	V_Y
2.0V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}	0.9 × V_{CC}

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 6.0ns.

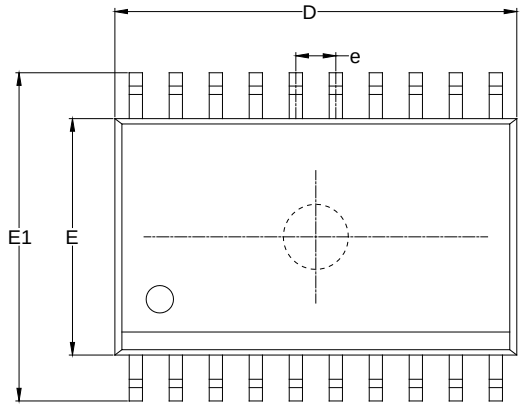
REVISION HISTORY

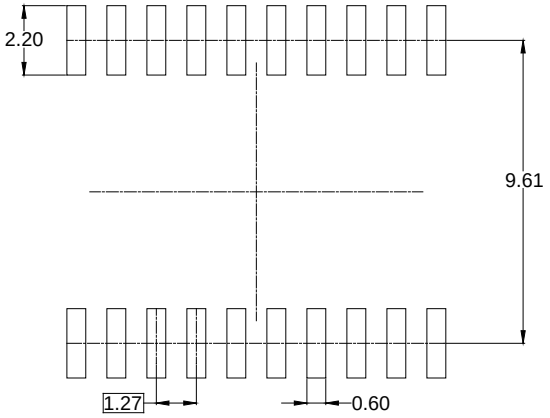
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

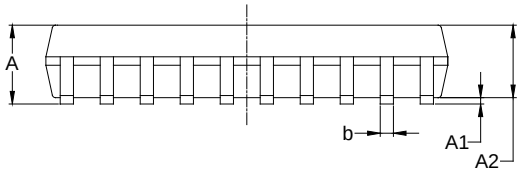
PACKAGE OUTLINE DIMENSIONS

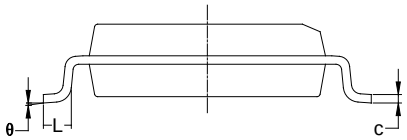
SOIC-20





RECOMMENDED LAND PATTERN (Unit: mm)



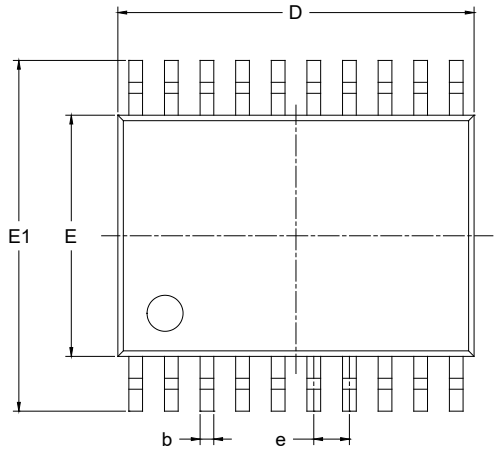


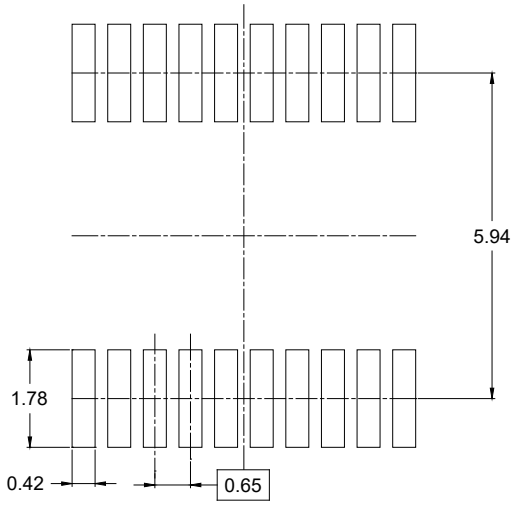
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	2.350	2.650	0.093	0.104
A1	0.100	0.300	0.004	0.012
A2	2.100	2.500	0.083	0.098
b	0.330	0.510	0.013	0.020
c	0.204	0.330	0.008	0.013
D	12.520	13.000	0.493	0.512
E	7.400	7.600	0.291	0.299
E1	10.210	10.610	0.402	0.418
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

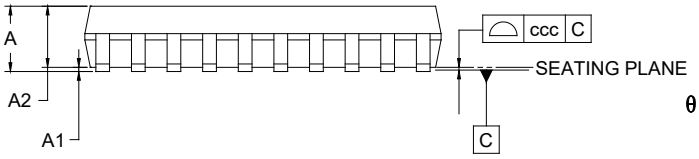
PACKAGE OUTLINE DIMENSIONS

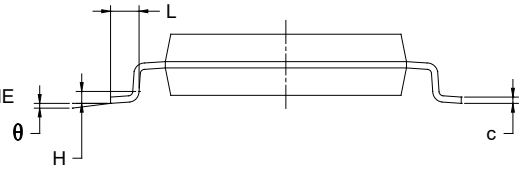
TSSOP-20





RECOMMENDED LAND PATTERN (Unit: mm)



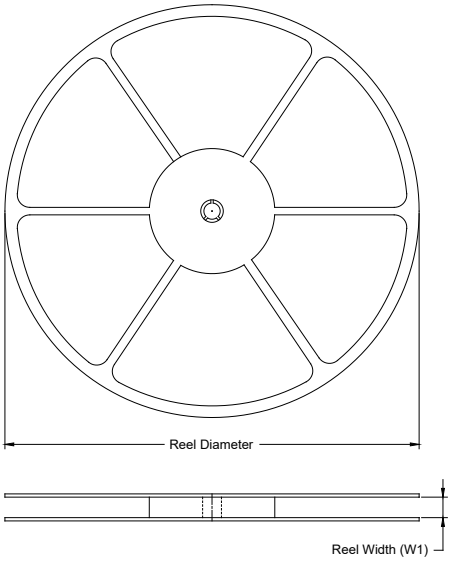


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

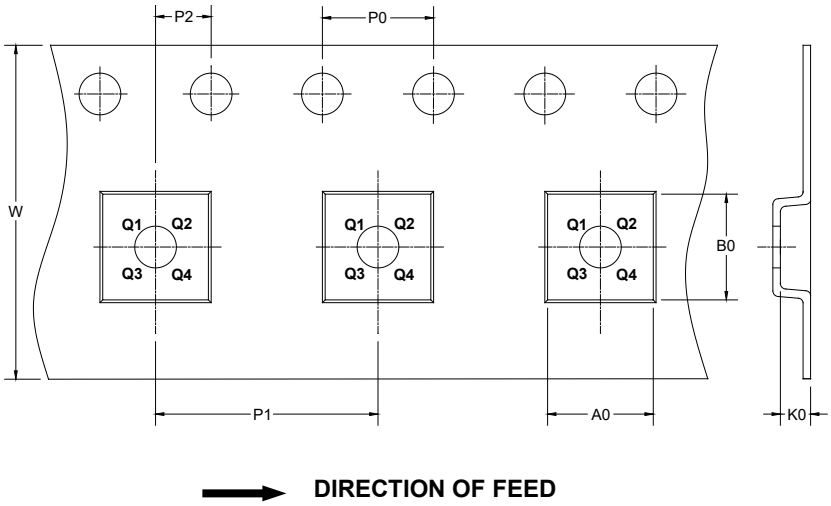
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



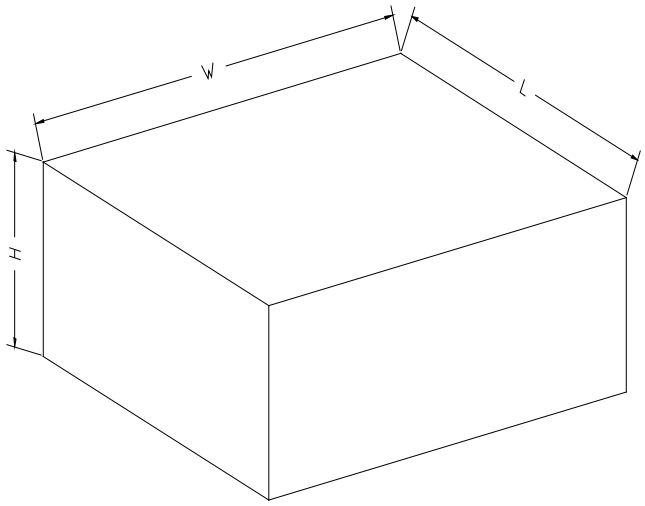
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-20	13″	24.4	10.90	13.30	3.00	4.0	12.0	2.0	24.0	Q1
TSSOP-20	13″	16.4	6.80	6.90	1.50	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002