

SGM40663/SGM40664/SGM40665 SGM40666/SGM40668/SGM40669 High-Current Over-Voltage Protector

GENERAL DESCRIPTION

The SGM40663/4/5/6/8/9 are over-voltage protection devices designed to protect low voltage systems from damage with a high voltage supply up to $+31V_{DC}$ and $+40V_{PEAK}$ (10s with 50mA current limit). They can also withstand surges up to +110V/-400V without damage.

The integrated $28m\Omega$ (TYP) R_{ON} FET allows it to pass through 4.5A continuous current. The FET is turned off when the input voltage exceeds the over-voltage threshold, which can be adjusted between 4V and 22V with the optional external resistors.

When the OVLO input is set below the external OVLO select threshold (0.27V TYP), the SGM40663/4/5/6/8/9 automatically choose the internal trip thresholds that are preset to 22.2V/15.3V/10.5V/6.83V/5.95V/6.35V typically.

The open-drain output (nACOK) indicates a stable power supply between minimum V_{IN} and $V_{\text{OVLO}}.$

The SGM40663/4/5/6/8/9 are available in a Green WLCSP-1.17×1.63-12B package.

FEATURES

- Wide Power Supply Voltage Range: 2.5V to 28V
- Input Voltage up to 40V with 50mA Current Limit for 10s Duration
- Integrated Switch On-Resistance: 28mΩ (TYP)
- Wide Adjustable OVLO Threshold Range: 4V to 22V
- Internal Over-Voltage Protection Thresholds: 22.2V (TYP) (SGM40663)
 15.3V (TYP) (SGM40664)
 10.5V (TYP) (SGM40665)
 6.83V (TYP) (SGM40666)
 5.95V (TYP) (SGM40668)
 - 6.35V (TYP) (SGM40669)
- Up to +110V/-400V Surge Immunity
- Over-Voltage Shutdown Response: 50ns (TYP)
- Start-Up Debounce Time: 15ms
- Soft-Start Function
- Enable Function
- Thermal Shutdown Protection
- Power Good Flag
- Available in a Green WLCSP-1.17×1.63-12B Package

APPLICATIONS

Battery Charging Ports Mobile Phones Tablet Computers

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40663	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40663YG/TR	XXXXX R28YG	Tape and Reel, 3000
SGM40664	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40664YG/TR	XXXXX R29YG	Tape and Reel, 3000
SGM40665	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40665YG/TR	XXXXX R3AYG	Tape and Reel, 3000
SGM40666	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40666YG/TR	XXXXX CBDYG	Tape and Reel, 3000
SGM40668	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40668YG/TR	XXXXX R3BYG	Tape and Reel, 3000
SGM40669	WLCSP-1.17×1.63-12B	-40°C to +85°C	SGM40669YG/TR	XXXXX CF5YG	Tape and Reel, 3000

MARKING INFORMATION

YYYYG

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

Date Code - Year

Trace Code

XXXXX Vendor Code

Serial Number

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.



ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

IN0.3V to 31V ⁽¹⁾
IN (Peak for 10s Duration, 50mA Limit)0.3V to 40V $^{(1)}$
IN
OUT0.3V to V _{IN} + 0.3V
OVLO0.3V to 26.4V
nACOK, nEN0.3V to 6V
IN, OUT Continuous Current ⁽⁴⁾
IN, OUT Peak Current (10ms)8A
Package Thermal Resistance
WLCSP-1.17×1.63-12B, θ _{JA} 103°C/W
Junction Temperature+150°C
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10s)+260°C
ESD Susceptibility
HBM4kV
CDM1kV
Air Gap Discharge on IN Pin (IEC 61000-4-2)20kV
Contact Discharge on IN Pin (IEC 61000-4-2)12kV

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

RECOMMENDED OPERATING CONDITIONS

NOTES:

1. Non-frequent repeated peak voltage during the input surge transient and ESD transient is not subject to this rating value, which may be higher than 40V in the surge test.

2. Surge test in compliance with IEC 61000-4-5 specification. 3. Survives burst pulse up to +110V/-400V with 2Ω series resistance.

4. Continuous current limit may vary with the circuit board thermal dissipation condition.

5. If protection discharging is triggered, the discharging keeps until the supply falls below the hysteresis range. Continuously force driving during discharging with a voltage in the hysteresis range can cause overstress and even damage the device. Supply voltage within the hysteresis range is not recommended.

ESD SENSITIVITY CAUTION

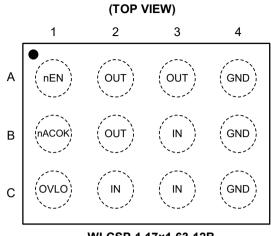
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.



PIN CONFIGURATION



WLCSP-1.17×1.63-12B

PIN DESCRIPTION

PIN	NAME	FUNCTION
A1	nEN	Device Enable Pin. Active low to enable the IN to OUT pass path.
A2, A3, B2	OUT	Output Pin. Internal switch output.
A4, B4, C4	GND	Ground.
B1	nACOK	Open-Drain Flag Output for Power Good. When the input voltage is stable between the minimum V_{IN} and V_{OVLO} , nACOK is driven low. nACOK is high impedance if thermal shutdown occurs.
B3, C2, C3	IN	Input and Device Supply Pin. Use a 0.1µF ceramic capacitor near to the device.
C1	OVLO	Over-Voltage Protection Threshold Adjustment. When the internal threshold is used, set the OVLO to connect to GND. Connect to a resistor divider network to adjust the OVLO threshold.



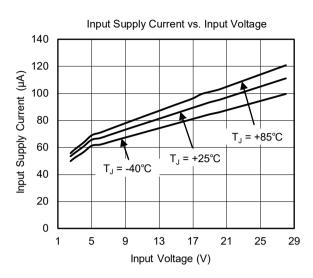
ELECTRICAL CHARACTERISTICS

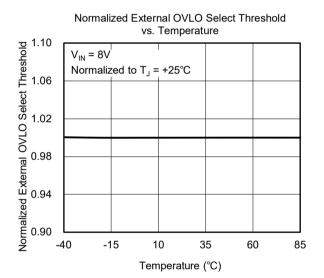
 $(V_{IN} = 2.5V \text{ to } 28V, C_{IN} = 0.1 \mu\text{F}, T_J = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ typical values are at } V_{IN} = 5V, I_{IN} \leq 3A, T_J = +25^{\circ}\text{C}, \text{ unless otherwise noted.})$

PARAMETER	SYMBOL	CONDI	MIN	TYP	MAX	UNITS	
Input Voltage Range	V _{IN}			2.5		28	V
Input Supply Current	l _{in}	V _{IN} = 5V			62	90	μA
OVLO Supply Current	I _{IN_Q}	V_{OVLO} = 3V, V_{IN} = 5V, V_{O}	UT = 0V		65	95	μA
			SGM40663	21.70	22.20	22.74	
			SGM40664	14.96	15.30	15.65	v
		V_{iN} rising	SGM40665	10.29	10.50	10.74	
			SGM40666	6.69	6.83	6.97	
			SGM40668	5.83	5.95	6.07	
Internal Over-Voltage Protection			SGM40669	6.22	6.35	6.50	
Threshold	V _{IN_OVLO}		SGM40663	21.38	21.90		
			SGM40664	14.76	15.10		
			SGM40665	10.17	10.40		
		V _{IN} falling	SGM40666	6.61	6.76		
			SGM40668	5.75	5.89		
			SGM40669	6.14	6.28		
V _{BG} Reference	V_{BG}			1.163	1.190	1.215	V
Adjustable OVLO Threshold Range				4		22	V
External OVLO Select Threshold	V _{OVLO_SELECT}			0.24	0.27	0.29	V
Switch On-Resistance	R _{ON}	V _{IN} = 5V, I _{OUT} = 0.5A, T _J = +25°C			28	39	mΩ
OUT Load Capacitance	C _{OUT}	V _{IN} = 5V, T _J = +25°C				1000	μF
OVLO Parasitic Capacitance	C_{P_OVLO}	T _J = +25°C			18		pF
OVLO Input Leakage Current	I _{OVLO}	V _{OVLO} = 1.3V, T _J = +25°C		-100		100	nA
IN Leakage Voltage by OVLO	$V_{\text{IN_LEAK}}$	V_{OVLO} = 20V, V_{IN} = unconnected, R_{OVLO} = 1M Ω				0.2	V
Thermal Shutdown					150		°C
Thermal Shutdown Hysteresis					20		°C
Digital Signal (nACOK, nEN)	1						
nACOK Output Low Voltage	V _{OL}	$V_{I/O}$ = 3.3V, I _{SINK} = 1mA, see Figure 1			0.08	0.32	V
nACOK Leakage Current	I _{ACOK_LEAK}	$V_{I/O}$ = 3.3V, nACOK de-asserted, T _J = +25°C, see Figure 1				1	μA
nEN Input Low Threshold	V _{LTH}					0.4	V
nEN Input High Threshold	V _{HTH}			1.2			V
nEN Input Leakage	I _{nEN_LEAK}	$V_{IN} = 5V, T_{J} = +25^{\circ}C$				1	μA
Timing Characteristics	•				•		
Debounce Time	t _{DEB}	Time from $V_{IN} > 2.5V$ to the time V_{OUT} starts rising, $T_J = +25^{\circ}C$			15		ms
Soft-Start Time	t _{ss}	Time from $V_{IN} > 2.5V$ to soft-start off, T _J = +25°C			30		ms
Switch Turn-On Time	t _{on}	$V_{IN} = 5V, R_L = 100\Omega, C_L O_{OUT}$ from 10%, V_{IN} to 90		1.5		ms	
Switch Turn-Off Time	t _{OFF}	$V_{IN} > V_{IN_OVLO}$ to $V_{OUT} = 80\%$ of V_{IN} , $R_L = 100\Omega$, with 20% overdrive, for the case of using the internal threshold, $T_J = +25^{\circ}C$			50		ns
Switch Turn-Off Propagation Delay	t _{DELAY}	$V_{OVLO} > V_{BG}$ with 20% overdrive to output falling 10%, $R_L = 100\Omega$, for the case of using external threshold, $T_J = +25^{\circ}C$			50		ns

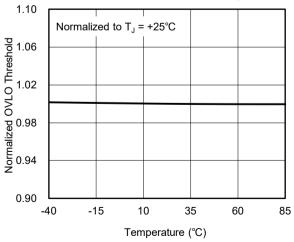


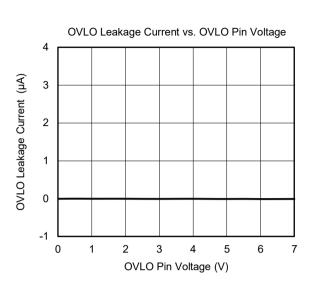
TYPICAL PERFORMANCE CHARACTERISTICS



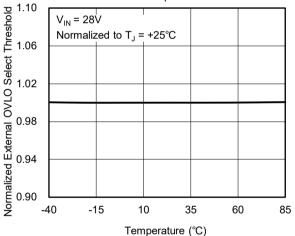


Normalized OVLO Threshold vs. Temperature

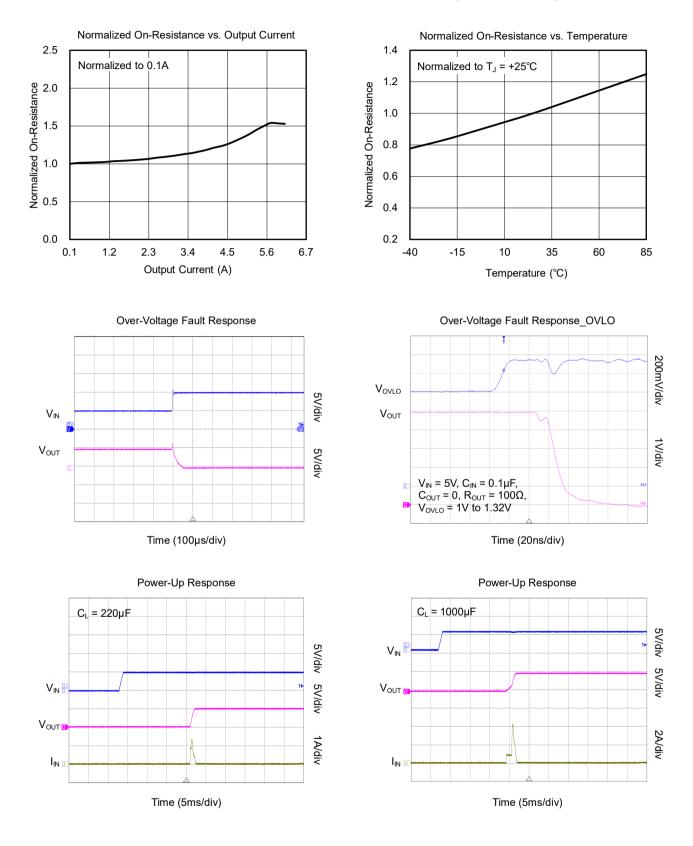






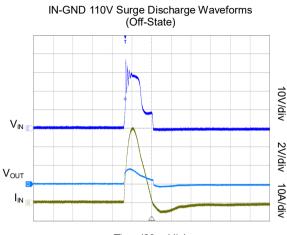


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

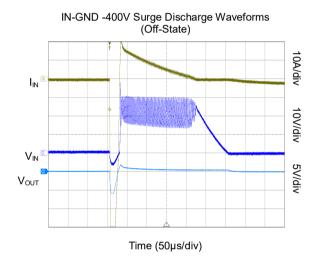


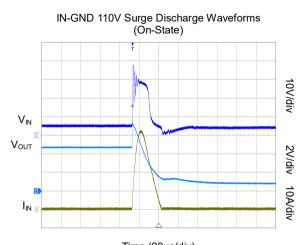


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

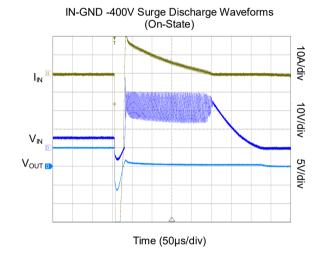


Time (20µs/div)

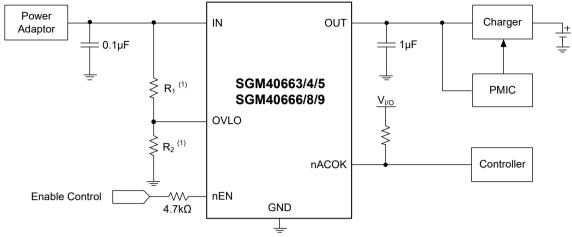








TYPICAL APPLICATION CIRCUIT



NOTE:

1. Voltage divider networks R_1 and R_2 are only used for adjustable OVLO. When using the default OVP threshold, connect OVLO to GND directly.



FUNCTIONAL BLOCK DIAGRAM

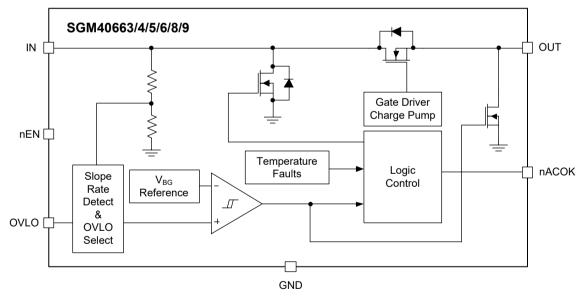
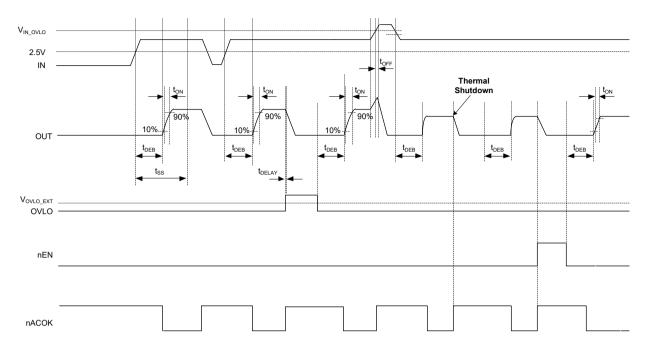


Figure 2. Block Diagram



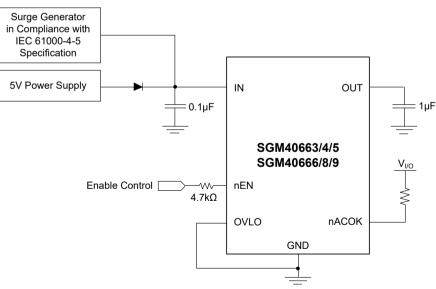
TIMING DIAGRAM



NOTE: The waveforms can not be scaled.



SURGE UP TEST CIRCUIT





DETAILED DESCRIPTION

The SGM40663/4/5/6/8/9 are designed to protect low voltage systems from damage with a high voltage supply up to +31V_{DC} and +40V_{PEAK} (10s with 50mA current limit). The devices can also withstand surges up to +110V/-400V without damage. Surge up tests are performed according to the test circuit in Figure 4. If the input voltage exceeds the over-voltage threshold, the internal 28m Ω (TYP) low R_{oN} FET is turned off to prevent damage to the protected components. A built-in 15ms (TYP) debounce time prevents turning the internal FET on falsely during start-up.

Device Operation

The SGM40663/4/5/6/8/9 have a timing logic controlled charge pump, which is used as gate driver of the internal FET. If the internal trip threshold is used, the charge pump is enabled when $V_{IN} < V_{IN_OVLO}$, while if external trip threshold is used, it is enabled when $V_{OVLO} < V_{OVLO_EXT}$.

The charge pump turns the internal FET on after a 15ms (TYP) debounce delay (see Figure 3), then soft-start function limits the FET inrush current for another 15ms (TYP). Once V_{IN} rises above $V_{\text{OVLO THRESH}}$, the FET is turned off.

Enable Function

The IC has an enable pin that is used to enable or disable the device. Pull nEN high to turn off the internal pass FET, while pull it low to turn on the FET, and the IC enters the start-up routine.

Over-Voltage Lockout (OVLO)

The typical over-voltage lockout (OVLO) thresholds of SGM40663/4/5/6/8/9 are 22.2V/15.3V/10.5V/6.83V/ 5.95V/6.35V respectively.

If the input voltage exceeds the OVP rising trip level, the switch will be turned off in about 50ns. The switch will remain off until $V_{\rm IN}$ falls below the OVP falling trip level.

External Adjustable OVLO

The devices detect the voltage on the OVLO pin to check if an external divider exists.

If the OVLO pin is connected to GND, the OVLO value set internally will be applied.

When an external resistor divider network is connected to OVLO pin and $V_{OVLO} > V_{OVLO_SELECT}$ (0.27V TYP), then this external resistor divider determines the $V_{IN_OVLO_EXT}$. At

present, $V_{IN_OVLO_EXT}$, V_{BG} , and R_1 are known, R_2 can be given by Equation 1:

$$V_{IN_{OVLO}_{EXT}} = V_{BG} \times \left(1 + \frac{R_1}{R_2}\right)$$
(1)

This external resistor divider network is completely independent of the internal resistor divider network.

Note that OVLO pin must not be floating.

Surge Protection

The SGM40663/4/5/6/8/9 integrate a clamping circuit to suppress the input surge voltage. When V_{IN} voltage rises sharply (typically > 4.5V/µs) above 25V, the internal clamping circuit will be triggered to discharge the surge energy to the ground.

Note that when the surge threshold is exceeded in the application, it is necessary to ensure the power filter or the current clamp of the power path to avoid triggering the surge by mistake, which may cause overstress damage to the chip.

Thermal Shutdown Protection

The SGM40663/4/5/6/8/9 have the thermal shutdown protection. If the junction temperature exceeds +150 °C (TYP), the internal FET turns off. And the devices exit thermal shutdown if the junction temperature cools down by 20 °C (TYP).

nACOK Output

The device has an open-drain nACOK output that indicates a stable power source to the host. When the input voltage is stable between minimum $V_{\rm IN}$ and $V_{\rm OVLO}$ after debounce delay, nACOK goes to low. A pull-up resistor is set from nACOK to the host system logic I/O voltage. nACOK is high impedance if thermal shutdown occurs.

USB OTG Support

When used in an OTG application, the SGM40663/4/5/6/8/9 can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. Once the voltage at IN exceeds the minimum input voltage of 2.5V and after debounce time, the main power switch will be fully turned on, reducing the voltage drop from OUT to IN significantly. In this mode, the part is able to supply a continuous current up to 3.5A to the OTG load.



APPLICATION INFORMATION

IN Bypass Capacitor

Place a 0.1μ F ceramic bypass capacitor between IN and GND pins as close as possible to the device for most applications. When the power source has significant inductance because of long lead length, the device clamps the overshoot because of LC tank circuit.

Output Capacitor

The soft-start function is provided by the slow turn-on time, which allows the SGM40663/4/5/6/8/9 to charge an output capacitor (up to 1000 μ F typically) without shutting down because of over-current condition.

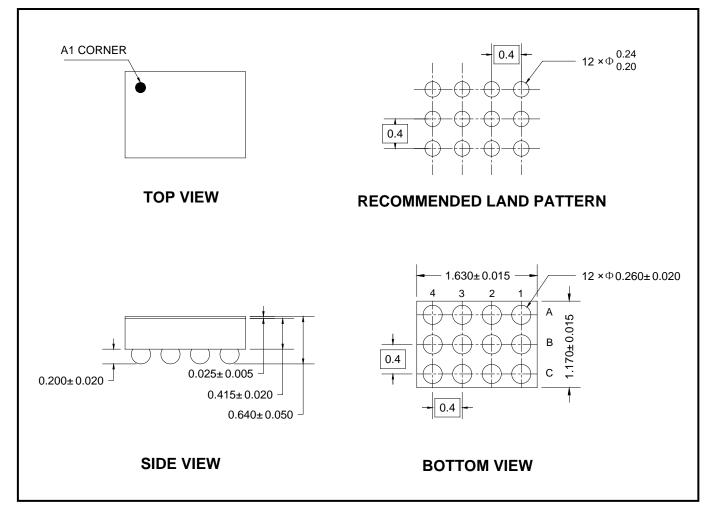
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DECEMBER 2022 – REV.A.3 to REV.A.4	Page
Updated Electrical Characteristics section	5
Updated Timing Diagram section	
Updated Detailed Description section	
JANUARY 2021 – REV.A.2 to REV.A.3	Page
Updated Detailed Description section	
DECEMBER 2020 – REV.A.1 to REV.A.2	Page
Updated Absolute Maximum Ratings section	
NOVEMBER 2020 – REV.A to REV.A.1	Page
Changed SGM40667 part number to SGM40669	All
Changes from Original (JUNE 2020) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

WLCSP-1.17×1.63-12B



NOTE: All linear dimensions are in millimeters.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.17×1.63-12B	7″	9.0	1.32	1.78	0.82	4.0	4.0	2.0	8.0	Q2

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton	
7" (Option)	368	227	224	8	
7"	442	410	224	18	00002

