# SGM40675A
# Over-Voltage Protector Supporting Bidirectional Blocking and Surge Protection

## GENERAL DESCRIPTION

The SGM40675A is an over-voltage protector with a complete set of protection functions. In low-voltage system applications, the OUT terminal can effectively prevent power supply failures up to 28V. Moreover, there is an internal clamping design that protects the product from surge events of up to ±100V. The SGM40675A incorporates a 25mΩ low $R_{ON}$ N-MOSFET to facilitate efficient current flow from IN to OUT.

Whenever the input voltage is higher than the over-voltage threshold, the internal MOSFETs are automatically shut down to prevent over-voltage from causing harm to downstream devices. The two OVP threshold voltages (12.9V/23V) can be programmed through VP pin. The over-voltage protection function can ensure the safe operation of surge events in any state. Additionally, it supports reverse bias blocking, when the device is turned off, the reverse protection function is activated. This function effectively prevents any voltage flowing from the OUT pin to the IN pin.

To further enhance protection, the SGM40675A has improved ESD and thermal protection function against overload conditions.

The SGM40675A is available in a Green WLCSP-2.27×1.86-20B package.

## FEATURES

- **Input Voltage Range: 3V to 24V with Surge up to ±100V**
- **On-Resistance: 25mΩ (TYP)**
- **Continuous Current: 5A**
- **Over-Voltage Threshold**
  - **12.9V: Leave VP Floating**
  - **23V: Connect VP to GND**
- **VSNS Pin: Fixed 5V Output**
- **Fast Over-Voltage Response: 100ns**
- **Input Quiescent Current: 130μA (TYP)**
- **Full Set of Protections**
  - **Soft-Start**
  - **Under-Voltage Protection**
  - **Thermal Shutdown**
  - **Reverse Blocking (OUT to IN)**
- **VSNS, nEN, nWRX, and nFLAG Pins**
- **Available in a Green WLCSP-2.27×1.86-20B Package**

## APPLICATIONS

Tablet
Smart Phone
Mobile Internet Device
Peripheral

## TYPICAL APPLICATION

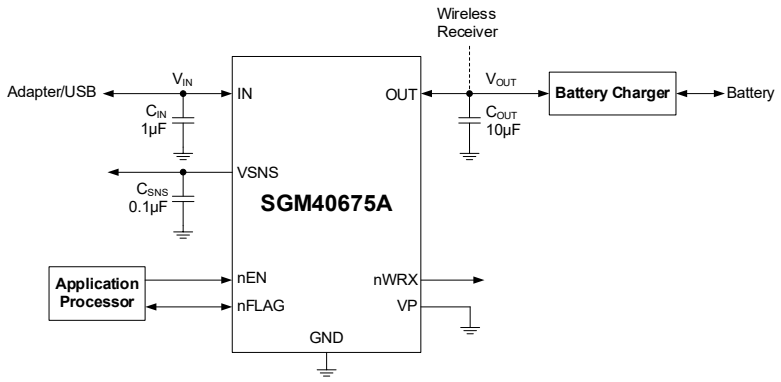


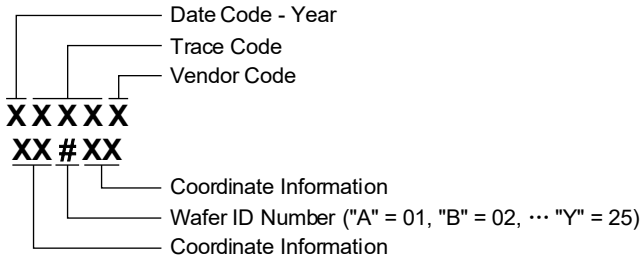

**Figure 1. Typical Application Circuit**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM40675A | WLCSP-2.27×1.86-20B | -40℃ to +125℃ | SGM40675AXG/TR | SGM05G<br>XXXXX<br>XX#XX | Tape and Reel, 3000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

IN Voltage Range ..... -0.3V to 28V
OUT Voltage Range ..... -0.3V to 26V
IN to OUT Voltage (When Off) ..... -26V to 28V
nEN, nFLAG and nWRX Pins ..... -0.3V to 6V
VSNS Pin Voltage ..... -0.3V to 6V
Continuous Current, IN, OUT ..... 5A
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... 4kV
CDM ..... 1kV
Air Gap Discharge on IN Pin (IEC 61000-4-2) ..... 15kV
Contact Discharge on IN Pin (IEC 61000-4-2) ..... 8kV

## RECOMMENDED OPERATING CONDITIONS

IN Voltage Range ..... 3V to 24V
OUT Voltage Range ..... 3V to 24V
Operating Ambient Temperature Range ..... -40℃ to +125℃
Input Capacitance, $C_{IN}$ ..... 10μF (MAX)
OTG Hot Swap Capacitance, $C_{OTG}$ ..... 200μF (MAX)
Output Capacitance, $C_{OUT}$ ..... 20μF (MAX)
VSNS Capacitance, $C_{VSNS}$ ..... 1μF (MAX)

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

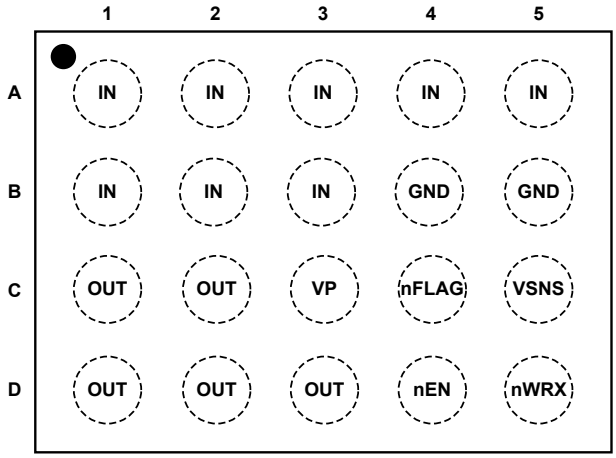
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




WLCSP-2.27×1.86-20B

## PIN DESCRIPTION

| PIN | NAME | TYPE | FUNCTION |
|---|---|---|---|
| A1, A2, A3, A4, A5, B1, B2, B3 | IN | Power | Load Switch Input Pin. |
| B4, B5 | GND | G | Ground. |
| C1, C2, D1, D2, D3 | OUT | Power | Load Switch Output Pin. |
| C3 | VP | Digital Input | Programmable OVP Voltage Pin. The two OVP threshold voltages can be programmed through VP pin. Connect the pin to GND to select 23V (TYP). Float the pin to select 12.9V (TYP). |
| C4 | nFLAG | Digital I/O | nFLAG Pin. When the system detects that OTG mode can be activated/triggered in master mode, the nFLAG pin is pulled high.<br>Slave mode: pull this pin logic low.<br>Master mode: to enter OTG mode, connect to the system digital I/O pin (or equivalent) and pull this pin logic low when connecting IN to the OTG load and supplying power to OUT. |
| C5 | VSNS | Analog Output | IN Pin Voltage Indicator. The internal LDO clamps the IN to 5V and output through the VSNS pin. |
| D4 | nEN | Digital Input | Asserting nEN Pin High Disables the Device.<br>Slave mode: connect the nEN pin to system enable pin.<br>Master mode: pull the nEN pin logic low or GND. |
| D5 | nWRX | Digital I/O | Active-Low Wireless Receiver (WRx) Enable Pin.<br>Slave mode: pull the nWRX pin logic low.<br>Master mode: if the system output control pin is not available, connect it to WRx active-low enable pin. |

## ELECTRICAL CHARACTERISTICS

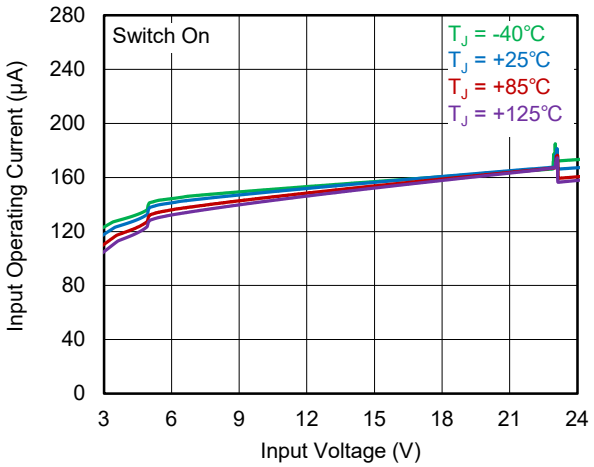
($T_J$ = -40℃ to +125℃, $V_{IN}$/$V_{OUT}$ = 5V, typical values are specified at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Input, OVP (IN to OUT)** | | | | | | | |
| Input Operating Supply Voltage | $V_{IN}$ | | | 3 | | 24 | V |
| Output Operating Supply Voltage | $V_{OUT}$ | | | 3 | | 24 | V |
| Input/Output UVLO Rising Threshold | $V_{UVLO}$ | Initiates soft-start after deglitch time | | 2.5 | 2.7 | 2.9 | V |
| UVLO Hysteresis | $V_{UVLO\_HYS}$ | Falling $V_{IN}$ | | | 0.13 | | V |
| Continuous Output Current | $I_{OUT}$, $I_{OTG}$ | | | | | 5 | A |
| Input OVP Rising Threshold | $V_{OVP}$ | $V_{IN}$ > $V_{OVP}$ enters fault mode | VP = GND | 22 | 23 | 24 | V |
| | | | VP = floating, | 12.3 | 12.9 | 13.5 | V |
| OVP Hysteresis | $V_{OVP\_HYS}$ | Falling $V_{IN}$ | | | 0.5 | | V |
| On-Resistance | $R_{DSON\ (IN-OUT)}$ | $I_{IN}$ = 1A, $T_J$ = +25℃ | | | 25 | 35 | mΩ |
| Input Quiescent Current, Standby/Fault State | $I_{Q\_IN}$ | nEN = high | | | 130 | 200 | μA |
| Input Operating Current | $I_{DD\_IN}$ | nEN = low, $I_{OUT}$ = 0mA | | | 130 | 200 | μA |
| Output Quiescent Current, Standby/Fault State | $I_{Q\_OUT}$ | OTG mode, nEN = high | | | 140 | 210 | μA |
| Output Operating Current | $I_{DD\_OUT}$ | OTG mode, nEN = low, no load | | | 130 | 200 | μA |
| Clamping IN Quiescent Current | $I_{Q\_IN\ CLAMP}$ | $V_{IN}$ = 28V, $V_{OUT}$ = 0V | | | 0.2 | 0.5 | mA |
| | | $V_{IN}$ = 28V, $V_{OUT}$ = 6V | | | 0.2 | 0.5 | |
| OUT Discharge Resistance | $R_{DIS}$ | Measured from OUT to GND during discharge event, $V_{IN}$ = 3V | | | 440 | 650 | Ω |
| OUT Float Voltage | $V_{IN-OUT\ (Float)}$ | Standby state, nFLAG = high and/or nEN = high, $V_{IN}$ = 4.5V to 16V | | | 0.2 | 0.8 | V |
| IN Float Voltage | $V_{OUT-IN\ (Float)}$ | OTG state, nFLAG = high and/or nEN = high, $V_{OUT}$ = 4.5V to 16V | | | 0.03 | 0.5 | V |
| **VSNS** | | | | | | | |
| Regulated Output | $V_{SNS}$ | $V_{IN}$ = 6V to OVP, $I_{SNS}$ = 0mA to 40mA | | 4.6 | 5 | 5.3 | V |
| **Timing Characteristics** | | | | | | | |
| Input Debounce Time | $t_{DEB}$ | $V_{UVLO}$ < $V_{IN}$ < $V_{OVP}$, nEN = low, time delay between IN rising and nWRX rising. | | | 50 | | ms |
| Discharge Time | $t_{DIS}$ | Time after debounce time nWRX rising to OUT soft-start. | | | 50 | | ms |
| Soft-Start Time | $t_{SST}$ | Bidirectional IN to OUT or OUT to IN, time is from 20% to 80% of input. | | | 0.8 | 1.6 | ms |
| Switch Turn-Off Response Time | $t_{OVP\_DLY}$ | $V_{IN}$ > $V_{OVP}$ to $V_{OUT}$ stop rising | | | 100 | | ns |
| Logic Pin Enable Delay (nEN, nFLAG) | $t_{DELAY}$ | Time delay from nEN, nFLAG enable/disable load switch, excluding soft-start | | | 200 | | μs |
| **Digital Signals** | | | | | | | |
| Digital Logic Thresholds (nEN, nFLAG, nWRX) | $V_{IL}$ | Input logic low | | | | 0.4 | V |
| | $V_{IH}$ | Input logic high | | 0.7 | | | V |
| Output Voltage (nFLAG, nWRX) | $V_{OL}$ | Output logic low, sinking = 1mA | | | 0.08 | 0.15 | V |
| | $V_{OH}$ | Output logic high, no load | | 3 | 3.25 | 3.5 | V |
| nFLAG Pull-Up Resistance | $R_{OH\_nFLAG}$ | | | | 400 | | kΩ |
| nWRX Pull-Up Resistance | $R_{OH\_nWRX}$ | | | | 200 | | kΩ |
| nEN Pull-Down Resistor | $R_{nEN}$ | | | | 400 | | kΩ |
| **Thermal Shutdown** | | | | | | | |
| Thermal Shutdown Threshold | $T_{SD}$ | | | | 150 | | ℃ |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | | 25 | | ℃ |

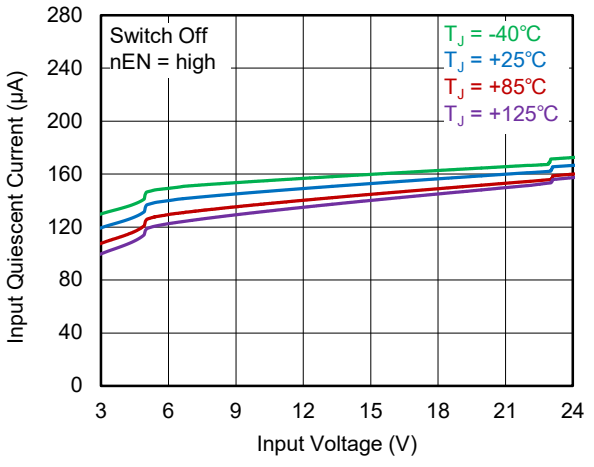
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}/V_{OUT}$ = 5V, $C_{IN}$ = 1μF, $C_{OUT}$ = 10μF, $T_J$ = +25℃, nWRX floating (high), nFLAG floating (high), nEN floating (low), VP = GND ($V_{OVP}$ = 23V), unless otherwise specified.

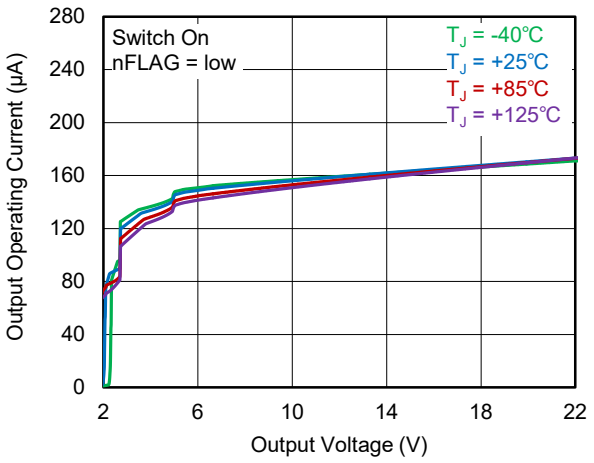
Input Operating Current vs. Input Voltage



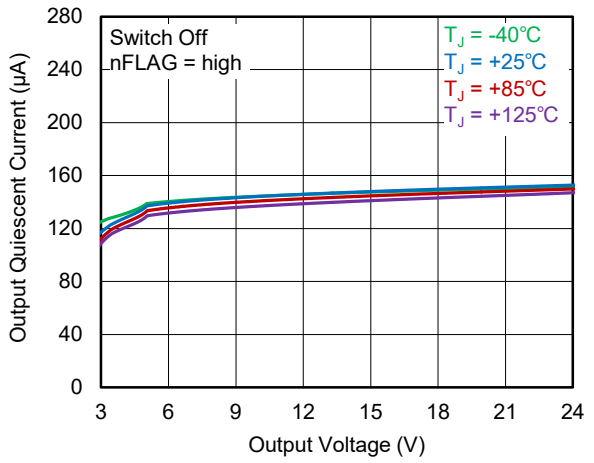

Input Quiescent Current vs. Input Voltage



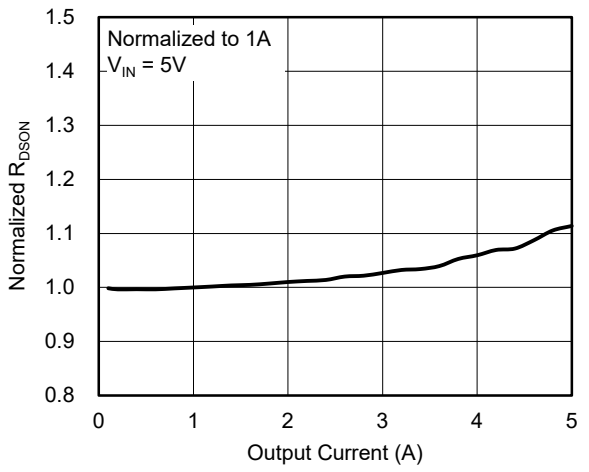

Output Operating Current vs. Output Voltage



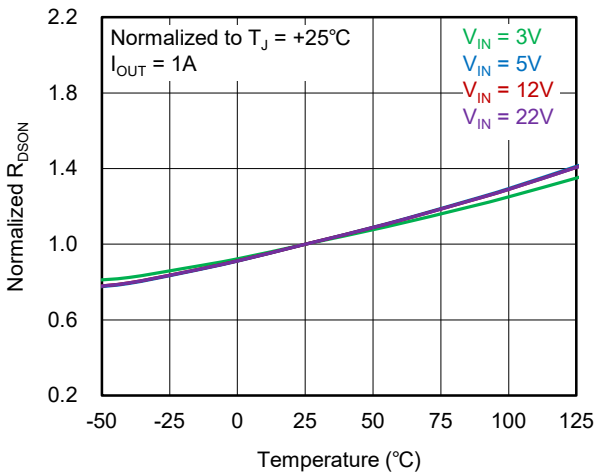

Output Quiescent Current vs. Output Voltage




Normalized $R_{DSON}$ vs. Output Current



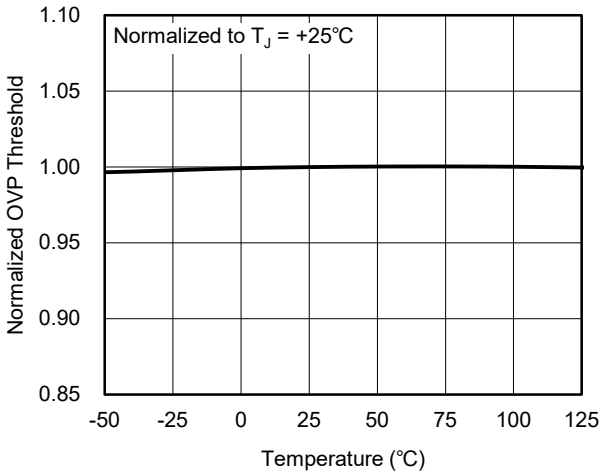

Normalized $R_{DSON}$ vs. Temperature



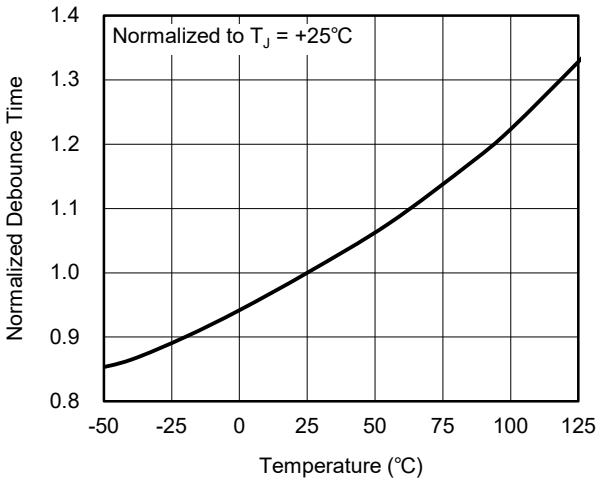
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}/V_{OUT}$ = 5V, $C_{IN}$ = 1μF, $C_{OUT}$ = 10μF, $T_J$ = +25℃, nWRX floating (high), nFLAG floating (high), nEN floating (low), VP = GND ($V_{OVP}$ = 23V), unless otherwise specified.

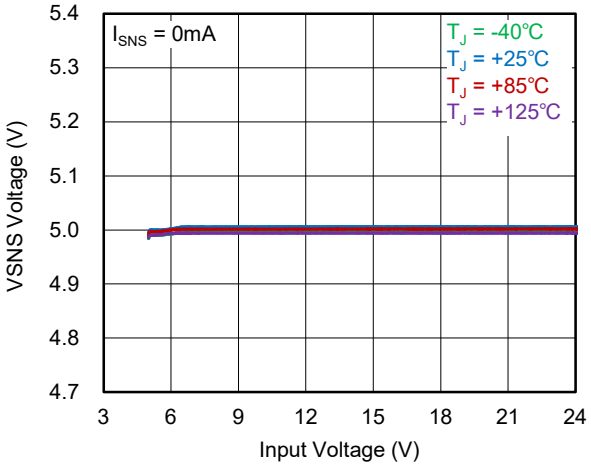
Normalized OVP Threshold vs. Temperature



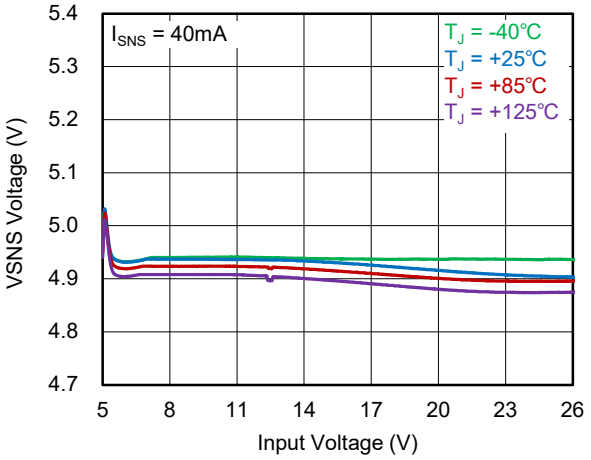

Normalized Debounce Time vs. Temperature




VSNS Voltage vs. Input Voltage



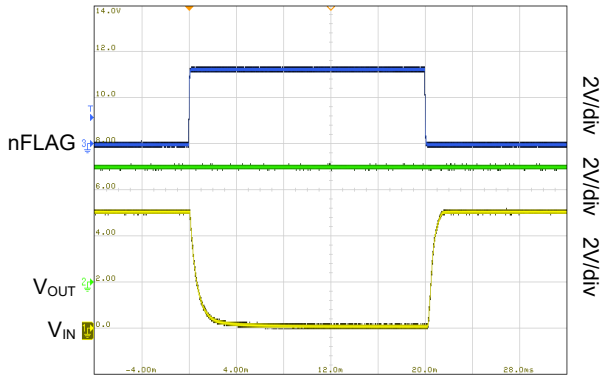

VSNS Voltage vs. Input Voltage



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

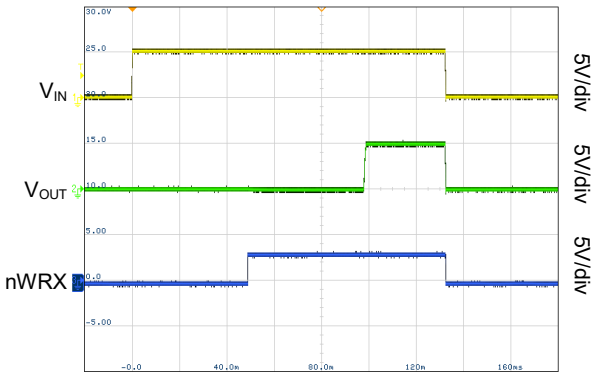
$V_{IN}$/$V_{OUT}$ = 5V, $C_{IN}$ = 1μF, $C_{OUT}$ = 10μF, $T_J$ = +25℃, nWRX floating (high), nFLAG floating (high), nEN floating (low), VP = GND ($V_{OVP}$ = 23V), unless otherwise specified.

OTG Mode nFLAG Turn On-Off



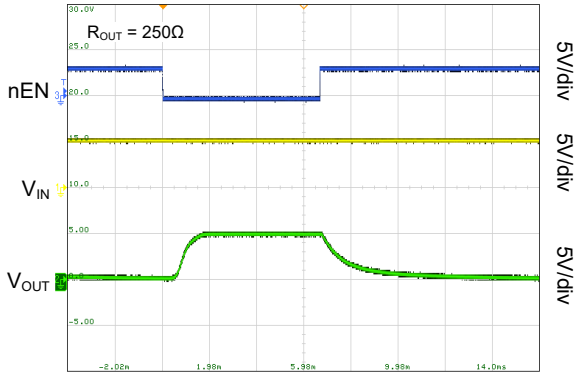

Time (4ms/div)

VIN 5V Insert-Remove



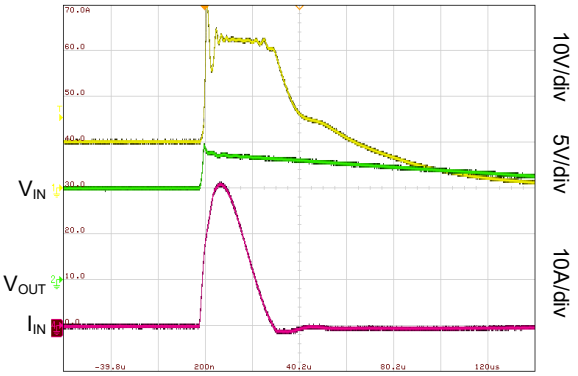

Time (20ms/div)

Turn On-Off with nEN
(Slave Mode nWRX = nFLAG = Low)




Time (2ms/div)

Surge Transient (100V)




Time (20μs/div)

## FUNCTIONAL BLOCK DIAGRAM

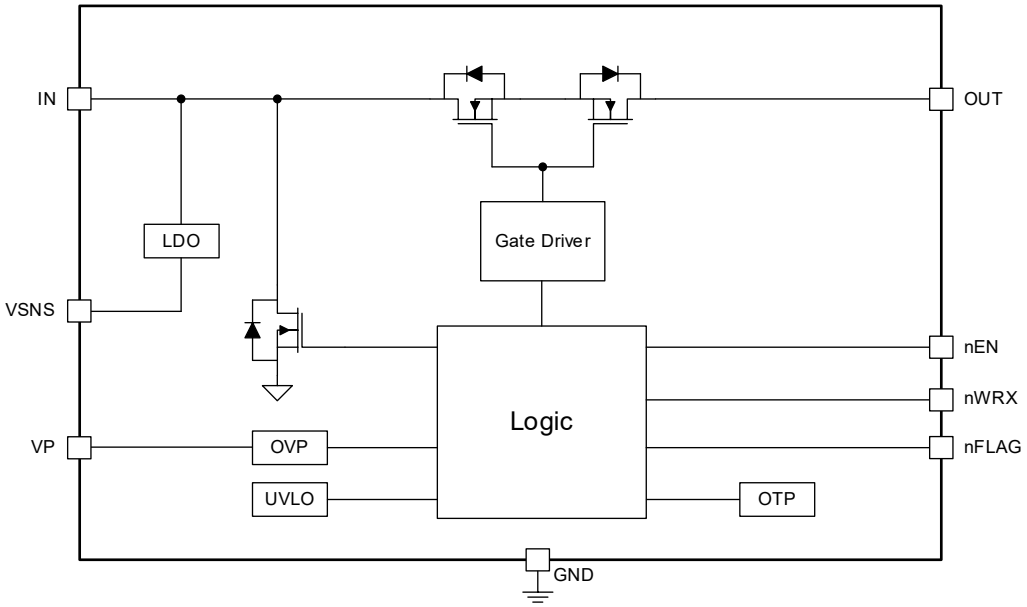



**Figure 2. SGM40675A Block Diagram**

# DETAILED DESCRIPTION

The SGM40675A is used for load protection to connect power/charger source. Two back-to-back" low impedance power NMOS switches are integrated. SGM40675A contains functions such as over-voltage detection, under-voltage protection, and power good indication.

The over-voltage protection function can protect device input voltage from rising faults up to +28$V_{DC}$. The internal TVS can provide +100V surge protection for the device. The internal power MOSFETs are turned off when the input voltage reaches the OVP value. A debounce time of 50ms is set before the output starts up to prevent false turn-on of the power MOSFETs. OTG mode allows the device to be bi-conductive. When OTG mode is disabled, the device's IN pin blocks any voltage from OUT pin.

The OVP value can be selected by controlling the state of the VP pin. Grounding VP pin selects the 23V OVP value. Leave the VP pin floating turns the OVP value to typically 12.9V.

## Dual Input Device Operation

The SGM40675A load switch can be equivalent to a 2:1 power multiplexer by adding a wireless Rx (WRx), as shown in Figure 3. When disabled, please make sure the wireless receiver withstand voltage value is greater than or equal to 24V, which is also the maximum operating voltage of the SGM40675A.

By controlling the input state (IN adapter and/or nWRx) can implement the mode transition between off and OTG. OTG plug-in event triggers mode transition into OTG mode.

## Operation Modes

The SGM40675A can operate in master or slave modes. The device assigns input priority to the IN power over the wireless receiver in master mode, while allows an external system (battery charger) to act as a master to determine input priority in slave mode.

Both master mode and slave mode contains a 50ms deglitch period and 0.8ms soft-start time.

Grounding the nWRX pin to enter the slave mode can cancel a 50ms automatic break-before-make discharge period that included in the master mode.

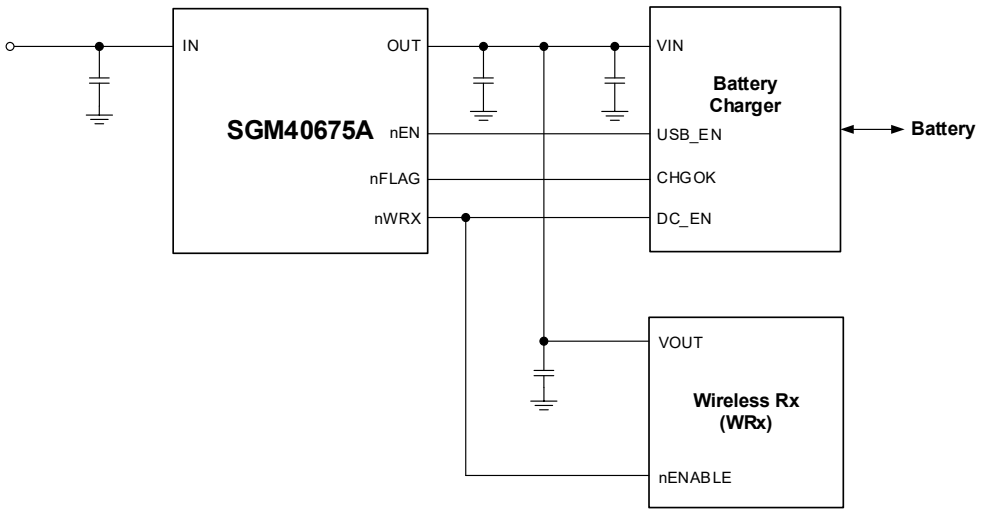



**Figure 3. Dual Input Device Operation**

# DETAILED DESCRIPTION (continued)

## Master Mode

In master mode, after a valid input voltage is appeared and the nEN pin is grounded, the load switch controller will turn on the power FETs after a fixed delay. IN pin has the input priority in master mode.

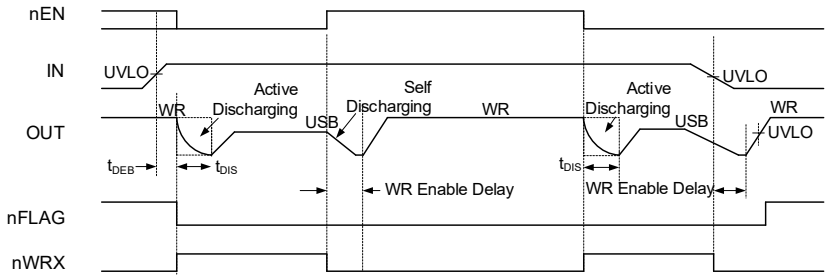
**Charging (IN to OUT):**

- The load switch assigns the input/wireless priority.
- The IN pin is connected to a valid voltage source.
- Grounding nEN to turn on the load switch and allow the current to flow from IN to OUT.
- Grounding nEN to pull nWRX high to shut down the wireless receiver.
- When OTG event occurs, nFLAG become high. (OUT is connected to a valid voltage source and IN is lower than UVLO.)

**OTG (OUT to IN):**

- The OUT pin is connected with a valid voltage source, and IN voltage is lower than UVLO.
- OTG event triggers nFLAG pulled high.
- Both nEN and nFLAG are pulled low to turn on the load switch and allow current flowing from OUT to IN.
- Grounding the nFLAG and nEN pins to trigger the nWRX pulled high to shut down the wireless receiver.

**Before $t_{DEB}$ expires, nEN is pulled to low:**




**After $t_{DEB}$ expires, nEN is pulled to low:**

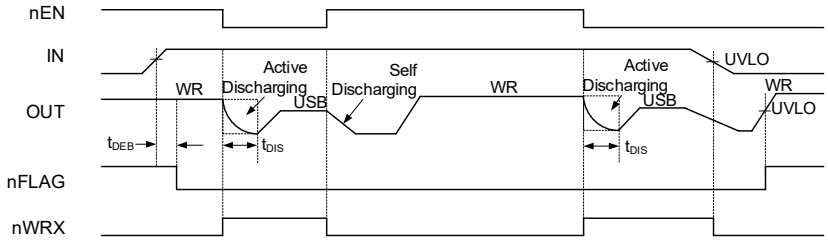



**Figure 4. Master Mode Charging**

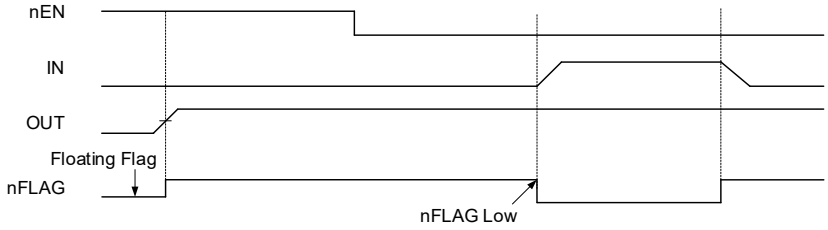



**Figure 5. Master Mode OTG**

## DETAILED DESCRIPTION (continued)

### Slave Mode

The external system (battery charger) works as master to enable load switch on-state through nEN pin. In this mode, both nFLAG and nWRX can tie to GND and the system (charger) assigns the input priority.

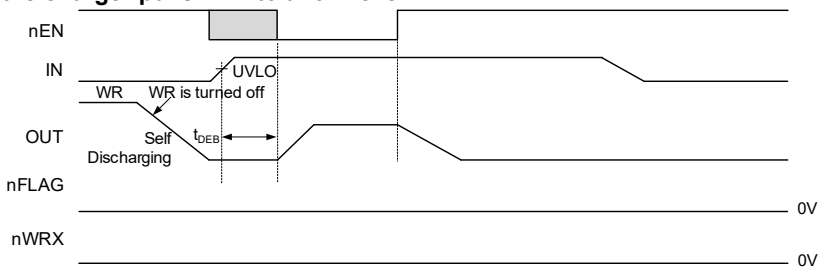
Charging (IN to OUT):

- The IN pin is connected to a valid voltage source.
- Before charging through SGM40675A, the charger will shut down the wireless receiver.
- Grounding nEN to turn on the load switch and allow the current flowing from IN to OUT.

OTG (OUT to IN):

- Once OUT is connected to a valid voltage source, nEN is grounded by charger to allow the current flowing from OUT to IN.

**Before the $t_{DEB}$ expires, the charger pulls nEN to a low level:**




**After $t_{DEB}$ expires, the charger pulls nEN to a low level:**

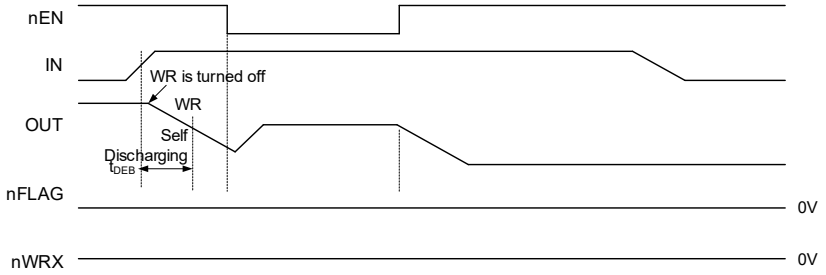
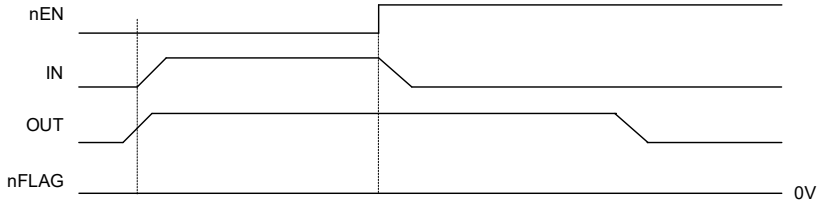



**Figure 6. Slave Mode Charging**

**Before $V_{OUT}$ ramps up, the nEN is pulled to a low level:**




**After $V_{OUT}$ ramps up, nEN is pulled to a low level:**

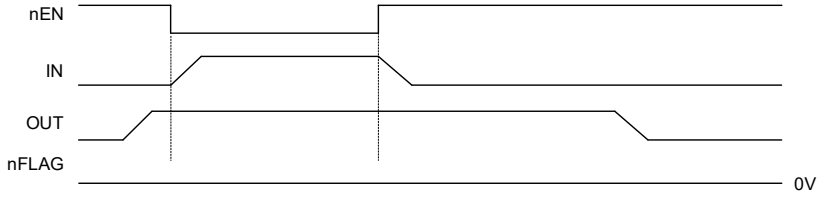



**Figure 7. Slave Mode OTG**

## DETAILED DESCRIPTION (continued)

### Input Surge Protection

The IN pin to GND pin of the device must withstand a +100V surge regardless the state of the load switch is on or off. The device's surge protection meets the requirements of the IEC 61000-4-5 specification, $R_{SOURCE}$ = 2.0Ω, 1.2/50μs waveform.

### Over-Voltage Protection

The load switch instantly turns off when input voltage is greater than the programmed OVP value. This function protects the device and downstream components from being damaged.

The OVP threshold value can be programed by the state of the VP pin. Grounding the VP pin gets a typical 23V OVP threshold value and floating this pin turns the OVP threshold value to typical 12.9V.

### Soft-Start

The function of soft-start minimizes the inrush current during the load switch enable duration either in master mode or slave mode.

### OTG

An OTG plug-in event triggers the OTG mode, about 5V power source is connected to the OUT pin and an OTG load is connected to the IN pin.

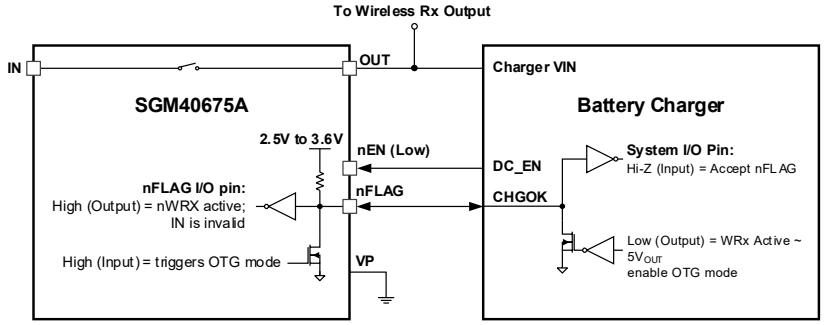
### Bidirectional Blocking

The SGM40675A integrates the bidirectional blocking function that will block any reverse current. When input voltage is less than the input start-up voltage or greater than the OVP threshold value and the nFLAG pin is pulled high (OTG mode is disabled), the FETs between IN and OUT are turned off and the internal body diodes are back-to-back.

### nFLAG Logic

The OTG mode can be enabled or disabled by controlling the state of the nFLAG pin in master mode.

When a valid OUT voltage is applied and the IN pin is disconnected from the power source, the nFLAG pin works as an output indication pin and is tied to high. Grounding the nFLAG pin triggers the OTG mode on.




| IN | OUT | nFLAG | CHGOK | Load Switch Behavior (nEN = Low) |
|---|---|---|---|---|
| < UVLO | > UVLO | High | Hi-Z | If the load switch is off, and the OTG mode can be enabled.<br>The battery charger determines the on/off state of WRx. |
| = $V_{OUT}$ | = $V_{OUT}$ | Low | Low | If the load switch is on, and the OTG mode is enabled.<br>The battery charger determines the on/off state of WRx. |
| > UVLO | Low | Low | X | Load switch is off (nEN is pulled to high), and OTG mode is not allowed. |

**Figure 8. nFLAG Logic**

## DETAILED DESCRIPTION (continued)

### Input Capacitor

It recommends 1μF or larger capacitor used as $C_{IN.}$ Besides, please locate $C_{IN}$ closely to device. The 50V rated ceramic capacitors are suitable for the OVP situation of the device and withstand most surges.

### Output Capacitor

The soft-start function can reduce the inrush current by slowly turning on the load switch. It is recommended to use a 1μF or larger ceramic capacitor as the output capacitor.

### VSNS Indication

VSNS pin is regulated to 5V typical and can support about 40mA to external loads. The VSNS sets up once IN is greater than UVLO. OTP event can disable the VSNS output. Large voltage drop between IN and VSNS can also cause the large power consumption when over-current protection is not triggered, so please try to avoid this situation.

Please refer to timing diagram below for more details of VSNS's behavior.

### VSNS Capacitor

It is recommended that 0.1μF or larger capacitor be used for bypass VSNS.

### Thermal Protection

The SGM40675A integrates over-temperature protection, and the device turns off the power FETs if the junction temperature exceeds +150℃ (TYP), and the recovery value is about +125℃ (TYP).

### ESD Test Conditions and HBM ESD Protection

The SGM40675A meets the requirement of IEC61000-4-2 standard (1μF used as input capacitor on board). IN integrates a protection feature that can tolerate ±15k$V_{ESD}$ in air condition. $V_{IN}$ can withstand ±8k$V_{ESD}$ in contact condition and air-gap condition.

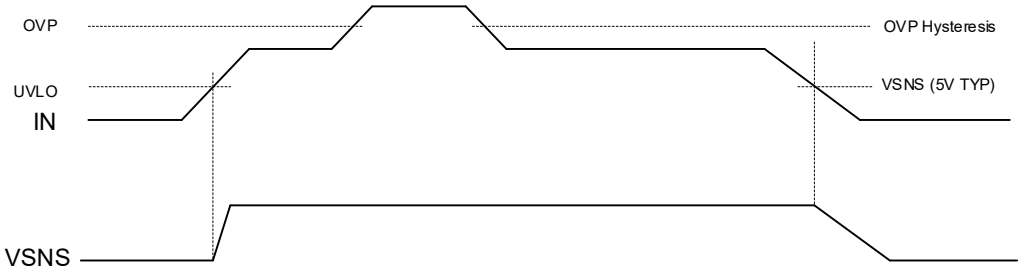



**Figure 9. Timing Diagram for VSNS**

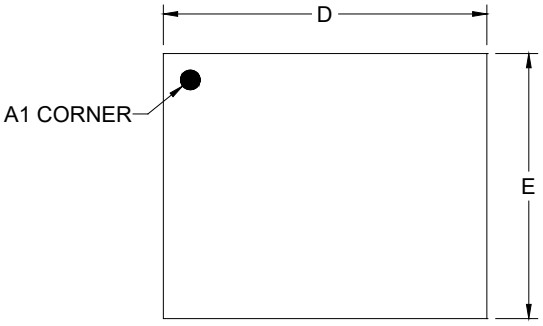
## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

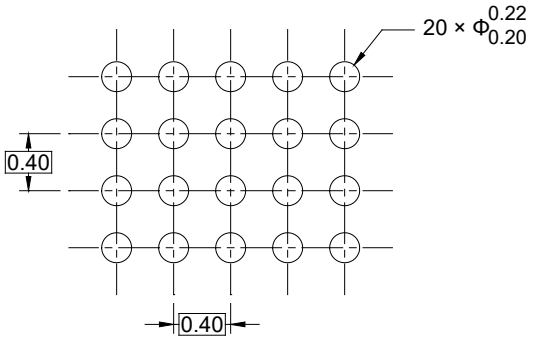
| Changes from Original (NOVEMBER 2023) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

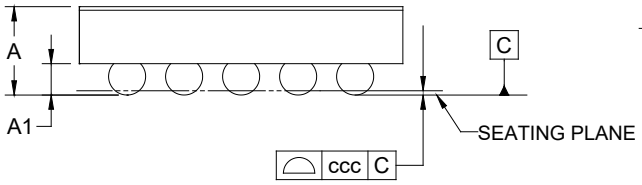
## WLCSP-2.27×1.86-20B



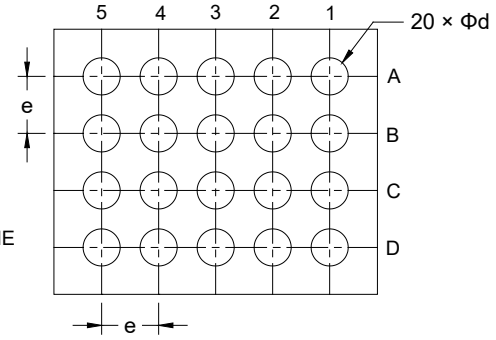

**TOP VIEW**




**RECOMMENDED LAND PATTERN** (Unit: mm)




**SIDE VIEW**



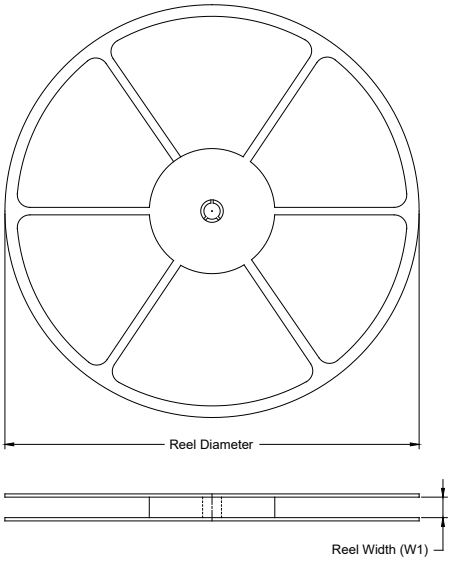

**BOTTOM VIEW**

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | MOD | MAX |
| A | - | - | 0.665 |
| A1 | 0.200 | - | 0.240 |
| D | 2.240 | - | 2.300 |
| E | 1.832 | - | 1.892 |
| d | 0.230 | - | 0.290 |
| e | 0.400 BSC | | |
| ccc | 0.050 | | |

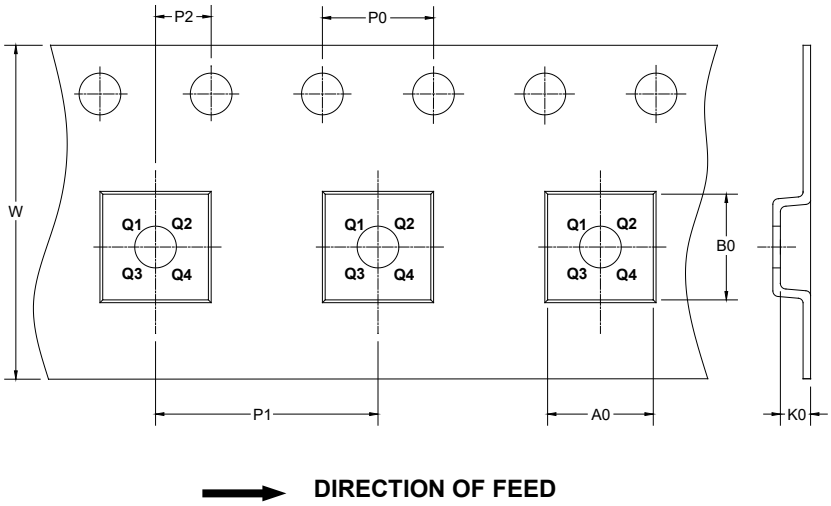
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



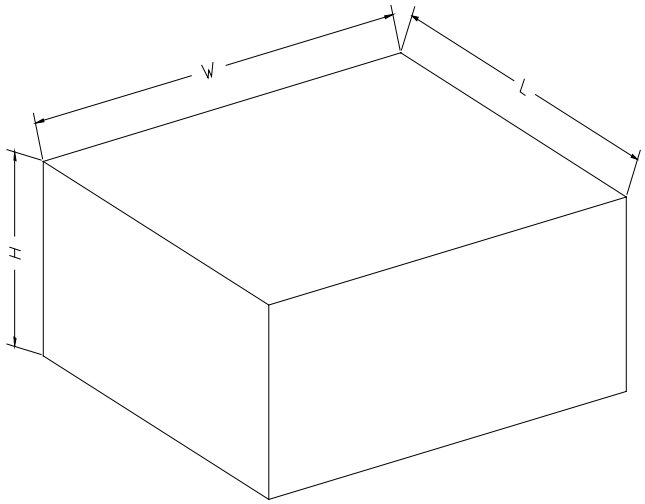

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP-2.27×1.86-20B | 7" | 9.5 | 2.01 | 2.42 | 0.78 | 4.0 | 4.0 | 2.0 | 8.0 | Q2 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 7″ (Option) | 368 | 227 | 224 | 8 |
| 7″ | 442 | 410 | 224 | 18 |

DD0002