# SGM41600S
# I²C Controlled Single Cell 8A Switched Cap Charger with Bypass Mode

## GENERAL DESCRIPTION

The SGM41600S is an efficient 8A switched-capacitor battery charging device with I²C control that can operate either in charge-pump voltage divider mode or in bypass mode. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.4V to 11.5V input voltage range (VBUS) from smart wall adapters or power banks. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-half of the battery current and reduce the wiring drops, losses and temperature rise in the application.

A two-channel switched-capacitor topology is used to reduce the required input capacitors, improve efficiency and minimize the output ripple. Necessary protection features for safe charging performance including input over-voltage protection by external OVPFET ($Q_{OVP}$) and input reverse blocking (using an internal NFET) are provided.

The SGM41600S is available in a Green WLCSP-2.7×2.75 -36B package and can operate in the -40℃ to +85℃ ambient temperature range.

## APPLICATIONS

Smart Phone, Tablet PC

## FEATURES

- **Efficiency Optimized Switched-Capacitor Architecture**
  - **Up to 8A Output Current**
  - **3.4V to 11.5V Input Voltage Range**
  - **200kHz to 1.6MHz Switching Frequency Setting**
  - **Above 97.11% Voltage Divider Mode Efficiency (when $V_{BAT}$ = 4V, $I_{BAT}$ = 6A)**
- **Comprehensive Integrated Protection Features**
  - **External OVP Control and Regulation**
  - **Input Over-Voltage Protection (VBUS_OVP)**
  - **Input Short-Circuit Protection (VBUS_SC)**
  - **Input Over-Current Protection (IBUS_OCP)**
  - **Input Under-Current Protection (IBUS_UCP)**
  - **Battery Over-Voltage Protection (VBAT_OVP)**
  - **Output Short-Circuit Protection (VOUT_SC)**
  - **IBAT Over-Current Protection (IBAT_OCP)**
  - **$C_{FLY}$ Short-Circuit Protection (CFLY_SC)**
  - **Switch Peak Over-Current Protection (PEAK_OCP)**
  - **Die Over-Temperature Protection (TDIE_OTP)**
  - **PMID to VOUT Over-Voltage Protection (PMID2OUT_OVP)**
  - **PMID to VOUT Under-Voltage Protection (PMID2OUT_UVP)**
- **6-Channel 12-Bit (Effective) ADC Converter**
  - **VBUS, IBUS, VBAT, IBAT, VOUT, TDIE for Monitoring**

## TYPICAL APPLICATION

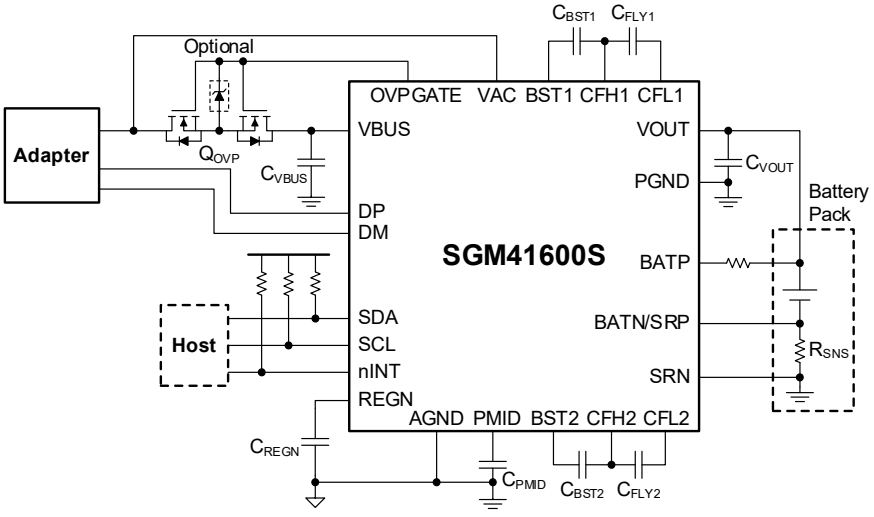


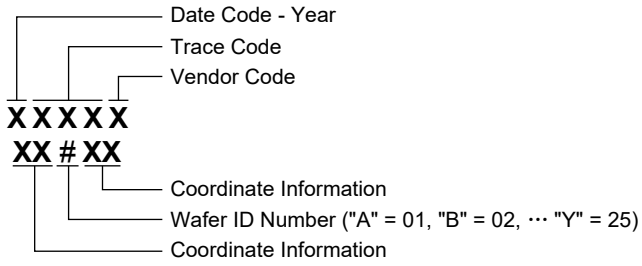

**Figure 1. Typical Application Circuit**

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM41600S | WLCSP-2.7×2.75-36B | -40℃ to +85℃ | SGM41600SYG/TR | 156<br>XXXXX<br>XX#XX | Tape and Reel, 5000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

VAC (Converter Not Switching) ..... -0.3V to 35V
OVPGATE to VBUS ..... -22V to 12V
VBUS, PMID (Converter Not Switching) ..... -0.3V to 22V
BST1, BST2 ..... -0.3V to (PMID + 5.5) V
VOUT ..... -0.3V to 6V
CFH1, CFH2 to VOUT ..... -0.3V to 6V
CFL1, CFL2 ..... -0.3V to 6V
DP, DM, REGN, BATP, SDA, SCL, nINT ..... -0.3V to 6V
BATN/SRP, SRN ..... -0.3V to 1.8V
SRP to SRN ..... -0.5V to 0.5V
Package Thermal Resistance
WLCSP-2.7×2.75-36B, $\theta_{JA}$ ..... 39.6℃/W
WLCSP-2.7×2.75-36B, $\theta_{JB}$ ..... 5.5℃/W
WLCSP-2.7×2.75-36B, $\theta_{JC}$ ..... 14.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## RECOMMENDED OPERATING CONDITIONS

VAC ..... 3.4V to 18V
VBUS (Bypass Mode) ..... 3.4V to 5.5V
VBUS (Voltage Divider Mode) ..... 5.5V to 11.5V
VOUT, BATP ..... 3V to 5.5V
$I_{VOUT}$ (Bypass Mode) ..... 0A to 5A
$I_{VOUT}$ (Voltage Divider Mode) ..... 0A to 8A
(CFH1 - VOUT), CFL1 ..... 0V to 5.5V
(CFH2 - VOUT), CFL2 ..... 0V to 5.5V
BATN/SRP, SRN ..... 0V to 1.5V
(SRP - SRN) ..... -0.05V to 0.05V
SDA, SCL, nINT ..... 0V to 5V
Operating Junction Temperature Range ..... -40℃ to +125℃

## ESD SENSITIVITY CAUTION

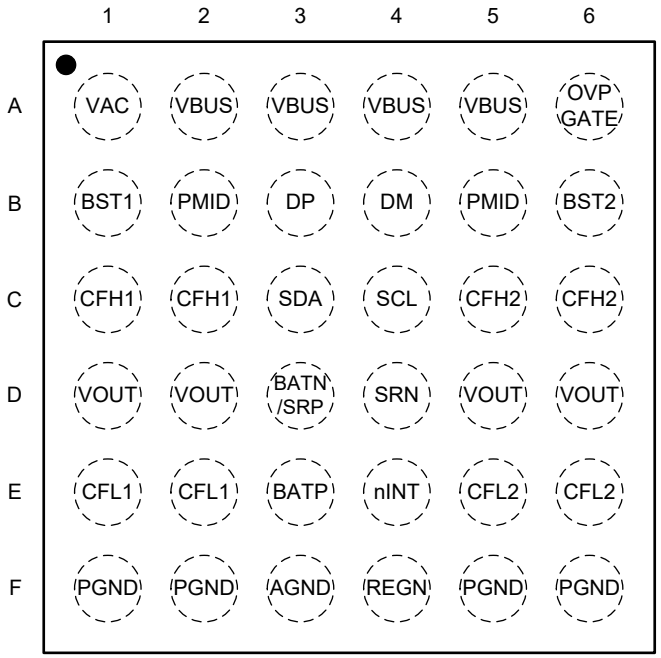
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## PIN CONFIGURATION

(TOP VIEW)




WLCSP-2.7×2.75-36B

# PIN DESCRIPTION

| PIN | NAME | TYPE (1) | FUNCTION |
|---|---|---|---|
| A1 | VAC | AI | Adapter DC Voltage Sense Input Pin. Connect it to the drain of the external OVPFET ($Q_{OVP}$). |
| A2, A3, A4, A5 | VBUS | P | Device Power Input Pins. Use a 10μF or larger ceramic capacitor between VBUS and PGND pins close to the device. |
| A6 | OVPGATE | AO | External N-FET Gate Control Pin. Connect to the gate of the external OVPFET ($Q_{OVP}$). (Note: The REG_RST bit does not affect the OVPGATE's output.) |
| B1 | BST1 | P | Channel-1 Bootstrap Pin. It is the BST pin to supply $Q_{CH1}$ gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CFH1 pin. |
| B2, B5 | PMID | P | Power Stage Supply Input Pins. Bypass them with at least two 4.7μF ceramic capacitors to PGND. |
| B3 | DP | AIO | USB Communication Interface Positive Line. Connect to the USB D+ data line. |
| B4 | DM | AIO | USB Communication Interface Negative Line. Connect to the USB D- data line. |
| B6 | BST2 | P | Channel-2 Bootstrap Pin. It is the BST pin to supply $Q_{CH2}$ gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CFH2 pin. |
| C1, C2 | CFH1 | P | Channel-1 Flying Capacitor Positive Pins. Connect two 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close as possible to the device. |
| C3 | SDA | DIO | I²C Interface Data Line. The SDA line is forced to release when the 25ms I²C timeout fault occurs. |
| C4 | SCL | DI | I²C Interface Clock Input Line. The device I²C controller block is forced to reset when receiving 9 clock pulses on the SCL line. |
| C5, C6 | CFH2 | P | Channel-2 Flying Capacitor Positive Pins. Connect two 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close as possible to the device. |
| D1, D2, D5, D6 | VOUT | P | Output Pins. Connect to the battery pack positive terminal. Two 10μF capacitors between VOUT and PGND pins are recommended. |
| D3 | BATN/SRP | AI | Battery Voltage Sensing Negative Input or Battery Current Sensing Positive Input. Short this pin and SRN together if $R_{SNS}$ is not used. |
| D4 | SRN | AI | Battery Current Sensing Negative Input. Place a 2mΩ or 5mΩ ($R_{SNS}$) shunt resistor between SRN and BATN/SRP pins. |
| E1, E2 | CFL1 | P | Channel-1 Flying Capacitor Negative Pins. Connect two 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close as possible to the device. |
| E3 | BATP | AI | Battery Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP and positive terminal of the battery pack. |
| E4 | nINT | DO | Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. It is normally high but generates a low 256μs pulse when a charge status or fault occurs to inform the host. |
| E5, E6 | CFL2 | P | Channel-2 Flying Capacitor Negative Pins. Connect two 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close as possible to the device. |
| F1, F2, F5, F6 | PGND | P | Power Ground Pin. |
| F3 | AGND | P | Analog Ground Pin (reference for low current signals). |
| F4 | REGN | AO | Internal 5V LDO Output. Connect a 4.7μF MLCC capacitor between this pin and AGND. |

NOTE:

1. P = power, AI = analog input, AO = analog output, AIO = analog input/output, DI = digital input, DO = digital output, DIO = digital input/output.

# ELECTRICAL CHARACTERISTICS

($T_J$ = -40℃ to +85℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **Supply Currents** | | | | | | |
| VAC Quiescent Current | $I_{Q_VAC}$ | ADC disabled, charge disabled, $Q_{OVP}$ used, $V_{VAC_OVP_R}$ = 12V (AC_OVP[3:0] bits = 1000) $V_{VAC}$ = 13V, $V_{VBUS}$ = 0V, $V_{VOUT}$ = 0V VAC_OVP activated | | 375 | 550 | μA |
| VBUS Quiescent Current | $I_{Q_VBUS}$ | ADC disabled, charge disabled, $Q_{OVP}$ used, $V_{VBUS}$ = 8V, $V_{VAC}$ = 8V | | 30 | 50 | μA |
| | | ADC enabled, charge enabled, $Q_{OVP}$ used, $V_{VBUS}$ = 8V > (2 × $V_{VOUT}$), $f_{SW}$ = 500kHz | | 13 | | mA |
| Battery Only Quiescent Current | $I_{Q_VOUT}$ | ADC disabled, charge disabled, VBUS not present, $V_{VAC}$ = 0V, $V_{VOUT}$ = 4.5V | | 14 | 25 | μA |
| | | ADC enabled, charge disabled, (after 1-shot ADC conversion complete), VBUS not present, $V_{VAC}$ = 0V, $V_{VOUT}$ = 4.5V | | 14 | | μA |
| VBUS Present Rising Threshold | $V_{BUS_PRESENT_R}$ | $V_{VBUS}$ rising | | 3.05 | 3.4 | V |
| VBUS Present Falling Threshold | $V_{BUS_PRESENT_F}$ | $V_{VBUS}$ falling | | 2.85 | | V |
| VBUS Present Hysteresis | $V_{BUS_PRESENT_HYS}$ | | | 200 | | mV |
| VBAT Present Rising Threshold | $V_{BAT_PRESENT_R}$ | BATP pin, $V_{BATP}$ rising | | 2.55 | | V |
| VBAT Present Falling Threshold | $V_{BAT_PRESENT_F}$ | BATP pin, $V_{BATP}$ falling | | 2.45 | | V |
| VBAT Present Hysteresis | $V_{BAT_PRESENT_HYS}$ | | | 100 | | mV |
| **External OVP Control** | | | | | | |
| VAC Present Rising Threshold | $V_{AC_PRESENT_R}$ | $V_{VAC}$ rising | | 3.05 | 3.4 | V |
| VAC Present Falling Threshold | $V_{AC_PRESENT_F}$ | $V_{VAC}$ falling | | 2.85 | | V |
| VAC Present Hysteresis | $V_{AC_PRESENT_HYS}$ | | | 200 | | mV |
| VAC OVP Rising Threshold Range | $V_{AC_OVP_R}$ | I²C programmable, 1V per step, 12V by default | 4 | | 19 | V |
| VAC OVP Threshold Accuracy | $V_{AC_OVPR_ACC}$ | $V_{AC_OVP_R}$ = 12V | -3.2 | | 3.2 | % |
| VAC OVP Rising Deglitch Time | $t_{VAC_OVPR_DEG}$ | Deglitch between $V_{VAC}$ rising (5V/μs) above $V_{AC_OVP_R}$ and triggering the protection action | | 200 | | ns |
| VBUS Pull-down Resistor | $R_{PDN_VBUS}$ | VBUS pin, BUS_PDN_EN = 1, $V_{VBUS}$ = 2.6V | | 1 | | kΩ |
| VAC Pull-down Resistor | $R_{PDN_VAC}$ | | | 200 | 400 | Ω |
| VAC Pull-down Timeout | $t_{VAC_PD}$ | AC_PDN_EN = 1 | | 400 | | ms |
| **Switched Cap Chargers** | | | | | | |
| VBUS to VOUT Resistance | $R_{DROPOUT}$ | Bypass mode, $V_{VOUT}$ = 4V, $I_{BAT}$ = 4A | | 15.2 | | mΩ |
| $R_{DSON}$ of Reverse Blocking FET | $R_{DS_QRB}$ | Bypass mode, $V_{VOUT}$ = 4V, $I_{BAT}$ = 4A | | 5.2 | | mΩ |
| $R_{DSON}$ of $Q_{CH1/2}$ | $R_{DS_QCH}$ | Bypass mode, $V_{VOUT}$ = 4V, $I_{BAT}$ = 4A | | 13 | | mΩ |
| $R_{DSON}$ of $Q_{DH1/2}$ | $R_{DS_QDH}$ | Bypass mode, $V_{VOUT}$ = 4V, $I_{BAT}$ = 4A | | 7 | | mΩ |
| $R_{DSON}$ of $Q_{CL1/2}$ | $R_{DS_QCL}$ | SC mode, $V_{VBUS}$ = 8V, $V_{VOUT}$ = 4V, $I_{BAT}$ = 4A | | 7 | | mΩ |
| $R_{DSON}$ of $Q_{DL1/2}$ | $R_{DS_QDL}$ | SC mode, $V_{VBUS}$ = 8V, $V_{VOUT}$ = 4V, $I_{BAT}$ = 4A | | 7 | | mΩ |
| **Protection** | | | | | | |
| nINT Low Pulse Duration when a Protection Occurs | $t_{INT}$ | | | 256 | | μs |
| VBUS OVP Rising Threshold Range | $V_{BUS_OVP_R}$ | I²C programmable, 100mV per step, 11.5V by default | 4 | | 14 | V |
| VBUS OVP Threshold Accuracy | $V_{BUS_OVPR_ACC}$ | $V_{BUS_OVP_R}$ = 11.5V | -3.1 | | 3.1 | % |
| VBUS OVP Rising Deglitch Time | $t_{VBUS_OVPR_DEG}$ | Deglitch between $V_{VBUS}$ rising above $V_{BUS_OVP_R}$ and triggering protection action | | 2 | | μs |
| IBUS OCP Threshold Range | $I_{BUS_OCP}$ | I²C programmable, 300mA per step, 3A by default | 1.2 | | 5.7 | A |
| IBUS OCP Threshold Accuracy | $I_{BUS_OCP_ACC}$ | $I_{BUS_OCP}$ = 3A | -5 | | 5 | % |
| IBUS OCP Deglitch Time | $t_{IBUS_OCP_DEG}$ | Deglitch between $I_{BUS}$ rising above $I_{BUS_OCP}$ and triggering protection action | | 50 | | μs |

## ELECTRICAL CHARACTERISTICS (continued)

($T_J$ = -40℃ to +85℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| IBUS UCP Rising Threshold | $I_{BUS_UCP_R}$ | Rising, set by REG0x07[6] = 0 | 230 | 300 | 370 | mA |
| | | Rising, set by REG0x07[6] = 1 | 420 | 500 | 580 | mA |
| IBUS UCP Rising Deglitch Time | $t_{IBUS_UCPR_DEG}$ | Deglitch between $I_{BUS}$ rising above $I_{BUS_UCP_R}$ and triggering protection action | | 15 | | μs |
| IBUS UCP Falling Threshold | $I_{BUS_UCP_F}$ | Falling, set by REG0x07[6] = 0 | 100 | 150 | 200 | mA |
| | | Falling, set by REG0x07[6] = 1 | 180 | 250 | 320 | mA |
| IBUS UCP Falling Deglitch Time | $t_{IBUS_UCPF_DEG}$ | Deglitch between $I_{BUS}$ falling below $I_{BUS_UCP_F}$ and triggering protection action, I²C programmable, 64ms by default | | 64 | | ms |
| VBAT OVP Rising Threshold Range | $V_{BAT_OVP_R}$ | I²C programmable, 25mV per step, 4.35V by default | 4 | | 5 | V |
| VBAT OVP Threshold Accuracy | $V_{BAT_OVPR_ACC}$ | $V_{BAT_OVP_R}$ = 4.35V, $T_J$ = +25℃ | -0.5 | | 0.5 | % |
| | | $V_{BAT_OVP_R}$ = 4.35V, $T_J$ = -40℃ to +85℃ | -0.7 | | 0.7 | % |
| VBAT OVP Rising Deglitch Time | $t_{VBAT_OVPR_DEG}$ | Deglitch between $V_{BAT}$ rising above $V_{BAT_OVP_R}$ and triggering protection action | | 50 | | μs |
| IBAT OCP Threshold Range | $I_{BAT_OCP}$ | I²C programmable, 100mA per step, 8.2A by default | 3 | | 9.3 | A |
| IBAT OCP Threshold Accuracy | $I_{BAT_OCP_ACC}$ | $I_{BAT_OCP}$ =3.2A, $R_{SNS}$ = 2mΩ | -125 | | 125 | mA |
| | | $I_{BAT_OCP}$ =5.2A, $R_{SNS}$ = 2mΩ | -2.5 | | 2.5 | % |
| IBAT OCP Deglitch Time | $t_{IBAT_OCP_DEG}$ | Deglitch between $I_{BAT}$ rising above $I_{BAT_OCP}$ and triggering protection action | | 50 | | μs |
| VDRP OVP Threshold Range | $V_{DRP_OVP}$ | I²C programmable, 45mV per step, 275mV by default, $V_{DRP}$ = $V_{VAC}$ - $V_{VBUS}$ | 50 | | 365 | mV |
| TDIE OTP Rising Threshold | $T_{DIE_OTP_R}$ | | | 150 | | ℃ |
| Watchdog Timeout Range | $t_{WDT}$ | I²C programmable, 0.5s by default | | 0.5 | | s |
| **ADC Specification** | | | | | | |
| ADC Resolution | $ADC_{RES}$ | | | 12 | | bits |
| ADC Conversion Time | $t_{ADC_CONV}$ | Report data for each channel | | 4 | | ms |
| ADC VBUS Voltage Readable in REG0x14 and REG0x15 | $V_{BUS_ADC}$ | Effective Range | 3.3 | | 11.5 | V |
| | | LSB | | 4 | | mV |
| VBUS ADC Accuracy | $V_{BUS_ADC_ACC}$ | $V_{VBUS}$ = 8V | -1.2 | | 1.2 | % |
| ADC IBUS Current Readable in REG0x16 and REG0x17 | $I_{BUS_ADC}$ | Effective Range | 0 | | 6 | A |
| | | LSB | | 2 | | mA |
| IBUS ADC Accuracy | $I_{BUS_ADC_ACC}$ | $I_{BUS}$ = 2A | -5 | | 5 | % |
| | | $I_{BUS}$ = 3A | -4 | | 4 | % |
| | | $I_{BUS}$ = 4A | -4 | | 4 | % |
| ADC VBAT Voltage Readable in REG0x18 and REG0x19 | $V_{BAT_ADC}$ | Effective Range | 3 | | 5 | V |
| | | LSB | | 2 | | mV |
| VBAT ADC Accuracy | $V_{BAT_ADC_ACC}$ | $V_{BAT}$ = 4.3V/4.4V/4.5V, internal accuracy, $T_J$ = +25℃ | -0.3 | | 0.3 | % |
| ADC IBAT Current Readable in REG0x1A and REG0x1B | $I_{BAT_ADC}$ | Effective Range | 0 | | 9 | A |
| | | LSB | | 2.5 | | mA |
| IBAT ADC Accuracy | $I_{BAT_ADC_ACC}$ | $I_{BAT}$ = 2A, $R_{SNS}$ = 2mΩ | -3 | | 3 | % |
| | | $I_{BAT}$ = 7A, $R_{SNS}$ = 2mΩ | -1.5 | | 1.5 | % |
| ADC DIE Temperature Readable in REG0x1E | $T_{DIE_ADC}$ | Effective Range | -40 | | 150 | ℃ |
| | | LSB | | 1 | | ℃ |
| TDIE ADC Accuracy | $T_{DIE_ADC_ACC}$ | | | ±5 | | ℃ |

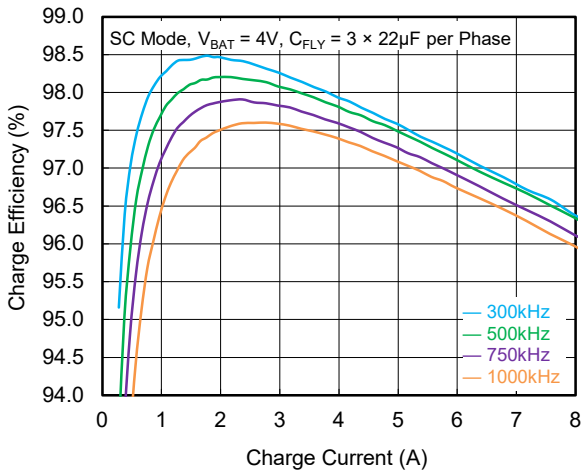
## ELECTRICAL CHARACTERISTICS (continued)

($T_J$ = -40℃ to +85℃, typical values are at $T_J$ = +25℃, unless otherwise noted.)

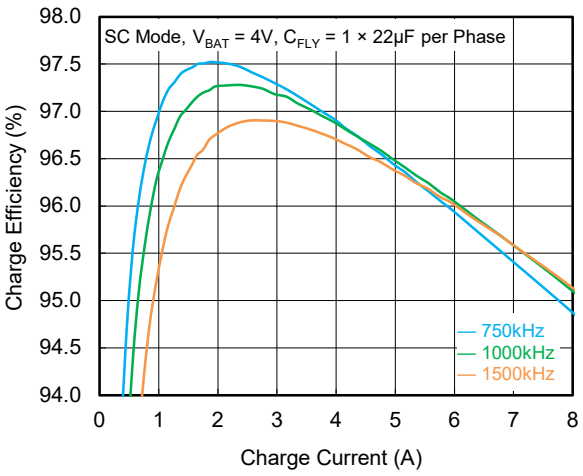
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| ADC VOUT Voltage Readable in REG0x1C and REG0x1D | $V_{OUT_ADC}$ | Effective Range | 2.7 | | 5 | V |
| | | LSB | | 2 | | mV |
| VOUT ADC Accuracy | $V_{OUT_ADC_ACC}$ | $V_{VOUT}$ = 4.3V/4.4V/4.5V, internal accuracy, $T_J$ = +25℃ | -0.3 | | 0.3 | % |
| **Logic I/O Threshold (SCL, SDA and nINT Pins)** | | | | | | |
| High Level Input Voltage | $V_{IH_I2C}$ | SCL and SDA pins<br>During rising from 0.3V to 1V, when SCL/SDA rises above 0.825V, it outputs High within 260ns | 0.825 | | | V |
| Low Level Input Voltage | $V_{IL_I2C}$ | SCL and SDA pins<br>During falling from 1V to 0.3V, when SCL/SDA falls below 0.4V, it outputs Low within 330ns. | | | 0.4 | V |
| Low Level Output Voltage | $V_{OL_I2C}$ | Sink 2mA, SDA and nINT pins | | | 0.4 | V |
| SCL Clock Frequency | $f_{CLK}$ | | 100 | | 1000 | kHz |
| **BC1.2 Detection (DP and DM Pins)** | | | | | | |
| Data Contact Detect Current Source | $I_{DP_SRC}$ | DP pin, $T_J$ = +25℃ | 9 | 12 | 15 | μA |
| DM Pull-down Resistance | $R_{DM_DWN_BC}$ | DM pin, $T_J$ = +25℃ | 15 | 19 | 23 | kΩ |
| Data Contact Detect Logic Low Threshold | $V_{LGC_LOW}$ | DP pin | | | 0.8 | V |
| Data Contact Detect Debounce Time | $t_{DCD_DBNC}$ | | | 15 | | ms |
| DP Force Detect Voltage | $V_{DP_SRC}$ | DP pin, $T_J$ = +25℃ | 0.5 | 0.6 | 0.7 | V |
| DM Sink Current | $I_{DM_SNK}$ | DM pin | 60 | 100 | 140 | μA |
| DP Voltage Source On Time | $t_{VDPSRC_ON}$ | DP pin | | 60 | | ms |
| Pull-down Detect Threshold | $V_{DAT_REF}$ | | 0.250 | 0.325 | 0.390 | V |
| DM Force Detect Voltage | $V_{DM_SRC}$ | DM pin, $T_J$ = +25℃ | 0.5 | 0.6 | 0.7 | V |
| DP Sink Current | $I_{DP_SNK}$ | DP pin | 60 | 100 | 140 | μA |
| DM Voltage Source On Time | $t_{VDMSRC_ON}$ | DM pin | | 60 | | ms |

## TYPICAL PERFORMANCE CHARACTERISTICS

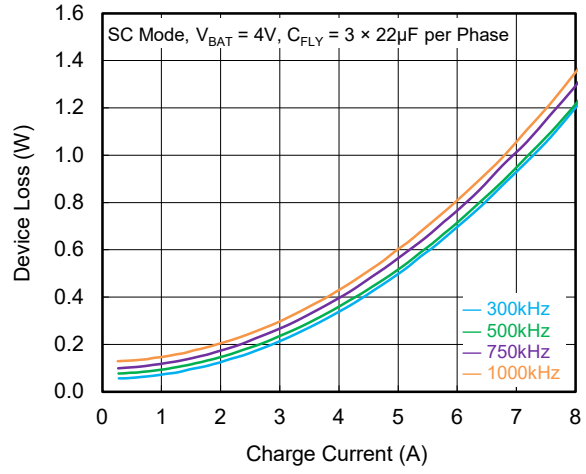
Charge Efficiency vs. Charge Current



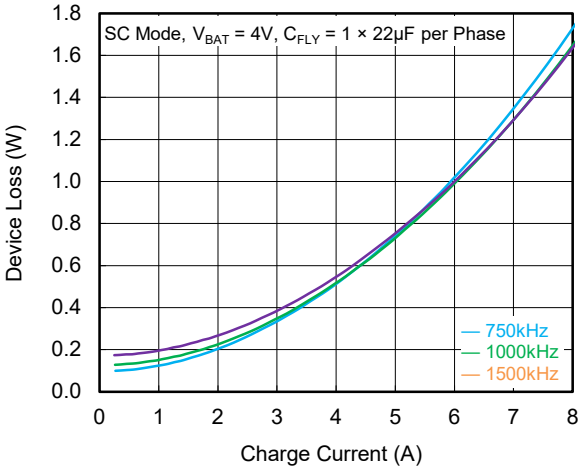

Charge Efficiency vs. Charge Current



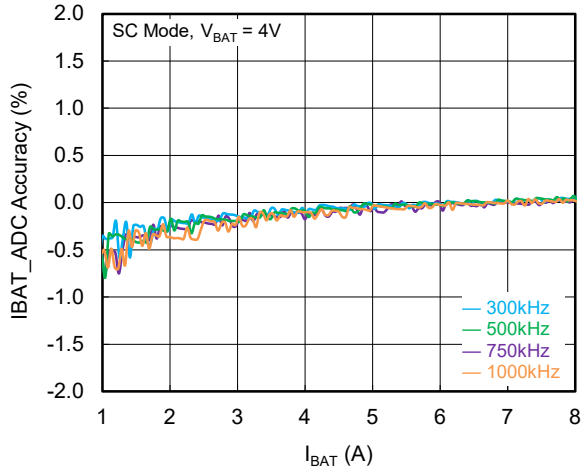

Device Loss vs. Charge Current



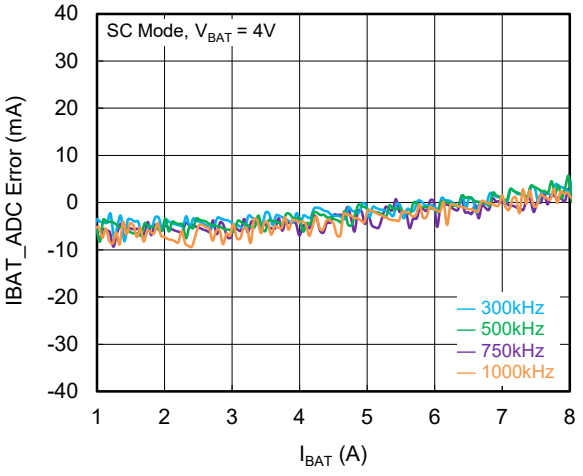

Device Loss vs. Charge Current




IBAT_ADC Accuracy vs. BAT Current

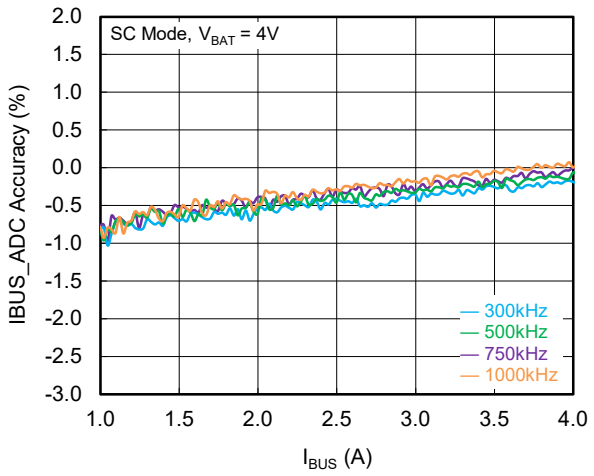



IBAT_ADC Error vs. BAT Current

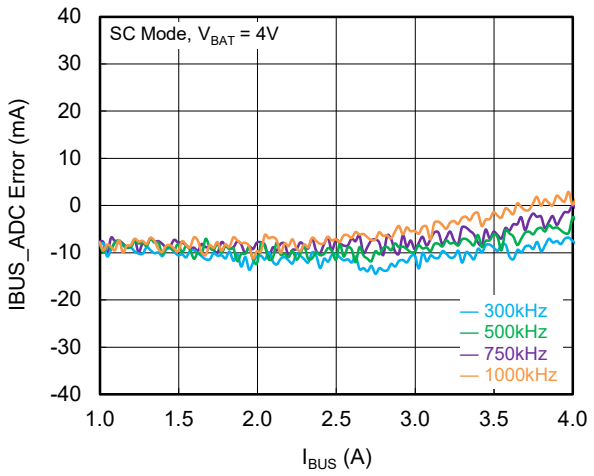


## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

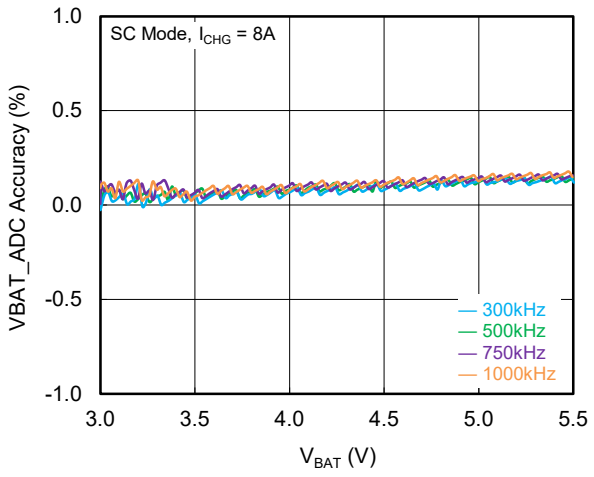
IBUS_ADC Accuracy vs. BUS Current



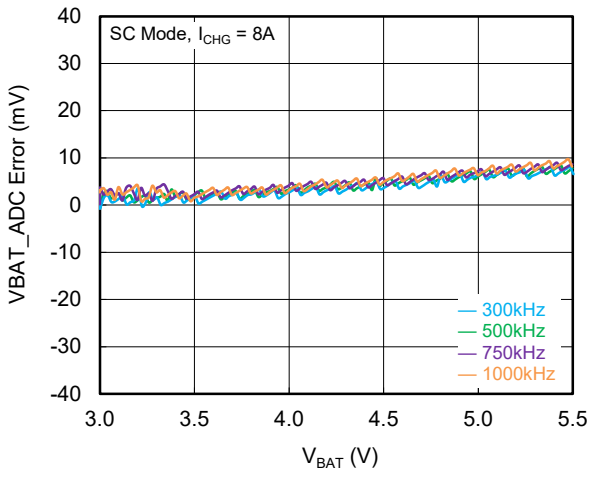

IBUS_ADC Error vs. BUS Current



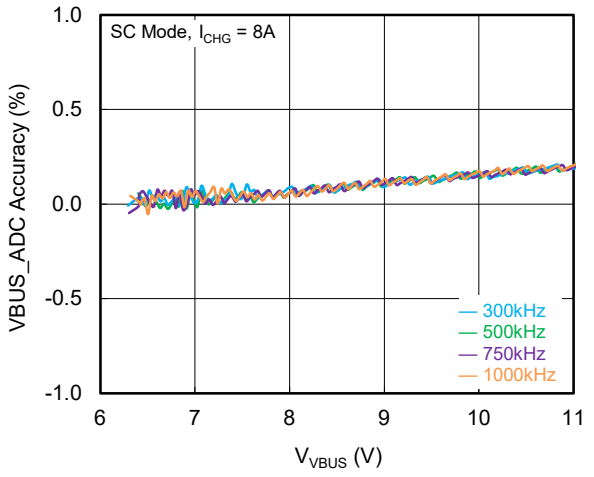

VBAT_ADC Accuracy vs. BAT Voltage



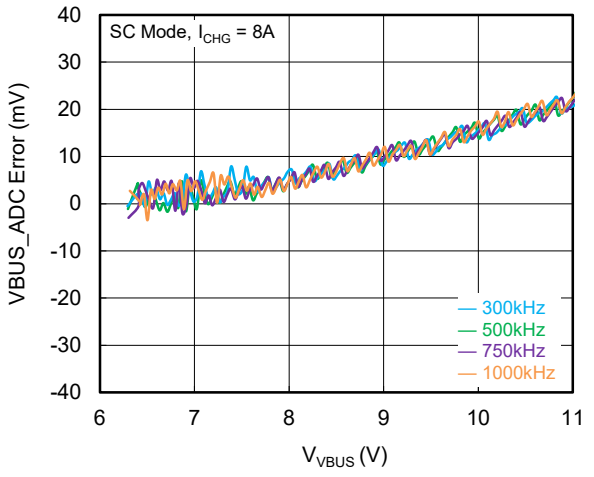

VBAT_ADC Error vs. BAT Voltage



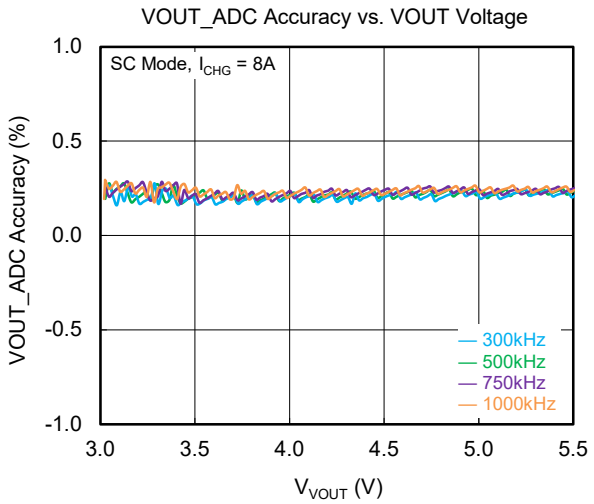

VBUS_ADC Accuracy vs. BUS Voltage

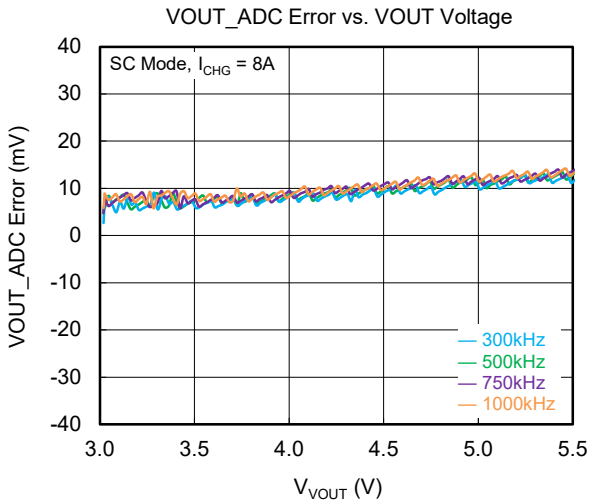



VBUS_ADC Error vs. BUS Voltage



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)



# FUNCTIONAL BLOCK DIAGRAM

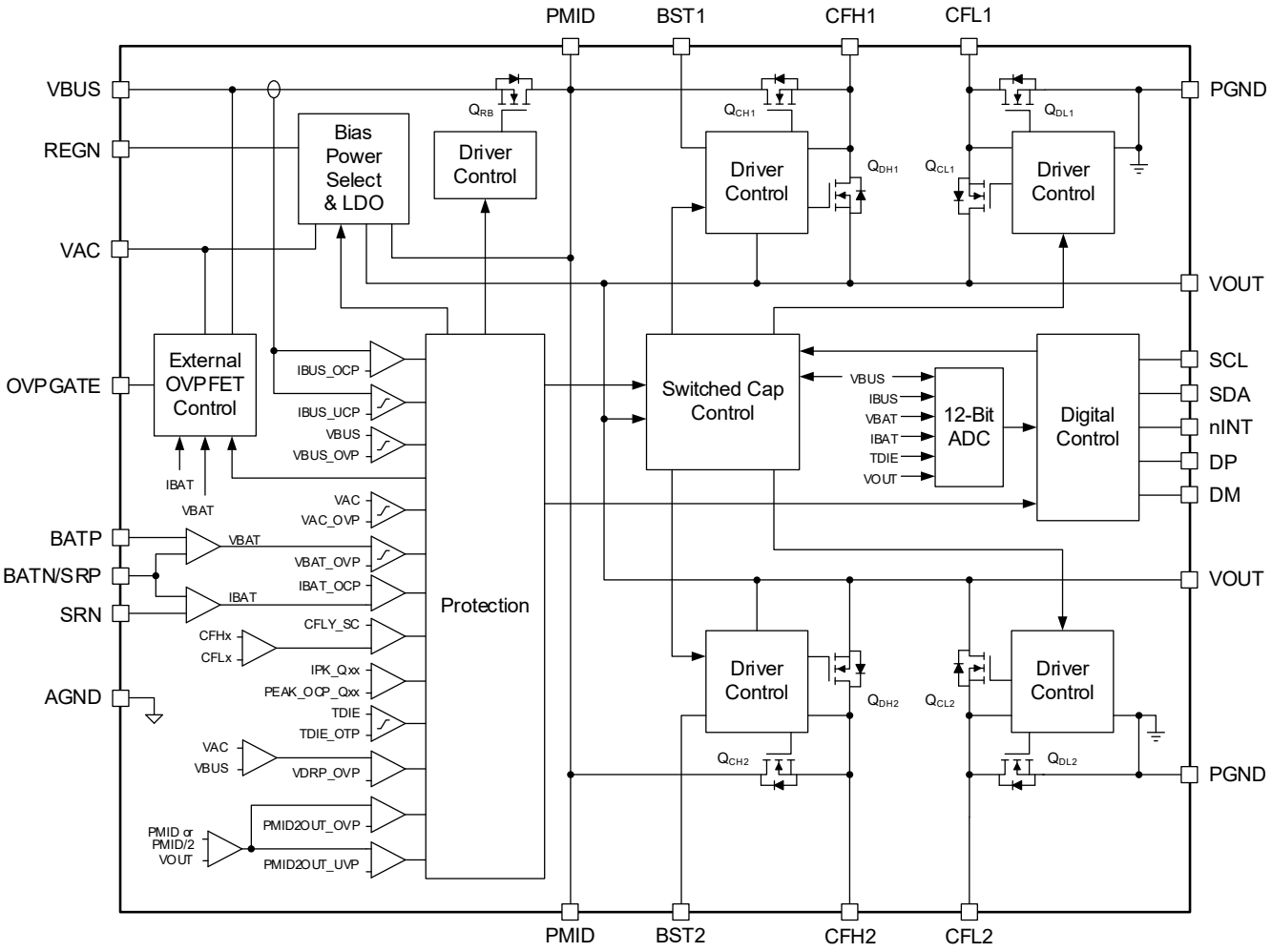



**Figure 2. Functional Block Diagram**

# REGISTER ADDRESS MAPPING

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

## Slave Device Address: 0x6E (0b1101 110 + W/R)

| FUNCTION | FLAG | MASK | THRESHOLD SETTING | ENABLE | DEGLITCH |
|---|---|---|---|---|---|
| DEVICE_REV | -- | -- | 0x03[7:4] | -- | -- |
| DEVICE_ID | -- | -- | 0x03[3:0] | -- | -- |
| REG_RST | -- | -- | 0x00[7] | -- | -- |
| CHG_MODE | -- | -- | 0x00[6:4] | -- | -- |
| WD_TIMEOUT | 0x11[5] | 0x12[5] | 0x00[2:0] | 0x00[3] | |
| FSW_SET | -- | -- | 0x01[7:4] | -- | -- |
| FSW_SHIFT | -- | -- | 0x01[3:2] | -- | -- |
| FSW_DITHER | -- | -- | -- | 0x02[6] | -- |
| OVPGATE | -- | -- | 0x04[7] | 0x04[5] & 0x05[6] | -- |
| VAC_OVP | 0x0D[7] | 0x0E[7] | 0x04[3:0] | 0x04[4] | |
| AC_PDN | 0x0D[6] | 0x0E[6] | -- | 0x05[7] | -- |
| VAC_ABSENT | 0x11[4] | 0x12[4] | -- | -- | -- |
| VDRP_OVP | 0x0D[4] | 0x0E[4] | 0x05[2:0] | 0x05[5] | 0x05[4] |
| VBUS_OVP | 0x0D[3] | 0x0E[3] | 0x06[6:0] | 0x06[7] | -- |
| BUS_PDN | 0x0D[5] | 0x0E[5] | -- | 0x05[6] | -- |
| VBUS_INSERT | 0x11[7] | 0x12[7] | -- | -- | -- |
| VBUS_ABSENT | 0x11[3] | 0x12[3] | -- | -- | -- |
| VBUS_HI | 0x0F[1] | 0x10[1] | 0x02[1:0] | 0x02[4] | 0x08[7] |
| VBUS_LO | 0x0F[2] | 0x10[2] | 0x02[3:2] | 0x02[5] | 0x08[6] |
| IBUS_UCP_TIMEOUT | 0x0D[1] | 0x0E[1] | 0x08[4:2] | 0x07[7] | -- |
| IBUS_UCP_FALL | 0x0D[0] | 0x0E[0] | 0x07[6] | 0x07[7] | 0x08[1:0] |
| IBUS_OCP | 0x0D[2] | 0x0E[2] | 0x07[3:0] | 0x07[5] | -- |
| VOUT_OVP | 0x11[2] | 0x12[2] | 0x0C[2:1] | 0x0C[3] | 0x0C[0] |
| VBAT_OVP | 0x0F[7] | 0x10[7] | 0x09[5:0] | 0x09[7] | -- |
| VBAT_INSERT | 0x11[6] | 0x12[6] | -- | -- | -- |
| VBAT_REG | 0x0F[5] | 0x10[5] | 0x0B[1:0] | 0x0B[2] | -- |
| IBAT_OCP | 0x0F[6] | 0x10[6] | 0x0A[5:0] & 0x0A[6] | 0x0A[7] | -- |
| IBAT_REG | 0x0F[4] | 0x10[4] | 0x0B[4:3] | 0x0B[5] | -- |
| REG_TIMEOUT | -- | -- | -- | 0x0B[6] | -- |
| PEAK_OCP_FWD | 0x0F[0] | 0x10[0] | 0x01[1:0] | -- | -- |
| PMID2OUT_UVP | 0x51[4] | 0x51[2] | 0x0C[7:6] | 0x51[6] | -- |
| PMID2OUT_OVP | 0x51[3] | 0x51[1] | 0x0C[5:4] | 0x51[5] | -- |
| PIN_DIAG (CFLY_SC & VOUT_SC) | 0x11[0] | 0x12[0] | -- | 0x02[7] | -- |
| TDIE_OTP | 0x0F[3] | 0x10[3] | -- | -- | -- |
| ADC | 0x11[1] | 0x12[1] | 0x13[6] | 0x13[7] | -- |

# REGISTER AND DATA

Bit Types:

R: Read only

R/W: Read/Write

RC: Read clears the bit

R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

## REG0x00: CONTROL1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | REG_RST | 0 | R/WC | Register Reset Bit<br>0 = No register reset (default)<br>1 = Reset registers to their default values. When enabled, the associated register bits are reset to their default value and then this bit is automatically reset to 0. | REG_RST |
| D[6:4] | CHG_MODE[2:0] | 000 | R/W | Charge Mode Control Bits<br>000 = Off mode (default)<br>001 = Forward bypass mode<br>010 = Forward Charge-pump voltage divider mode<br>011 ~ 111 = Off mode<br><br>Note: It is not allowed to change charge mode during charging. | REG_RST or WDT |
| D[3] | WDT_DIS | 0 | R/W | Watchdog Enable Bit<br>0 = Watchdog enabled (default)<br>1 = Watchdog disabled | REG_RST |
| D[2:0] | WDT_TIMER[2:0] | 000 | R/W | Watchdog Timer Setting Bits<br>000 = 0.5sec (default)<br>001 = 1sec<br>010 = 2sec<br>011 = 5sec<br>100 = 10sec<br>101 = 20sec<br>110 = 40sec<br>111 = 80sec | REG_RST |

## REG0x01: CONTROL2 Register [reset = 0x31]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:4] | SW_SET[3:0] | 0011 | R/W | Voltage Divider Switching Frequency Setting Bits<br>0000 = 200kHz<br>0001 = 300kHz<br>0010 = 400kHz<br>0011 = 500kHz (default)<br>0100 = 600kHz<br>0101 = 700kHz<br>0110 = 750kHz<br>0111 = 800kHz<br>1000 = 900kHz<br>1001 = 1000kHz<br>1010 = 1100kHz<br>1011 = 1200kHz<br>1100 = 1300kHz<br>1101 = 1400kHz<br>1110 = 1500kHz<br>1111 = 1600kHz | REG_RST |
| D[3:2] | SW_SHIFT[1:0] | 00 | R/W | Bits of Adjusting Switching Frequency for EMI<br>00/11 = Nominal frequency (default)<br>01 = Nominal frequency +10%<br>10 = Nominal frequency -10% | REG_RST |
| D[1:0] | PEAK_OCP_SET[1:0] | 01 | R/W | $Q_{CHx}$ and $Q_{DLx}$ OCP Threshold Setting Bits<br>00 = 11A<br>01 = 13A (default)<br>10 = 15A<br>11 = 17A | REG_RST |

# REGISTER AND DATA (continued)

## REG0x02: CONTROL3 Register [reset = 0xB2]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | PIN_DIAG_EN | 1 | R/W | Pin Diagnosis Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[6] | FSW_DITHER_EN | 0 | R/W | Switching Frequency Dithering Enable Bit<br>0 = Disabled (default)<br>1 = Enabled. Dither varies switching frequency ±10% | REG_RST |
| D[5] | VBUS_LO_EN | 1 | R/W | Low VBUS Error Detection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[4] | VBUS_HI_EN | 1 | R/W | High VBUS Error Detection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[3:2] | VBUS_LO[1:0] | 00 | R/W | Low VBUS Error Reference Setting Bits<br>00 = 1.01 (default)<br>01 = 1.02<br>10 = 1.03<br>11 = 1.04 | REG_RST |
| D[1:0] | VBUS_HI[1:0] | 10 | R/W | High VBUS Error Reference Setting Bits<br>00 = 1.10<br>01 = 1.15<br>10 = 1.20 (default)<br>11 = 1.25 | REG_RST |

## REG0x03: DEVICE_INFO Register [reset = 0x12]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:4] | DEVICE_REV[3:0] | 0001 | R | Device Revision<br>0001 = NTO-A SGM41600S | N/A |
| D[3:0] | DEVICE_ID[3:0] | 0010 | R | Device ID<br>0010 = SGM41600S | N/A |

## REG0x04: AC_OVP Register [reset = 0x18]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | OVPGATE_SET | 0 | R/W | External OVPFET Gate Drive Voltage Setting Bit<br>0 = 4.8V (default)<br>1 = 9V | REG_RST |
| D[6] | Reserved | 0 | R | Reserved | REG_RST |
| D[5] | OVPGATE_EN | 0 | R/W | When VAC is not present but VBUS is present, turn on/off OVPFET by OVPGATE pin.<br>0 = Turn off OVPFET when VAC is not present (default)<br>1 = Turn on OVPFET even when VAC is not present<br><br>Note: when OVPGATE_EN = 1, OVPFET cannot be turned off by BUS_PDN_EN = 1; while OVPGATE_EN = 0, OVPFET can be turned off by BUS_PDN_EN = 1. | REG_RST |
| D[4] | AC_OVP_EN | 1 | R/W | VAC OVP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[3:0] | AC_OVP[3:0] | 1000 | R/W | VAC OVP Protection Rising Threshold Setting Bits<br><br>VAC OVP Rising Threshold Value: = 4V + AC_OVP[3:0] × 1V<br>Offset: 4V<br>Range: 4V (0000) - 19V (1111)<br>Default: 12V (1000) | REG_RST |

# REGISTER AND DATA (continued)

## REG0x05: PULL-DOWN & VDRP_OVP Register [reset = 0x25]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | AC_PDN_EN | 0 | R/WC | VAC Pull-down Resistor Enable Bit<br>0 = Pull-down disabled (default)<br>1 = Pull-down enabled. When enabled, the VAC is pulled down for 400ms and then this bit is automatically reset to 0. | N/A |
| D[6] | BUS_PDN_EN | 0 | R/W | VBUS Pull-down Resistor Enable Bit<br>0 = Pull-down disabled (default)<br>1 = Pull-down enabled. When enabled, it will turn off the external OVPFET and discharge VBUS and PMID with $R_{PDN_VBUS}$ and $R_{PDN_PMID}$. This action is important during a hot-plug event to prevent transient over-voltages. | REG_RST |
| D[5] | VDRP_OVP_EN | 1 | R/W | VDRP OVP Protection Enable Bit, $V_{DRP} = (V_{VAC} - V_{VBUS})$<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[4] | VDRP_OVP_DEG | 0 | R/W | VDRP OVP Protection Deglitch Time Setting Bit<br>This is deglitch time ($t_{DRP_OVP_DEG}$) between the moment $V_{DRP}$ exceeding $V_{DRP_OVP}$ threshold and triggering the protection action.<br>0 = 10μs (default)<br>1 = 5ms | REG_RST |
| D[3] | Reserved | 0 | R | Reserved | N/A |
| D[2:0] | VDRP_OVP[2:0] | 101 | R/W | VDRP OVP Protection Threshold Setting Bits<br><br>VDRP OVP Threshold Value: = 50mV + VDRP_OVP[2:0] × 45mV<br>Offset: 50mV<br>Range: 50mV (000) - 365mV (111)<br>Default: 275mV (101) | REG_RST |

## REG0x06: BUS_OVP Register [reset = 0xCB]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | BUS_OVP_EN | 1 | R/W | VBUS OVP and Peak OVP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[6:0] | BUS_OVP[6:0] | 100 1011 | R/W | Setting Bits of VBUS OVP Protection Rising Threshold<br><br>VBUS OVP Rising Threshold Value: = 4V + BUS_OVP[6:0] × 100mV<br>Offset: 4V<br>Range: 4V (000 0000) - 14V (110 0100)<br>Default: 11.5V (100 1011)<br>If BUS_OVP[6:0] ≥ 110 0100, $V_{BUS_OVP}$ = 14V | REG_RST |

# REGISTER AND DATA (continued)

## REG0x07: IBUS_OCP & UCP Register [reset = 0xA6]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | IBUS_UCP_EN | 1 | R/W | IBUS UCP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default)<br><br>Note: Including IBUS_UCP_TIMEOUT and IBUS_UCP_FALL protections. | REG_RST |
| D[6] | IBUS_UCP | 0 | R/W | IBUS UCP Threshold Setting<br>0 = $I_{BUS_UCP_R}$ = 300mA rising, $I_{BUS_UCP_F}$ = 150mA falling (default)<br>1 = $I_{BUS_UCP_R}$ = 500mA rising, $I_{BUS_UCP_F}$ = 250mA falling<br><br>The system should control the $I_{BUS}$ current to rise above $I_{BUS_UCP_R}$ before $t_{IBUS_UCP_BLK}$ time expires.<br>Note: This bit can only be changed before enabling switching. | REG_RST |
| D[5] | IBUS_OCP_EN | 1 | R/W | IBUS OCP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[4] | Reserved | 0 | R | Reserved | N/A |
| D[3:0] | IBUS_OCP[3:0] | 0110 | R/W | IBUS OCP Threshold Setting<br>IBUS_OCP = 1.2A + IBUS_OCP[3:0] × 300mA<br>Offset: 1.2A<br>Range: 1.2A (0000) - 5.7A (1111)<br>Default: 3A (0110) | REG_RST |

## REG0x08: BUS_PROT_DEG Register [reset = 0x06]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | VBUS_HI_DEG | 0 | R/W | High VBUS Error Detection Deglitch Time Setting Bit<br>This is deglitch time ($t_{VBUS_HI_DEG}$) between the moment $V_{PMID}$ rising above n × ($V_{BUS_HI}$ × $V_{VOUT}$ + 100mV) and triggering protection action (n = 1 or 2, depending on the operation mode)<br>0 = 100ns (default)<br>1 = 100μs | REG_RST |
| D[6] | VBUS_LO_DEG | 0 | R/W | Low VBUS Error Detection Deglitch Time Setting Bit<br>This is deglitch time ($t_{VBUS_LO_DEG}$) between the moment $V_{PMID}$ falling below n × ($V_{BUS_LO}$ × $V_{VOUT}$ - 100mV) and triggering protection action (n = 1 or 2, depending on the operation mode)<br>0 = 10μs (default)<br>1 = 1ms | REG_RST |
| D[5] | Reserved | 0 | R | Reserved | N/A |
| D[4:2] | IBUS_UCP_BLK[2:0] | 001 | R/W | IBUS UCP Protection Blanking Time Setting Bits<br>If IBUS cannot exceed IBUS_UCP_R within $t_{IBUS_UCP_BLK}$, the charging will be stopped and CHG_MODE[2:0] bits are reset to 000.<br>000 = 100ms<br>001 = 200ms (default)<br>010 = 400ms<br>011 = 800ms<br>100 = 2.5s<br>101 = 5s<br>110 = 10s<br>111 = 20s | REG_RST |
| D[1:0] | IBUS_UCP_FALL_DEG[1:0] | 10 | R/W | IBUS UCP Protection Falling Deglitch Time Setting Bit<br>This is deglitch time ($t_{IBUS_UCPF_DEG}$) between the moment $I_{BUS}$ falling below $I_{BUS_UCP_F}$ threshold and triggering protection action.<br>00 = 10μs<br>01 = 8ms<br>10 = 64ms (default)<br>11 = 256ms | REG_RST |

# REGISTER AND DATA (continued)

## REG0x09: BAT_OVP Register [reset = 0x8E]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | BAT_OVP_EN | 1 | R/W | VBAT OVP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[6] | Reserved | 0 | R | Reserved | N/A |
| D[5:0] | BAT_OVP[5:0] | 00 1110 | R/W | VBAT OVP Rising Threshold Setting<br><br>VBAT OVP Rising Threshold Value: = 4V + BAT_OVP[5:0] × 25mV<br>Offset: 4V<br>Range: 4V (00 0000) - 5V (10 1000)<br>Default: 4.35V (00 1110)<br>When BAT_OVP[5:0] ≥ 10 1000, $V_{BAT_OVP}$ = 5V | REG_RST |

## REG0x0A: IBAT_OCP Register [reset = 0xB4]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | IBAT_OCP_EN | 1 | R/W | IBAT OCP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[6] | IBAT_RSNS | 0 | R/W | External IBAT Current Sense Resistor Setting Bit<br>0 = 2mΩ (default)<br>1 = 5mΩ | REG_RST |
| D[5:0] | IBAT_OCP[5:0] | 11 0100 | R/W | IBAT OCP Threshold Setting Bits<br><br>IBAT OCP Threshold Value: = 3A + IBAT_OCP[5:0] × 100mA<br>Offset: 3A<br>Range: 3A (00 0000) to 9.3A (11 1111)<br>Default: 8.2A (11 0100) | REG_RST |

# REGISTER AND DATA (continued)

## REG0x0B: Regulation Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | Reserved | 0 | R | Reserved | N/A |
| D[6] | REG_TIMEOUT_DIS | 0 | R/W | Regulation Timeout Disable<br>0 = Enabled (default)<br>1 = Disabled<br><br>When enabled, charging will be disabled if the regulation lasts longer than 650ms. | REG_RST |
| D[5] | IBAT_REG_EN | 0 | R/W | IBAT Regulation Enable<br>0 = Disabled (default)<br>1 = Enabled<br>When enabled, $t_{IBAT_OCP_DEG}$ is increased to 500μs to avoid unwanted triggering of IBAT_OCP during regulation. | REG_RST |
| D[4:3] | IBAT_REG[1:0] | 00 | R/W | IBAT Regulation Threshold Setting<br>00 = 200mA below IBAT_OCP[5:0] register setting (default)<br>01 = 300mA below IBAT_OCP[5:0] register setting<br>10 = 400mA below IBAT_OCP[5:0] register setting<br>11 = 500mA below IBAT_OCP[5:0] register setting<br><br>The margin below IBAT_OCP[5:0] register at which IBAT regulation starts. | REG_RST |
| D[2] | VBAT_REG_EN | 0 | R/W | VBAT Regulation Enable<br>0 = Disabled (default)<br>1 = Enabled<br>When enabled, $t_{VBAT_OVP_DEG}$ is increased to 500μs to avoid unwanted triggering of VBAT OVP during regulation. | REG_RST |
| D[1:0] | VBAT_REG[1:0] | 00 | R/W | VBAT Regulation Threshold Setting<br>00 = 50mV below BAT_OVP[5:0] register setting (default)<br>01 = 100mV below BAT_OVP[5:0] register setting<br>10 = 150mV below BAT_OVP[5:0] register setting<br>11 = 200mV below BAT_OVP[5:0] register setting<br><br>The margin below BAT_OVP[5:0] register at which VBAT regulation starts. | REG_RST |

## REG0x0C: VOUT_OVP & PMID2OUT_OVP_UVP Register [reset = 0x5B]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:6] | PMID2OUT_ UVP[1:0] | 01 | R/W | PMID/2-VOUT UVP is used to protect input short.<br>00 = -50mV<br>01 = -100mV (default)<br>10 = -150mV<br>11 = -200mV | REG_RST |
| D[5:4] | PMID2OUT_ OVP[1:0] | 01 | R/W | PMID/2-VOUT OVP is used to protect input short.<br>00 = 300mV<br>01 = 400mV (default)<br>10 = 500mV<br>11 = 600mV | REG_RST |
| D[3] | VOUT_OVP_EN | 1 | R/W | VOUT OVP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[2:1] | VOUT_OVP[1:0] | 01 | R/W | VOUT OVP Protection Rising Threshold Setting Bits<br><br>$V_{VOUT_OVP_R}$ = 4.6V + VOUT_OVP[1:0] × 200mV<br>00 = 4.6V<br>01 = 4.8V (default)<br>10 = 5V<br>11 = 5.2V | REG_RST |
| D[0] | VOUT_OVP_DEG | 1 | R/W | VOUT OVP Protection Deglitch Time Setting Bit<br>This is deglitch time ($t_{VOUT_OVP_DEG}$) between the moment $V_{VOUT}$ exceeding $V_{OUT_OVP_R}$ threshold and triggering protection action.<br>0 = 100μs<br>1 = 1ms (default) | REG_RST |

# REGISTER AND DATA (continued)

## REG0x0D: FLT_FLAG1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | AC_OVP_FLAG | 0 | RC | VAC OVP Fault Flag<br>0 = No VAC OVP fault<br>1 = VAC OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VAC OVP fault is cleared, a read on this bit will reset it to 0. | N/A |
| D[6] | AC_PDN_FLAG | 0 | RC | VAC Pull-down Event Flag<br>0 = No VAC pull-down event<br>1 = VAC pull-down event has occurred. It generates an interrupt on nINT pin if unmasked. After the VAC pull-down event is complete, a read on this bit will reset it to 0. | N/A |
| D[5] | BUS_PDN_FLAG | 0 | RC | VBUS Pull-down Event Flag<br>0 = No VBUS pull-down event<br>1 = VBUS pull-down event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS pull-down event is complete, a read on this bit will reset it to 0. | REG_RST |
| D[4] | VDRP_OVP_FLAG | 0 | RC | VDRP OVP Fault Flag<br>0 = No VDRP OVP fault<br>1 = VDRP OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. | N/A |
| D[3] | BUS_OVP_FLAG | 0 | RC | VBUS OVP Fault Flag<br>0 = No VBUS OVP fault<br>1 = VBUS OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS OVP fault is cleared, a read on this bit will reset it to 0. | N/A |
| D[2] | IBUS_OCP_FLAG | 0 | RC | IBUS OCP Fault Flag<br>0 = No IBUS OCP fault<br>1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. | N/A |
| D[1] | IBUS_UCP_ TIMEOUT_FLAG | 0 | RC | IBUS UCP Timeout Fault Flag<br>0 = No IBUS UCP timeout fault<br>1 = IBUS UCP timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. | N/A |
| D[0] | IBUS_UCP_FALL_ FLAG | 0 | RC | IBUS UCP Fall Event Flag<br>0 = No IBUS UCP fall event<br>1 = IBUS UCP fall event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. | REG_RST |

## REGISTER AND DATA (continued)

### REG0x0E: FLT_INT_MASK1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | AC_OVP_MASK | 0 | R/W | Mask VAC OVP Fault Interrupt<br>0 = VAC OVP fault interrupt can work (default)<br>1 = Mask VAC OVP fault interrupt. AC_OVP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[6] | AC_PDN_MASK | 0 | R/W | Mask VAC Pull-down Event Interrupt<br>0 = VAC pull-down event interrupt can work (default)<br>1 = Mask VAC pull-down event interrupt. AC_PDN_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[5] | BUS_PDN_MASK | 0 | R/W | Mask VBUS Pull-down Event Interrupt<br>0 = VBUS pull-down event interrupt can work (default)<br>1 = Mask VBUS pull-down event interrupt. BUS_PDN_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[4] | VDRP_OVP_MASK | 0 | R/W | Mask VDRP OVP Fault Interrupt<br>0 = VDRP OVP fault interrupt can work (default)<br>1 = Mask VDRP OVP fault interrupt. VDRP_OVP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[3] | BUS_OVP_MASK | 0 | R/W | Mask BUS OVP Fault Interrupt<br>0 = BUS OVP fault interrupt can work (default)<br>1 = Mask BUS OVP fault interrupt. BUS_OVP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[2] | IBUS_OCP_MASK | 0 | R/W | Mask IBUS OCP Fault Interrupt<br>0 = IBUS OCP fault interrupt can work (default)<br>1 = Mask IBUS OCP fault interrupt. IBUS_OCP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[1] | IBUS_UCP_<br>TIMEOUT_MASK | 0 | R/W | Mask IBUS_UCP_TIMEOUT Fault Interrupt<br>0 = IBUS_UCP_TIMEOUT fault interrupt can work (default)<br>1 = Mask IBUS_UCP_TIMEOUT fault interrupt.<br>IBUS_UCP_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[0] | IBUS_UCP_FALL_<br>MASK | 0 | R/W | Mask IBUS UCP Fall Event Interrupt<br>0 = IBUS UCP fall event interrupt can work (default)<br>1 = Mask IBUS UCP fall event interrupt. IBUS_UCP_FALL_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |

# REGISTER AND DATA (continued)

## REG0x0F: FLT_FLAG2 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | BAT_OVP_FLAG | 0 | RC | VBAT OVP Fault Flag<br>0 = No VBAT OVP fault<br>1 = VBAT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT OVP fault is cleared, reading this bit will reset it to 0. | N/A |
| D[6] | IBAT_OCP_FLAG | 0 | RC | IBAT OCP Fault Flag<br>0 = No IBAT OCP fault<br>1 = IBAT OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. | N/A |
| D[5] | VBAT_REG_FLAG | 0 | RC | VBAT Regulation Event Flag<br>0 = No VBAT regulation event<br>1 = VBAT regulation event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT regulation event is complete, reading this bit will reset it to 0. | N/A |
| D[4] | IBAT_REG_FLAG | 0 | RC | IBAT Regulation Event Flag<br>0 = No IBAT regulation event<br>1 = IBAT regulation event has occurred. It generates an interrupt on nINT pin if unmasked. After the IBAT regulation event is complete, reading this bit will reset it to 0. | N/A |
| D[3] | TDIE_OTP_FLAG | 0 | RC | TDIE OTP Fault Flag (Die Over-Temperature)<br>0 = No TDIE OTP fault<br>1 = TDIE OTP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the TDIE OTP fault is cleared, reading this bit will reset it to 0. | N/A |
| D[2] | VBUS_LO_FLAG | 0 | RC | VBUS Under-Voltage Fault Flag<br>It is set to 1 if $V_{VBUS}/V_{VOUT} < 2 \times V_{BUS_LO}$ in voltage divider mode, or $V_{VBUS}/V_{VOUT} < V_{BUS_LO}$ in bypass mode.<br>0 = No VBUS under-voltage fault<br>1 = VBUS under-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS under-voltage fault is cleared, reading this bit will reset it to 0. | N/A |
| D[1] | VBUS_HI_FLAG | 0 | RC | VBUS Over-Voltage Fault Flag<br>It is set to 1 if $V_{VBUS}/V_{VOUT} > 2 \times V_{BUS_HI}$ in voltage divider mode, or $V_{VBUS}/V_{VOUT} > V_{BUS_HI}$ in bypass mode.<br>0 = No VBUS over-voltage fault<br>1 = VBUS over-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS over-voltage fault is cleared, reading this bit will reset it to 0. | N/A |
| D[0] | PEAK_OCP_FWD_FLAG | 0 | RC | Switching FETs Peak OCP Fault Flag<br>It is set to 1 if at least one of the internal switching FETs $Q_{CHx}$ and $Q_{DLx}$ reaches its peak OCP threshold.<br>0 = No switching FETs peak OCP fault<br>1 = Switching FETs peak OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0. | N/A |

## REGISTER AND DATA (continued)

### REG0x10: FLT_INT_MASK2 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | BAT_OVP_MASK | 0 | R/W | Mask VBAT OVP Fault Interrupt<br>0 = VBAT OVP fault interrupt can work (default)<br>1 = Mask VBAT OVP fault interrupt. BAT_OVP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[6] | IBAT_OCP_MASK | 0 | R/W | Mask IBAT OCP Fault Interrupt<br>0 = IBAT OCP fault interrupt can work (default)<br>1 = Mask IBAT OCP fault interrupt. IBAT_OCP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[5] | VBAT_REG_MASK | 0 | R/W | Mask VBAT Regulation Event Interrupt<br>0 = VBAT regulation event interrupt can work (default)<br>1 = Mask VBAT regulation event interrupt. VBAT_REG_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[4] | IBAT_REG_MASK | 0 | R/W | Mask IBAT Regulation Event Interrupt<br>0 = IBAT regulation event interrupt can work (default)<br>1 = Mask IBAT regulation event interrupt. IBAT_REG_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[3] | TDIE_OTP_MASK | 0 | R/W | Mask TDIE OTP Fault Interrupt<br>0 = TDIE OTP fault interrupt can work (default)<br>1 = Mask TDIE OTP fault interrupt. TDIE_OTP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[2] | VBUS_LO_MASK | 0 | R/W | Mask VBUS Under-Voltage Fault Interrupt<br>0 = VBUS under-voltage fault interrupt can work (default)<br>1 = Mask VBUS under-voltage fault interrupt. VBUS_LO_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[1] | VBUS_HI_MASK | 0 | R/W | Mask VBUS Over-Voltage Fault Interrupt<br>0 = VBUS over-voltage fault interrupt can work (default)<br>1 = Mask VBUS over-voltage fault interrupt. VBUS_HI_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[0] | PEAK_OCP_FWD_MASK | 0 | R/W | Mask PEAK OCP Fault Interrupt<br>0 = PEAK OCP fault interrupt can work (default)<br>1 = Mask PEAK OCP fault interrupt. PEAK_OCP_FWD_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |

# REGISTER AND DATA (continued)

## REG0x11: FLT_FLAG3 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | BUS_INSERT_FLAG | 0 | RC | VBUS Insert Event Flag<br>This bit is set to 1 if $V_{VBUS}$ > $V_{BUS_PRESENT_R}$.<br>0 = No VBUS insert event<br>1 = VBUS insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS is absent, reading this bit will reset it to 0. | N/A |
| D[6] | BAT_INSERT_FLAG | 0 | RC | VBAT Insert Event Flag<br>If ADC_EN bit = 1 or $V_{VAC}$ > $V_{AC_PRESENT_R}$ or $V_{VBUS}$ > $V_{BUS_PRESENT_R}$, this bit will set to 1 when $V_{BATP}$ > $V_{BAT_PRESENT_R}$.<br>0 = No VBAT insert event<br>1 = VBAT insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the battery is absent, reading this bit will reset it to 0. | N/A |
| D[5] | WD_TIMEOUT_FLAG | 0 | RC | Watchdog Timeout Fault Flag<br>0 = No watchdog timeout fault<br>1 = Watchdog timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. | REG_RST |
| D[4] | AC_ABSENT_FLAG | 0 | RC | VAC Absent Fault Flag<br>This bit is set to 1 if $V_{VAC}$ < $V_{AC_PRESENT_F}$.<br>0 = No VAC absent fault<br>1 = VAC absent fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VAC is present, a read on this bit will reset it to 0. | N/A |
| D[3] | BUS_ABSENT_FLAG | 0 | RC | VBUS Absent Fault Flag<br>It is set to 1 if $V_{VBUS}$ < $V_{BUS_PRESENT_F}$.<br>0 = No VBUS absent fault<br>1 = VBUS absent fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS is present, a read on this bit will reset it to 0. | N/A |
| D[2] | VOUT_OVP_FLAG | 0 | RC | VOUT OVP Fault Flag<br>0 = No VOUT OVP fault<br>1 = VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VOUT OVP fault is cleared, reading this bit will reset it to 0. | N/A |
| D[1] | ADC_DONE_FLAG | 0 | RC | ADC Conversion Complete Flag<br>In 1-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is completed.<br>0 = Normal<br>1 = ADC conversion complete. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. | N/A |
| D[0] | PIN_DIAG_FLAG | 0 | RC | Pin Diagnosis Fail Fault Flag<br>When switching is enabled, certain conditions are checked on the $C_{FLY}$ and VOUT pins to assure proper operation.<br>0 = Normal<br>1 = $C_{FLY}$ short or VOUT pin short fault has occurred. It generates an interrupt on nINT pin. Reading this bit will reset it to 0. | N/A |

## REGISTER AND DATA (continued)

### REG0x12: FLT_INT_MASK3 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | BUS_INSERT_MASK | 0 | R/W | Mask BUS_INSERT Event Interrupt<br>0 = BUS_INSERT event interrupt can work (default)<br>1 = Mask BUS_INSERT event interrupt. BUS_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[6] | BAT_INSERT_MASK | 0 | R/W | Mask BAT_INSERT Event Interrupt<br>0 = BAT_INSERT event interrupt can work (default)<br>1 = Mask BAT_INSERT event interrupt. BAT_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[5] | WD_TIMEOUT_MASK | 0 | R/W | Mask WD_TIMEOUT Fault Interrupt<br>0 = WD_TIMEOUT fault interrupt can work (default)<br>1 = Mask WD_TIMEOUT fault interrupt. WD_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[4] | AC_ABSENT_MASK | 0 | R/W | Mask AC_ABSENT Fault Interrupt<br>0 = AC_ABSENT fault interrupt can work (default)<br>1 = Mask AC_ABSENT fault interrupt. AC_ABSENT_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[3] | BUS_ABSENT_MASK | 0 | R/W | Mask BUS_ABSENT Fault Interrupt<br>0 = BUS_ABSENT fault interrupt can work (default)<br>1 = Mask BUS_ABSENT fault interrupt. BUS_ABSENT_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[2] | VOUT_OVP_MASK | 0 | R/W | Mask VOUT OVP Fault Interrupt<br>0 = VOUT OVP fault interrupt can work (default)<br>1 = Mask VOUT OVP fault interrupt. VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated. | REG_RST |
| D[1] | ADC_DONE_MASK | 0 | R/W | Mask ADC Complete Event Interrupt<br>0 = ADC_DONE event interrupt can work (default)<br>1 = Mask ADC_DONE event interrupt. ADC_DONE_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[0] | PIN_DIAG_MASK | 0 | R/W | Mask Pin Diagnosis Fail Interrupt<br>0 = Pin diagnosis fail interrupt can work (default)<br>1 = Mask pin diagnosis fail interrupt. PIN_DIAG_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |

# REGISTER AND DATA (continued)

## REG0x13: ADC_CTRL Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | ADC_EN | 0 | R/W | ADC Conversion Enable<br>0 = Disabled (default)<br>1 = Enabled<br><br>Note: In 1-shot mode when the selected channel conversions are completed, the ADC_EN bit is automatically reset to 0.<br>All channel conversions except IBUS_ADC and IBAT_ADC can be enabled even when the device is not during charging (CHG_MODE[2:0] = 000). | REG_RST or WDT |
| D[6] | ADC_RATE | 0 | R/W | ADC Conversion Mode Control<br>0 = Continuous conversion (default)<br>1 = 1-shot conversion | REG_RST |
| D[5] | VBUS_ADC_DIS | 0 | R/W | VBUS ADC Control<br>0 = Enable conversion (default)<br>1 = Disable conversion | REG_RST |
| D[4] | IBUS_ADC_DIS | 0 | R/W | IBUS ADC Control<br>0 = Enable conversion (default)<br>1 = Disable conversion | REG_RST |
| D[3] | VBAT_ADC_DIS | 0 | R/W | VBAT ADC Control<br>0 = Enable conversion (default)<br>1 = Disable conversion | REG_RST |
| D[2] | IBAT_ADC_DIS | 0 | R/W | IBAT ADC Control<br>0 = Enable conversion (default)<br>1 = Disable conversion | REG_RST |
| D[1] | TDIE_ADC_DIS | 0 | R/W | TDIE ADC Control<br>0 = Enable conversion (default)<br>1 = Disable conversion | REG_RST |
| D[0] | VOUT_ADC_DIS | 0 | R/W | VOUT ADC Control<br>0 = Enable conversion (default)<br>1 = Disable conversion | REG_RST |

## REG0x14: VBUS_ADC1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:4] | Reserved | 0000 | R | Reserved | N/A |
| D[3:0] | VBUS_ADC[11:8] | 0000 | R | Higher 4 bits of the 12-bit ADC VBUS Data (4mV resolution)<br>MSB<3:0>: 8192mV, 4096mV, 2048mV, 1024mV | REG_RST |

## REG0x15: VBUS_ADC0 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:0] | VBUS_ADC[7:0] | 0000 0000 | R | Low Byte of the ADC VBUS Data (4mV resolution)<br>LSB<7:0>: 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV | REG_RST |

## REG0x16: IBUS_ADC1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:4] | Reserved | 0000 | R | Reserved | N/A |
| D[3:0] | IBUS_ADC[11:8] | 0000 | R | Higher 4 bits of the 12-bit ADC IBUS Data (2mA resolution)<br>MSB<3:0>: 4096mA, 2048mA, 1024mA, 512mA | REG_RST |

## REG0x17: IBUS_ADC0 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:0] | IBUS_ADC[7:0] | 0000 0000 | R | Low Byte of the ADC IBUS Data (2mA resolution)<br>LSB<7:0>: 256mA, 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA | REG_RST |

# REGISTER AND DATA (continued)

## REG0x18: VBAT_ADC1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:4] | Reserved | 0000 | R | Reserved | N/A |
| D[3:0] | VBAT_ADC[11:8] | 0000 | R | Higher 4 bits of the 12-bit ADC VBAT Data (2mV resolution)<br>MSB<3:0>: 4096mV, 2048mV, 1024mV, 512mV | REG_RST |

## REG0x19: VBAT_ADC0 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:0] | VBAT_ADC[7:0] | 0000 0000 | R | Low Byte of the ADC VBAT Data (2mV resolution)<br>LSB<7:0>: 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV | REG_RST |

## REG0x1A: IBAT_ADC1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:4] | Reserved | 0000 | R | Reserved | N/A |
| D[3:0] | IBAT_ADC[11:8] | 0000 | R | Higher 4 bits of the 12-bit IBAT Data (2.5mA resolution)<br>MSB<3:0>: 5120mA, 2560mA, 1280mA, 640mA | REG_RST |

## REG0x1B: IBAT_ADC0 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:0] | IBAT_ADC[7:0] | 0000 0000 | R | Low Byte of ADC IBAT Data (2.5mA resolution)<br>LSB<7:0>: 320mA, 160mA, 80mA, 40mA, 20mA, 10mA, 5mA, 2.5mA | REG_RST |

## REG0x1C: VOUT_ADC1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:4] | Reserved | 0000 | R | Reserved | N/A |
| D[3:0] | VOUT_ADC[11:8] | 0000 | R | Higher 4 bits of the 12-bit ADC VOUT Data (2mV resolution)<br>MSB<3:0>: 4096mV, 2048mV, 1024mV, 512mV | REG_RST |

## REG0x1D: VOUT_ADC0 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:0] | VOUT_ADC[7:0] | 0000 0000 | R | Low Byte of the ADC VOUT Data (2mV resolution)<br>LSB<7:0>: 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV | REG_RST |

## REG0x1E: TDIE_ADC Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:0] | TDIE_ADC[7:0] | 0000 0000 | R | ADC TDIE Data (8-bit, 1℃ resolution)<br>LSB<7:0>: 128℃, 64℃, 32℃, 16℃, 8℃, 4℃, 2℃, 1℃<br>$T_{DIE}$ = TDIE_ADC[7:0] × 1℃ - 40℃ | REG_RST |

# REGISTER AND DATA (continued)

## REG0x21: BC1.2_FLAG1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:6] | Reserved | 00 | R | Reserved | N/A |
| D[5] | VAC_CHG_FLAG | 0 | RC | Event Flag of VAC Voltage Change<br>0 = No VAC voltage change event<br>1 = VAC voltage change event has occurred, namely that VAC present or absent event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0. | N/A |
| D[4] | USB_DEVICE_CHG_FLAG | 0 | RC | Event Flag of USB BC1.2 Device Status Bits Change<br>0 = No USB_DEVICE_STAT[2:0] bits change event<br>1 = USB_DEVICE_STAT[2:0] bits change event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0. | N/A |
| D[3:0] | Reserved | 0000 | R | Reserved | N/A |

## REG0x22: BC1.2_MASK1 Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:6] | Reserved | 00 | R | Reserved | N/A |
| D[5] | VAC_CHG_MASK | 0 | R/W | Mask Interrupt of VAC Voltage Change Event<br>0 = Interrupt of VAC voltage change event can work. (default)<br>1 = Mask interrupt of VAC voltage change event.<br>VAC_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin. | N/A |
| D[4] | USB_DEVICE_CHG_MASK | 0 | R/W | Mask Interrupt of USB BC1.2 Device Status Bits Change Event<br>0 = Interrupt of USB_DEVICE_STAT[2:0] bits change event can work. (default)<br>1 = Mask interrupt of USB_DEVICE_STAT[2:0] bits change event. USB_DEVICE_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin. | N/A |
| D[3:0] | Reserved | 0000 | R | Reserved | N/A |

## REG0x23: DPDM_DETC Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | DPDM_DETC_EN | 0 | R/W | Enable Bit of DP/DM Detection for Debug<br>0 = Disabled (default)<br>1 = Enabled. The DP/DM detection results are updated every 8ms. | N/A |
| D[6:4] | DP_RSLT[2:0] | 000 | R | DP Pin Voltage Detection Result Bits<br>000 = 0V. The DP pin voltage is in the range of 0 to 0.05V.<br>001 = 0.2V. The DP pin voltage is in the range of 0.15V to 0.25V.<br>010 = 0.6V. The DP pin voltage is in the range of 0.55V to 0.65V.<br>011 = 1.8V. The DP pin voltage is in the range of 1.65V to 1.95V.<br>100 = 3.3V.The DP pin voltage is in the range of 3V to 3.6V.<br>111 = Error. The DP pin voltage is not listed above.<br><br>Only valid when DPDM_DETC_EN bit is set to 1. | N/A |
| D[3] | Reserved | 0 | R | Reserved | N/A |
| D[2:0] | DM_RSLT[2:0] | 000 | R | DM Pin Voltage Detection Result Bits<br>000 = 0V. The DM pin voltage is in the range of 0 to 0.05V.<br>001 = 0.2V. The DM pin voltage is in the range of 0.15V to 0.25V.<br>010 = 0.6V. The DM pin voltage is in the range of 0.55V to 0.65V.<br>011 = 1.8V. The DM pin voltage is in the range of 1.65V to 1.95V.<br>100 = 3.3V.The DM pin voltage is in the range of 3V to 3.6V.<br>111 = Error. The DM pin voltage is not in the ranges listed above.<br><br>Only valid when DPDM_DETC_EN bit is set to 1. | N/A |

# REGISTER AND DATA (continued)

## REG0x24: BC1.2_CTRL Register [reset = 0x18]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:6] | Reserved | 00 | R | Reserved | N/A |
| D[5:4] | DCD_TIMER[1:0] | 01 | R/W | DCD Timer $t_{DCD_TIMEOUT}$ Setting Bits<br>00 = The DCD detection is disabled.<br>01 = 600ms (default)<br>10 = 900ms<br>11 = The DCD timer is infinite. The BC1.2 detection cannot step forward until DP voltage is detected below $V_{LGC_LOW}$. | N/A |
| D[3] | DCD_DELAY | 1 | R/W | DCD Detection Delay Time Setting Bit for BC1.2<br>This is delay time ($t_{DCD_DLY}$) from when BC1.2 is enabled and VBUS is present to when the DCD detection starts.<br>0 = 150ms<br>1 = 300ms (default) | N/A |
| D[2] | BC_AUTO_EN | 0 | R/W | BC1.2 Automatic Detection Enable Bit<br>0 = Disabled (default)<br>1 = Enabled. When $V_{VAC}$ is present, it will automatically start BC1.2 detection. | N/A |
| D[1:0] | Reserved | 00 | R | Reserved | N/A |

## REG0x25: DPDM_CTRL Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7:6] | Reserved | 00 | R | Reserved | N/A |
| D[5:4] | DP_DAC[1:0] | 00 | R/W | DP Pin Output Driver Voltage Setting Bits<br>00 = HiZ mode (default)<br>01 = 0V ($V_{0P0_VSRC}$)<br>10 = 0.6V ($V_{0P6_VSRC}$)<br>11 = 3.3V ($V_{3P3_VSRC}$)<br><br>Note: The bit configurations are invalid during BC1.2 detection. | N/A |
| D[3:2] | DM_DAC[1:0] | 00 | R/W | DM Pin Output Driver Voltage Setting Bits<br>00 = HiZ mode (default)<br>01 = 0V ($V_{0P0_VSRC}$)<br>10 = 0.6V ($V_{0P6_VSRC}$)<br>11 = 3.3V ($V_{3P3_VSRC}$)<br><br>Note: The bit configurations are invalid during BC1.2 detection. | N/A |
| D[1] | DPDM_DAC_EN | 0 | R/W | Enable Bit of DP/DM DAC<br>0 = Disabled (default)<br>1 = Enabled | N/A |
| D[0] | Reserved | 0 | R | Reserved | N/A |

## REG0x28: USB_STAT Register [reset = 0x00]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | Reserved | 0 | R | Reserved | N/A |
| D[6:4] | USB_DEVICE_STAT[2:0] | 000 | R | Status Bit of USB BC1.2 Device Detection<br>000 = No input<br>001 = BC1.2 detection in progress<br>010 = SDP device detected<br>011 = Non-standard adapter detected<br>100 = DCP device detected<br>101 = CDP device detected<br>110 ~ 111 = Reserved | N/A |
| D[3:1] | Reserved | 000 | R | Reserved | N/A |
| D[0] | DCD_TIMEOUT_FLAG | 0 | RC | BC1.2 DCD Timeout Fault Flag Bit<br>0 = No BC1.2 DCD timeout fault<br>1 = BC1.2 DCD timeout fault has occurred. Generate an interrupt on nINT pin. Read this bit to reset it to 0. | N/A |

# REGISTER AND DATA (continued)

## REG0x51: PMID2OUT CTRL Register [reset = 0x60]

| BITS | BIT NAME | DEFAULT | TYPE | DESCRIPTION | RESET BY |
|---|---|---|---|---|---|
| D[7] | Reserved | 0 | R | Reserved | N/A |
| D[6] | PMID2OUT_UVP_EN | 1 | R/W | PMID2OUT_UVP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[5] | PMID2OUT_OVP_EN | 1 | R/W | PMID2OUT_OVP Protection Enable Bit<br>0 = Disabled<br>1 = Enabled (default) | REG_RST |
| D[4] | PMID2OUT_UVP_FLAG | 0 | RC | PMID to OUT UVP Flag<br>0 = Normal (default)<br>1 = PMID2OUT_UVP fault event has occurred. It generates an interruption nINT pin if unmasked. | N/A |
| D[3] | PMID2OUT_OVP_FLAG | 0 | RC | PMID to OUT OVP Flag<br>0 = Normal (default)<br>1 = PMID2OUT_OVP fault event has occurred. It generates an interruption nINT pin if unmasked. | N/A |
| D[2] | PMID2OUT_UVP_MASK | 0 | R/W | Mask PMID2OUT_UVP Fault Interrupt<br>0 = PMID2OUT_UVP fault interrupt can work (default)<br>1 = Mask PMID2OUT_UVP fault interrupt.<br>PMID2OUT_UVP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[1] | PMID2OUT_OVP_MASK | 0 | R/W | Mask PMID2OUT_OVP Fault Interrupt<br>0 = PMID2OUT_OVP fault interrupt can work (default)<br>1 = Mask PMID2OUT_OVP fault interrupt.<br>PMID2OUT_OVP_FLAG bit is set after the event, but the interrupt signal is not generated. | REG_RST |
| D[0] | Reserved | 0 | R | Reserved | N/A |

# DETAILED DESCRIPTION

The SGM41600S is an efficient 8A battery charger that operates in voltage divider mode (switched-capacitor charge pump) or in bypass mode. A two-channel switched-capacitor core is integrated in the device to minimize the ripples and improve efficiency in the voltage divider mode. A FET control output for protection, a reverse blocking NFET and all other necessary protection features for safe charging are included. A high speed 12-bit ADC converter is also included to provide bus voltage, bus current, battery voltage, battery current, output voltage and die temperature information for the charge management host via I²C serial interface.

## Charge-Pump Voltage Divider Mode

The charge-pump voltage divider mode operates with a fixed 50% duty cycle. The basic principle of operation is shown in Figure 3. In period 1, Q1 and Q3 are tuned on and $V_{PMID}$ charges the $C_{FLY}$ and the battery (in series) such that:

$$V_{CFLY} = V_{PMID} - V_{BAT} \quad (1)$$

In period 2, Q2 and Q4 are turned on and $C_{FLY}$ appears in parallel with the battery:

$$V_{CFLY} = V_{BAT} \quad (2)$$

Ignoring the small fluctuation of the capacitor and battery voltages in period 1 and 2 in steady state operation, Equation 1 and 2 can be combined to calculate capacitor voltage:

$$V_{CFLY} = V_{BAT} = V_{PMID}/2 \quad (3)$$

Ignoring small energy loss in each switching period, the input and output cycle-average powers are equal. Therefore,

$$V_{PMID} \times I_{BUS} = V_{BAT} \times I_{BAT} \quad (4)$$

or

$$I_{BUS} = I_{BAT}/2 \quad (5)$$

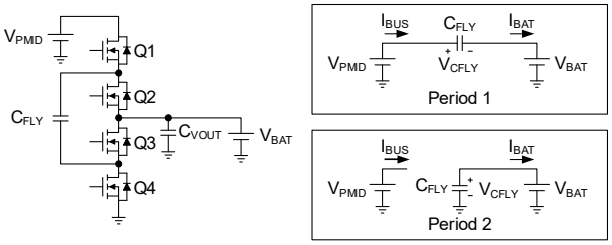



**Figure 3. Voltage Divider Charger Operating Principle**

Assuming no charge leakage path and considering $R_{EFF}$ as the effective input to output resistance (due to the switch on-resistances and $C_{FLY}$ losses), the divider can be modeled as shown in Figure 4. Using this model, the output voltage is half of the input voltage under no load conditions as explained before. The SGM41600S has two channels of such architecture operating at $f_{SW}$ frequency with 180° phase difference. Each channel provides $I_{VOUT}/2$ at the VOUT node, so:

$$V_{VOUT} = ½V_{PMID} - ½R_{EFF} \times I_{VOUT} \quad (6)$$

At low switching frequencies the capacitor charge sharing losses are dominant and $R_{EFF} \approx 1/(4f_{SW}C_{FLY})$. As frequency increases, $R_{EFF}$ finally approaches ($R_{DS_QCH} + R_{DS_QDH} + R_{DS_QCL} + R_{DS_QDL}$)/2.

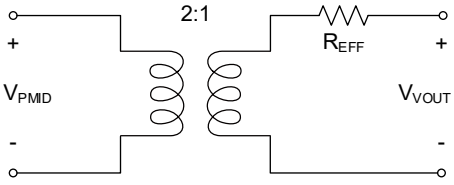



**Figure 4. Model of Voltage Divider**

The two-channel interleaved operation ensures a smooth input current and simplifies the noise filtering. The VOUT ripple can be estimated by first order approximation of $C_{FLY}$ voltage drop due to the discharge in the half period, plus the discharge drop during the short dead time (15ns, TYP).

Selecting high quality $C_{FLY}$ capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance ($R_{EFF}$). An optimum switching frequency can be found for any selected $C_{FLY}$ capacitor to minimize losses.

## Bypass Mode

The SGM41600S is designed to operate in bypass mode when $V_{VBUS}$ is close to the $V_{VOUT}$. When such valid voltage is present on VBUS, the device enters bypass mode and all switches between VBUS and VOUT are fully turned on while the other switches are kept off. When $V_{VBUS}$ is near $V_{VOUT}$, the bypass mode offers the best efficiency and the device is capable of sourcing up to 5.6A.

The output voltage is close to the $V_{VBUS}$ minus a voltage drop caused by the on-resistances of the RBFET plus the two high-side switches of the two channels in parallel:

$$R_{EFF}(\text{Bypass mode}) \approx R_{DS_QRB} + (R_{DS_QCH1} + R_{DS_QDH1}) \| (R_{DS_QCH2} + R_{DS_QDH2}) \quad (7)$$

where $R_{DS_QXX}$ is the on-resistance of the switch $Q_{XX}$.

# DETAILED DESCRIPTION (continued)

## Charge System

The SGM41600S is a slave charger device and needs a host. The host must set up all protection functions and disable the main charger before enabling the SGM41600S. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 5 shows the block diagram of a charge system using the SGM41600S along with other devices. In this system, the SGM41600S can be used to detect the adapter by BC1.2 and the PD controller is used to communicate with adapter by PD protocol. When the smart wall adapter is detected, the AP unit controls the switching charger (SGM41516) that powers the load system and the switched capacitor charger (SGM41600S) that provides high current charging. The communication between those devices is through I²C interface.

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 6. During the trickle charge and pre-charge, the charging is controlled by the switching charger. Once the battery voltage reaches 3V, the adapter can negotiate for a higher bus voltage and enable the SGM41600S for charging (bypass or voltage divider mode). Once the battery voltage reaches the $V_{BAT_REG}$ point, the SGM41600S provides feedback to the adapter to reduce the current. This will eventually reduce and ramp down the bus current below $I_{BUS_UCP_F}$.

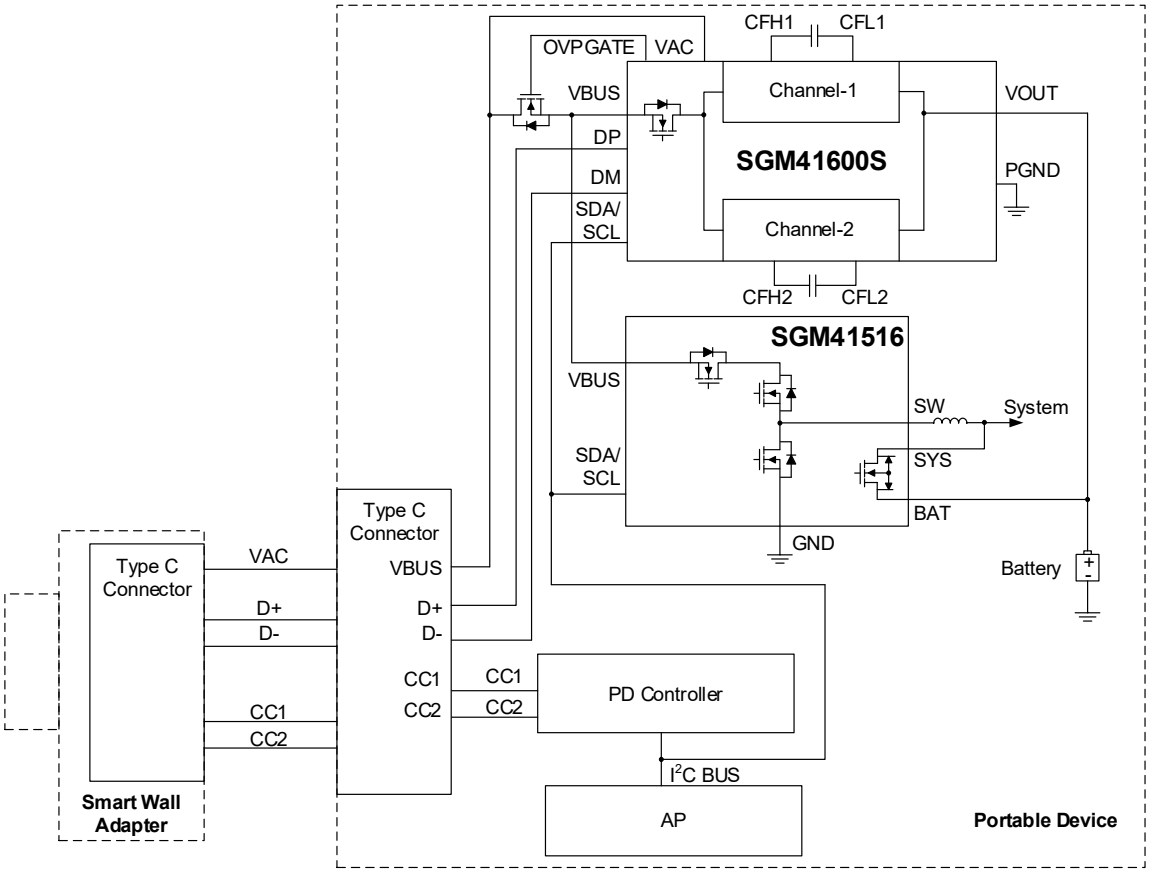



**Figure 5. Simplified Charge System**

## DETAILED DESCRIPTION (continued)

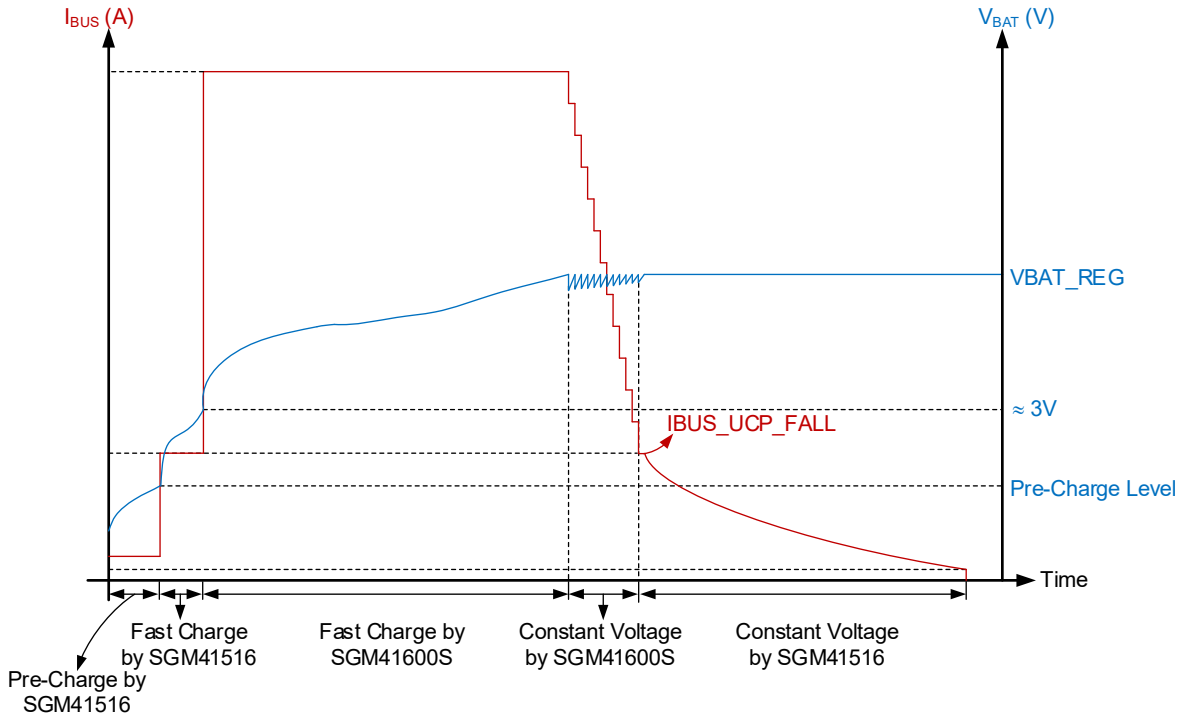



**Figure 6. SGM41600S System Charging Profile**

### Startup Sequence

The SGM41600S is powered from the greater of VAC or VOUT (VAC is used as sense input for adapter voltage as well). The internal watchdog timer is enabled by default and if no I²C read or write occurs before its expiry, the ADC_EN and CHG_MODE[2:0] bits are reset to their default values and after an initial 8ms power-up time, an INT pulse is triggered to show watchdog timeout. The host should not attempt to read or write before this initial nINT signal.

The device does not start charging after powered up, because by default the charger is disabled but the ADC is enabled and the host can read the system parameters before enabling charge. The charge can be enabled only if $V_{VBUS}$ > $V_{BUS_PRESENT_R}$ and $V_{BATP}$ > $V_{BAT_PRESENT_R}$.

### Device Power-up from Battery without Input Source

To reduce the quiescent current and maximize the battery run time when it is the only available source, the REGN LDO and most of the sensing circuits are turned off, except AC_PRESENT, BUS_INSERT and BAT_INSERT functions. When the BUS_PDN_EN bit is set, the external OVPFET is turned off, and VBUS pull-down $R_{PDN_VBUS}$ is activated to help discharging VBUS after a hot-plug event. This will keep the device in low quiescent current mode even after an input source is plugged.

### Device Power-up from Input Source

When an input source is plugged-in and the $V_{VBUS}$ > $V_{BUS_PRESENT_R}$ condition is valid, the host must initialize all protections to the desired thresholds before enabling charge. The protection thresholds that need to be set are VAC_OVP, VBUS_LO, VBUS_HI, VBUS_OVP, IBUS_OCP, IBUS_UCP, VBAT_OVP, IBAT_OCP, VBAT_REG, IBAT_REG, and VDRP_OVP. If one of the protection trigger conditions is met, the charger stops switching. It will also be turned off the external OVPFET when VAC_OVP or VBUS_SC event occurs.

After setting protections, the VBUS voltage is checked to be between 2 × $V_{BUS_LO}$ × $V_{VOUT}$ and 2 × $V_{BUS_HI}$ × $V_{VOUT}$ to allow voltage divider mode operation, or between $V_{BUS_LO}$ × $V_{VOUT}$ and $V_{BUS_HI}$ × $V_{VOUT}$ for bypass mode operation. Charging is enabled and current flows into the battery when the host sets bypass or voltage divider mode by writing 001 or 010 in the CHG_MODE[2:0] bits respectively. Then raising the VBUS voltage will increase the battery charge current. When the converter is on, any command to change the charge mode is ignored. To do so, the charging must be disabled first, and then the charge mode can be changed by I²C serial interface.

# DETAILED DESCRIPTION (continued)

## ADC

The SGM41600S integrates a fast 6-channel, 12-bit ADC converter to monitor input/output currents and voltages and the temperature of the device. The ADC is controlled by the ADC_CTRL register. Setting the ADC_EN bit to 1 enables the ADC. This bit can be used to turn off the ADC and save power when it is not needed. The ADC_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC operates independent of the faults, unless the host sets the ADC_EN bit to 0.

The ADC can operate if $V_{VAC}$ > $V_{AC_PRESENT_R}$ or $V_{VBUS}$ > $V_{BUS_PRESENT_R}$ or $V_{BATP}$ > 2.8V condition is valid. Otherwise the ADC conversion is postponed until one of them is satisfied. The ADC readings are valid only for DC values and not for transients.

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the ADC_CTRL register. If the 1-shot conversion mode is selected, the ADC_DONE_FLAG bit is set to 1 when all channels are converted, then the ADC_EN bit is reset to 0. In the continuous conversion mode, the ADC_DONE_FLAG bit is set to 0.

## nINT Pin, Flag and Mask Bits

The nINT pin is an open-drain output and must be pulled up to a logic high rail. It is pulled low with a duration of $t_{INT}$ to notify the host when it is triggered by an event. See the register map for all event flag and control bits.

When an event occurs, a nINT signal is sent to the host and the corresponding flag bit is set to 1. The flag bit can be read and reset only after the fault is cleared. The nINT signal is not re-sent if an event is still present after the flag bit is read, unless another kind of event occurs. If an event mask bit is set, that event will not send nINT signal, but the flag bit is still updated independent of the mask bit.

The INT pulse generation behavior examples are shown in Figure 7, and Table 1 lists all the enable condition and corresponding actions for different fault events.

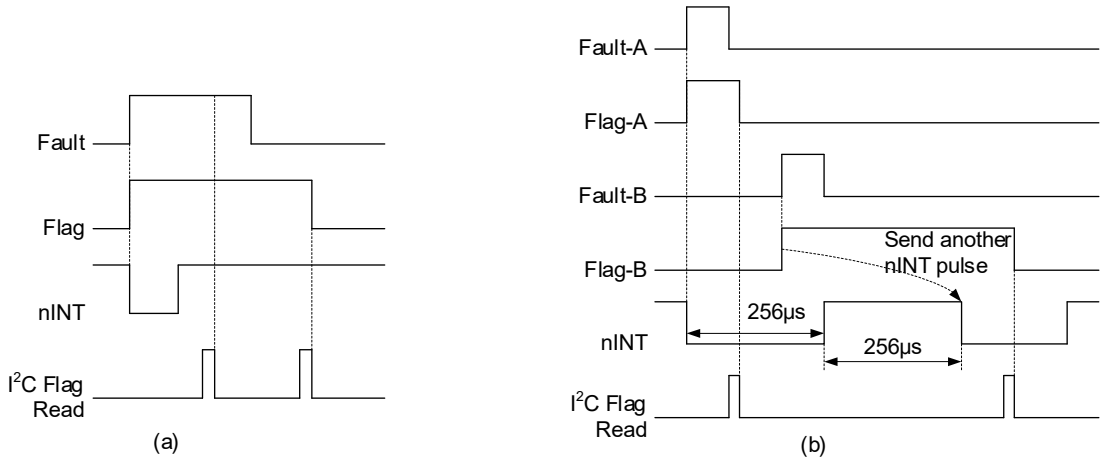



**Figure 7. nINT Pulse Generation Behavior Examples**

# DETAILED DESCRIPTION (continued)

**Table 1. Fault Event Activation List**

| FAULT EVENT | CONDITIONS | PROTECTION ACTION |
|---|---|---|
| **VAC_OVP** | During AC_PRESENT interval, $V_{AC}$ > $V_{AC_OVP_R}$ with 200ns deglitch | Turn off OVPFET in 100ns and enable $R_{PDN_VBUS}$ and $R_{PDN_PMID}$ discharging, reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VBUS_SC** | During BUS_INSERT or OVPFET turn-on interval, $V_{VBUS}$ < 2.7V with 100ns deglitch | Turn off OVPFET in 100μs and enable $R_{PDN_VBUS}$ discharging, reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VBUS_LO** | CHG_MODE[2:0] <> 000 (disabled during $t_{FWSS}$ soft-start timer) or ADC_EN = 1<br>During $Q_{RB}$ OFF, $V_{VBUS}$ < (nVBUS_LO × $V_{VOUT}$ - 200mV)<br>During $Q_{RB}$ ON, $V_{PMID}$ < (nVBUS_LO × $V_{VOUT}$ - 200mV)<br>(n = 1 or 2, depending on the operation mode) | Before charging starts, suspend initiation;<br>or after soft-start timer, reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VBUS_HI** | CHG_MODE[2:0] <> 000 (disabled during $t_{FWSS}$ soft-start timer) or ADC_EN = 1<br>During $Q_{RB}$ OFF, $V_{VBUS}$ > (nVBUS_HI × $V_{VOUT}$ + 200mV)<br>During $Q_{RB}$ ON, $V_{PMID}$ > (nVBUS_HI × $V_{VOUT}$ + 200mV)<br>(n = 1 or 2, depending on the operation mode) | Before charging starts, suspend initiation;<br>or after soft-start timer, reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VBUS_OVP** | During BUS_INSERT interval, $V_{VBUS}$ > $V_{BUS_OVP_R}$ with 2μs deglitch | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **IBUS_OCP** | CHG_MODE[2:0] <> 000, $I_{BUS}$ > $I_{BUS_OCP}$ with 50μs deglitch | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **IBUS_UCP_TIMEOUT** | CHG_MODE[2:0] <> 000, $I_{BUS}$ < $I_{BUS_UCP_R}$ when $t_{IBUS_UCP_BLK}$ timeout | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **IBUS_UCP_FALL** | CHG_MODE[2:0] <> 000, $I_{BUS}$ < $I_{BUS_UCP_F}$ with $t_{IBUS_UCPF_DEG}$ deglitch after $t_{IBUS_UCP_BLK}$ timer expired | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VOUT_OVP** | $V_{VOUT}$ > $V_{OUT_OVP_R}$ with $t_{VOUT_OVPR_DEG}$ deglitch during BAT_INSERT interval | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VOUT_SC** | CHG_MODE[2:0] <> 000, $V_{VOUT}$ < 2.7V with 100ns deglitch | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VBAT_OVP** | $V_{BAT}$ > $V_{BAT_OVP_R}$ with 50μs deglitch during BAT_INSERT interval | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **IBAT_OCP** | CHG_MODE[2:0] <> 000, $I_{BAT}$ > $I_{BAT_OCP}$ with 50μs deglitch | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **CFLY_SC** | CHG_MODE[2:0] = 010, $V_{CFLY}$ < ($V_{VOUT}$ - 1.2V) with 100ns deglitch after $C_{FLY}$ pre-charge | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **PEAK_OCP** | CHG_MODE[2:0] = 010, $I_{QSW}$ > $I_{CONV_OCP}$ with 100ns blanking | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **VDRP_OVP** | CHG_MODE[2:0] <> 000, ($V_{VAC}$ - $V_{VBUS}$) > $V_{DRP_OVP}$ with $t_{VDRP_OVP_DEG}$ deglitch | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **PMID2OUT_OVP** | CHG_MODE[2:0] <> 000, $V_{PMID}$/2 - $V_{VOUT}$ (SC) or $V_{PMID}$ - $V_{VOUT}$ (BP), I²C programmable, 400mV by default | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **PMID2OUT_UVP** | CHG_MODE[2:0] <> 000, $V_{PMID}$/2 - $V_{VOUT}$ (SC) or $V_{PMID}$ - $V_{VOUT}$ (BP), I²C programmable, -100mV by default | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **REG_TIMEOUT** | CHG_MODE[2:0] <> 000 | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |
| **TDIE_OTP** | CHG_MODE[2:0] <> 000 or ADC_EN = 1<br>$T_{DIE}$ > $T_{DIEOTP_ALM_R}$ | Reset CHG_MODE[2:0] = 000 and turn off $Q_{RB}$ |

# DETAILED DESCRIPTION (continued)

## VAC Over-Voltage Protection (VAC_OVP)

The SGM41600S monitors the adapter voltage on the VAC pin to control the external OVPFET using OVPGATE output. The VAC over-voltage protection circuit is powered by VAC and is enabled if $V_{VAC}$ rises above $V_{AC_PRESENT_R}$. If $V_{VAC}$ is above $V_{VAC_PRESENT_R}$ for at least $t_{VAC_IN_DEG}$ (5ms) and $t_{PDN_VBUS_IN}$ (15ms) time, a 4.8V gate voltage is sent to the OVPGATE output to turn on the external OVPFET. If the $V_{VAC}$ reaches the $V_{AC_OVP}$ threshold, the gate voltage starts to drop and eventually the OVPFET is fully turned off. Figure 8 shows the VAC_OVP and OVPGATE operation timings. The $V_{AC_OVP}$ threshold can be set by I²C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VAC pin and the external OVPFET.

## Input Short-Circuit Protection (VBUS_SC)

The VBUS_SC function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFET is turned on or if $V_{VBUS}$ rises above $V_{BUS_PRESENT_R}$. If the $V_{VBUS}$ falls below 2.7V, the OVPFET is turned off, and charging is stopped. CHG_MODE[2:0] bits are reset to 000 (disable). Also, BUS_ABSENT_FLAG bit is set to 1, and an INT pulse is asserted. The device will wait for 512ms before automatically re-enabling and initiating startup sequence.

During charging, if $V_{VBUS}$ is less than 1.9 × $V_{VOUT}$ in divider mode or 0.95 × $V_{VOUT}$ in bypass mode, the $Q_{RB}$ and OVPFET are turned off, and charging is stopped. CHG_MODE[2:0] bits are reset to 000 (disable). Also, VBUS_ABSENT_FLAG bit is set to 1, and an INT pulse is asserted.

## VBUS Charge Voltage Range (VBUS_LO & VBUS_HI)

The VBUS_LO and VBUS_HI functions are included to avoid problems due to wrong VBUS setting for charging. If $V_{VBUS}$ is less than ($V_{VOUT}$ × $V_{BUS_LO}$ × 2) or above ($V_{VOUT}$ × $V_{BUS_HI}$ × 2), the device remains in charge initiation operation if the voltage divider mode is selected. If the bypass mode is selected, the range is from ($V_{VOUT}$ × $V_{BUS_LO}$) to ($V_{VOUT}$ × $V_{BUS_HI}$). Charging will start once $V_{VBUS}$ is within the charge range. VBUS_LO and VBUS_HI functions are kept enabled after soft-start timer timeout. The VBUS_LO and VBUS_HI thresholds can be set by I²C serial interface.

## Input, OUTPUT and Battery Over-Voltage Protection (VBUS_OVP, VOUT_OVP and VBAT_OVP)

The VBUS_OVP, VOUT_OVP and VBAT_OVP functions detect input and output charge voltage conditions. If either input or output voltage is higher than the protection threshold, the charger is turned off and CHG_MODE[2:0] bits are reset to 000 (disable). The VBUS_OVP function monitors VBUS pin voltage. The VOUT_OVP function monitors VOUT pin voltage. The VBAT_OVP uses BATP and BATN/SRP remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, a series 100Ω resistor on the BATP pin is required. The VBUS_OVP, VOUT_OVP and VBAT_OVP thresholds can be set by I²C serial interface.

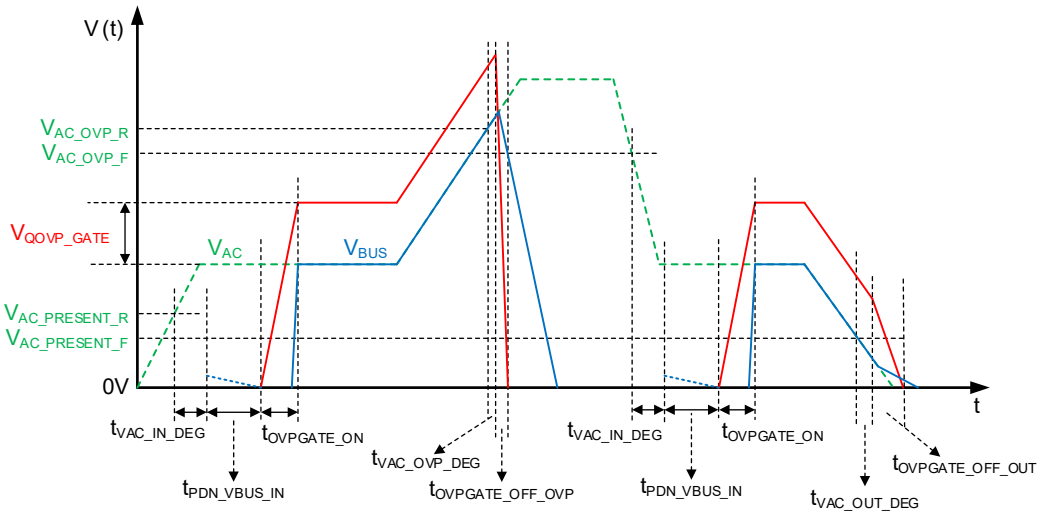



**Figure 8. OVPGATE Operation Timing**

# DETAILED DESCRIPTION (continued)

## Input and Battery Over-Current Protection (IBUS_OCP and IBAT_OCP)

The IBUS_OCP function monitors the input current via $Q_{RB}$. If CHG_MODE[2:0] bits are set to enable charge, the $Q_{RB}$ is turned on and the IBUS_OCP function starts detecting the input current. If the $I_{BUS}$ reaches $I_{BUS_OCP}$ threshold, the device stops charging and resets CHG_MODE[2:0] bits to 000 (disable). The battery current is monitored by the voltage across an external series shunt resistor. This differential voltage is measured between BATN/SRP and SRN pins. If $I_{BAT_OCP}$ threshold is reached, the device stops charging and resets CHG_MODE[2:0] bits to 000 (disable). The IBUS_OCP and IBAT_OCP thresholds can be set by I²C serial interface.

## Input Under-Current Protection (IBUS_UCP)

The IBUS_UCP function detects the input current via $Q_{RB}$ during forward charging. After charging is started, the $t_{IBUS_UCP_BLK}$ timer is enabled and $I_{BUS}$ current is compared with $I_{BUS_UCP_R}$. If $I_{BUS}$ cannot exceed $I_{BUS_UCP_R}$ within $t_{IBUS_UCP_BLK}$, the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). If $I_{BUS}$ exceeds $I_{BUS_UCP_R}$ within $t_{IBUS_UCP_BLK}$, from then on, if $I_{BUS}$ falls below the $I_{BUS_UCP_F}$ threshold, the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The $t_{IBUS_UCP_BLK}$ timer can be set by I²C serial interface.

## VOUT Short-Circuit Protection (VOUT_SC)

The VOUT_SC function monitors the VOUT pin for short-circuit. This function is enabled during charging. If $V_{VOUT}$ falls below 2.7V when the voltage divider mode is selected, the charger is turned off and CHG_MODE[2:0] bits are reset to 000 (disable). Also, the PIN_DIAG_FLAG bit is set to 1, and an INT pulse is generated.

## CFLY Short-Circuit Protection (CFLY_SC)

The CFLY_SC function identifies the health of flying capacitors before and during voltage divider switching (charging). The device initialization process is started after CHG_MODE[2:0] bits are set to 010. When $V_{VBUS}$ is in the charge range, the flying capacitors ($C_{FLY}$) in both channels are pre-charged. A CFLY short-circuit is detected if they cannot be charged, and the voltage between $V_{CFHx}$ and $V_{CFLx}$ remains below ($V_{VOUT}$ - 1.2V). If so, the initialization process is stopped and CHG_MODE[2:0] bits are reset to 000 (disable). Even if $C_{FLY}$ capacitors pass the short-circuit test in the initialization process, the CFLY_SC function remains active and whenever a $V_{CFLY}$ voltage falls below ($V_{VOUT}$ - 1.2V), the charger is turned off and CHG_MODE[2:0] bits are reset to 000 (disable). The PIN_DIAG_FLAG bit is set to 1 and an INT pulse is generated as well. During a CFLY_SC event, other protection events such as IBUS_OCP, VBAT_OVP or PEAK_OCP may occur.

A CFLY discharge circuit is activated before the internal RBFET ($Q_{RB}$) is turned on if $V_{VBUS} > V_{BUS_PRESENT_R}$ to prevent over-current stress at the start of charging.

## Converter Peak Over-Current Protection (PEAK_OCP)

The PEAK_OCP function monitors the converter switch operating currents. If the $Q_{CHx}$ and $Q_{DLx}$ current reach switch OCP threshold during charging, the PEAK_OCP_FWD_FLAG bit is set to 1 and an INT pulse is generated, the charging is stopped and CHG_MODE[2:0] bits are reset to 000 (disable).

## Regulation Feature

The SGM41600S has VBAT_REG and IBAT_REG regulation functions to regulate the battery voltage and current for a short period before the system can re-adjust the conditions such that these functions can be disabled. The regulation thresholds can be set by I²C serial interface.

The VBAT_REG function monitors the differential voltage between BATP and BATN/SRP pins and if the battery voltage is above the $V_{BAT_REG}$ threshold, the OVPGATE voltage is controlled to regulate the battery voltage.

The VBAT_REG_FLAG bit is also set to 1, and an INT pulse is generated. Then the host can negotiate with the adapter to reduce the current. This will gradually reduce the current until the bus current falls to the $I_{BUS_UCP_F}$ and charging will end.

Similarly, the IBAT_REG function monitors the differential voltage between BATN/SRP and SRN pins to find the battery current and if the $I_{BAT_REG}$ threshold is exceeded, the OVPGATE voltage is controlled (reduced) to regulate the charge current.

If one of the regulation functions is triggered and persist for 650ms when REG_TIMEOUT_DIS bit is set to 0, the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The system should adjust the charging conditions to prevent the battery voltage and current regulation for more than 650ms (or prevent triggering of the VDRP_OVP).

# DETAILED DESCRIPTION (continued)

## Dropout Over-Voltage Protection (VDRP_OVP)

When VBAT_REG or IBAT_REG is active, a large voltage drop may appear on the external OVPFET and cause excessive power loss and heat. To avoid that, the VDRP_OVP function monitors the voltage drop between VAC and VBUS pins. If it is higher than $V_{DRP_OVP}$ threshold with $t_{DRP_OVP_DEG}$ deglitch time (set by VDRP_OVP_DEG bit in REG0x05), the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The $V_{DRP_OVP}$ threshold and $t_{DRP_OVP_DEG}$ deglitch time can be programmed by $I^2C$ serial interface.

## TDIE Over-Temperature Protection (TDIE_OTP)

The TDIE_OTP function prevents charging in over-temperature condition. The die temperature is monitored and if the +150℃ threshold is reached, the charging is stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The startup sequence cannot be initiated again until the die temperature falls down to +130℃.

# APPLICATION INFORMATION

## Input Capacitors ($C_{VAC}$, $C_{VBUS}$ and $C_{PMID}$)

Input capacitors are selected by considering two main factors:
1. Adequate voltage margin above maximum surge voltage;
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For $C_{VAC}$, use at least a 1μF low ESR bypass ceramic capacitor placed close to the VAC and PGND pins. The $C_{VBUS}$ and $C_{PMID}$ are determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, 10μF or larger X5R ceramic capacitors are sufficient for $C_{VBUS}$ and $C_{PMID}$. Consider the DC bias derating of the ceramic capacitors. The X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

## External OVPFET ($Q_{OVP}$)

The maximum recommended $V_{VBUS}$ input range is 11.5V. If the supplied VAC voltage is above 11.5V, or if regulation functions are needed during load or wall adapter transients, an external OVPFET is recommended between the USB connector and the SGM41600S. Choose a low $R_{DSON}$ MOSFET for the OVPFET to minimize power losses.

## Flying Capacitors ($C_{FLY}$)

For selection of the $C_{FLY}$ capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The $C_{FLY}$ capacitors are biased to half of the input voltage. To trade-off between efficiency and power density, set the $C_{FLY}$ voltage ripple to the 2% of the $V_{VOUT}$ as a good starting point. The $C_{FLY}$ for each channel can be calculated by Equation 8:

$$C_{FLY} = \frac{I_{BAT}}{4f_{SW}V_{CFLY_RPP}} = \frac{I_{BAT}}{8\%f_{SW}V_{VOUT}} \quad (8)$$

where $I_{BAT}$ is the charging current and $V_{CFLY_RPP}$ is the peak-to-peak voltage ripple of the $C_{FLY}$.

Choosing a too small capacitor for $C_{FLY}$ results in lower efficiency and high output voltage/current ripples. However, choosing a too large $C_{FLY}$ only provides minor efficiency and output ripple improvements.

The default switching frequency is $f_{SW}$ = 500kHz. It can be adjusted by FSW_SET[2:0] bits in REG0x01. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance ($R_{EFF}$). An optimum switching frequency can be found for any selected $C_{FLY}$ capacitor to minimize losses.

## Output Capacitor ($C_{VOUT}$)

$C_{VOUT}$ selection criteria are similar to the $C_{FLY}$ capacitor. Larger $C_{VOUT}$ value results in less output voltage ripple, but due to the dual-channel operation, the $C_{VOUT}$ RMS current is much smaller than $C_{FLY}$, so smaller capacitance value can be chosen for $C_{VOUT}$ as given in Equation 9:

$$C_{VOUT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{VOUT_RPP}} \quad (9)$$

where $t_{DEAD}$ is the dead time between the two channels and $V_{VOUT_RPP}$ is the peak-to-peak output voltage ripple and is typically set to the 2% of $V_{OUT}$.

$C_{VOUT}$ is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically two 10μF, X5R or better grade ceramic capacitors placed close to the VOUT and PGND pins provide stable performance.

## External Bootstrap Capacitor ($C_{BST}$)

The bootstrap capacitors provide the gate driver supply voltage for the internal high-side switches ($Q_{CH1}$ and $Q_{CH2}$). Place a 100nF low ESR ceramic capacitor between BST1 and CFH1 pins and another one between BST2 and CFH2 pins.

## PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41600S. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VBUS, PMID and VOUT pins to PGND with ceramic capacitors as close to the device pins as possible.
5. Place $C_{FLY}$ capacitors as close as possible to the device with small pad areas to reduce switching noise and EMI.
6. Connect or reference all quiet signals to the AGND pin.
7. Connect and reference all power signals to the PGND pins (preferably the nearest ones).
8. Try not to interrupt or break the power planes by signal traces.

## TYPICAL APPLICATION CIRCUIT

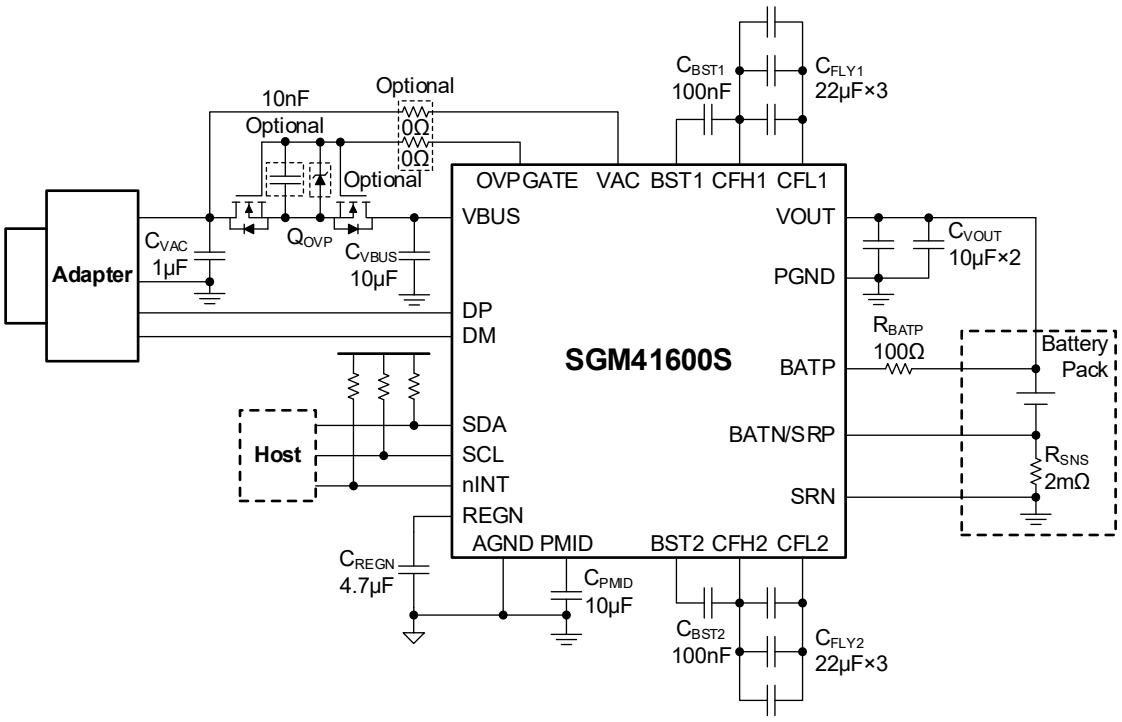



**Figure 9. Typical Application Circuit**

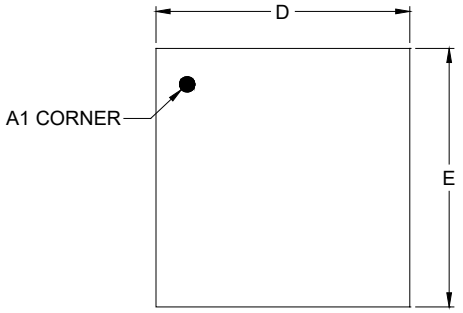
## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

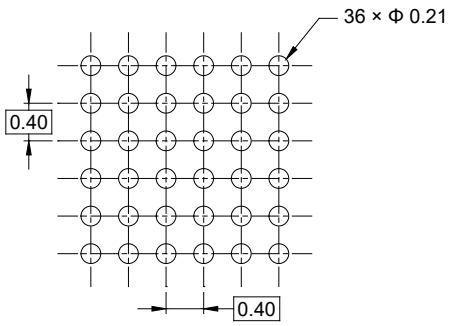
| Changes from Original (NOVEMBER 2024) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

# PACKAGE OUTLINE DIMENSIONS

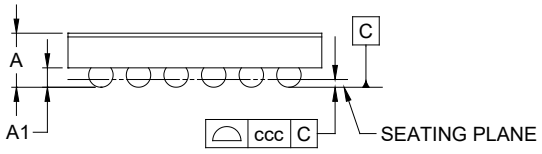
## WLCSP-2.7×2.75-36B



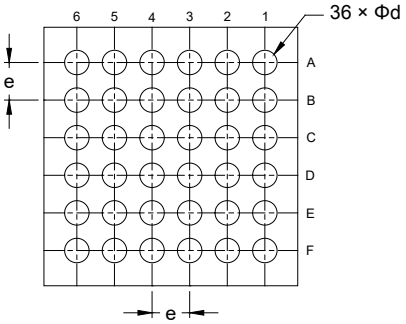

TOP VIEW




RECOMMENDED LAND PATTERN (Unit: mm)




SIDE VIEW



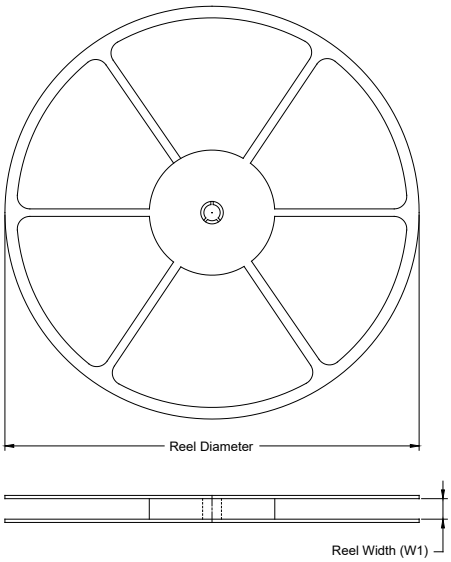

BOTTOM VIEW

| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 0.613 |
| A1 | 0.186 | - | 0.226 |
| D | 2.670 | - | 2.730 |
| E | 2.720 | - | 2.780 |
| d | 0.230 | - | 0.290 |
| e | 0.400 BSC | | |
| ccc | 0.050 | | |

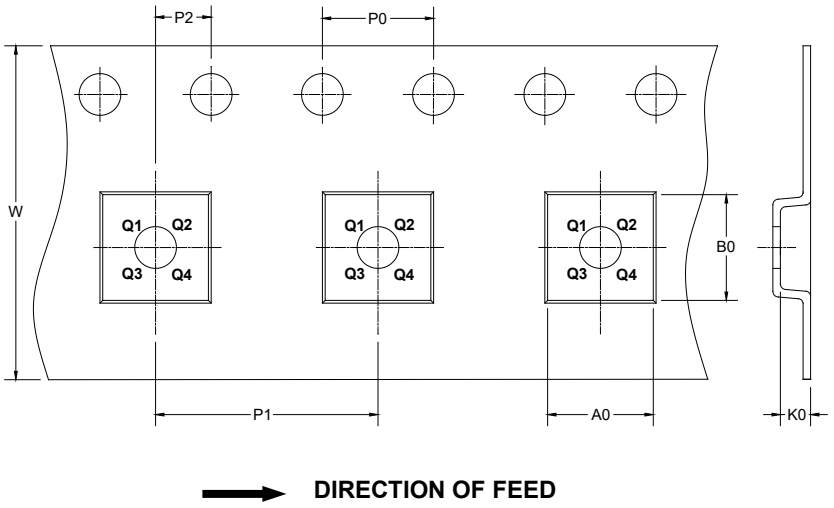
NOTE: This drawing is subject to change without notice.

# TAPE AND REEL INFORMATION

## REEL DIMENSIONS




## TAPE DIMENSIONS



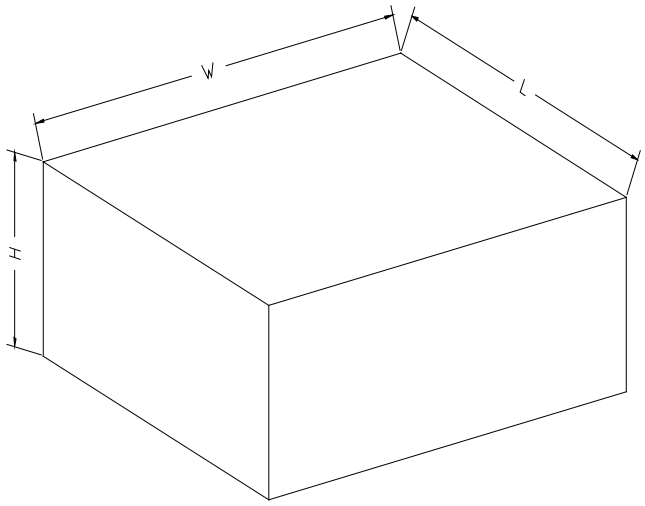

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP-2.7×2.75-36B | 13" | 12.4 | 2.98 | 2.98 | 0.78 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002