SGM71612R81/SGM71612R82/SGM71612R83
8 Channels, 16-Bit, SPI Interface, Voltage-Output DAC with 10ppm/℃ On-Chip Reference

GENERAL DESCRIPTION

The SGM71612R81/SGM71612R82/SGM71612R83 family is a 16-bit, 8 channels, voltage-output digital-to-analog converter (DAC). These chips are guaranteed monotonic by design.

The SGM71612R81Z has an on-chip 1.25V 10ppm/℃ reference, giving a full-scale output range of 2.5V. The SGM71612R82Z/SGM71612R82M/SGM71612R83M have an on-chip 2.5V 10ppm/℃ reference, giving a full-scale output range of 5V.

The chips have a power-on control circuit, which can ensure that DAC has a fixed output when the system is powered on. The SGM71612R81Z and SGM71612R82Z output 0V when the system is powered up, and the SGM71612R82M/SGM71612R83M outputs mid-scale when the system is powered up.

The chips have an nLDAC pin that allows the DAC to update the output simultaneously. And the chips have an nCLR pin that allows the DAC to be updated to a configurable state, zero-code, mid-scale, or full-scale.

The SGM71612R81/SGM71612R82/SGM71612R83 family uses a 3-wire SPI-compatible interface, and its operation data rate is up to 50MHz.

The SGM71612R81Z and SGM71612R82Z are available in Green TSSOP-16, TQFN-4×4-16BL and FOCSP-2.6×2.6-16B packages. The SGM71612R82M and SGM71612R83M are available in Green TSSOP-16 and TQFN-4×4-16BL packages.

FEATURES

- **Power Supply Range: 2.7V to 5.5V**
- **On-Chip 1.25V/2.5V, 10ppm/℃ Reference**
  - **SGM71612R81Z: 1.25V**
  - **SGM71612R82Z/SGM71612R82M/SGM71612R83M: 2.5V**
- **Power Down to 500nA (TYP) at 5V, 300nA (TYP) at 3V**
- **Monotonicity Guaranteed by Design**
- **Power-On Reset to Zero-Scale or Mid-Scale**
  - **SGM71612R81Z/SGM71612R82Z: Power-On Reset to Zero**
  - **SGM71612R82M/SGM71612R83M: Power-On Reset to Mid-Scale**
- **3 Power-Down Modes**
- **Hardware nLDAC and nLDAC Override Function**
- **nCLR Function to Programmable Code**
- **Rail-to-Rail Buffered Voltage-Output Operation**
- **Available in Green TSSOP-16, TQFN-4×4-16BL and FOCSP-2.6×2.6-16B Packages**

APPLICATIONS

Process Control and DCS Systems
Data Acquisition Systems
Lab Instrumentations

PACKAGE/ORDERING INFORMATION

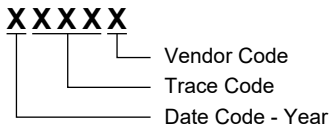
MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM71612R81Z	TSSOP-16	-40℃ to +125℃	SGM71612R81ZXTS16G/TR	SGM01N XTS16 XXXXX	Tape and Reel, 4000
			SGM71612R81ZXTS16SG/TR	SGM01N XTS16 XXXXX	Tape and Reel, 250
	TQFN-4×4-16BL	-40℃ to +125℃	SGM71612R81ZXTSG16G/TR	SGM01O XTSG16 XXXXX	Tape and Reel, 3000
			SGM71612R81ZXTSG16SG/TR	SGM01O XTSG16 XXXXX	Tape and Reel, 250
	FOCSP-2.6×2.6-16B	-40℃ to +125℃	SGM71612R81ZXG/TR	SGM 71612R81Z XXXXX XX#XX	Tape and Reel, 5000
			SGM71612R81ZXSG/TR	SGM 71612R81Z XXXXX XX#XX	Tape and Reel, 250
SGM71612R82Z	TSSOP-16	-40℃ to +125℃	SGM71612R82ZXTS16G/TR	SGM0DC XTS16 XXXXX	Tape and Reel, 4000
			SGM71612R82ZXTS16SG/TR	SGM0DC XTS16 XXXXX	Tape and Reel, 250
	TQFN-4×4-16BL	-40℃ to +125℃	SGM71612R82ZXTSG16G/TR	SGM0DD XTSG16 XXXXX	Tape and Reel, 3000
			SGM71612R82ZXTSG16SG/TR	SGM0DD XTSG16 XXXXX	Tape and Reel, 250
	FOCSP-2.6×2.6-16B	-40℃ to +125℃	SGM71612R82ZXG/TR	SGM 71612R82Z XXXXX XX#XX	Tape and Reel, 5000
			SGM71612R82ZXSG/TR	SGM 71612R82Z XXXXX XX#XX	Tape and Reel, 250
SGM71612R82M	TSSOP-16	-40℃ to +125℃	SGM71612R82MXTS16G/TR	SGM0EJ XTS16 XXXXX	Tape and Reel, 4000
			SGM71612R82MXTS16SG/TR	SGM0EJ XTS16 XXXXX	Tape and Reel, 250
	TQFN-4×4-16BL	-40℃ to +125℃	SGM71612R82MXTSG16G/TR	SGM0EK XTSG16 XXXXX	Tape and Reel, 3000
			SGM71612R82MXTSG16SG/TR	SGM0EK XTSG16 XXXXX	Tape and Reel, 250

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM71612R83M	TSSOP-16	-40℃ to +125℃	SGM71612R83MXTS16G/TR	SGM0M4 XTS16 XXXXX	Tape and Reel, 4000
			SGM71612R83MXTS16SG/TR	SGM0M4 XTS16 XXXXX	Tape and Reel, 250
	TQFN-4×4-16BL	-40℃ to +125℃	SGM71612R83MXTSG16G/TR	SGM0M5 XTSG16 XXXXX	Tape and Reel, 3000
			SGM71612R83MXTSG16SG/TR	SGM0M5 XTSG16 XXXXX	Tape and Reel, 250

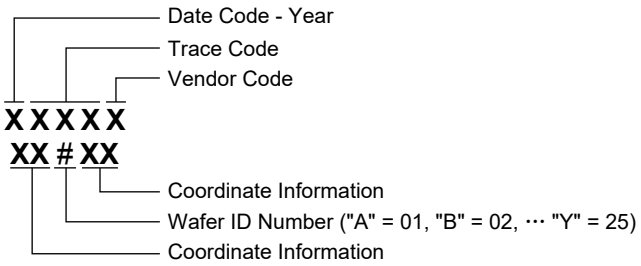
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

TSSOP-16/TQFN-4×4-16BL



FOCSP-2.6×2.6-16B



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range ..... -0.3V to 6V
Digital Input Voltage Range ..... -0.3V to V_{CC} + 0.3V
Output Voltage Range ..... -0.3V to V_{CC} + 0.3V
V_{REFIN}/V_{REFOUT} to GND ..... -0.3V to V_{CC} + 0.3V
Package Thermal Resistance
TSSOP-16, θ_{JA} ..... 92℃/W
TQFN-4×4-16BL, θ_{JA} ..... 34℃/W
FOCSP-2.6×2.6-16B, θ_{JA} ..... 58℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

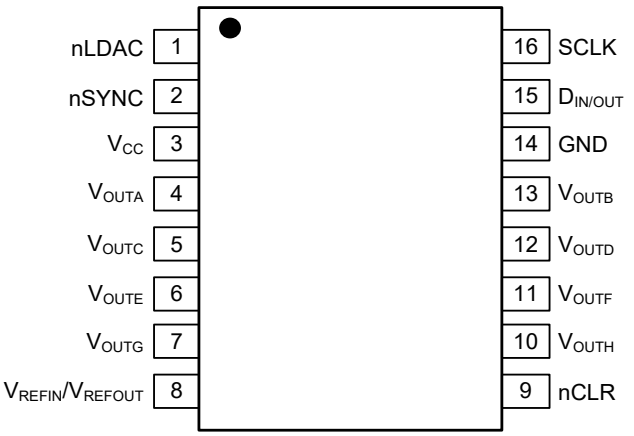
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

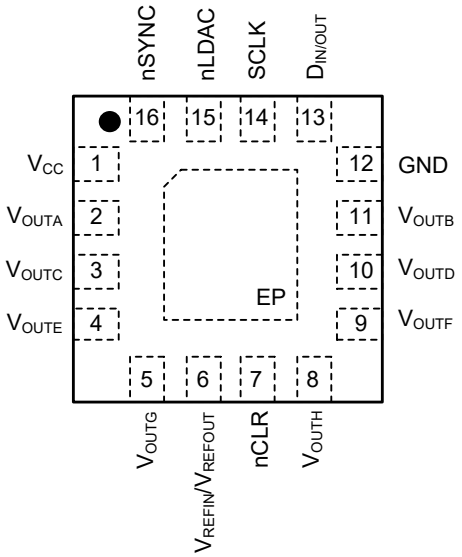
PIN CONFIGURATIONS

(TOP VIEW)



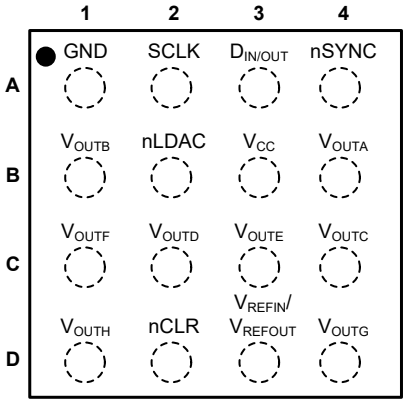
TSSOP-16

(TOP VIEW)



TQFN-4×4-16BL

(TOP VIEW)



FOCSP-2.6×2.6-16B

PIN DESCRIPTION

PIN			NAME	FUNCTION
TSSOP-16	TQFN-4×4-16BL	FOCSP-2.6×2.6-16B		
1	15	B2	nLDAC	Active low. Set this pin high and then set it low. On the falling edge of nLDAC, the DAC outputs are updated simultaneously. If the simultaneous update function of hardware is not used, this pin can be kept low.
2	16	A4	nSYNC	Frame Synchronization Input Pin. Active low. During 32-bit data shifting in, the pin must be kept low.
3	1	B3	V_{CC}	Power Supply Input.
4	2	B4	V_{OUTA}	Analog Output Voltage from DAC.
5	3	C4	V_{OUTC}	
6	4	C3	V_{OUTE}	
7	5	D4	V_{OUTG}	
8	6	D3	V_{REFIN}/ V_{REFOUT}	Analog Voltage Reference Input and Reference Output.
9	7	D2	nCLR	Active low. Set this pin high and then set it low. On the falling edge of nCLR, the DAC register is updated with the data contained in the clear code register. When nCLR is low, all nLDAC pulses are invalid.
10	8	D1	V_{OUTH}	Analog Output Voltage from DAC.
11	9	C1	V_{OUTF}	
12	10	C2	V_{OUTD}	
13	11	B1	V_{OUTB}	
14	12	A1	GND	Ground.
15	13	A3	$D_{IN/OUT}$	Serial Data Input/Output Pin.
16	14	A2	SCLK	Serial Clock Input Pin. Data is clocked on the falling edge of SCLK.
–	Exposed Pad	–	EP	Exposed Pad. This pad should be connected to GND.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{CC}, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Static Performance (1)							
Resolution				16			Bits
Relative Accuracy		INL			1.8	6	LSB
Differential Nonlinearity		DNL	Guaranteed monotonic by design			1	LSB
Zero-Code Error			All 0s loaded to DAC register		0.5	4	mV
Zero-Code Error Drift					5.5		μV/℃
Full-Scale Error			All 1s loaded to DAC register		0.1	0.4	% FSR
Gain Error						0.4	% FSR
Gain Temperature Coefficient			Of FSR/℃		1.5		ppm
Offset Error					0.7	5	mV
Power Supply Rejection Ratio		PSRR	V_{CC} ± 10%		-100		dB
DC Crosstalk	External Reference		Due to full-scale output change, R_L = 2kΩ to GND or V_{CC}		5		μV
			Due to load current change		18		μV/mA
			Due to powering down (per channel)		10		μV
	Internal Reference		Due to full-scale output change, R_L = 2kΩ to GND or V_{CC}		5		μV
			Due to load current change		40		μV/mA
Output Characteristics (2)							
Output Voltage Range				0		V_{CC}	V
Capacitive Load Stability			R_L = ∞		2		nF
			R_L = 2kΩ		10		
DC Output Impedance					0.15		Ω
Short-Circuit Current			V_{CC} = 5V		56		mA
Power-Up Time			Coming out of power-down mode, V_{CC} = 5V		15		μs
Reference Inputs							
Reference Current			V_{REF} = V_{CC} = 5.5V (per DAC channel)		25	37.5	μA
Reference Input Range				0		V_{CC}	V
Reference Input Impedance					28		kΩ
Reference Outputs							
Output Voltage			At ambient	2.495		2.505	V
Reference TC (2)					10	25	ppm/℃
Reference Output Impedance					0.3		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{CC}, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (2)							
Input Current		All digital inputs				1	μA
Input Low Voltage	V_{IL}	V_{CC} = 5V				0.8	V
Input High Voltage	V_{IH}	V_{CC} = 5V		2.0			V
Pin Capacitance					5		pF
Power Requirements							
Power Supply Range	V_{CC}	All digital inputs at 0 or V_{CC}, DAC active, excludes load current		4.5		5.5	V
Supply Current	I_{CC}	Normal mode (3)	V_{CC} = 4.5V to 5.5V, V_{IH} = V_{CC} and V_{IL} = GND, internal reference off		1	1.3	mA
			V_{CC} = 4.5V to 5.5V, V_{IH} = V_{CC} and V_{IL} = GND, internal reference on		1.4	1.9	
		All power-down modes (4)	V_{CC} = 4.5V to 5.5V, V_{IH} = V_{CC} and V_{IL} = GND		0.5	10	μA

NOTES:

1. Linearity calculated uses a reduced code range of SGM71612R81/SGM71612R82/SGM71612R83 family (code 512 to 65,024). Output unloaded.
2. Guaranteed by design. Not production tested.
3. Interface inactive. All DACs are active. DAC outputs unloaded.
4. All 8 DACs are powered down.

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 3.6V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{CC}, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Static Performance (1)							
Resolution				16			Bits
Relative Accuracy		INL			1.8	6	LSB
Differential Nonlinearity		DNL	Guaranteed monotonic by design			1	LSB
Zero-Code Error			All 0s loaded to DAC register		0.3	3	mV
Zero-Code Error Drift					1.2		μV/℃
Full-Scale Error			All 1s loaded to DAC register		0.1	0.4	% FSR
Gain Error						0.4	% FSR
Gain Temperature Coefficient			Of FSR/℃		3.3		ppm
Offset Error					0.7	3.5	mV
Power Supply Rejection Ratio (2)		PSRR	V_{CC} ± 10%		-90		dB
DC Crosstalk (2)	External Reference		Due to full-scale output change, R_L = 2kΩ to GND or V_{CC}		5		μV
			Due to load current change		18		μV/mA
			Due to powering down (per channel)		8		μV
	Internal Reference		Due to full-scale output change, R_L = 2kΩ to GND or V_{CC}		5		μV
			Due to load current change		40		μV/mA
Output Characteristics (2)							
Output Voltage Range				0		V_{CC}	V
Capacitive Load Stability			R_L = ∞		2		nF
			R_L = 2kΩ		10		
DC Output Impedance					0.15		Ω
Short-Circuit Current			V_{CC} = 3V		40		mA
Power-Up Time			Coming out of power-down mode, V_{CC} = 3V		15		μs
Reference Inputs							
Reference Current			V_{REF} = V_{CC} (per DAC channel)		12.5	25	μA
Reference Input Range				0		V_{CC}	V
Reference Input Impedance					28		kΩ
Reference Outputs							
Output Voltage			At ambient	1.245		1.255	V
Reference TC (2)					10	25	ppm/℃
Reference Output Impedance					0.3		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.7V to 3.6V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{CC}, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs (2)							
Input Current		All digital inputs				1	μA
Input Low Voltage	V_{IL}	V_{CC} = 3V				0.8	V
Input High Voltage	V_{IH}	V_{CC} = 3V		2.0			V
Pin Capacitance					5		pF
Power Requirements							
Power Supply Range	V_{CC}	All digital inputs at 0 or V_{CC}, DAC active, excludes load current		2.7		3.6	V
Supply Current	I_{CC}	Normal mode (3)	V_{CC} = 2.7 to 3.6V, V_{IH} = V_{CC} and V_{IL} = GND, internal reference off		0.8	1.3	mA
			V_{CC} = 2.7 to 3.6V, V_{IH} = V_{CC} and V_{IL} = GND, internal reference on		1.3	1.9	
		All power-down modes (4)	V_{CC} = 2.7 to 3.6V, V_{IH} = V_{CC} and V_{IL} = GND		0.3	10	μA

NOTES:
1. Linearity calculated uses a reduced code range of SGM71612R81/SGM71612R82/SGM71612R83 family (code 512 to 65,024). Output unloaded.
2. Guaranteed by design. Not production tested.
3. Interface inactive. All DACs are active. DAC outputs unloaded.
4. All 8 DACs are powered down.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, R_L = 2kΩ to GND, C_L = 200pF to GND, V_{REFIN} = V_{CC}, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Settling Time		¼ to ¾ scale settling to ±2LSB (16-bit resolution)			4		μs
Slew Rate					1		V/μs
Digital-to-Analog Glitch Impulse		1LSB (16-bit resolution) change around major carry			2.3		nV-s
		From code 0xEA00 to code 0xE9FF (16-bit resolution)			12		
Digital Feedthrough					0.05		nV-s
Digital Crosstalk					0.003		nV-s
Analog Crosstalk					2.4		nV-s
DAC-to-DAC Crosstalk					2.4		nV-s
Multiplying Bandwidth		V_{REF} = 2V ± 0.2V_{PP}			270		kHz
Total Harmonic Distortion	THD	V_{REF} = 2V ± 0.1V_{PP}, frequency = 10kHz			-80		dB
Output Noise Spectral Density		DAC code = 0x8400 (16-bit resolution)	1kHz		110		nV/√Hz
			10kHz		100		
Output Noise		0.1Hz to 10Hz, DAC code = 0x0000			2		μV_{PP}

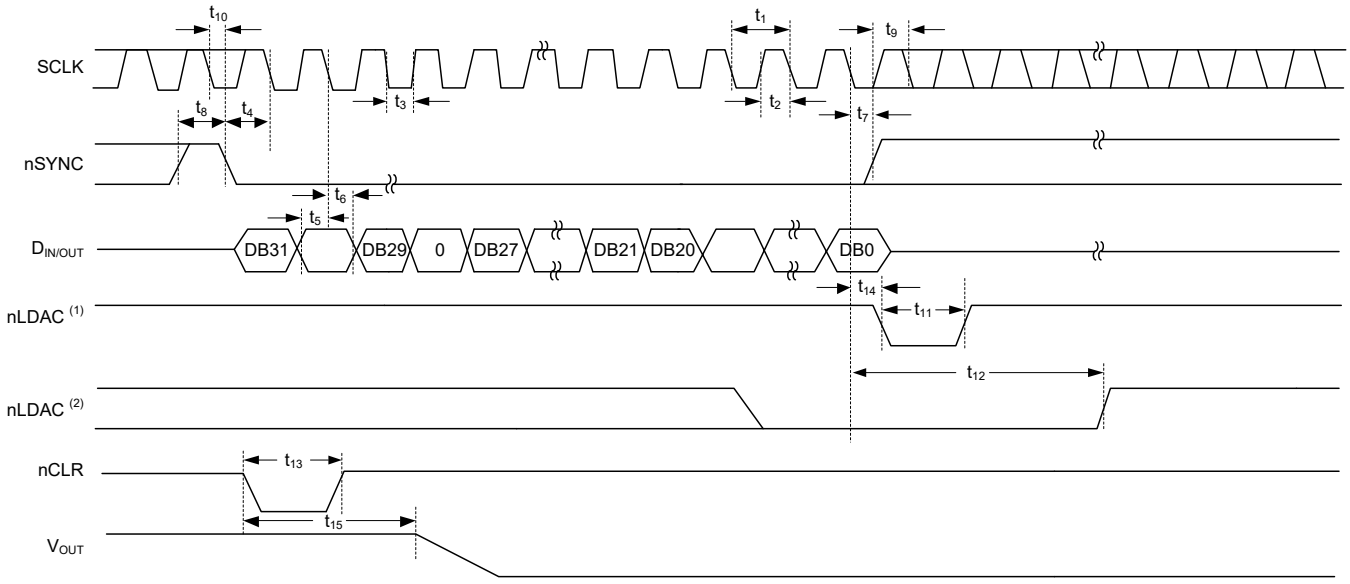
TIMING CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40℃ to +125℃. All input signals are specified with t_r = t_f = 1ns/V (10% to 90% of V_{CC}) and timed from a voltage level of (V_{IL} + V_{IH})/2, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Cycle Time	t_1 (2)		20			ns
SCLK High Time	t_2		8			ns
SCLK Low Time	t_3		8			ns
nSYNC to SCLK Falling Edge Setup Time	t_4		13			ns
Data Setup Time	t_5		4			ns
Data Hold Time	t_6		4			ns
SCLK Falling Edge to nSYNC Rising Edge	t_7		0			ns
Minimum nSYNC High Time	t_8		15			ns
nSYNC Rising Edge to SCLK Fall Ignore	t_9		13			ns
SCLK Falling Edge to nSYNC Fall Ignore	t_{10}		0			ns
nLDAC Pulse Width Low	t_{11}		10			ns
SCLK Falling Edge to nLDAC Rising Edge	t_{12}		15			ns
nCLR Pulse Width Low	t_{13}		5			ns
SCLK Falling Edge to nLDAC Falling Edge	t_{14}		0			ns
nCLR Pulse Activation Time	t_{15}		300			ns

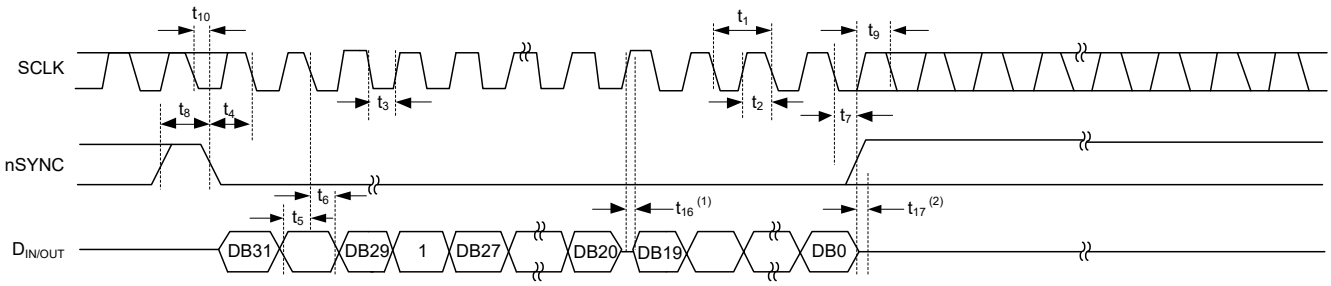
NOTES:
1. Refer to Figure 1 and Figure 2.
2. The SCLK frequency is 50MHz (MAX) at V_{CC} = 2.7V to 5.5V. Guaranteed by design, not production tested.

TIMING DIAGRAMS



NOTES:
1. Asynchronous load update mode. DAC is updated on the falling edge of nLDAC.
2. Synchronous load update mode. nLDAC can be tied low permanently.
3. Once 3-wire SPI read function is enabled, DB28 must be '0', otherwise DB28 will be ignored by DAC.

Figure 1. Serial Write Operation



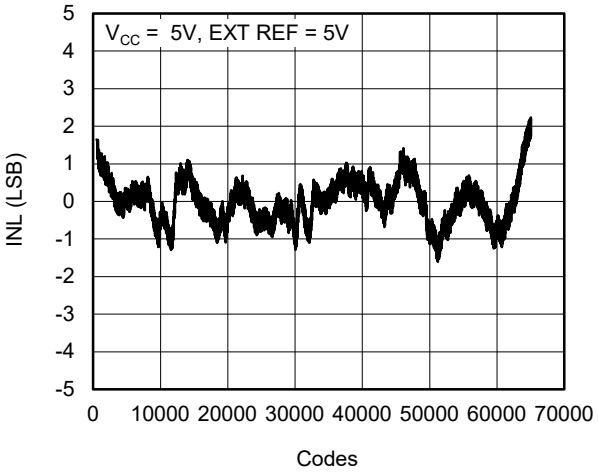
NOTES:
1. When DB28 = 1, this is a read operation, the data DB[19:0] is read from DAC. On the 12th rising edge of SCLK, the $D_{IN/OUT}$ switches from input to output, the data of internal register is put on the bus on each rising edge of SCLK.
2. On the rising edge of nSYNC, the $D_{IN/OUT}$ is turned off to HI-Z.
3. Before issuing a read sequence, it is necessary to enable read function by setting read enable control register firstly.

Figure 2. Serial Read Operation

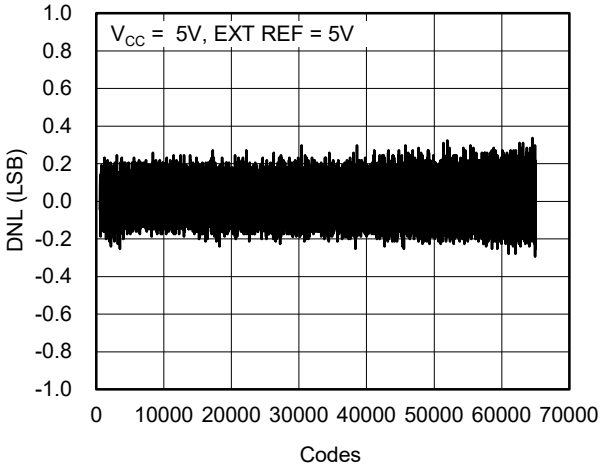
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, unless otherwise noted.

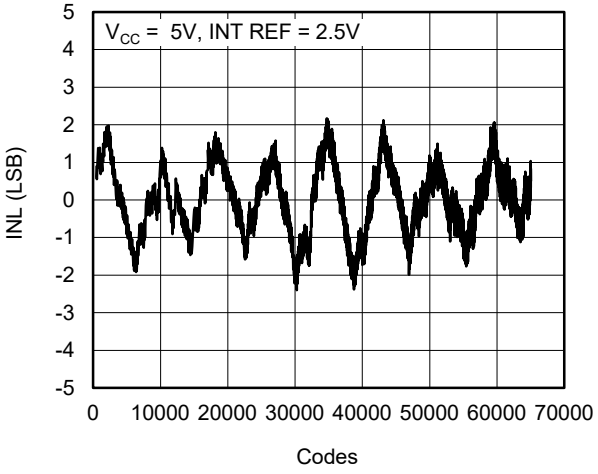
INL vs. Codes (External Reference)



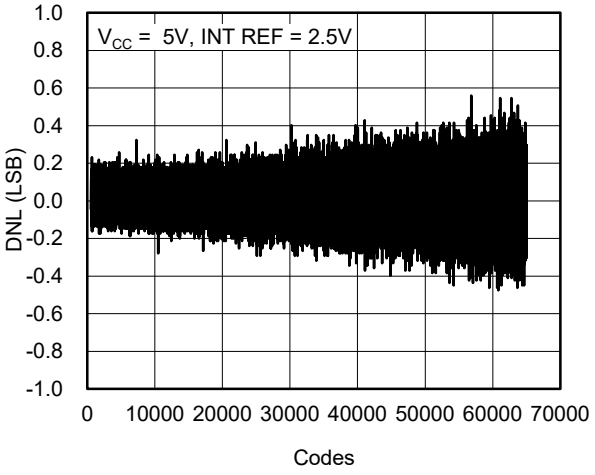
DNL vs. Codes (External Reference)



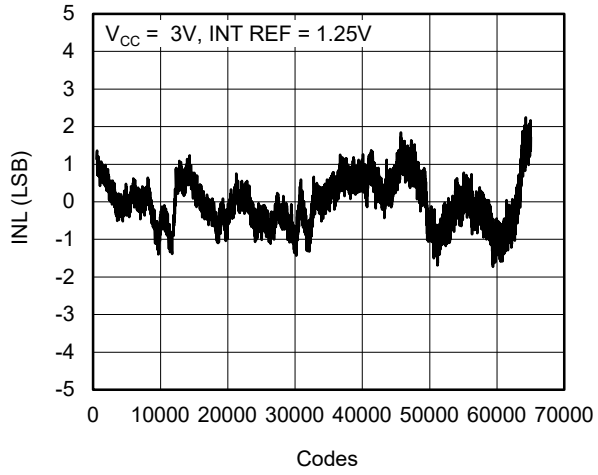
INL vs. Codes



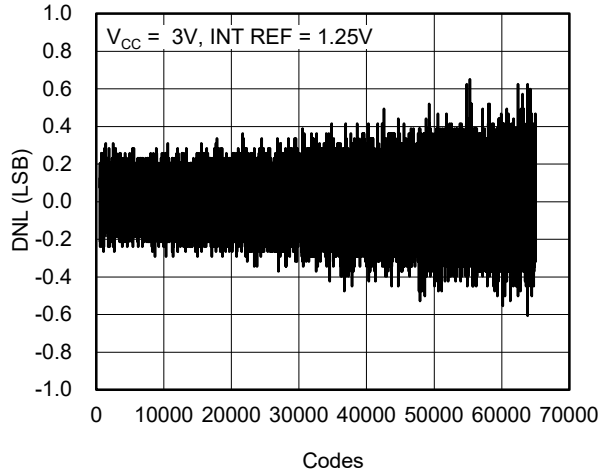
DNL vs. Codes



INL vs. Codes



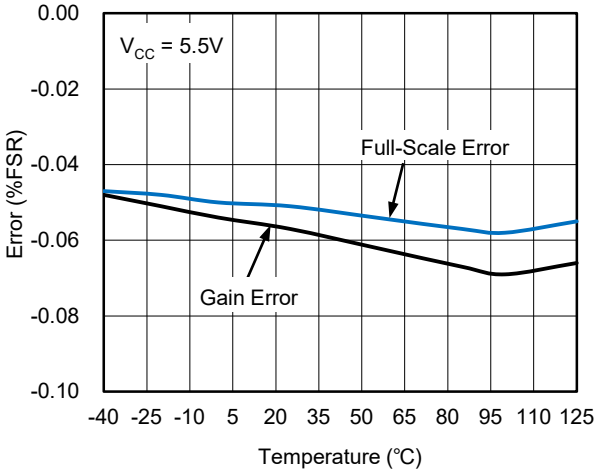
DNL vs. Codes



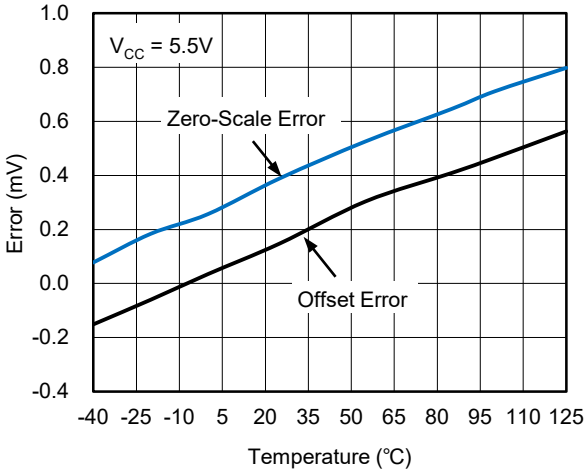
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

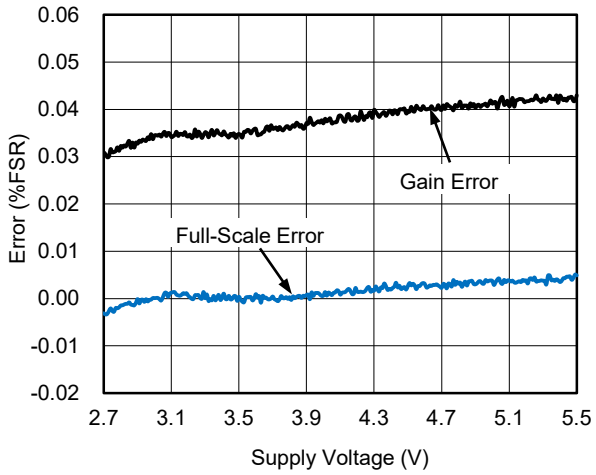
Gain Error and Full-Scale Error vs. Temperature



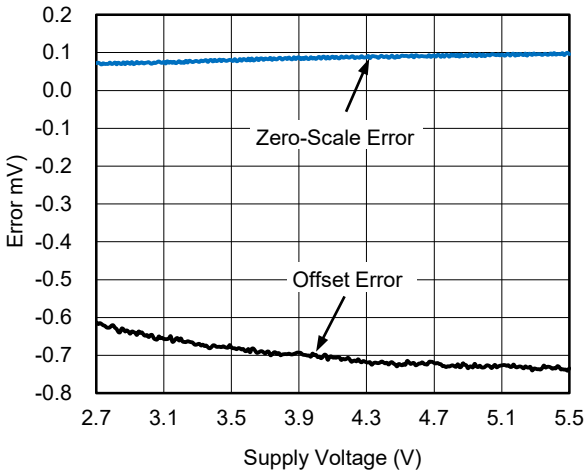
Offset Error and Zero-Scale Error vs. Temperature



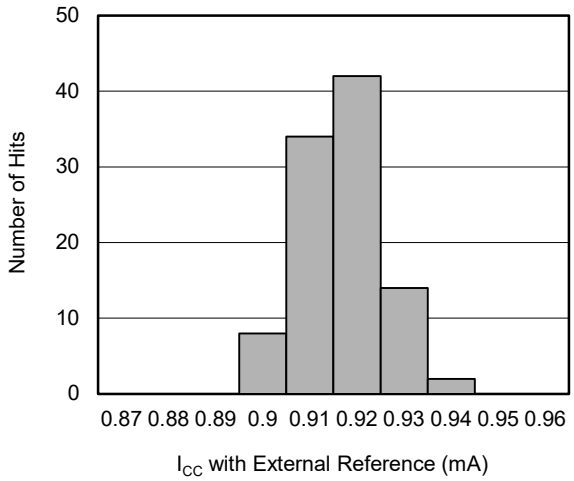
Gain Error and Full-Scale Error vs. Supply Voltage



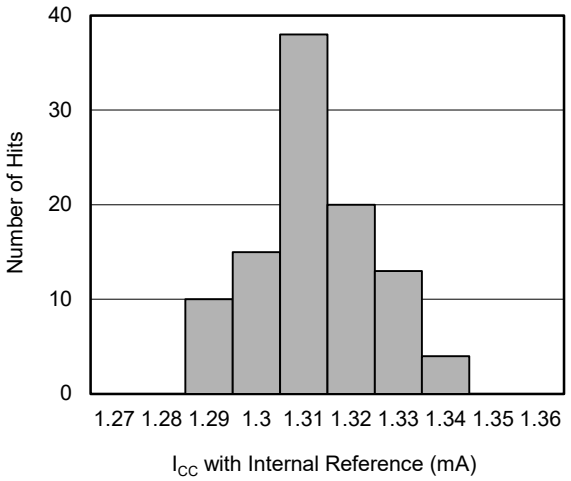
Offset Error and Zero-Scale Error vs. Supply Voltage



I_{CC} Histogram with External Reference



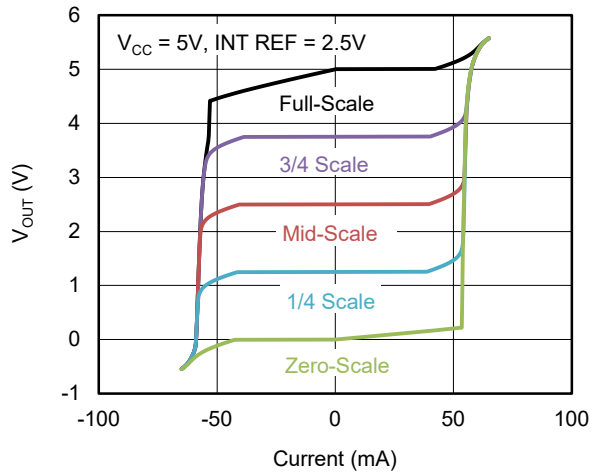
I_{CC} Histogram with Internal Reference



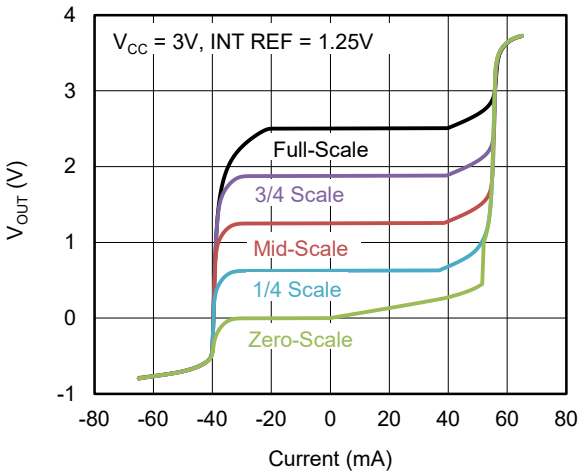
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

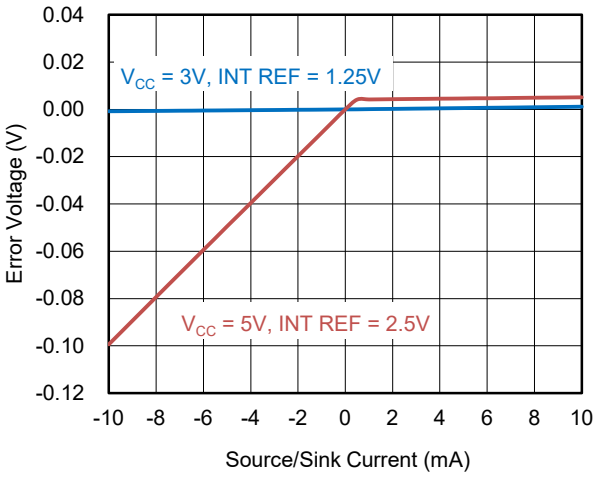
Source and Sink Capability



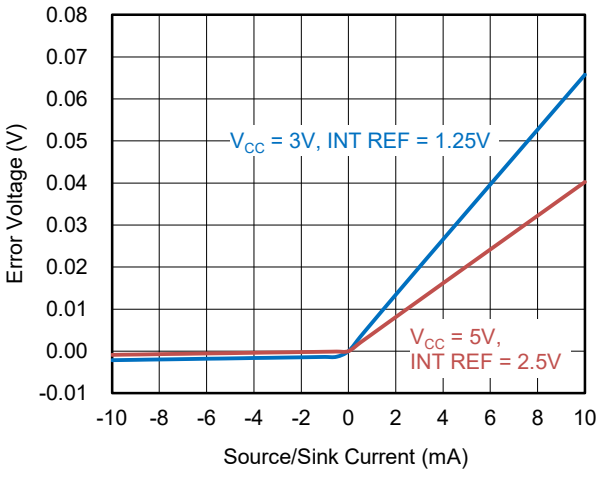
Source and Sink Capability



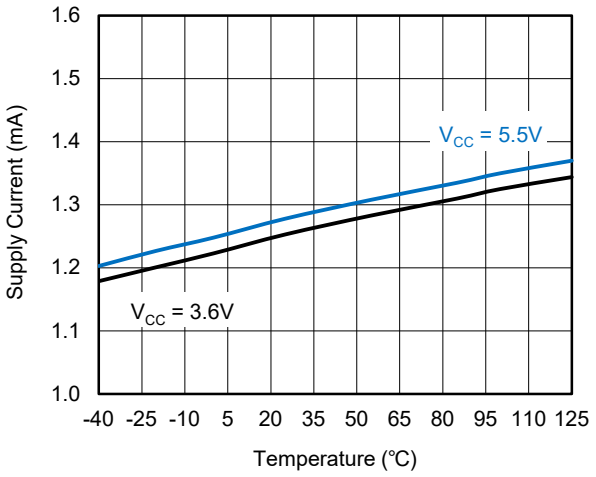
Headroom at Rails vs. Source and Sink



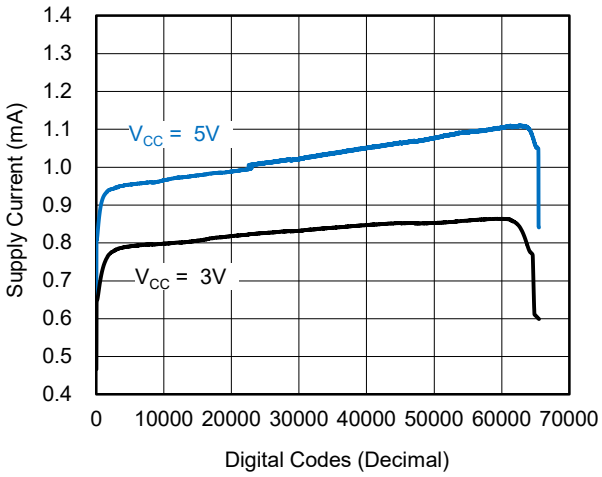
Headroom at Ground vs. Source and Sink



Supply Current vs. Temperature



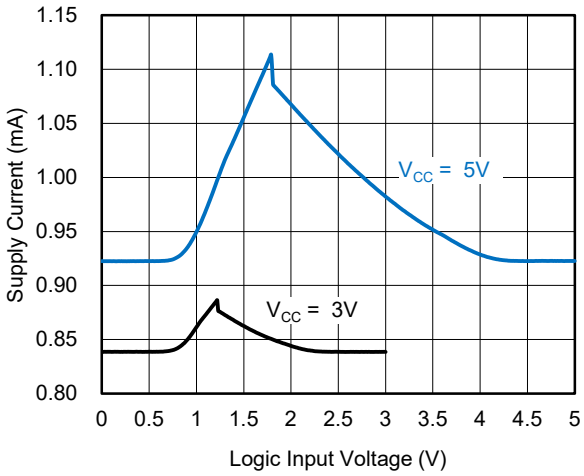
Supply Current vs. Digital Codes



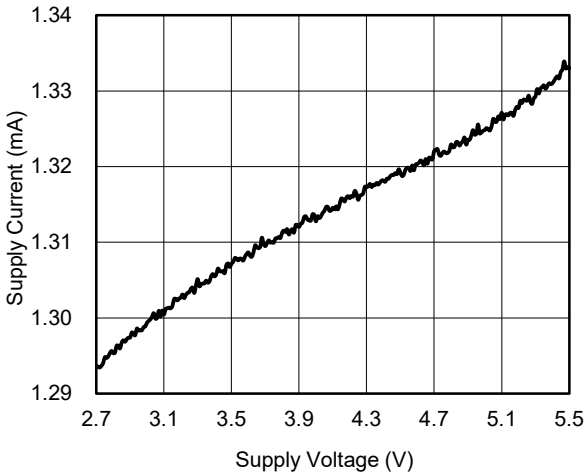
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

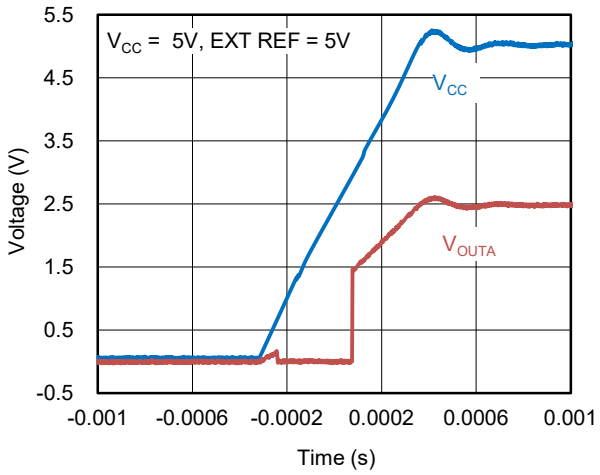
Supply Current vs. Logic Input Voltage



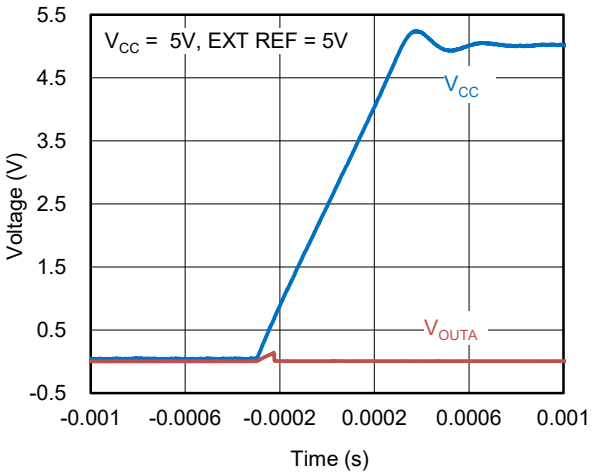
Supply Current vs. Supply Voltage



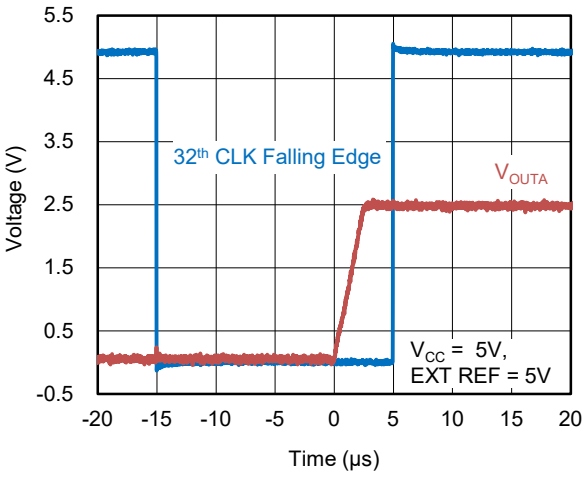
Power-On Reset to Mid-Scale



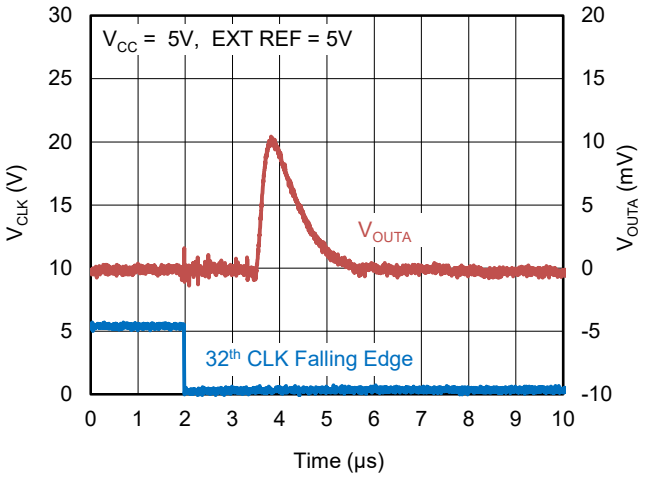
Power-On Reset to 0V



Exiting Power-Down to Mid-Scale



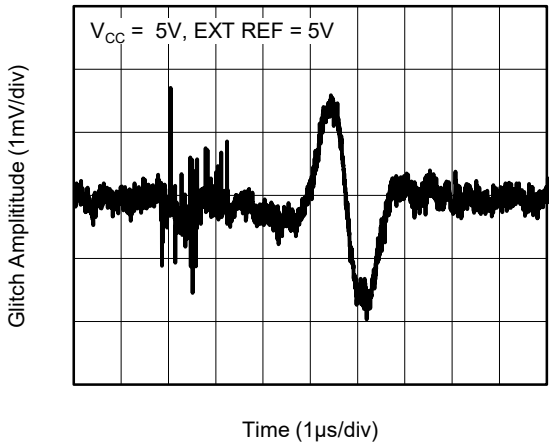
Digital-to-Analog Glitch Impulse (Negative)



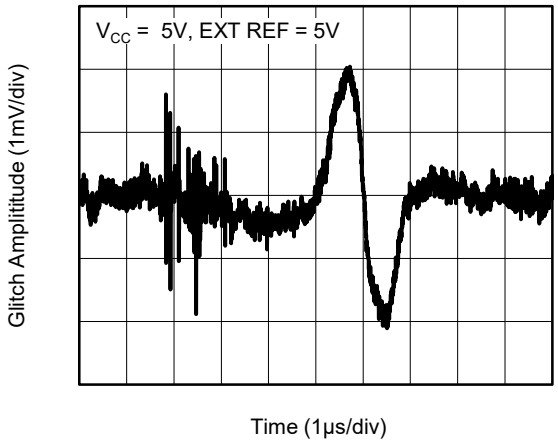
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

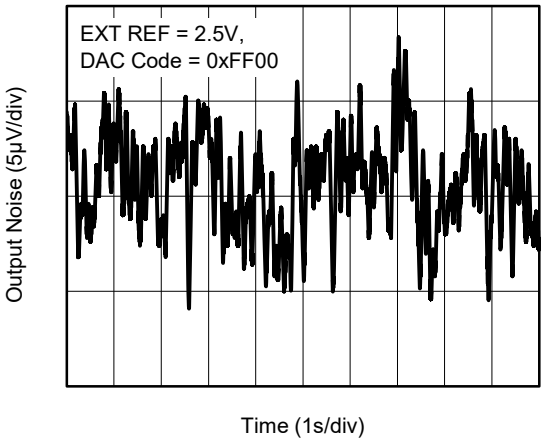
Analog Crosstalk



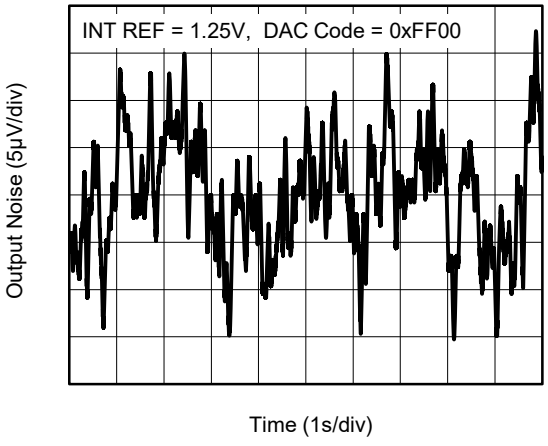
DAC-to-DAC Crosstalk



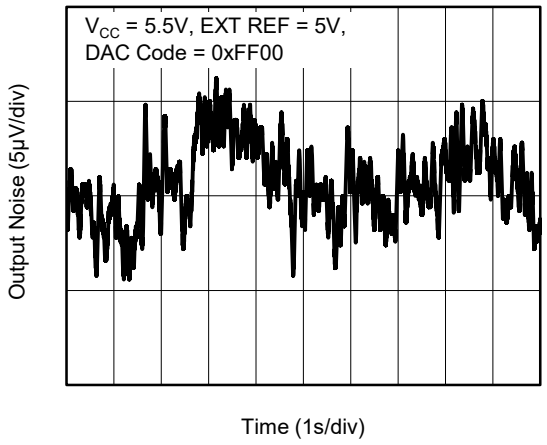
0.1Hz to 10Hz Output Noise Plot (External Reference)



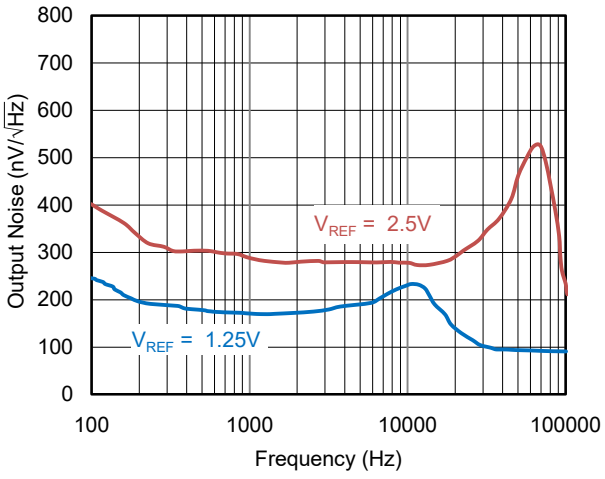
0.1Hz to 10Hz Output Noise Plot (Internal Reference)



0.1Hz to 10Hz Output Noise Plot (External Reference)



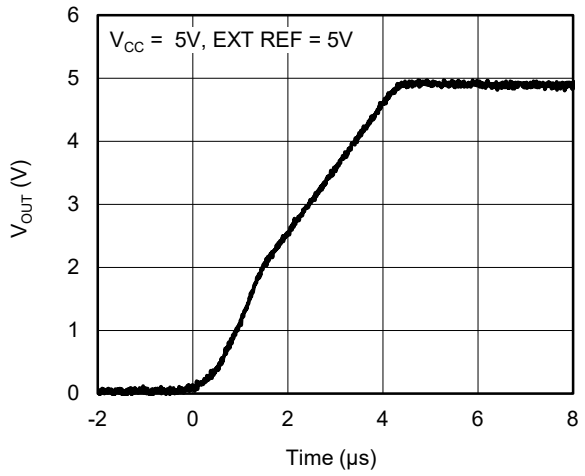
Noise Spectral Density (Internal Reference)



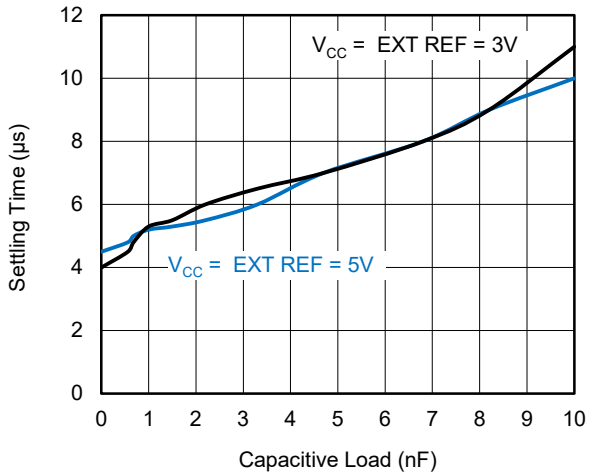
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

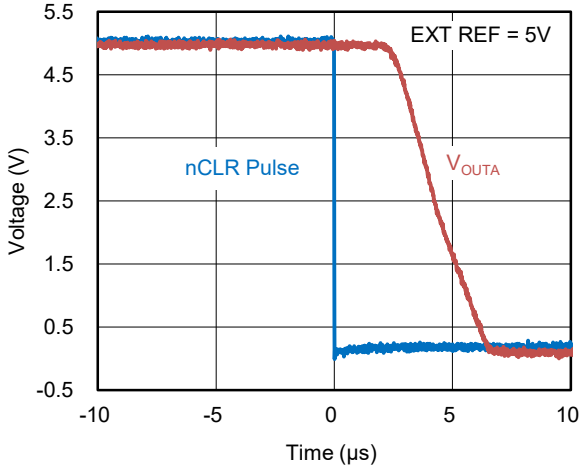
Full-Scale Settling Time



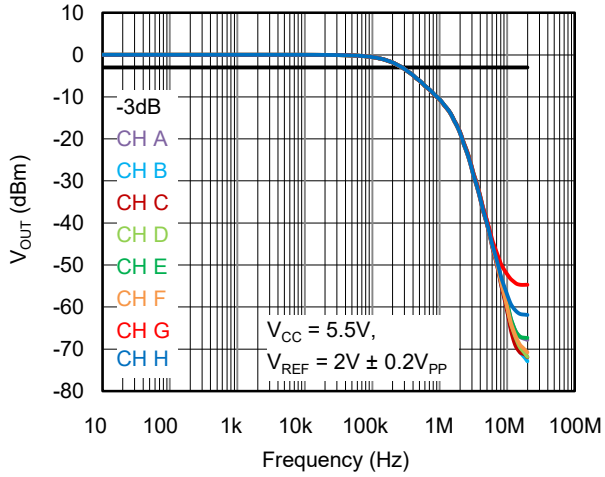
Settling Time vs. Capacitive Load



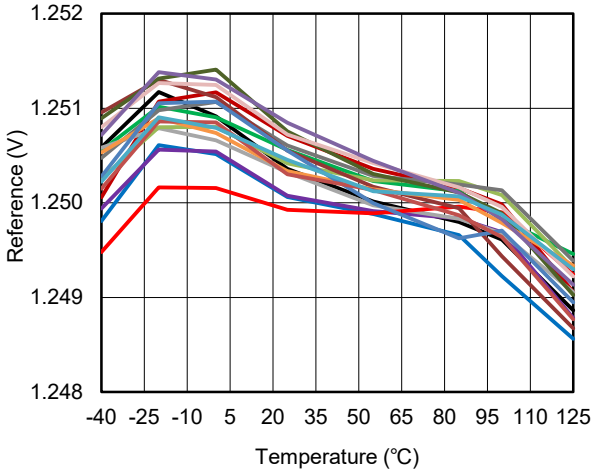
Hardware nCLR



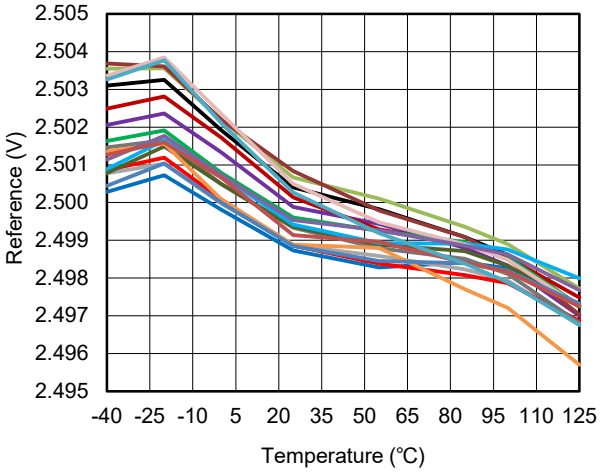
Multiplying Bandwidth



1.25V Reference Temperature Coefficient vs. Temperature



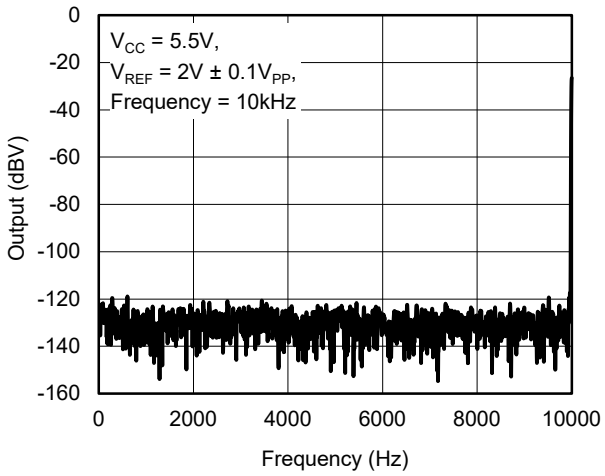
2.5V Reference Temperature Coefficient vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, unless otherwise noted.

Total Harmonic Distortion vs. Frequency



FUNCTIONAL BLOCK DIAGRAM

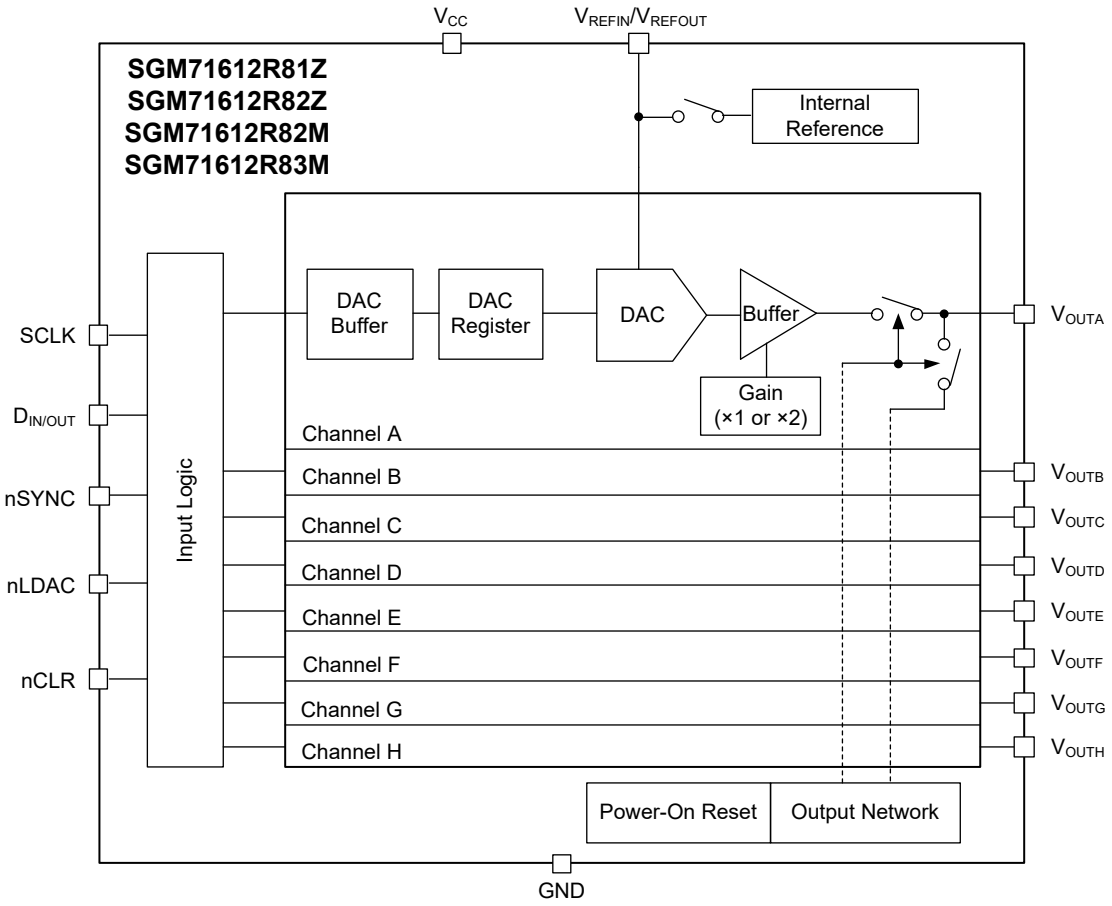


Figure 3. Block Diagram

DETAILED DESCRIPTION

DAC Section

The SGM71612R81/SGM71612R82/SGM71612R83 family is a CMOS DAC, which is the string architecture with a programmable gain amplifier output buffer. The device has an on-chip 1.25V/2.5V, 10ppm/℃ reference.

The output codes of the SGM71612R81/SGM71612R82/SGM71612R83 family are straight binary. The ideal output voltage is given by:

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right) \times Gain \quad (1)$$

where:
D = Equal decimal value is 0 to 65,535.
N = 16.
Gain = Output gain setting. (If using the internal reference, Gain = 2. If using the external reference, Gain = 1.)

Internal Reference

The SGM71612R81Z has an on-chip 1.25V, 10ppm/℃ reference. If the internal reference is enabled, it gives a full-scale output of 2.5V.

The SGM71612R82Z, SGM71612R82M and SGM71612R83M have an on-chip 2.5V, 10ppm/℃ reference. If the internal reference is enabled, it gives a full-scale output of 5V.

For SGM71612R81/SGM71612R82 family, the internal reference is disabled by default when the chip is powered on, and for SGM71612R83 family, its internal reference is enabled by default when the chip is powered on. The internal reference can be enabled/disabled by setting the control register (see Table 1). When using the internal reference, all channels must be powered down at the same time. The individual channel power-down is not supported if the internal reference is enabled.

Output Amplifier

The output buffer amplifier has the rail-to-rail output.

Serial Interface

The SGM71612R81/SGM71612R82/SGM71612R83 family has a 3-wire SPI-compatible interface.

For the detail operation timing sequence, please see Figure 1 and Figure 2. To prepare a new write sequence, nSYNC must be pulled up at least 15ns before the new write sequence, so that the falling edge of nSYNC can initiate the new write sequence.

Table 1. Command Definitions

DB[27:24]				Description
C3	C2	C1	C0	
0	0	0	0	Write to input register n
0	0	0	1	Update DAC register n
0	0	1	0	Write to input register n, update all (software load DAC function)
0	0	1	1	Write to and update DAC channel n
0	1	0	0	Set power-down modes register
0	1	0	1	Set clear code register
0	1	1	0	Set nLDAC register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set internal reference register
1	0	0	1	Set read enable control register
1	0	1	0	Reserved
–	–	–	–	Reserved
1	1	1	1	Reserved

Table 2. Address Commands

DB[23:20]				Selected DAC Channel
A3	A2	A1	A0	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

DETAILED DESCRIPTION (continued)

Input Shift Register

The input shift register is a 32-bit data. The first 3-bit DB[31:29] are Don't care bits. The second bit DB28 is a read or write command bit. The third 4-bit DB[27:24] are command bits C3 to C0 (see Table 1). The meaning of left bits is different from commands.

If C3 to C0 are DAC output data updating associated, the fourth 4-bit DB[23:20] are DAC address bits A3 to A0 (see Table 2). And the following 16-bit DB[19:4] are the DAC data bits. The final 4-bit DB[3:0] are not used data bits (see Figure 4).

If C3 to C0 is command to set the internal reference register, please refer to Table 3 and Table 4.

If C3 to C0 is command to set the power-down modes register, please refer to Table 5, Table 6 and Table 7.

If C3 to C0 is command to set the clear code register, please refer to Table 8 and Table 9.

If C3 to C0 is command to set the nLDAC register, please refer to Table 10 and Table 11.

If C3 to C0 is command to set the read enable control register, please refer to Table 12 and Table 13.

All 32-bit data are locked into the input register on the 32nd falling edge of SCLK.

nSYNC Interrupt

In a normal write sequence, the nSYNC line must be kept low for at least 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge. However, if nSYNC goes high before the 32nd falling edge, this write operation will be invalid and ignored. An example is shown in Figure 5.

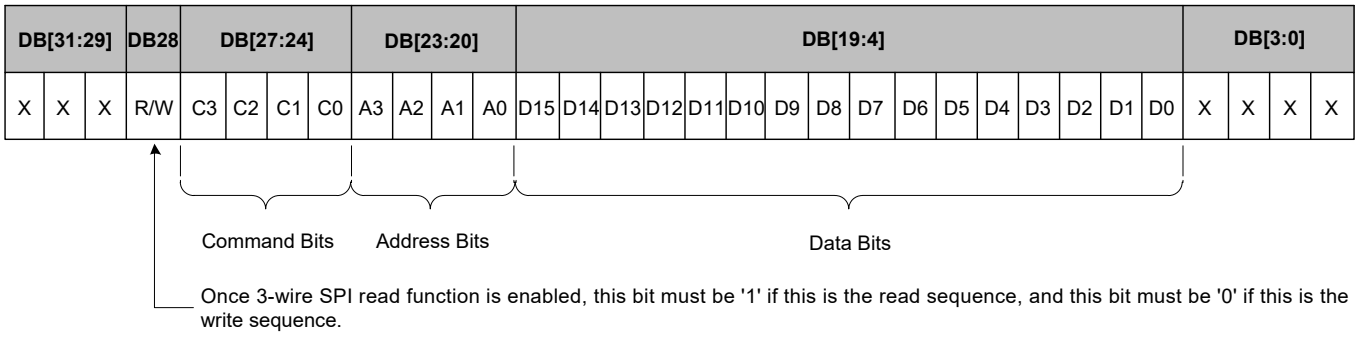


Figure 4. Input Register Contents

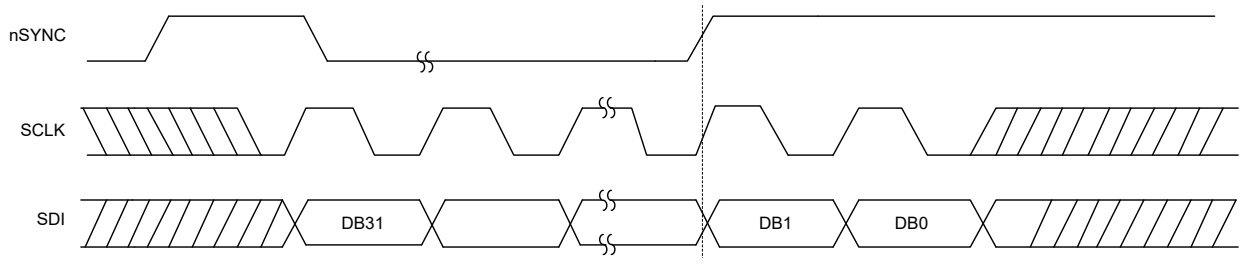


Figure 5. nSYNC Interrupt Facility

DETAILED DESCRIPTION (continued)

Internal Reference Register

The SGM71612R81/SGM71612R82 family on-chip internal voltage is off by default at power-on, while the SGM71612R83M on-chip internal voltage is on by default at power-on. In Table 1, the command '1000' (C3 to C0) is used to set the internal reference register. Table 3 shows how to enable or disable the internal reference. Table 4 shows the data format for setting the internal reference register.

Power-On Reset

The SGM71612R81Z and SGM71612R82Z reset to 0V output when the chip is powered up. The SGM71612R82M and SGM71612R83M reset to mid-scale output when the chip is powered up.

There is a software reset that can perform the same DAC reset function. And during the reset, any nLDAC and nCLR operations are invalid.

Table 3. Internal Reference Register

Internal Reference Register (DB0)	Description
0	Reference off (default for SGM71612R81/SGM71612R82 family)
1	Reference on (default for SGM71612R83M only)

Table 4. 32-Bit Input Shift Register Format for Reference Set-Up Command

MSB **LSB**

DB31 to DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB1	DB0
X	0/1	1	0	0	0	X	X	X	X	X	1/0
Don't cares	W/R	Command bits (C3 to C0)				Address bits (A3 to A0) Don't cares				Don't cares	Internal reference register

NOTE:
1. Once 3-wire SPI read function is enabled, DB28 = '0' represents that this is a write sequence, and DB28 = '1' represents that this is a read sequence. Otherwise, 3-wire SPI read function is disabled (default), DB28 will be ignored.

DETAILED DESCRIPTION (continued)

Power-Down Modes

The SGM71612R81/SGM71612R82/SGM71612R83 family has 3 power-down modes.

Table 5 shows these power-down modes configurations. And the operation data format is shown in Table 6 and Table 7. In Table 6, some or all DACs can be powered down to the selected modes by setting the according bits to '1'. Note that when the internal reference is enabled, the chip only supports all channels powered down at the same time. During power-down, the content of DAC register is retained.

To exit the power-down mode, configure the target DAC channels to normal operation mode.

Table 5. Power-Down Modes Register

DB9	DB8	Operating Mode
0	0	Normal operation
DB9	**DB8**	**Power-Down Modes**
0	1	1kΩ to GND
1	0	100kΩ to GND
1	1	Three-state

Table 6. 32-Bit Input Shift Register Format for Power-Down/Power-Up Write Operation

MSB **LSB**

DB31 to DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	1	0	0	X	X	X	X	X	PD1	PD0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A
Don't cares	W	Command bits (C3 to C0)				Address bits (A3 to A0) Don't cares				Don't cares	Power-down mode		Power-down/power-up channel selection (set bit to 1 to select)							

NOTE:
1. Once 3-wire SPI read function is enabled, DB28 = '0' represents that this is a write sequence, and DB28 = '1' represents that this is a read sequence. Otherwise, 3-wire SPI read function is disabled (default), DB28 will be ignored.

Table 7. 32-Bit Input Shift Register Format for Power-Down/Power-Up Read Operation

MSB **LSB**

DB31 to DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	1	0	1	0	0	X	X	X	X	0000	PDH1	PDH0	PDG1	PDG0	PDF1	PDF0	PDE1	PDE0	PDD1	PDD0	PDC1	PDC0	PDB1	PDB0	PDA1	PDA0
Don't cares	R	Command bits (C3 to C0)				Address bits (A3 to A0) Don't cares					Power-down/power-up channel selection															

NOTE:
1. Once 3-wire SPI read function is enabled, DB28 = '0' represents that this is a write sequence, and DB28 = '1' represents that this is a read sequence. Otherwise, 3-wire SPI read function is disabled (default), DB28 will be ignored.

DETAILED DESCRIPTION (continued)

Clear Code Register

The outputs of the SGM71612R81/SGM71612R82/SGM71612R83 family can be cleared asynchronously by hardware pin nCLR. The nCLR is active low and the falling edge is sensitive. If the nCLR pin goes from high to low, the chip clears the input register and resets DAC register to the users' configured data that is set in clear code register. And the chip resets the output according to the setting of clear code register at the same time.

The nCLR pin can be used to set the DAC register and output asynchronously. The nCLR status is set in clear code register (see Table 8).

To set clear code register, please refer to command format in Table 9.

When the nCLR pin is hold high, a full valid write operation can call the chip to exit the clear code mode. In the operation sequence, the part quits the clear code mode on the 32nd falling edge of SCLK.

It will take the chip about 300ns to start changing the output from receiving the nCLR falling edge. More details please refer to Electrical Characteristics tables.

Table 8. Clear Code Register

CR1 (DB1)	CR0 (DB0)	Clears to Code
0	0	0x0000 (default)
0	1	0x8000
1	0	0xFFFF
1	1	No operation

Table 9. 32-Bit Input Shift Register Format for Clear Code Operation

MSB **LSB**

DB31 to DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB2	DB1	DB0
X	0/1	0	1	0	1	X	X	X	X	X	CR1	CR0
Don't cares	W/R	Command bits (C3 to C0)				Address bits (A3 to A0) Don't cares				Don't cares	Clear code register	

NOTE:
1. Once 3-wire SPI read function is enabled, DB28 = '0' represents that this is a write sequence, and DB28 = '1' represents that this is a read sequence. Otherwise, 3-wire SPI read function is disabled (default), DB28 will be ignored.

DETAILED DESCRIPTION (continued)

nLDAC Function

There are two ways of updating DAC output by using hardware nLDAC pin.

The first way is that the nLDAC pin can be tied or kept low for a while (specified in Figure 1), after a full write command performing, the DAC is updated on the 32nd falling edge of SCLK.

The second way is that the nLDAC is kept high during the 32-bit write sequence, then a pulse of nLDAC is given (see Figure 1), the DAC output is updated asynchronously.

There are also software ways to control DAC updating, which is equal to nLDAC pin operation. Please refer to Table 10 and Table 11.

In Table 11, when according DAC channel bit is set to '0', the DAC output load mode is determined by nLDAC pin operation. When according DAC channel bit is set to '1', it is equal to the nLDAC pin connected to low, and the DAC is updated on the 32nd falling edge of SCLK.

Table 10. nLDAC Register

Load DAC Register		nLDAC Operation
nLDAC Bits (DB7 to DB0)	nLDAC Pin	
0	1/0	DAC update determined by nLDAC hardware pin operation
1	X—Don't care	DAC channels update, regardless the nLDAC pin. It is equal to the nLDAC pin connected to '0'

Table 11. 32-Bit Input Shift Register Format for nLDAC Operation

MSB **LSB**

DB31 to DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0/1	0	1	1	0	X	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A
Don't cares	W/R	Command bits (C3 to C0)				Address bits (A3 to A0) Don't cares				Don't cares	If set to '1', regardless of hardware nLDAC pin operation.							

NOTE:
1. Once 3-wire SPI read function is enabled, DB28 = '0' represents that this is a write sequence, and DB28 = '1' represents that this is a read sequence. Otherwise, 3-wire SPI read function is disabled (default), DB28 will be ignored.

DETAILED DESCRIPTION (continued)

3-Wire SPI Read Function

The SGM71612R81/SGM71612R82/SGM71612R83 family supports 3-wire SPI read function. This function is valid when the control bit of the read control register is set to '1', and this function is disabled when the control bit of the read control register is set to '0'. Once the read function is enabled, the DB28 bit of every 32-bit reading data stream must be '1' to tell DAC that this is a read operation. The detailed sequence of the read operation is shown in Figure 2. Correspondingly, once the read function is enabled, the DB28 bit of every 32-bit writing data stream must be '0' to tell DAC that this is a write operation, and the detailed sequence of the write operation is shown in Figure 1.

Table 12. Read Enable Control Register

Internal Read Enable Control Register (DB0)	Description
0	Disable 3-wire SPI read function (default)
1	Enable 3-wire SPI read function

Table 13. 32-Bit Input Shift Register Format for Read Enable Control Register Set-Up Command

MSB **LSB**

DB31 to DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19 to DB1	DB0
X	0/1	1	0	0	1	X	X	X	X	X	1/0
Don't cares	W/R	Command bits (C3 to C0)				Address bits (A3 to A0) Don't cares				Don't cares	Internal read enable control register

NOTE:
1. Once 3-wire SPI read function is enabled, DB28 = '0' represents that this is a write sequence, and DB28 = '1' represents that this is a read sequence. Otherwise, 3-wire SPI read function is disabled (default), DB28 will be ignored.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

APRIL 2024 – REV.A.1 to REV.A.2 **Page**

Updated Tape and Reel Information section 31, 32

OCTOBER 2023 – REV.A to REV.A.1 **Page**

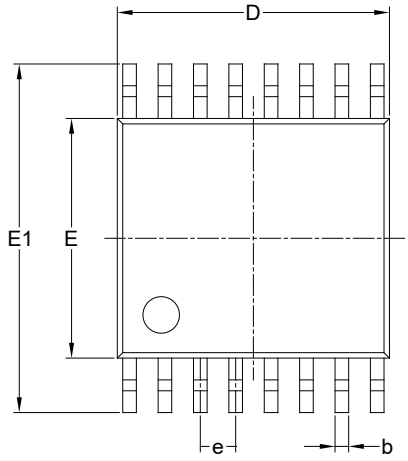
Updated Package/Ordering Information section 2, 3

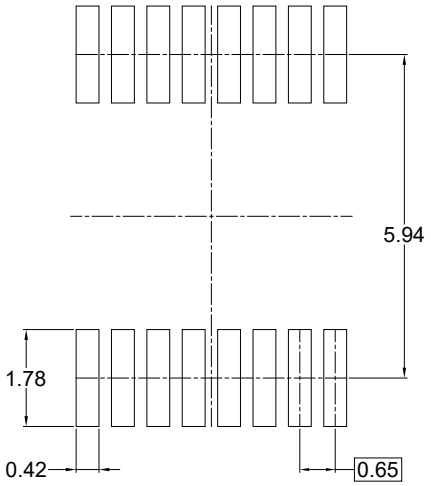
Changes from Original (SEPTEMBER 2023) to REV.A **Page**

Changed from product preview to production data ..... All

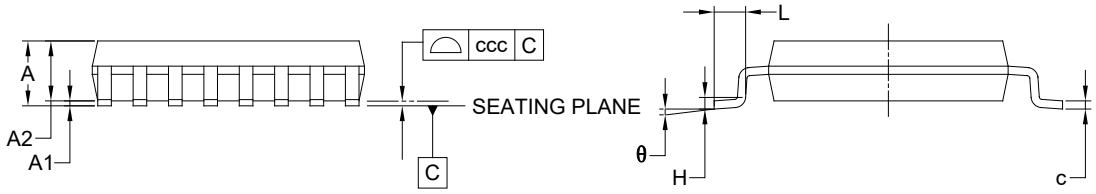
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

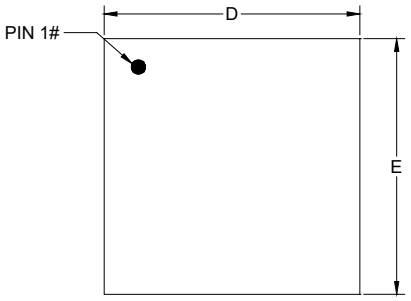


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

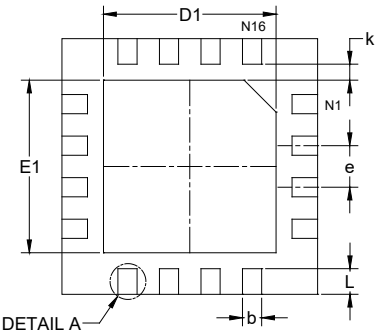
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

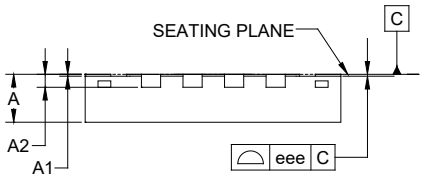
TQFN-4×4-16BL



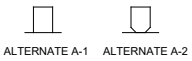
TOP VIEW



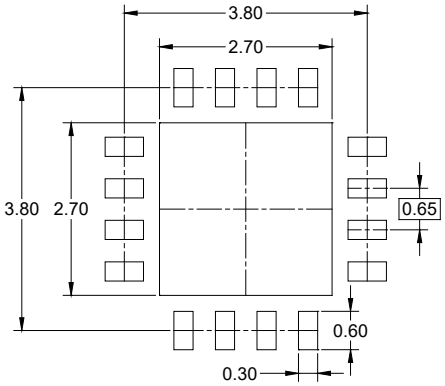
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



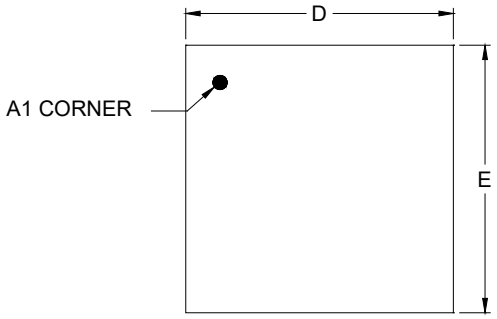
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.250	-	0.350
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.600	2.700	2.800
E1	2.600	2.700	2.800
e	0.650 BSC		
k	0.250 REF		
L	0.300	-	0.500
eee	0.080		

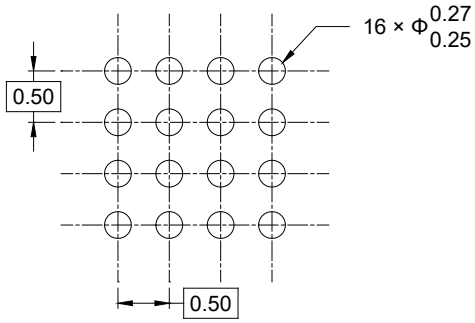
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

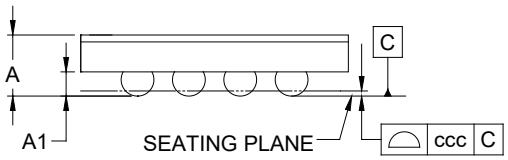
FOCSP-2.6×2.6-16B



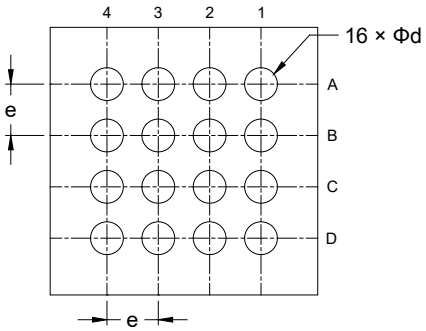
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



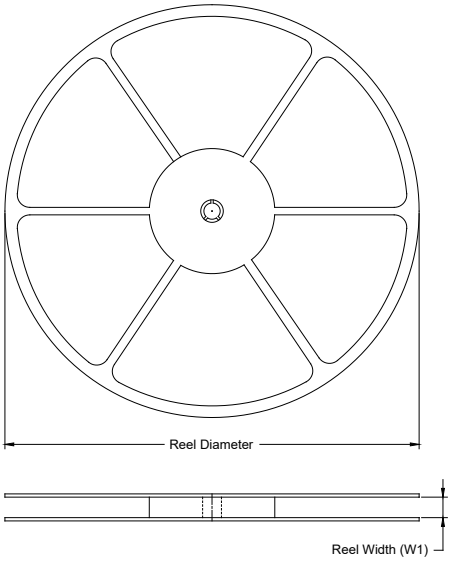
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.628
A1	0.216	-	0.256
D	2.575	-	2.635
E	2.575	-	2.635
d	0.289	-	0.349
e	0.500 BSC		
ccc	0.050		

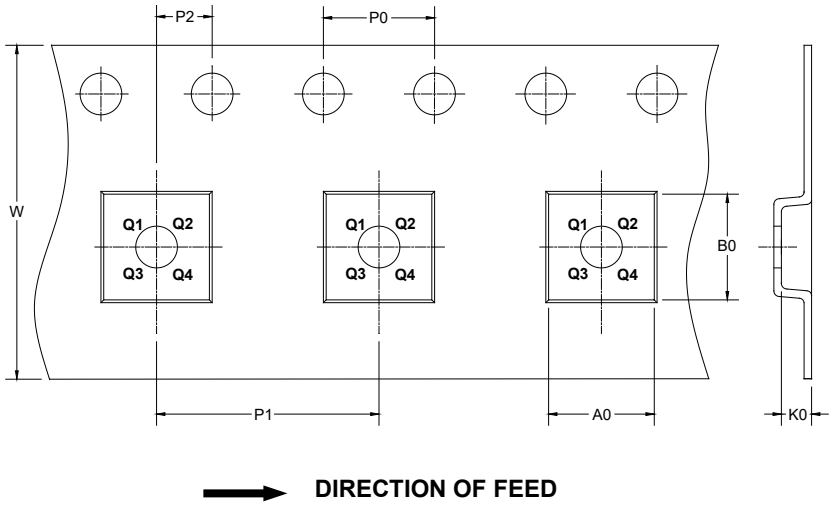
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



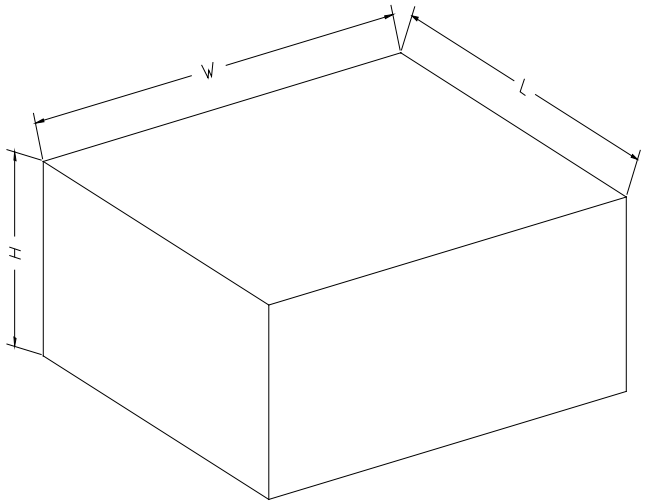
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	MPQ	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	4000	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TSSOP-16	13″	250	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-4×4-16BL	13″	3000	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2
TQFN-4×4-16BL	13″	250	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2
FOCSP-2.6×2.6-16B	13″	5000	12.4	2.72	2.72	0.70	4.0	8.0	2.0	12.0	Q1
FOCSP-2.6×2.6-16B	7″	250	12.4	2.72	2.72	0.70	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002