SGM4560B
CA Card Power Supply and Level Translator

GENERAL DESCRIPTION

The SGM4560B is used for power conversion and level translation of the signal in the application of CA cards. Also, it can be used for the applications of 3.0V or 5.0V CA cards, which is powered by its internal LDOs from 3.0V to 5.5V input signal. The value of the output voltage can be controlled with the voltage selection pins of the SGM4560B with the maximum load current of 200mA.

The level translator integrated on the SGM4560B can boost the input signal which is powered by 1.6V to 3.0V or 5.0V interface. The lifespan of the battery can be enhanced as the 100μA (TYP) operating current and 1μA (MAX) shutdown current.

The SGM4560B is available in a Green TSSOP-14 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **CA Card Power Supply: 3.0V/5.0V at 200mA**
- **3.0V to 5.5V Input Voltage Range**
- **1.6V to 5.5V Controller Voltage Range**
- **Fast Rising Time for the Signals**
- **Built-In Fault Protection Circuitry**
- **Level Translators to 3.0V or 5.0V**
- **Low Supply Voltage and Shutdown Current**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in a Green TSSOP-14 Package**

APPLICATIONS

CA Card Interface

TYPICAL APPLICATION

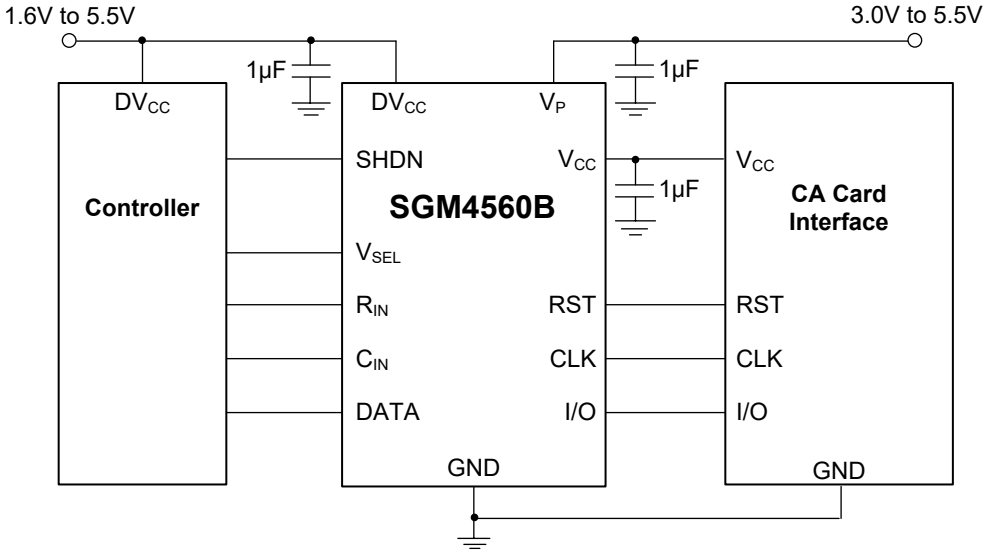


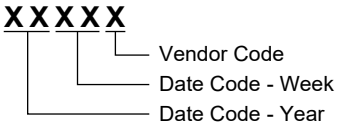
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM4560B	TSSOP-14	-40℃ to +85℃	SGM4560BYTS14G/TR	SGM4560B YTS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

V_P, DV_{CC} ..... -0.3V to 6V

V_{CC} ..... -0.3V to V_P + 0.3V

SHDN, V_{SEL}, R_{IN}, C_{IN} ..... -0.3V to 6V

CLK, RST, I/O ..... -0.3V to V_{CC} + 0.3V

DATA ..... -0.3V to DV_{CC}+0.3V

Package Thermal Resistance

TSSOP-14, θ_{JA} ..... 154℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 4000V

MM 400V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

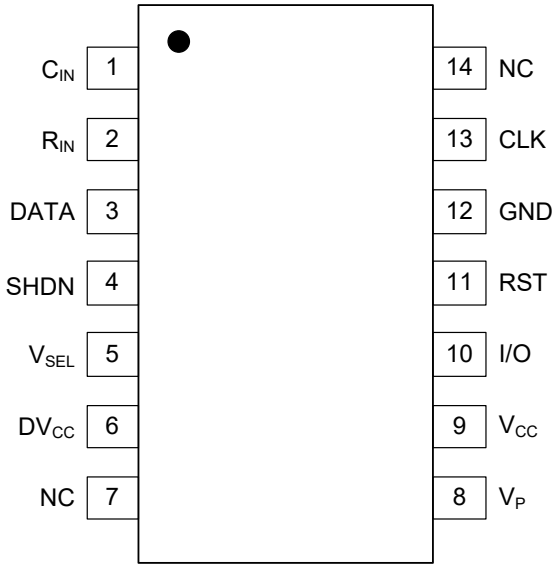
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-14

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	C_{IN}	Controller Clock Input Pin.
2	R_{IN}	Controller Reset Input Pin.
3	DATA	Controller Bidirectional Data Input/Output Pin. A weak pull-up current source ensures that the DATA pin is held HIGH during shutdown, as long as DV_{CC} is powered.
4	SHDN	Controller Driven Shutdown Pin. This pin goes to high (DV_{CC}) in the normal operation, and the pin goes to low when in the shutdown mode.
5	V_{SEL}	Select Pin for V_{CC} Voltage. Select V_{CC} = 3.0V for the low level and V_{CC} = 5.0V for driving the pin to DV_{CC}.
6	DV_{CC}	Controller Supply Voltage, for the Input/Output Pins (C_{IN}, R_{IN}, DATA). Bypass with a 1μF ceramic capacitor to GND.
7, 14	NC	No Connection.
8	V_P	V_{CC} Supply Input Pin. It can be operated between 3.0V and 5.5V. It is recommended to use a 1μF or larger ceramic capacitor from V_P pin to GND to get good power supply decoupling. This ceramic capacitor should be placed as close as possible to V_P pin.
9	V_{CC}	CA Card V_{CC} Supply Voltage. It is recommended to use a 1μF ceramic capacitor to ensure stability. This ceramic capacitor should be placed as close as possible to V_{CC} pin. The pin is discharged to GND in the shutdown mode.
10	I/O	CA Card Bidirectional Data Input/Output Pin. The pin is pulled to GND in the shutdown mode.
11	RST	CA Card Reset Output Pin. The pin is pulled to GND in the shutdown mode.
12	GND	Ground.
13	CLK	CA Card Clock Output Pin. The pin is pulled to GND in the shutdown mode. Careful board layout of CLK pin is necessary for fast rising and falling edges.

ELECTRICAL CHARACTERISTICS

(V_P = 5.0V, DV_{CC} = 1.8V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Power Supply						
V_P Operating Voltage			3.0		5.5	V
V_P Operating Current		V_P = 5.5V, I_{VCC} = 0mA		100	195	μA
V_P Shutdown Current		SHDN = 0V, V_P = 5.5V		0.4	8	μA
DV_{CC} Operating Voltage			1.6		5.5	V
DV_{CC} Operating Current				5	10	μA
DV_{CC} Shutdown Current		SHDN = 0V		0.01	1	μA
DV_{CC} Under-Voltage Lockout			0.8	1.0	1.2	V
V_{CC} Output Voltage		V_{SEL} = DV_{CC}, V_P = 5.0V, I_{VCC} = 200mA		4.88		V
		V_{SEL} = DV_{CC}, V_P = 5.5V, I_{VCC} = 0mA to 200mA	4.825	5.0	5.175	
		V_{SEL} = 0V, V_P = 5.5V, I_{VCC} = 0mA to 200mA	2.895	3.0	3.105	
Controller Inputs/Outputs						
Input Voltage Range		SHDN, V_{SEL}, R_{IN}, C_{IN}, DATA	0		DV_{CC}	V
High-Level Input Voltage	V_{IH}	R_{IN}, C_{IN}, T_A = -40℃ to +85℃	0.9 × DV_{CC}			V
		SHDN, V_{SEL}, T_A = -40℃ to +85℃	1.55			
Low-Level Input Voltage	V_{IL}	R_{IN}, C_{IN}, T_A = -40℃ to +85℃			0.1 × DV_{CC}	V
		SHDN, V_{SEL}, T_A = -40℃ to +85℃			0.35	
High-Level Input Current	I_{IH}	DATA	-5		5	μA
Low-Level Input Current	I_{IL}	DATA			1.75	mA
High-Level Output Voltage	V_{OH}	DATA, I_{OH} = 20μA, I/O = V_{CC}	0.9 × DV_{CC}			V
Low-Level Output Voltage	V_{OL}	DATA, I_{OL} = -200μA, I/O = 0V			0.2	V
DATA Pull-Up Current		DATA = 1V		200	600	μA

ELECTRICAL CHARACTERISTICS (continued)

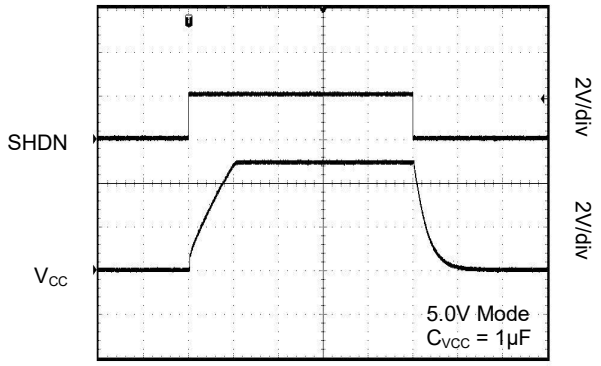
(V_P = 5.0V, DV_{CC} = 1.8V, T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CA Card Inputs/Outputs (V_{CC} = 3.0V)						
High-Level Output Voltage	V_{OH}	I/O, I_{OH} = 20μA, DATA = DV_{CC}	0.9 × V_{CC}			V
Low-Level Output Voltage	V_{OL}	I/O, I_{OL} = -1mA, DATA = 0V			0.3	V
High-Level Output Voltage	V_{OH}	CLK, I_{OH} = 20μA	0.9 × V_{CC}			V
Low-Level Output Voltage	V_{OL}	CLK, I_{OL} = -200μA			0.15	V
High-Level Output Voltage	V_{OH}	RST, I_{OH} = 20μA	0.9 × V_{CC}			V
Low-Level Output Voltage	V_{OL}	RST, I_{OL} = -200μA			0.2	V
I/O Pull-Up Current		I/O = 1V		320	850	μA
CA Card Inputs/Outputs (V_{CC} = 5.0V)						
High-Level Output Voltage	V_{OH}	I/O, I_{OH} = 20μA, DATA = DV_{CC}	0.9 × V_{CC}			V
Low-Level Output Voltage	V_{OL}	I/O, I_{OL} = -1mA, DATA = 0V			0.3	V
High-Level Output Voltage	V_{OH}	CLK, I_{OH} = 20μA	0.9 × V_{CC}			V
Low-Level Output Voltage	V_{OL}	CLK, I_{OL} = -200μA			0.15	V
High-Level Output Voltage	V_{OH}	RST, I_{OH} = 20μA	0.9 × V_{CC}			V
Low-Level Output Voltage	V_{OL}	RST, I_{OL} = -200μA			0.2	V
I/O Pull-Up Current		I/O = 1V		400	1000	μA
CA Card Timing Parameters						
CLK Rise/Fall Time		Loaded with 30pF, V_{CC} = 3.0V/5.0V (10% to 90%)		3		ns
RST Rise/Fall Time		Loaded with 30pF, V_{CC} = 3.0V/5.0V (10% to 90%)		30		ns
I/O Rise/Fall Time		Loaded with 30pF, V_{CC} = 3.0V/5.0V (10% to 90%)		150		ns
CLK Frequency		Loaded with 30pF			10	MHz
V_{CC} Turn-On Time		SHDN = 1		0.4		ms
V_{CC} Discharge Time to 1V		SHDN = 0		0.2		ms

TYPICAL PERFORMANCE CHARACTERISTICS

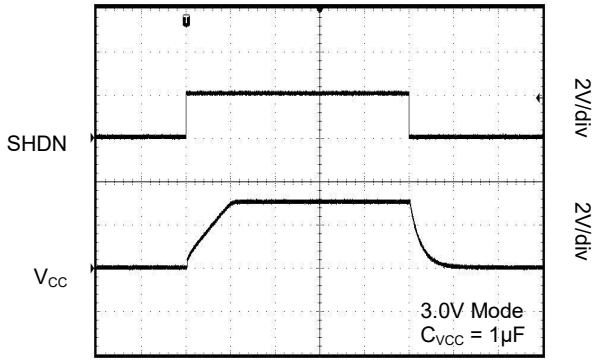
V_P = 5.0V, DV_{CC} = 1.8V, T_A = +25℃, unless otherwise noted.

V_{CC} Turn-On and Turn-Off



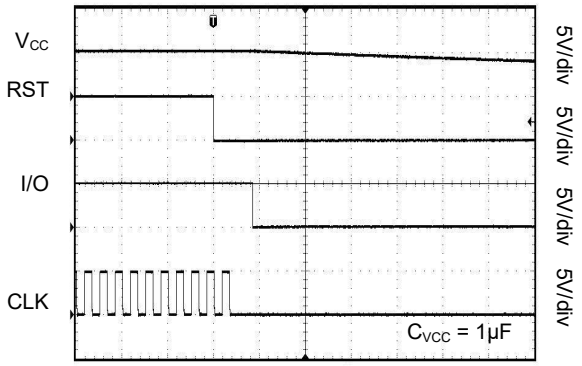
Time (400μs/div)

V_{CC} Turn-On and Turn-Off



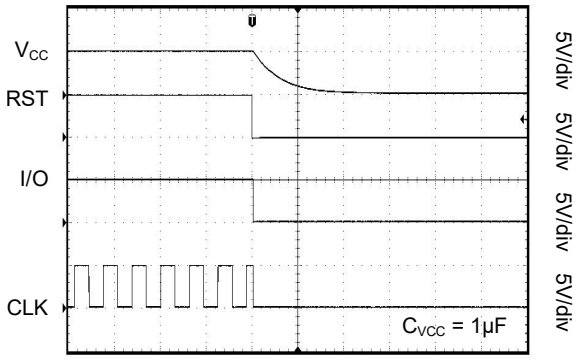
Time (400μs/div)

Deactivation Sequence



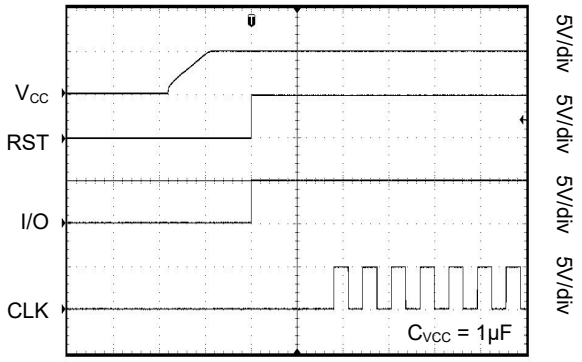
Time (10μs/div)

Deactivation Sequence



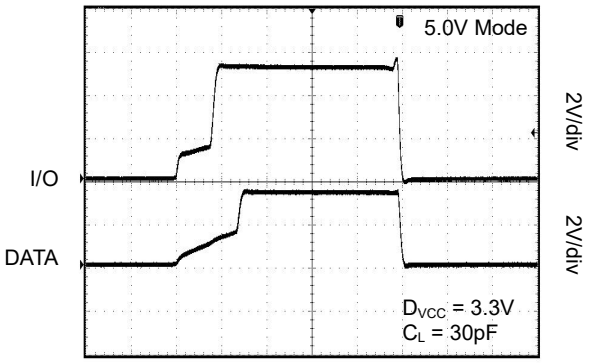
Time (400μs/div)

Activation Sequence



Time (400μs/div)

Bidirectional Data Transfer



Time (200ns/div)

FUNCTIONAL BLOCK DIAGRAM

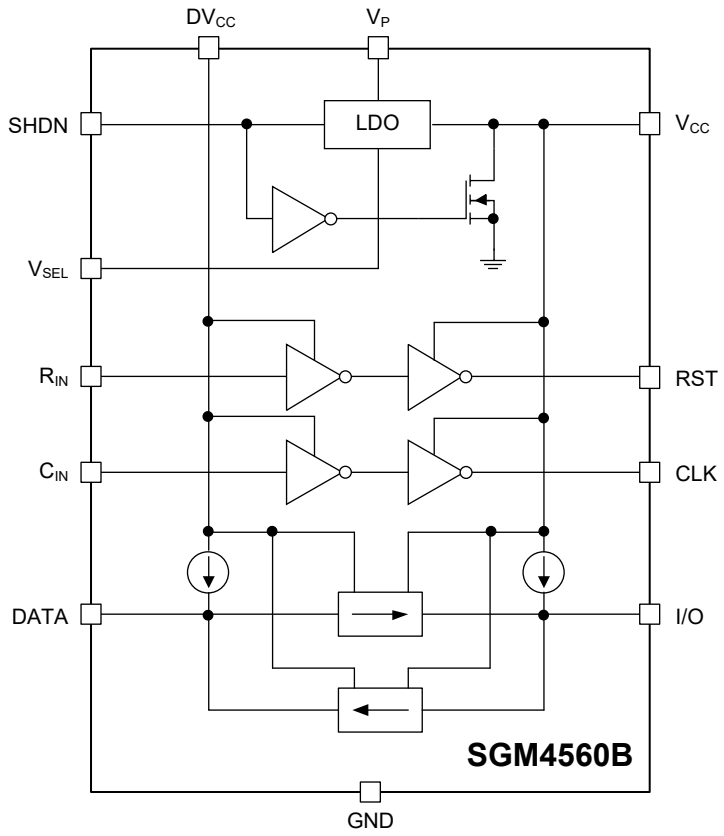


Figure 2. Block Diagram

APPLICATION INFORMATION

V_{CC} Voltage Regulator

The SGM4560B features a 200mA low dropout (LDO) regulator that used as the V_{CC} voltage regulator with a digital selection of 3.0V or 5.0V output. The output voltage is selected by V_{SEL} pin. It is recommended that the V_{CC} output can be connected to a 1μF bypass capacitor and the V_P can be connected to a 1μF bypass ceramic capacitor.

Level Translators

The SGM4560B supports level translators that allow low voltage controllers to interface with the 3.0V or 5.0V CA cards. The CLK and RST lines to the CA card are level shifted from the controller supply (GND to DV_{CC}) to the CA card supply (GND to V_{CC}). The bidirectional channel is level shifted to the appropriate V_{CC} voltage at the I/O pin.

Pull-Up Current Sources

The pull-up current sources with low static current for DATA and I/O pins can make sure that the rise time of the associated pins enhances dramatically. If the bidirectional mode is disabled, the node will be charged by the start-up current.

Activation/Deactivation

The internal built-in circuitry determines the sequence of the activation or deactivation. Also, the connected channels can be activated or deactivated by the SGM4560B. Pulling SHDN to high state can activate the associated channel. The sequence of activation is shown as below:

1. The RST, CLK and I/O pins should be pulled low at first.
2. Enabling V_{CC}.
3. The RST and I/O cannot be enabled until the voltage level of V_{CC} is stable.
4. After the pin of I/O is enabled, the CLK is enabled as well on the rising edge of the second clock signal cycle.

Pulling SHDN to low state can deactivate the associated channel. The sequence of deactivation is shown as below:

1. Disabling the reset signal by bringing RST to low state.
2. After the pin of SHDN is disabled, the CLK is disabled as well by bringing low two clock cycles. The clock channel will be disabled at 9μs after SHDN pin is disabled if there is no clock signal coming through.
3. When the SHDN is pulled to a low state, the I/O is pulled to low state and the I/O channel is disabled after 9μs.
4. The I/O is pulled to a low state before V_{CC} is disabled.

Fault Detection

The internal circuitry can limit the current flow in a short-circuit condition for the pins of V_{CC}, RST and I/O. Before the output of the SGM4560B is reduced, the typical supply current of V_{CC} is 300mA.

The capability of the current driving of the output stage can be significantly decreased by CLK pin in order to tolerate any faults. Once the internal circuitry detects the fault, it cannot decrease the current capability of the output stage until the fault detection delay is elapsed. If the fault is removed, SGM4560B will be permitted to detect the reduced current.

ESD Protection

A good PCB layout is important for the protection of ESD. Also, the GND pin of the SGM4560B should be connected directly to the plane of GND. The capacitors which are used to bypass the V_{CC} pin should be located as close as possible to these pins and tied to the GND plane directly.

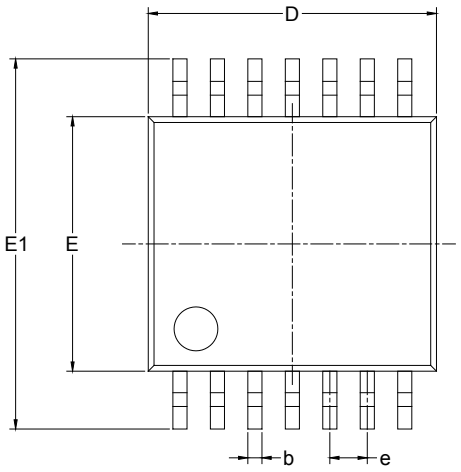
REVISION HISTORY

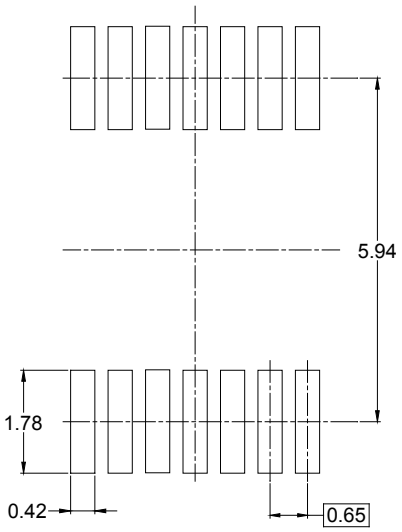
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (AUGUST 2014) to REV.A	Page
Changed from product preview to production data	All

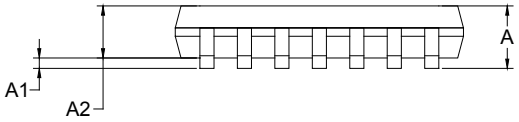
PACKAGE OUTLINE DIMENSIONS

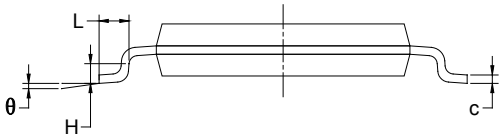
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

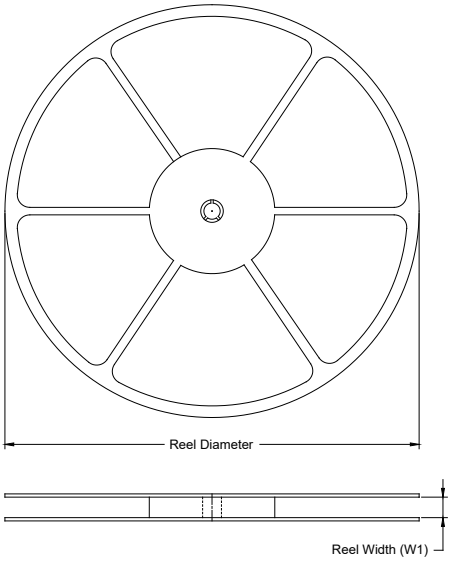




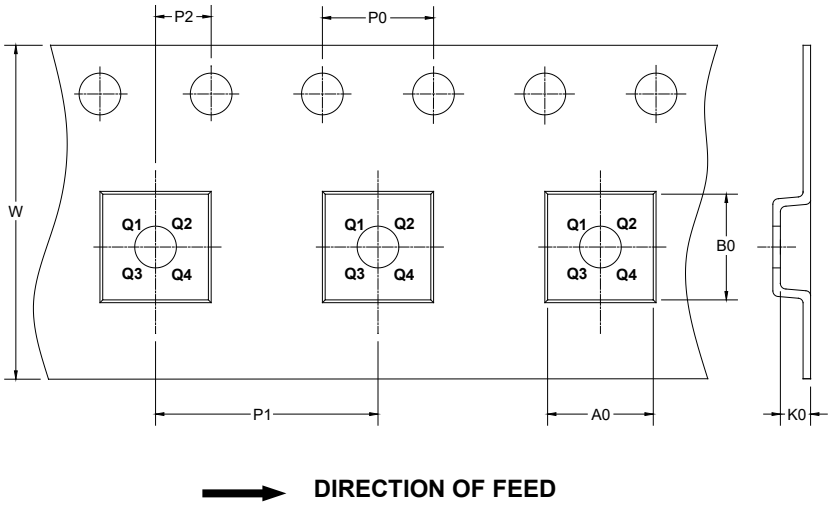
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.100		0.043
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



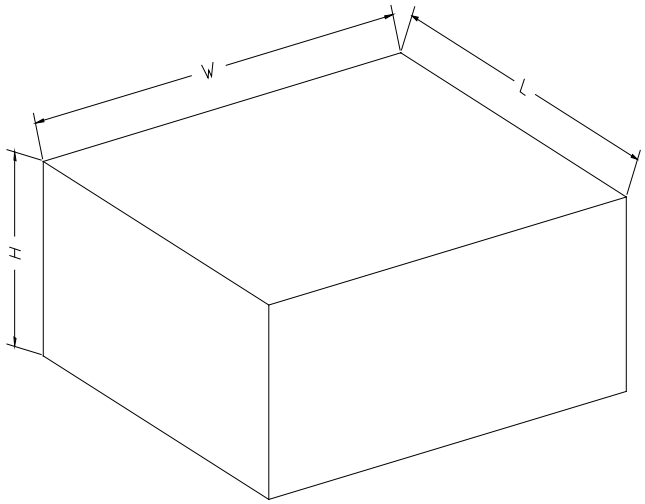
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002