74HCT595
8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with 3-State Controlled Outputs

GENERAL DESCRIPTION

The 74HCT595 is an 8-bit serial-in/serial-out or parallel-out shift register with 3-state outputs designed for 4.5V to 5.5V V_{CC} operation.

The device integrates an 8-bit shift register and an 8-bit D-type storage register. The storage register features parallel 3-state outputs. The shift register provides a clear input ($\overline{SRCLR}$) with direct overriding function, a serial input (SER) and a serial output ($Q_{H'}$) to implement cascading. When output enable input ($\overline{OE}$) is held low, the data in storage register will appear at the outputs. When $\overline{OE}$ is held high, all outputs except $Q_{H'}$ are in high-impedance state. $\overline{OE}$ does not affect internal register data and the serial output ($Q_{H'}$).

Both the shift register and storage register have separate clocks. The shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered. If the SRCLK and RCLK are connected together, the shift register always leads one clock pulse than the storage register all the time.

The 74HCT595 is available in Green TSSOP-16 and SOIC-16 packages. It operates over an operating temperature range of -40℃ to +125℃.

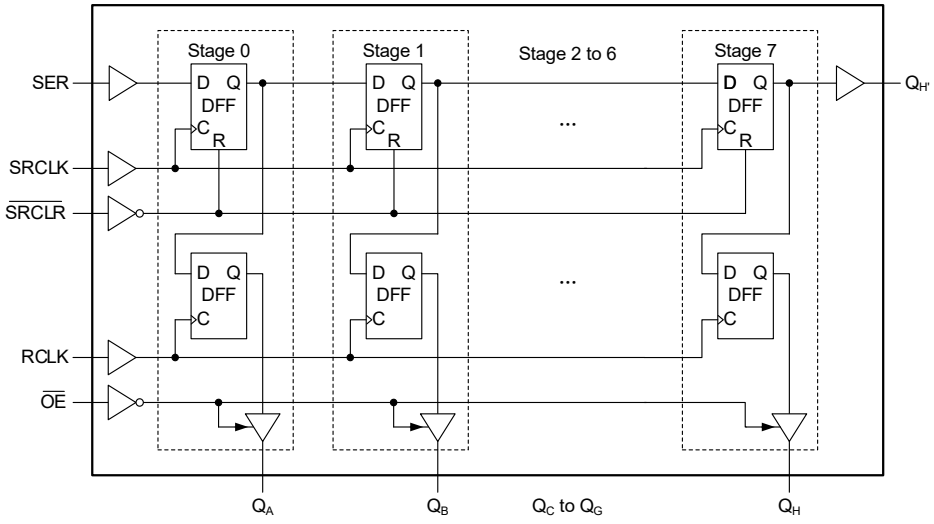
FEATURES

- **Supply Voltage Range: 4.5V to 5.5V**
- **8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register**
- **Direct Clear Input of Shift Register**
- **Compatible with Input Logic LSTTL: V_{IL} = 0.8V (MAX), V_{IH} = 2.0V (MIN)**
- **Fan-Out Supports up to 10 LSTTL Loads**
- **Latch-Up Performance (> 100mA) Meets JESD 78, Class II Standard**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-16 and SOIC-16 Packages**

APPLICATIONS

Industrial Equipment
Medical Equipment
Telecom Equipment

LOGIC DIAGRAM

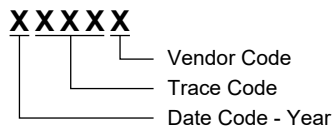


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74HCT595	TSSOP-16	-40℃ to +125℃	74HCT595XTS16G/TR	74HCT595 XTS16 XXXXX	Tape and Reel, 4000
	SOIC-16	-40℃ to +125℃	74HCT595XS16G/TR	74HCT595XS16 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} ..... -0.5V to 7.0V
Input Voltage Range, V_I (1) .... -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Output Voltage Range, V_O (1) -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Input Clamp Current, I_{IK} (V_I < 0V or V_I > V_{CC}) ..... ±20mA
Output Clamp Current, I_{OK} (V_O < 0V or V_O > V_{CC}) ..... ±20mA
Continuous Output Current, I_O (V_O = 0V to V_{CC}) ..... ±35mA
Continuous Current through V_{CC} or GND ..... ±70mA
Junction Temperature (2) ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (3) (4)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} ..... 4.5V to 5.5V
Input Voltage Range, V_I ..... 0V to V_{CC}
Output Voltage Range, V_O ..... 0V to V_{CC}
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 4.5V to 5.5V ..... 500ns/V (MAX)
Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	*X*	*X*	*X*	H	Outputs Q_A ~ Q_H are disabled.
X	*X*	*X*	*X*	L	Outputs Q_A ~ Q_H are enabled.
X	X	L	*X*	*X*	Data of the shift register is cleared.
L	↑	H	*X*	*X*	Logic low-level shifted into shift register stage 0. Other stages can transfer data from the previous stage respectively.
H	↑	H	*X*	*X*	Logic high-level shifted into shift register stage 0. Other stages can transfer data from the previous stage respectively.
X	*X*	H	↑	*X*	Data of the shift register is transferred to the storage register.
X	↑	H	↑	*X*	Data of the shift register is transferred to the storage register and then the data is shifted through.

H = High Voltage Level

L = Low Voltage Level

↑ = Low-to-High Clock Transition

X = Don't Care

TIMING DIAGRAM

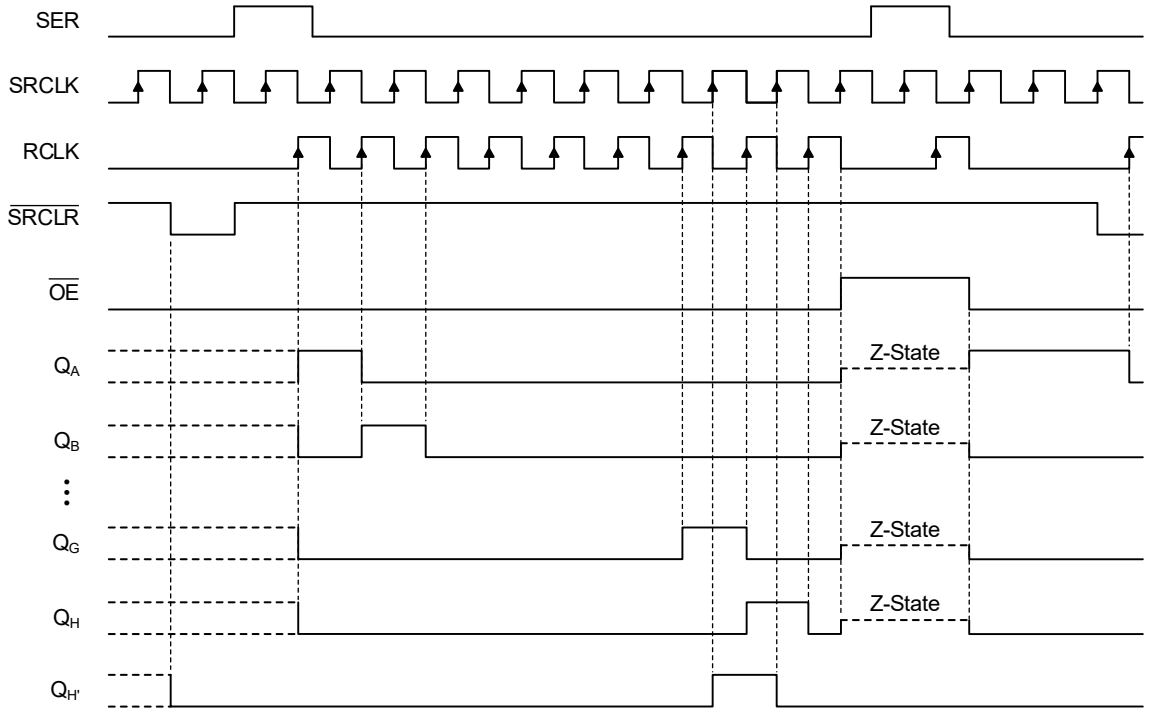
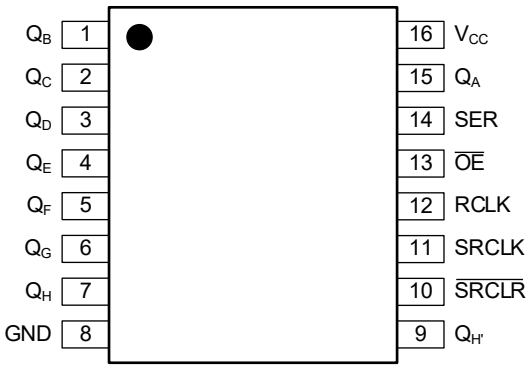


Figure 1. Timing Diagram

PIN CONFIGURATIONS

(TOP VIEW)



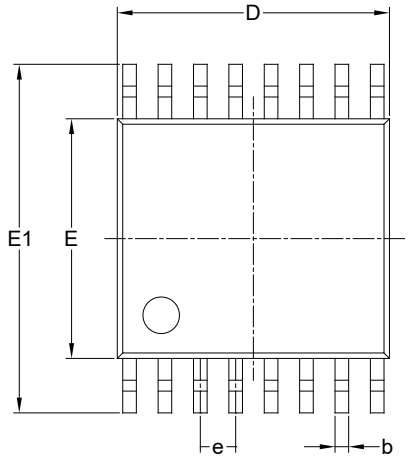
TSSOP-16/SOIC-16

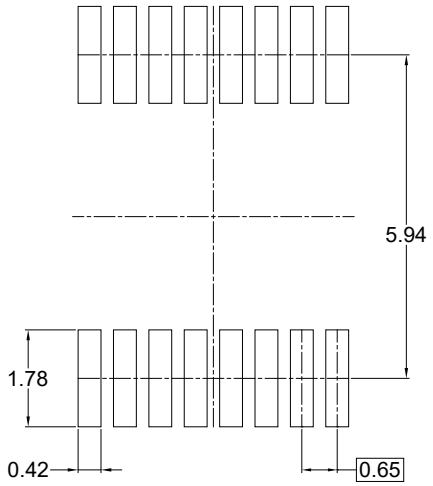
PIN DESCRIPTION

PIN	NAME	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q_A, Q_B, Q_C, Q_D, Q_E, Q_F, Q_G, Q_H	Parallel Data Outputs.
8	GND	Ground.
9	$Q_{H'}$	Serial Data Output.
10	$\overline{SRCLR}$	Shift Register Clear Input (Active-Low).
11	SRCLK	Shift Register Clock Input (Rising Edge Triggered).
12	RCLK	Storage Register Clock Input (Rising Edge Triggered).
13	$\overline{OE}$	Output Enable Input (Active-Low).
14	SER	Serial Data Input.
16	V_{CC}	Power Supply.

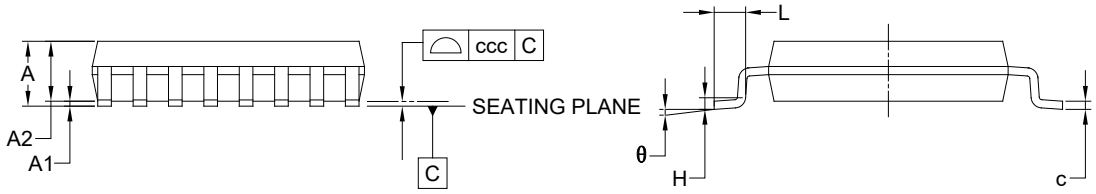
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

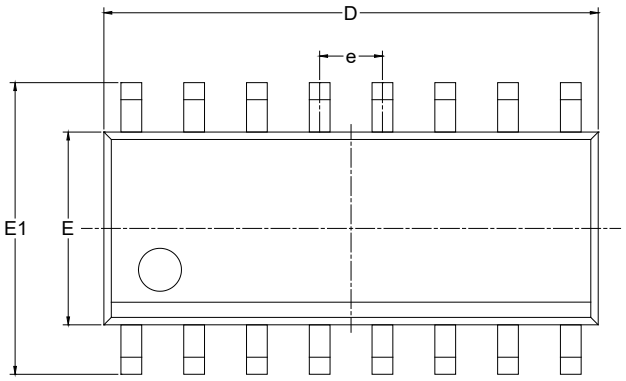


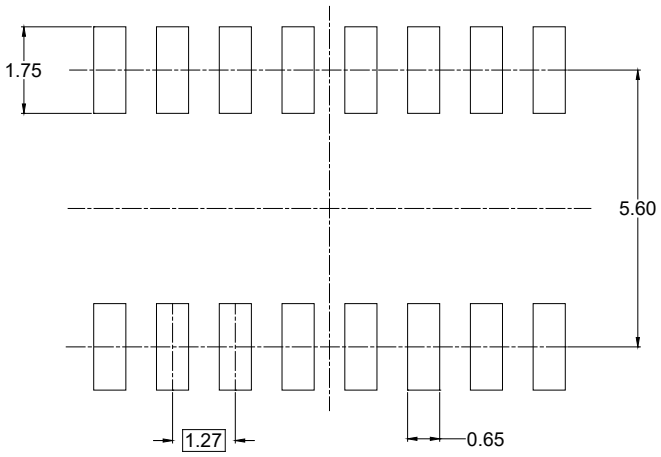
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

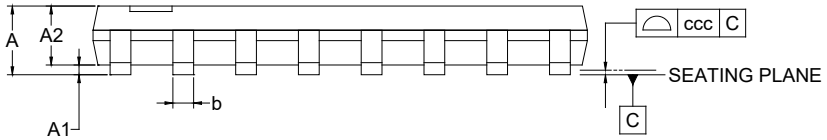
PACKAGE OUTLINE DIMENSIONS

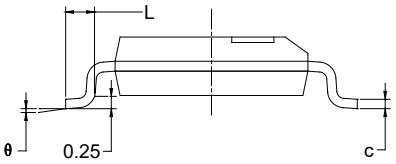
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)



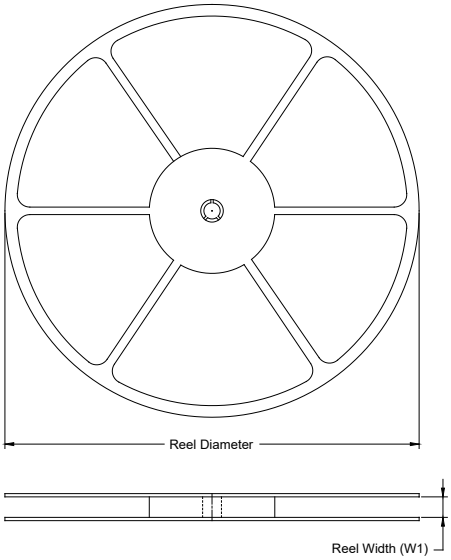


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.750
A1	0.100	-	0.250
A2	1.250	-	1.550
b	0.310	-	0.510
c	0.100	-	0.250
D	9.800	-	10.200
E	3.800	-	4.000
E1	5.800	-	6.200
e	1.270 BSC		
L	0.400	-	1.270
θ	0°	-	8°
ccc	0.100		

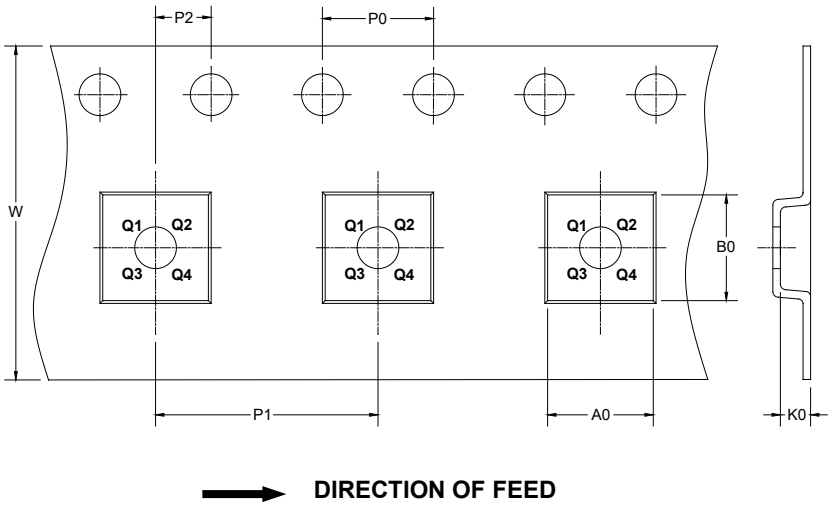
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-012.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

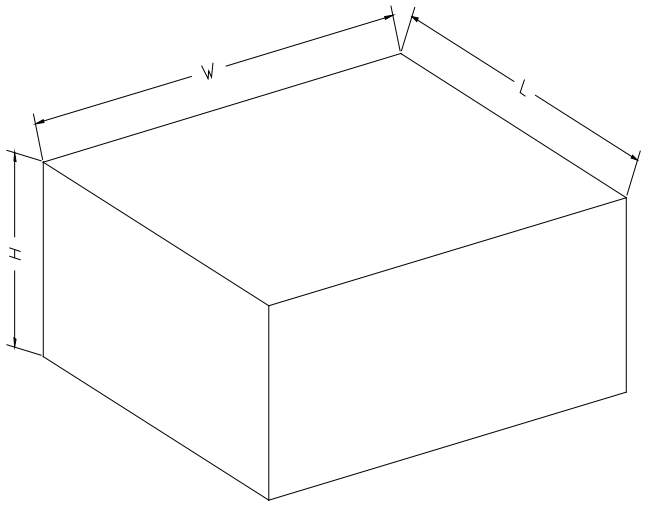
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13"	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002