SGM41282S
70V, 2.5mA Precision Protection APD Bias Dual-Gain Track/Hold Current Mirror

GENERAL DESCRIPTION

The SGM41282S integrates a Boost converter for generating up to 70V regulated output, a 1×/3 × dual-gain current mirror with a track and hold output buffer, which is unique to simplify the fiber module circuit design due to the use of low resolution ADC.

The SGM41282S is available in a Green TQFN-3×3-16L package.

FEATURES

- **Input Voltage Range: 2.8V to 5.5V**
- **Wide Output Voltage Range from (V_{IN} + 5V) to 70V**
- **850kHz Switching Frequency**
- **1:30 Output Voltage Programming**
- **Adjustable Over-Current Protection**
- **Internal 1×/3× Dual-Gain Current Mirror**
- **2.48V Voltage Buffer for Full-Scale Output Current**
- **Less than 1μA Shutdown Current**
- **Full Chain Circuit: Bias-Mirror-Track/Hold**
- **Replacement of *15059/*3430+*3923**
- **Available in a Green TQFN-3×3-16L Package**

APPLICATIONS

Fiber Modules with APD Photon Sensor
Laser Beam Finders (LIDA)

TYPICAL APPLICATION

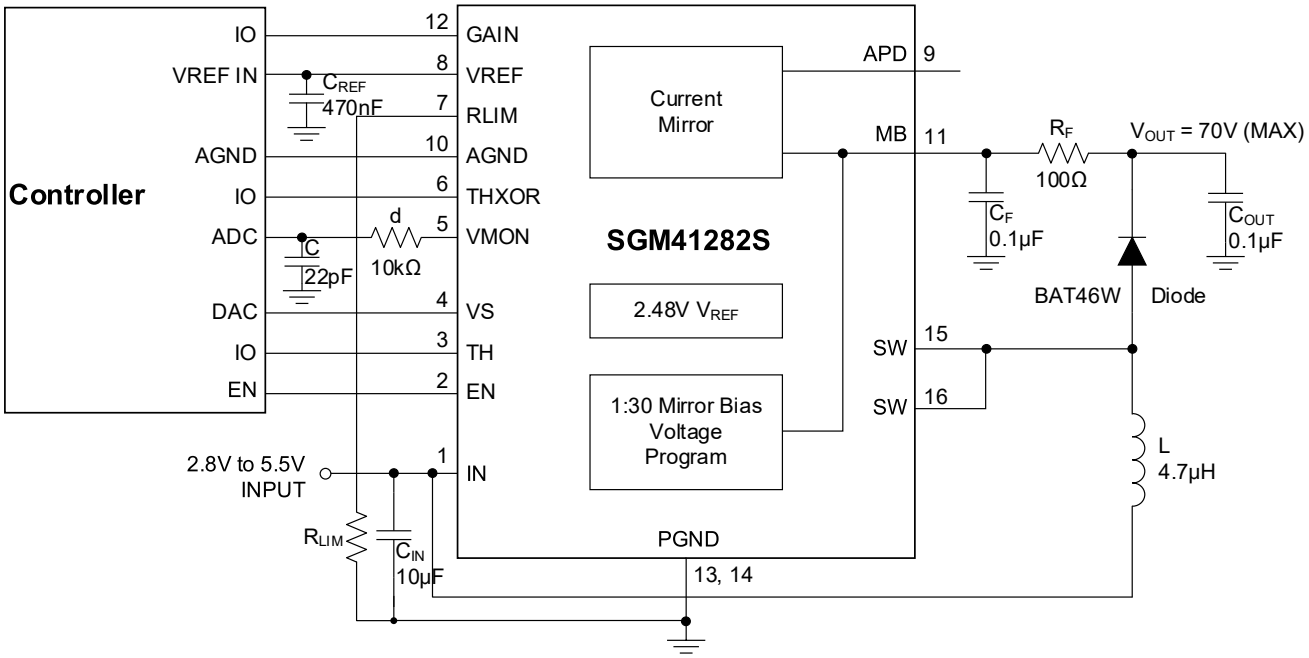


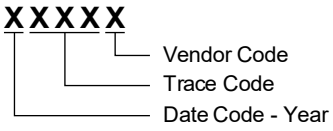
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41282S	TQFN-3×3-16L	-40℃ to +85℃	SGM41282SYTQ16G/TR	0XVTQ XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

IN, EN, VS, TH, THXOR, VMON, RLIM, VREF, GAIN ..... -0.3V to 6V
SW, MB ..... -0.3V to 76V
SW (Transient, 10ns) ..... -1V to 78V
APD ..... -0.3V to (V_{MB} + 0.3V)
Package Thermal Resistance
TQFN-3×3-16L, θ_{JA} ..... 38.5℃/W
TQFN-3×3-16L, θ_{JB} ..... 14.6℃/W
TQFN-3×3-16L, $\theta_{JC\ (TOP)}$ ..... 43.1℃/W
TQFN-3×3-16L, $\theta_{JC\ (BOT)}$ ..... 3.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.8V to 5.5V
V_{APD} Range ..... 20V to 70V
I_{APD} ..... <2mA
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

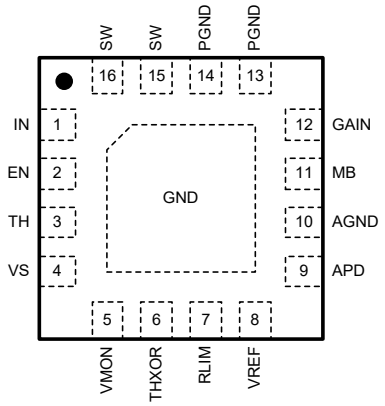
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	IN	P	Power Input to All Internal Circuits. Bypass IN to PGND with a ceramic capacitor of 10μF minimum value.
2	EN	I	Enable Input. Input high to enable this chip, and low to shut down the chip.
3	TH	I	Track or Hold Input. Input high for tracking (when THXOR is logic low; check THXOR description for more detail), where the VMON follows the current output of the APD pin simultaneously. Input low for holding where the VMON outputs a snapshot of APD current captured right after the following edge of the signal applied on the TH pin, in which the APD current snapshot is converted into a voltage and is stored in an internal capacitor.
4	VS	I	Proportional input for programming the MB voltage with an increment gain of 1:30.
5	VMON	O	Current Monitoring Output. Its voltage is proportional to the current of the APD pin.
6	THXOR	I	Logic Input. Effective logic level for selecting the tracking state at the TH input. The complementary logic level to the logic level of the THXOR at the TH is put for tracking.
7	RLIM	I	Current Limit Program Pin. Use an external resistor to set current limit threshold. Connect a resistor from this pin to signal ground.
8	VREF	O	Reference Voltage Output.
9	APD	O	Output for Biasing the APD Device. The current out of this pin is sampled with a mirror circuit for current monitoring and over-current protection.
10	AGND	G	Signal Ground.
11	MB	I	Mirror Bias Input. Connect to the boost stage output. Do not leave it floating.
12	GAIN	I	1×/3× Gain Selection Input. Input low to select 1× gain and high to select 3× gain; where the 1× gain has an equivalent conversion gain of 1.25kΩ and 3.75kΩ for 3× gain.
13, 14	PGND	G	Power Ground. Returns of the C_{IN} and C_{OUT} capacitors should be connected close to this pin. Connect to system ground, exposed pad and AGND together.
15, 16	SW	O	Low End Boost Switch Output. Inductor should be connected between C_{IN} capacitor and this pin, Diode should be connected between this pin and C_{OUT} capacitor. Put inductor and diode as close to this pin as possible to minimize parasitic impedance and thermal resistance.
Exposed Pad	GND	G	Exposed Pad. It is on the bottom side of device and not actually electrically connected to any electrical net. Connect the exposed pad to AGND and PGND using a large copper plane during PCB layout for better thermal performance.

NOTE：I: input, O: output, G: ground, P: power for the circuit.

ELECTRICAL CHARACTERISTICS

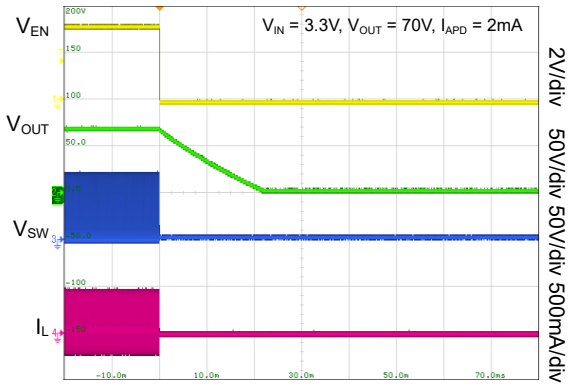
(V_{IN} = 3.3V, T_J = -40℃ to +85℃, typical value are measured at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}		2.8		5.5	V
Efficiency	η	70V, 1mA loading		25		%
Quiescent Current	I_Q			1.4	2	mA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	2.5	2.6	2.76	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}	$V_{EN/UVLO} < V_{SD\_F}$		180		mV
Shutdown Current	I_{SHDN}	V_{SHDN} = 0V		0.01	1	μA
Output Short Circuit Operation Current	I_{SHRT}	V_{OUT} = 40V, R_{LIM} = 28kΩ		80		mA
BOOST and APD Biasing						
Switching Frequency	f_{SW}		750	850	950	kHz
Maximum Duty Cycle	D_{MAX}		88	92	94	%
V_{VS} to V_{MB} Programming Ratio	VPR		29	30	31	V/V
Boost Start-Up Time	t_{UP}	From EN to 90%, 70V output voltage, 1mA load		4		ms
Power Switch On-Resistance	R_{ON}			0.6	1	Ω
Peak Switch Current Limit	I_{LIM_SW}		0.85	1.2	1.55	A
Switch Leakage Current		V_{SW} = 72V		0.02	1	μA
Mirror Voltage Drop	V_{MD}	I_{APD} = 100μA, V_{OUT} = 50V	2.85	3	3.15	V
		I_{APD} = 1mA, V_{OUT} = 50V	2.95	3.1	3.25	V
Current Monitoring						
1× Transfer Resistance	$TR_{1×}$	APD current to VMON transferring ratio, 1× gain	1.18	1.25	1.31	kΩ
3× Transfer Resistance	$TR_{3×}$	APD current to VMON transferring ratio, 3× gain	3.56	3.75	3.93	kΩ
1× Least End -0.5dB Gain Error Point	IM1×	Where the output is -0.5dB off the linear trend line		25		μA
1× Most End 0.5dB Gain Error Point	IM1×	Where the output is 0.5dB off the linear trend line		2.65		mA
Settle Time	t_{ST}	APD to VMON settle time, to 90% for rising and 10% for falling, to 1mA and to 10μA		250		ns
TH Effective Delay	t_{DELAY}	TH to track/hold and 1×/3× effective delay		50		ns
Effective Hold Aperture Window		The time window for effectively holding		3		ns
Holding Droop	V_{DROOP}	Voltage droop measured in 10ms when holding 1V		1		V/s
I_{LIM} Programming Accuracy	I_{LIM_APD}	Test with R_{LIM} = 28kΩ for I_{LIM} = 2.4mA	2	2.4	2.8	mA
VREF Pin						
Reference Voltage	V_{REF}		2.43	2.48	2.54	V
Load Regulation		From 0 to 1mA		0.4	1	%
Temperature Co-efficiency				50		ppm/℃
Logic IO						
Input Low Threshold	V_{IL}				0.4	V
Input High Threshold	V_{IH}		1.6			V
Input Low Souring	I_{LS}	Bias to V_{IL}		0.01	1	μA
Thermal Protection						
Thermal Shutdown Temperature		Temperature rising		150		℃
Thermal Shutdown Hysteresis				15		℃

TYPICAL PERFORMANCE CHARACTERISTICS

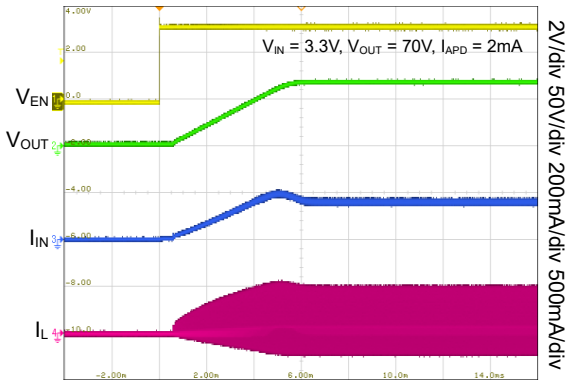
V_{IN} = V_{EN} = 3.3V, V_{OUT} = 70V, T_J = +25℃, unless otherwise noted.

Entering Shutdown



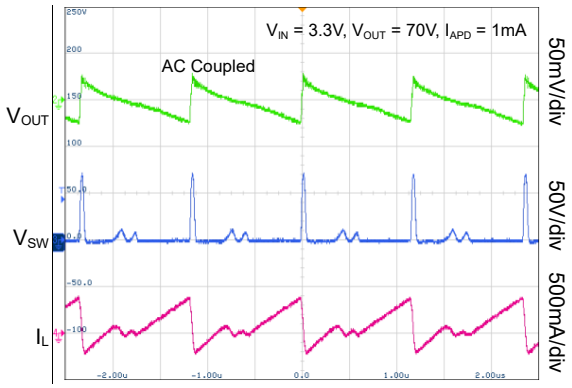
Time (10ms/div)

Exiting Shutdown



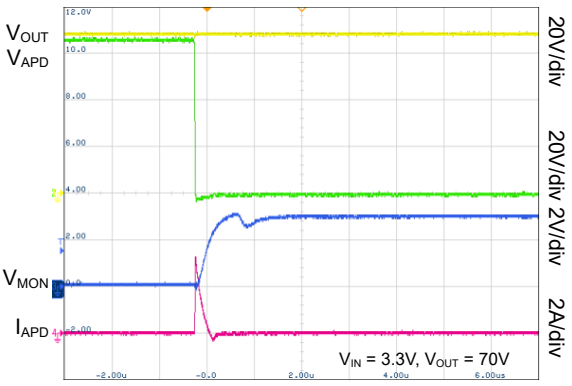
Time (2ms/div)

Steady State



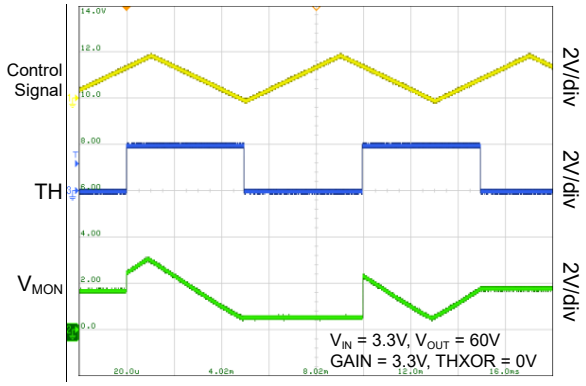
Time (500ns/div)

APD Short-Circuit Response



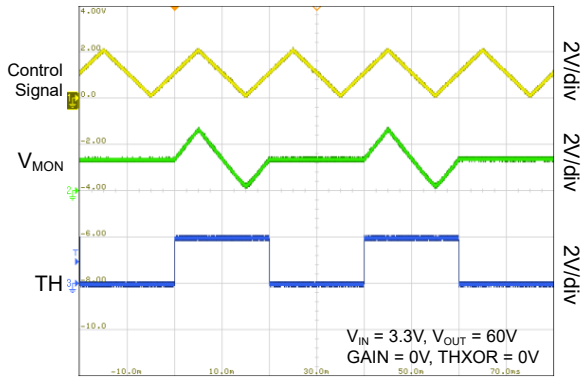
Time (1μs/div)

TH to V_{MON} Timings



Time (2ms/div)

TH to V_{MON} Timings

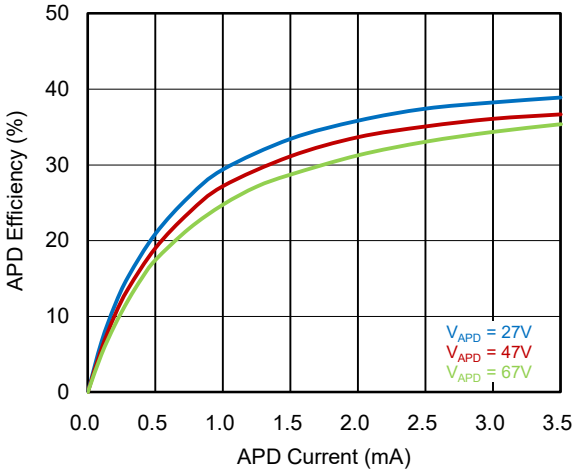


Time (10ms/div)

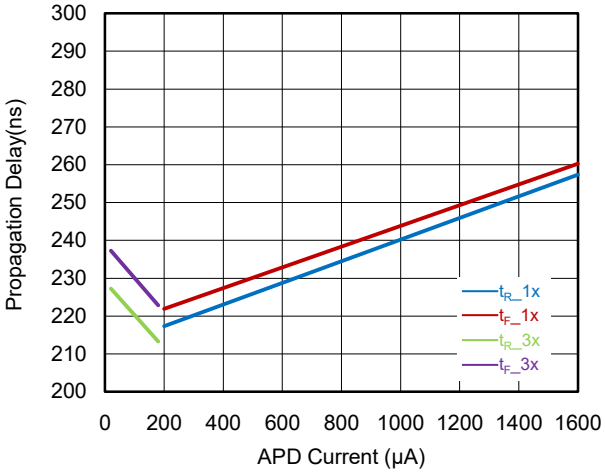
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 70V, T_J = +25℃, unless otherwise noted.

APD Efficiency vs. APD Current



VMON 0.5V Step Propagation Delay vs. DC Offset Current



FUNCTIONAL BLOCK DIAGRAM

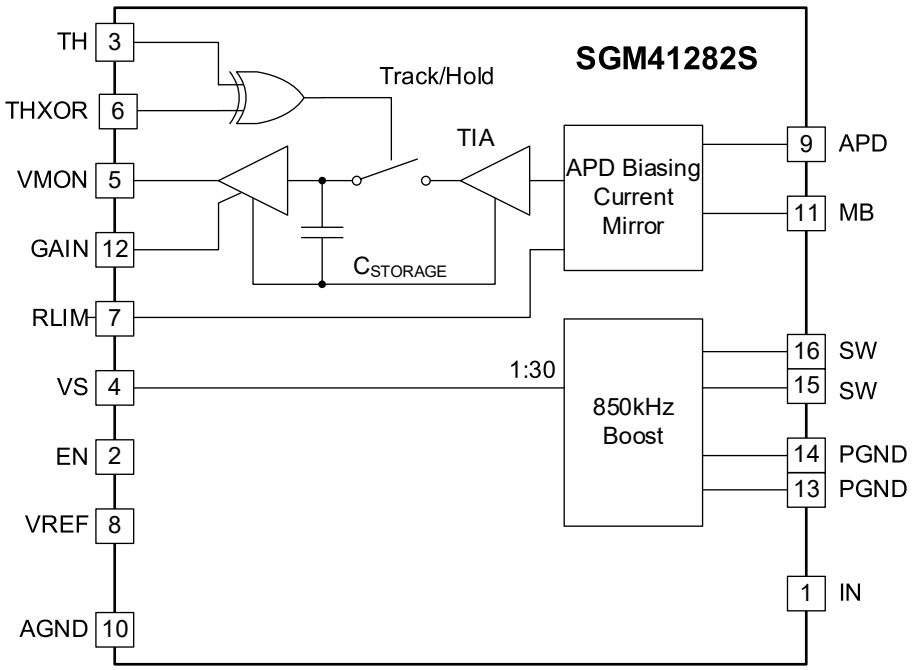


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM41282S is a non-synchronous Boost converter using the constant frequency peak current mode control scheme for high-output voltage application such as APD high voltage biasing.

The SGM41282S operates in discontinuous mode (DCM) to maintain the system stability for high conversion ratio for low input voltage to high output voltage. For DCM, it can eliminate the effect of right-hand zero of Boost converter. Inductor current rises from zero each cycle, there is no accumulation of inductor current when duty cycle is higher than 50%, so it can simplify the need for compensation circuit.

The SGM41282S integrates APD biasing current mirror and trans-impedance amplifier (TIA) function. The TIA converts the mirror current to voltage signal and sends to VMON pin. 1× or 3× current mirror gain can be set by GAIN pin. Track and hold function can be set by XOR logic of THXOR and TH pin.

Enable and Disable

When the EN pin is pulled to high voltage, the SGM41282S is enabled. When the EN pin is pulled to low voltage, the SGM41282S goes into shutdown mode. Less than 1μA input current is consumed in shutdown mode.

APPLICATION INFORMATION

Extending the Monitoring Range

The GAIN pin input is for selecting 1×/3× gains for proper output levels, extending the appreciated monitoring range by 3 times. The gain could be changed during tracking or holding, with less interference injection. As the fiber receiver monitors signal in very high dynamic range but less resolution, this circuit brings out a unique tradeoff between the resolution and dynamic range.

Programming the Current Limit Level

Connect a resistor from RLIM pin to AGND to program the current-limit threshold. The R_{LIM} for setting the current limit level is calculated with the following equation, and please refer to the Figure 3 for the typical I_{LIM} to R_{LIM} plot.

$$R_{LIM}(k\Omega) = \frac{70}{I_{APD\_MAX}} \ (mA)$$

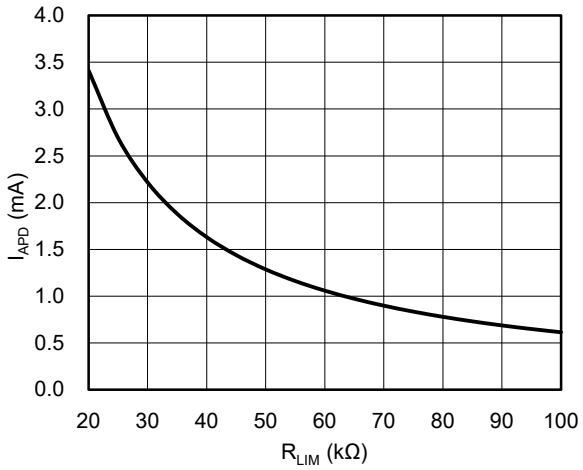


Figure 3. APD Current Limit vs. R_{LIM}

Ripple Filtering

A simple RC filtering circuit could help in suppression of ripple applied at MB input, which then improving the modulation effect to the signal picked-up in the optical channel, which helps in getting better eye diagram opening. Refer to the Figure 4, the resistance of the R inserts drop to be compensated.

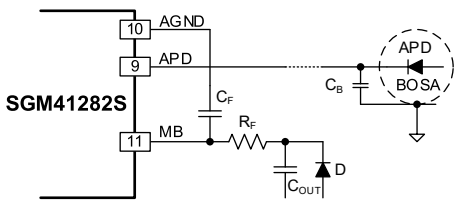


Figure 4. An RC Filtering for Ripple Suppression

Burst Pulse Response

The Figure 5 shows the capture of waveform at the VMON pin in tracking mode, where a train of current pulses with two different peak values is applied to the APD output, representing the case of burst pulse receiving.

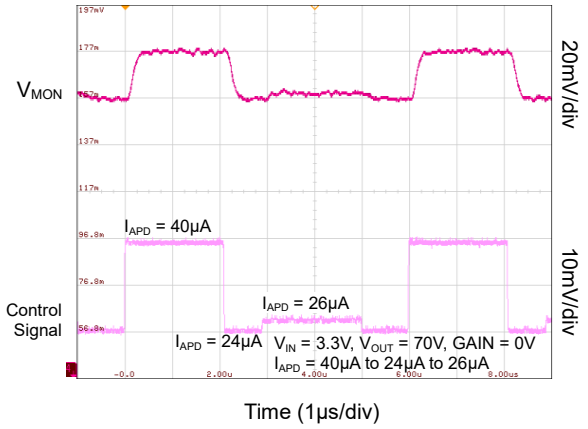


Figure 5. Burst Pulse Receiving Waveform

Backward Scattering

Careful layout of the circuit optimization is desired for assuring fast transient measurement to APD current. Illustrative circuit is showed in the Figure 6, which shows necessary layout considerations. The C_B is low loss capacitor installed in the TO-can in a BOSA, which holds the potential applied on the APD, and the C_B should be evaluated on the final PCB, or , it will slow down the settling time of the monitoring output at the VMON besides the intrinsic propagation and settling of the SGM41282S.

APPLICATION INFORMATION (continued)

The d and the c placed close to the ADC input are for ringing dump, which occurs when the ADC input switch cuts for holding. These two components do not affect the transient, but induce interference to the measurement. Those components should also be evaluated on the final PCB. The recommended values of d and c are 10kΩ and 22pF.

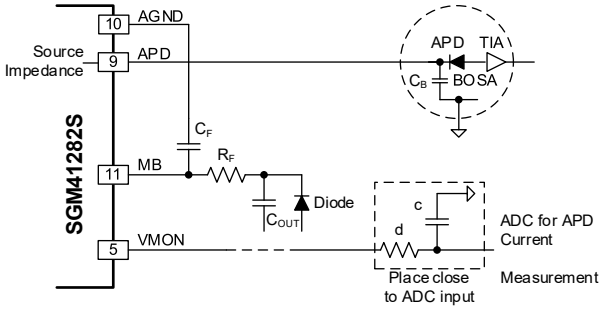


Figure 6. Illustration Circuit

External Components Selection

As the boost circuit works at about 850kHz, capacitors with good high frequency performance are needed for the application circuit. As the storage capacitor (the C_{OUT} in the Figure 1 or the Figure 2) works under high bias voltage, please refer to the capacitor's datasheet to assure its effective capacitance is more than 0.1μF at the output voltage.

Table 1. Key Components Selection Reference

L (μH)	Diode (Schottky Small Signal)	C_{OUT} (μF 100V)	C_{IN} (μF)	R_F (Ω)	C_F (μF 100V)	C_{REF} (nF)
4.7	BAT46W	0.1	10	100	0.1	470

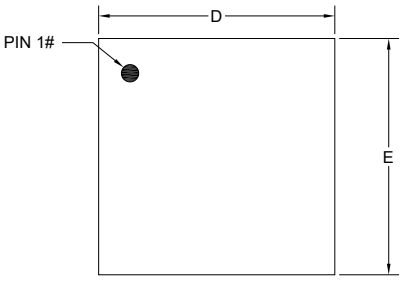
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

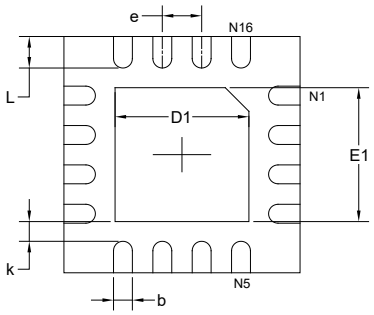
Changes from Original (OCTOBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

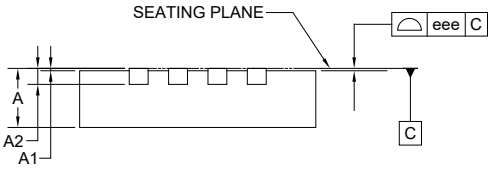
TQFN-3×3-16L



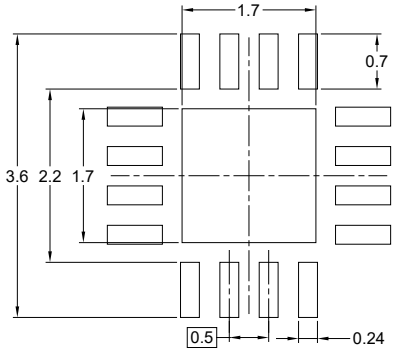
TOP VIEW



BOTTOM VIEW



SIDE VIEW



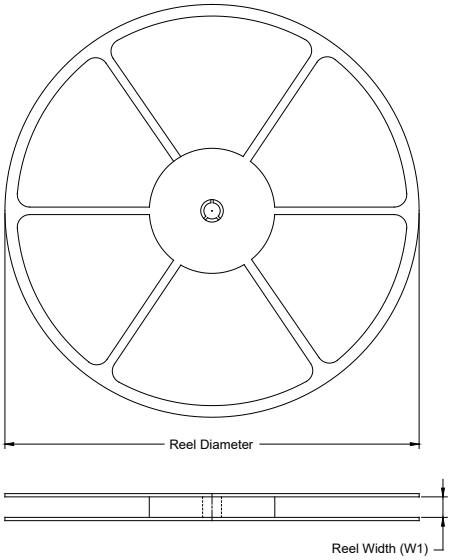
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020
eee	0.080		0.003	

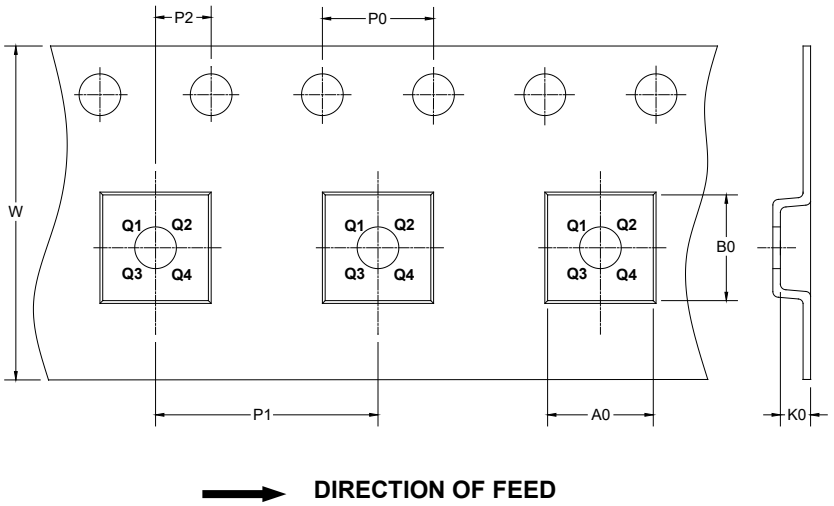
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



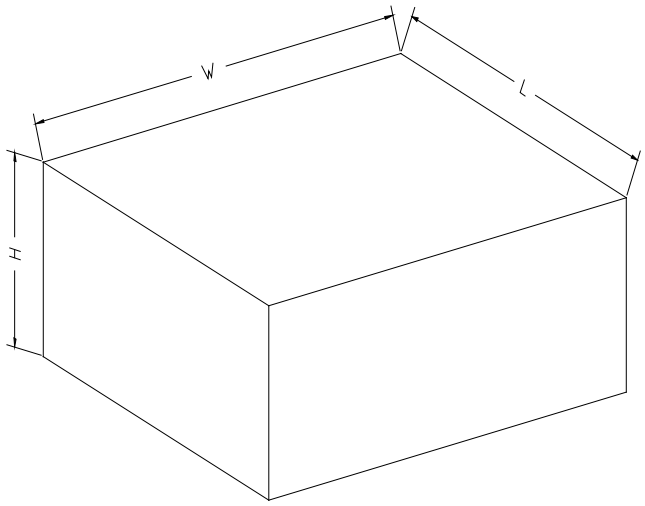
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002