SGM51613S8
8-Channel, 16-Bit, Bipolar Input Simultaneous Sampling ADC

GENERAL DESCRIPTION

The SGM51613S8 is a 16-bit, 8-channel simultaneous sampling, high-precision successive approximation (SAR) analog-to-digital converter (ADC).

This ADC is powered by a single unipolar 5V, and supports true bipolar ±10V and ±5V inputs. The input range is configured by hardware pin.

The chip provides over-voltage protection up to ±20V at the input.

The chip has an on-chip high accuracy and low drift 8ppm/℃ reference.

The input impedance of the chip is 1MΩ and it is independent of the input range selection.

The ADC supports both high-speed serial and parallel interfaces.

The SGM51613S8 is available in a Green LQFP-10×10-64L package. It is specified from -40℃ to +125℃.

FEATURES

- **8 Channels Simultaneous Sampling**
  - **Support 800kSPS on All Channels Simultaneously**
- **True Bipolar Analog Input Ranges: ±10V, ±5V**
- **Single 5V Analog Supply and 2.7V to 5V V_{DRIVE}**
- **Input Buffer with 1MΩ Analog Input Impedance**
- **On-Chip Accurate Reference and Reference Buffer**
- **Configurable Oversampling Capability with Digital Filter**
- **Flexible Parallel Interface or Serial Interface**
  - **SPI-Compatible**
- **Performance**
  - **SNR: 87.4dB (TYP)**
  - **THD: -96dB (TYP)**
  - **INL: ±2.5LSB (TYP)**
  - **DNL: +1.8LSB/-0.85LSB (TYP)**
  - **7kV ESD Rating on Analog Input Channels**
- **Operating Temperature Range: -40℃ to +125℃**
- **Available in a Green LQFP-10×10-64L Package**

APPLICATIONS

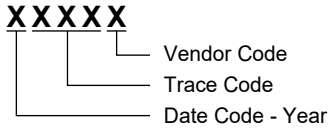
Power-Line Monitoring and Protection Systems
Instrumentation and Control Systems
Multi-Axis Sensor Systems

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM51613S8	LQFP-10×10-64L	-40℃ to +125℃	SGM51613S8XLFH64G/TR	SGM51613S8 XLFH64 XXXXX	Tape and Reel, 1500
			SGM51613S8XLFH64SG/TR	SGM51613S8 XLFH64 XXXXX	Tape and Reel, 250

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

AV_{CC} to AGND ..... -0.3V to 6V
V_{DRIVE} to AGND ..... -0.3V to AV_{CC} + 0.3V
Analog Input Voltage to AGND (1) ..... ±20V
Digital Input Voltage to AGND ..... -0.3V to V_{DRIVE} + 0.3V
Digital Output Voltage to AGND ..... -0.3V to V_{DRIVE} + 0.3V
REFIN to AGND ..... -0.3V to AV_{CC} + 0.3V
Input Current to Any Pin except Supplies (1) ..... ±10mA
Package Thermal Resistance
LQFP-10×10-64L, θ_{JA} ..... 42.2℃/W
LQFP-10×10-64L, θ_{JB} ..... 23.2℃/W
LQFP-10×10-64L, θ_{JC} ..... 8.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM (Analog Input Pins Only) 7000V
HBM (All Pins except Analog Inputs) 3000V
CDM 1000V

NOTE:

1. Transient currents of up to 100mA do not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

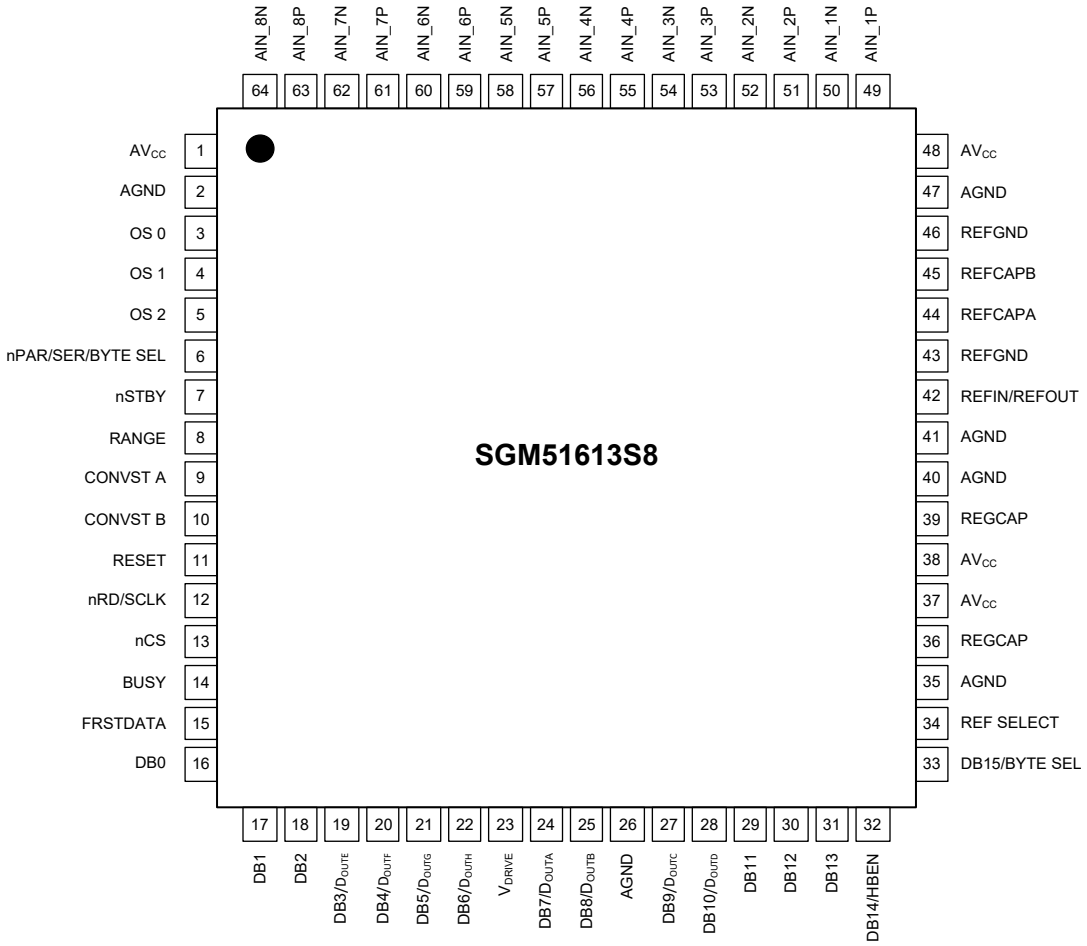
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



LQFP-10×10-64L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1, 37, 38, 48	AV_{CC}	P	Analog Power Supply Pin. It is the power supply of analog front end and ADC core circuit.
2, 26, 35, 40, 41, 47	AGND	P	Analog Ground Pin. All AGND pins must share the same system connection plane.
3	OS 0	DI	Oversampling Mode Setting Pins. They are logic input control pins. More details please refer to Table 4.
4	OS 1		
5	OS 2		
6	nPAR/SER/ BYTE SEL	DI	Parallel/Serial/Byte Interface Setting Pin. It is a logic input. If it is set to logic low, the parallel interface is enabled. If it is set to logic high, the serial interface is enabled. To select byte parallel interface, set the pin and DB15/BYTE SEL pin to logic high at the same time for a combined enable controlling (refer to Table 3). If the chip works in serial mode, the nRD/SCLK pin is the serial interface clock input pin. The DB7/D_{OUTA} pin and DB8/D_{OUTB} pin are combined together as two lane serial interface data output pins. The DB[15:9] and DB[6:0] pins should be connected to GND. If the chip works in byte parallel interface mode, DB14 is used as the HBEN pin. DB[7:0] is read out in two nRD read frame. The data format is high byte first.
7	nSTBY	DI	Standby Mode Setting Input Pin. This pin is a logic input pin. It works with the RANGE pin together to determine whether the chip is going to enter standby mode or shutdown mode. More details please refer to Table 2.
8	RANGE	DI	Analog Input Range Setting Pin. This pin is a logic input pin. If it is set to logic high, the analog input range ±10V is set for all channels. If it is set to logic low, the analog input range ±5V is set for all channels. Any change on the logic of the input range setting pin takes effect immediately. It is strongly not recommended to change the input range during a conversion or a consequences inputs scanning.
9	CONVST A	DI	Conversion Start Input Pin A and Conversion Start Input Pin B. They are logic input pins. When the input logic from low to high, the input tracking and holding circuitry stops sampling and changes to hold, and the ADC initiates a conversion. CONVST A and CONVST B can be tied together for all channels sampling simultaneously. When the oversampling function is not enabled, CONVST A and CONVST B can be used to control ADC conversion separately. CONVST A can be used to control channel V1, V2, V3 and V4. CONVST B can be used to control channel V5, V6, V7 and V8.
10	CONVST B		
11	RESET	DI	Reset Input Pin. An input from logic low to logic high, the rising edge of the input signal triggers the reset action, and the high pulse must be held at least 50ns. Reset input will terminate the ongoing ADC conversion. And the reset input also will set the ADC output registers to all zero.
12	nRD/SCLK	DI	Multi-Function Pin nRD/SCLK. When the chip is in parallel interface mode, the nRD/SCLK is active logic low. When the chip is in serial interface mode, the nRD/SCLK is active logic low. The data on data bus are locked out on the rising edge of SCLK. For more information, see the Conversion Control section.
13	nCS	DI	Chip Select Control Pin. This pin is active logic low. In serial interface mode, the nCS is used as data frame signal, and the MSB of the serial output is shifted out on the falling edge of nCS.
14	BUSY	DO	Busy Indicator Output Pin. If there is a trigger rising edge of CONVST A or CONVST B, this BUSY pin goes to high immediately. It does not go to low until all the channels conversions have been completed. The falling edge of the BUSY pin indicates that the conversion results are ready to read (it needs a reasonable time delay t_4). Any data read operation must be finished before the next falling edge of BUSY coming. During the high of BUSY, any ADC trigger signals of CONVST A and CONVST B are ignored.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
15	FRSTDATA	DO	Digital Indicator Output Pin. This pin is active high. In parallel interface mode, the falling edge of nRD which is corresponded to read V1 channel sets the FRSTDATA pin high, and the next following edge of nRD sets the FRSTDATA pin low. In serial interface mode, the falling edge of nCS sets the FRSTDATA pin high. In the same read operation frame, the 16th SCLK falling edge sets the FRSTDATA pin low. If nCS is high, the FRSTDATA pin is in three-state.
16, 17, 18	DB0, DB1, DB2	DO	Parallel Interface Output Data Bits. In serial interface mode, these pins should be connected to AGND.
19	DB3/D_{OUTE}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 3 (DB3)/Serial Interface Data Output Pin (D_{OUTE}). In parallel interface mode, this pin works as DB3. In serial interface mode, this pin works as D_{OUTE}.
20	DB4/D_{OUTF}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 4 (DB4)/Serial Interface Data Output Pin (D_{OUTF}). In parallel interface mode, this pin works as DB4. In serial interface mode, this pin works as D_{OUTF}.
21	DB5/D_{OUTG}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 5 (DB5)/Serial Interface Data Output Pin (D_{OUTG}). In parallel interface mode, this pin works as DB5. In serial interface mode, this pin works as D_{OUTG}.
22	DB6/D_{OUTH}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 6 (DB6)/Serial Interface Data Output Pin (D_{OUTH}). In parallel interface mode, this pin works as DB6. In serial interface mode, this pin works as D_{OUTH}.
23	V_{DRIVE}	P	Login Interface Power Supply Pin.
24	DB7/D_{OUTA}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 7 (DB7)/Serial Interface Data Output Pin (D_{OUTA}). In parallel interface mode, this pin works as DB7. In serial interface mode, this pin works as D_{OUTA}.
25	DB8/D_{OUTB}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 8 (DB8)/Serial Interface Data Output Pin (D_{OUTB}). In parallel interface mode, this pin works as DB8. In serial interface mode, this pin works as D_{OUTB}.
27	DB9/D_{OUTC}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 9 (DB9)/Serial Interface Data Output Pin (D_{OUTC}). In parallel interface mode, this pin works as DB9. In serial interface mode, this pin works as D_{OUTC}.
28	DB10/D_{OUTD}	DO	Multi-Function Pin, Parallel Interface Output Data Bit 10 (DB10)/Serial Interface Data Output Pin (D_{OUTD}). In parallel interface mode, this pin works as DB10. In serial interface mode, this pin works as D_{OUTD}.
29, 30, 31	DB11, DB12, DB13	DO	Parallel Interface Output Data Bits. In byte parallel interface mode and serial interface mode (nPAR/SER/BYTE SEL = 1), these pins should be connected to AGND.

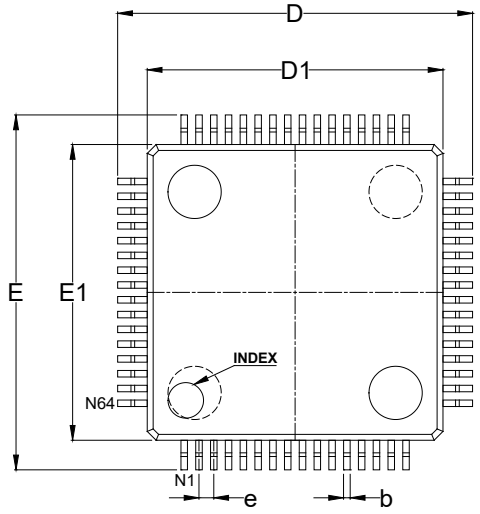
PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
32	DB14/HBEN	DO/DI	Multi-Function Pin, Parallel Interface Output Data Bit 14 (DB14)/High Byte Enable (HBEN). In parallel interface mode, this pin works as DB14. In parallel byte interface mode, this pin is used to select if the most significant byte (MSB) or the least significant byte (LSB) of the data is output first. If HBEN is set to high, MSB is output first. If HBEN is set to low, LSB is output first. In serial mode, this pin should be tied to GND.
33	DB15/ BYTE SEL	DO/DI	Multi-Function Pin, Parallel Interface Output Data Bit 15 (DB15)/Parallel Interface Byte Mode Select (BYTE SEL). In parallel interface mode, this pin works as DB15. If nPAR/SER/BYTE SEL is set to high and DB15/BYTE SEL is set to low, the chip works in serial interface mode. If nPAR/SER/BYTE SEL is set to high and DB15/BYTE SEL is set to high, the chip works in parallel byte interface mode.
34	REF SELECT	DI	Internal/External Reference Selection Pin. This is a logic input pin. If it is set to logic high, the internal reference is enabled. If it is set to logic low, an external reference must be connected to the chip.
36, 39	REGCAP	P	Internal Regulator Decoupling Pins. Each pin needs a separate 1μF decoupling capacitor connected to AGND.
42	REFIN/REFOUT	REF	Reference Input Pin (REFIN)/Reference Output Pin (REFOUT). A 10μF decoupling capacitor needs to be connected between this pin and REFGND.
43, 46	REFGND	REF	Reference Ground Pins. These pins should be connected to AGND.
44, 45	REFCAPA, REFCAPB	REF	Reference Buffer Output Sense Pins. These pins must be tied together. A 10μF decoupling capacitor needs to be connected between these pins and AGND.
49	AIN_1P	AI	Channel 1 Positive Analog Input.
50	AIN_1N	AI	Channel 1 Negative Analog Input.
51	AIN_2P	AI	Channel 2 Positive Analog Input.
52	AIN_2N	AI	Channel 2 Negative Analog Input.
53	AIN_3P	AI	Channel 3 Positive Analog Input.
54	AIN_3N	AI	Channel 3 Negative Analog Input.
55	AIN_4P	AI	Channel 4 Positive Analog Input.
56	AIN_4N	AI	Channel 4 Negative Analog Input.
57	AIN_5P	AI	Channel 5 Positive Analog Input.
58	AIN_5N	AI	Channel 5 Negative Analog Input.
59	AIN_6P	AI	Channel 6 Positive Analog Input.
60	AIN_6N	AI	Channel 6 Negative Analog Input.
61	AIN_7P	AI	Channel 7 Positive Analog Input.
62	AIN_7N	AI	Channel 7 Negative Analog Input.
63	AIN_8P	AI	Channel 8 Positive Analog Input.
64	AIN_8N	AI	Channel 8 Negative Analog Input.

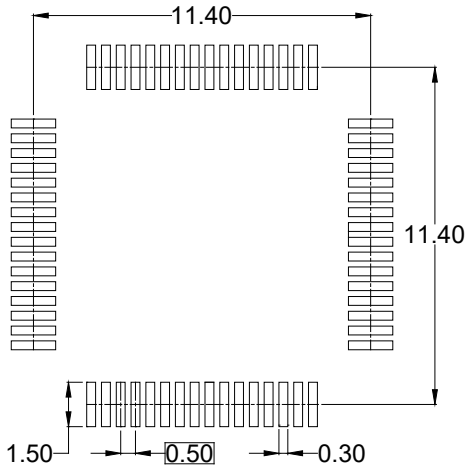
NOTE: P = power supply, DI = digital input, DO = digital output, REF = reference input/output, AI = analog input.

PACKAGE OUTLINE DIMENSIONS

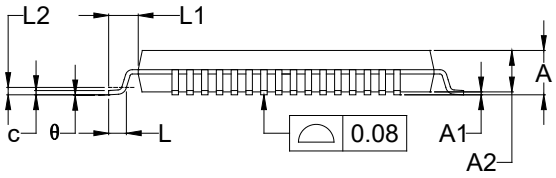
LQFP-10×10-64L



TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



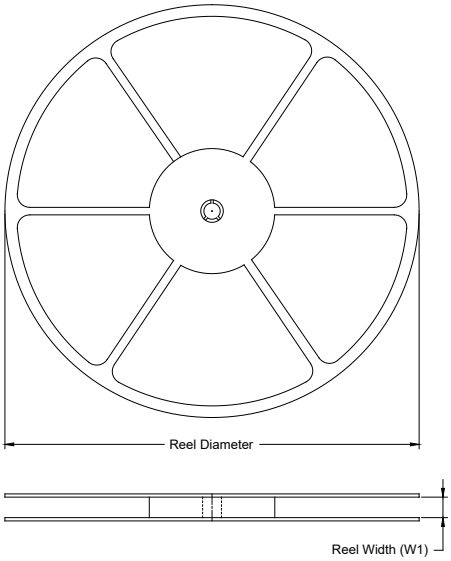
SIDE VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.170	-	0.270
c	0.090	-	0.200
D	11.800	-	12.200
D1	9.900	-	10.100
E	11.800	-	12.200
E1	9.900	-	10.100
e	0.500 BSC		
L	0.450	-	0.750
L1	1.000 REF		
L2	0.250 BSC		
θ	0°	-	7°

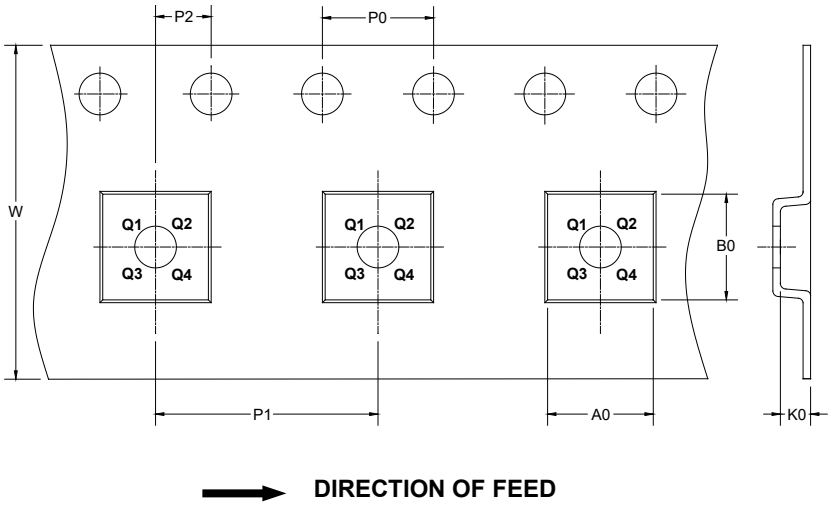
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MS-026.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



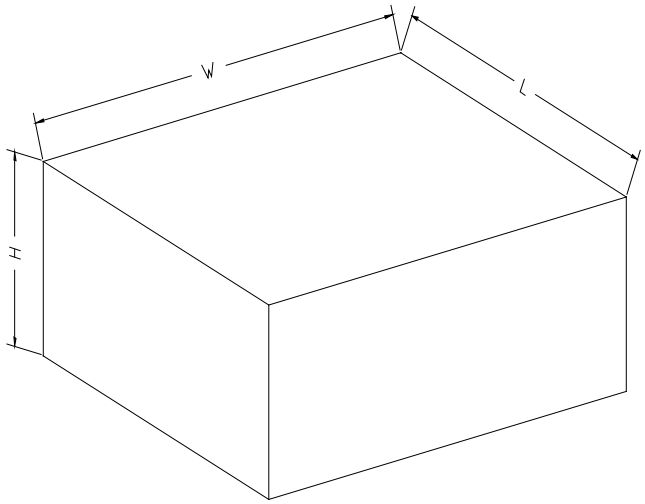
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
LQFP-10×10-64L	13″	24.4	12.5	12.5	2.05	4.0	16.0	2.0	24.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002