SGM41510

I²C Controlled 5A Single-Cell Fast Charger with High Input Voltage and Adjustable Voltage USB On-the-Go Boost Mode

FEATURES

- High Efficiency, 1.5MHz, Synchronous Buck Charger
  - 93.5% Charge Efficiency at 1A Charge Current
  - 92.5% Charge Efficiency at 2A Charge Current
  - 90.8% Charge Efficiency at 3A Charge Current
  - PFM Mode for Light Load Efficiency
- USB On-The-Go (OTG) Support (Boost Mode)
  - Boost Converter with up to 2.4A (Default) Output
  - Boost Efficiency of 94% at 5V/1A Output
  - Accurate Hiccup Mode Over-Current Protection
  - Soft-Start Capable with up to 500μF Capacitive Load
  - Output Short Circuit Protection
  - Selectable PFM Mode for Light Load Operations
- Single Input for USB or High Voltage Adapters
  - 3.9V to 14V Operating Input Voltage Range
  - 20V Absolute Maximum Input Voltage Rating
  - Programmable Input Current Limit and Dynamic Power Management (IINLIM, 100mA to 4.9A with 100mA Resolution) to Support USB 2.0 and USB 3.0 Standards and High Voltage Adaptors
  - Maximum Power Tracking by Input Voltage Limit up to 15.3V (VINDPM)
  - VINDPM Tracking of Battery Voltage
- Resistance Compensation (IRCOMP) Function
- High Battery Discharge Efficiency with 15mΩ Switch
- Narrow Voltage DC (NVDC) Power Path Management
  - Instant-On with No or Highly Depleted Battery
  - Ideal Diode Operation in Battery Supplement Mode
- Ship Mode, Wake-Up and Full System Reset Capability by Battery FET Control
- Flexible Autonomous and I²C Operation Modes for Optimal System Performance
- Fully Integrated Switches, Current Sense and Compensation
- 10μA Ship Mode Low Battery Leakage Current
- High Accuracy
  - ±0.5% Charge Voltage Regulation
- Safety
  - Thermal Regulation and Thermal Shutdown
  - Input Under-Voltage Lockout (UVLO)
  - Input Over-Voltage (ACOV) Protection

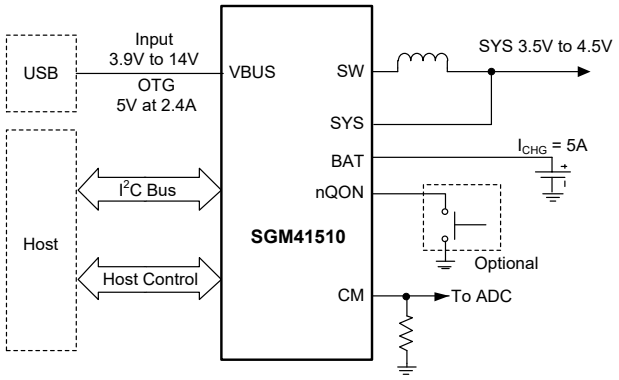
APPLICATIONS

Tablet PC

Smart Phones, EPOS

Portable Internet Devices and Accessory

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION

The SGM41510 is a battery charger and system power path management device with integrated converter and power switches for use with single-cell Li-Ion or Li-polymer batteries. This highly integrated 5A device is capable of fast charging and supports up to 14V input voltage suitable for smart phones, tablets and portable systems. During discharging phase, the low impedance power path optimizes the efficiency and reduces the battery charging time. It integrates resistance compensation (IRCOMP) to deliver maximum charging power to battery. I^2C programming makes it a very flexible powering and charger design solution.

The device includes four main power switches: input reverse blocking FET (RBFET, Q1), high-side switching FET for buck or boost mode (HSFET, Q2), low-side switching FET for buck or boost mode switching (LSFET, Q3) and battery FET that controls the interconnection of the system and battery (BATFET, Q4). The bootstrap diode for the high-side gate driving is also integrated. The internal power path has a very low impedance that reduces the charging time and maximizes the battery discharge efficiency. Moreover, the input voltage and current regulations provide maximum charging power delivery to the battery with various types of input sources.

The device also meets USB On-The-Go (OTG) operation power rating specification by supplying 5V (adjustable 4.5V to 5.5V) on VBUS pin with a default current limit of 2.4A (adjustable 1.2A to 4A).

The system voltage is regulated slightly above the battery voltage by the power path management circuit and is kept above the programmable minimum system voltage (3.5V by default). Therefore, system power is maintained even if the battery is completely depleted or removed. Dynamic power management (DPM) feature is also included that automatically reduces the charge current if the input current or voltage limit is reached. If the system load continues to increase after reduction of charge current down to zero, the power path management provides the deficit from battery by discharging battery to the system until the system power demand is fulfilled. This is called supplement mode, which prevents the input source from overloading.

Starting and termination of a charging cycle can be accomplished without software control. The sensed battery voltage is used to decide for starting phase of charging in one of the three phases of charging cycle: pre-conditioning, constant current or constant voltage. When the charge current falls below a preset limit and the battery voltage is above recharge threshold, the charger function will automatically terminate and end the charging cycle. If the voltage of a charged battery falls below the recharge threshold, the charger starts another charging cycle.

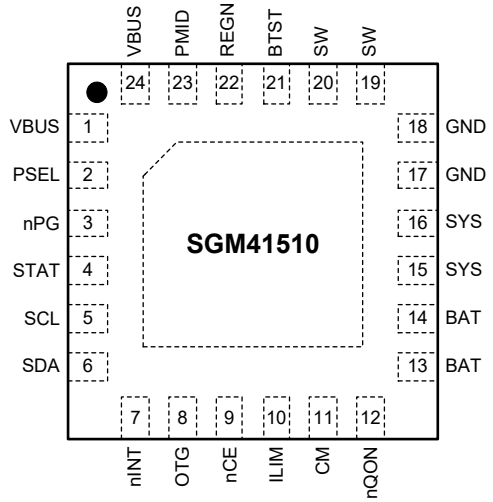
Several safety features are provided in the SGM41510 such as over-voltage and over-current protections, charging safety timing, thermal shutdown and input UVLO. This device also features thermal regulation in which the charge current is reduced if the junction temperature exceeds 120℃ (selectable).

Charging status is reported by the STAT output and fault/status bits. A negative pulse is sent to the nINT output pin as soon as a fault occurs to notify the host. BATFET reset control is provided by nQON pin to exit ship mode or for a full system reset.

The device is available in a Green TQFN-4×4-24L package.

PIN CONFIGURATION

(TOP VIEW)



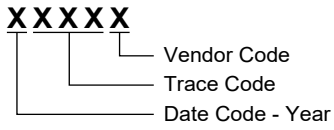
TQFN-4×4-24L

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41510	TQFN-4×4-24L	-40℃ to +85℃	SGM41510YTQF24G/TR	SGM41510 YTQF24 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- VBUS (Converter not Switching) ..... -2V to 20V (1)
- BTST, PMID (Converter not Switching) ..... -0.3V to 20V
- SW ..... -2V to 16V
- SW (Peak for 10ns Duration) ..... -3V to 18V
- BTST to SW ..... -0.3V to 6V
- REGN, nCE, nPG, BAT, SYS (Converter not Switching) ..... -0.3V to 6V
- PSEL, SDA, SCL, nINT, nQON, STAT OTG, CM ..... -0.3V to 6V
- ILIM ..... -0.3V to 5V

Output Sink Current
- STAT 6mA
- nPG 6mA
- nINT 6mA

Package Thermal Resistance
- TQFN-4×4-24L, θ_{JA} ..... 37℃/W
- TQFN-4×4-24L, θ_{JC} ..... 24℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

NOTE: 1. Maximum 28V for 10 seconds.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{VBUS} ..... 3.9V to 14V
Input Current (VBUS), I_{IN} ..... 4.9A (MAX)
Output DC Current (SW), I_{SWOP} ..... 5A (MAX)
Battery Voltage, V_{BATOP} ..... 4.608V (MAX)
Fast Charging Current, I_{BATOP} ..... 5A (MAX)
Discharging Current (Continuous), I_{BATOP} ..... 6A (MAX)
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1, 24	VBUS	P	Charger Input (V_{IN}). The internal N-channel reverse blocking MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1μF ceramic capacitor from VBUS pin to GND close to the device.
2	PSEL	DI	Power Source Selection Input. An adapter source: low. A USB host source: high.
3	nPG	DO	Open-Drain Active Low Input Power Good Indicator. Use a 10kΩ pull-up to the logic high rail. A low state indicates a good input (UVLO < V_{VBUS} < ACOV, and above sleep mode threshold, I_{LIM} > 30mA).
4	STAT	DO	Open-Drain Charge Status Output. Use a 10kΩ pull-up to the logic high rail (or an LED + a resistor). The STAT pin acts as follows: During charge: low (LED ON). Charge completed or charger in sleep mode: high (LED OFF). Charge suspended (in response to a fault): 1Hz, 50% duty cycle pulses (LED BLINKS). The function can be disabled via STAT_DIS bit.
5	SCL	DI	I^2C Clock Signal. Use a 10kΩ pull-up to the logic high rail.
6	SDA	DIO	I^2C Data Signal. Use a 10kΩ pull-up to the logic high rail.
7	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. The nINT pin is active low and sends a negative 256μs pulse to inform host about a new charger status update or a fault.
8	OTG	DI	Boost Mode Enable Input Pin (Active High). The boost mode is activated when OTG_CONFIG bit is 1, OTG pin is pulled high, and no input source is detected at VBUS.
9	nCE	DI	Charge Enable Input Pin (Active Low). Battery charging is enabled when CHG_CONFIG bit is 1 and nCE pin is pulled low. The nCE pin must be pulled high or low.
10	ILIM	AI	Input Current Limit Input. ILIM pin sets the maximum input current and can be used to monitor input current. The ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 0.8V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{INMAX} = K_{ILIM}/R_{ILIM}$. The actual input current limit is the lower limit set by ILIM pin (when BAT_LOADEN bit is 1) or IINLIM[5:0] register. Input current limit of less than 500mA is not support on ILIM pin. The ILIM pin can also be used to monitor input current when the voltage is below 0.8V. The input current is proportional to the voltage on ILIM pin and can be calculated by $I_{IN} = (K_{ILIM} \times V_{ILIM})/(R_{ILIM} \times 0.8)$. The ILIM pin function can be disabled when EN_ILIM bit is 0.
11	CM	AO	Current Monitor Output. 1/40000 sampling of input current, charge current or discharge current. 1/40000 sampling of BAT current with 160μA DC offset. 1/2 sampling of BAT voltage or SYS voltage. 1/10 sampling of VBUS voltage. The sampling function is determined by CM_OUT[2:0] register. Connect this pin to an ADC interface of the host.
12	nQON	DI	BATFET Enable/Reset Control Input. Use an internal pull-up to a small voltage for maintaining the default high logic (whenever a source or battery is available). In the ship mode, the BATFET is off. To exit ship mode and turn BATFET on, a logic low pulse with a duration of $t_{SHIPMODE}$ (1s TYP) can be applied to nQON. When VBUS source is not connected, a logic low pulse with a duration of t_{QON_RST} (16s TYP) resets the system power (SYS) by turning BATFET off for t_{BATFET_RST} (250ms TYP) and then back on to provide a full power reset for system.
13, 14	BAT	P	Battery Positive Terminal Pin. Use a 10μF capacitor between BAT and GND pins close to the device. SYS and BAT pins are internally connected by BATFET with current sensing capability.
15, 16	SYS	P	Connection Point to Converter Output. SYS connects to the converter LC filter output that powers the system. BAT to SYS internal current (power from battery to system) is sensed. Connect a 20μF capacitor between SYS pin and GND close to the device (in addition to C_{OUT}).
17, 18	GND	—	Ground Pin of the Device.
19, 20	SW	P	Switching Node Output. Connect SW pin to the output inductor. Connect a 47nF bootstrap capacitor from SW pin to BTST pin.
21	BTST	P	High-side Driver Positive Supply. It is internally connected to the boost-strap diode cathode. Use a 47nF ceramic capacitor from SW pin to BTST pin.
22	REGN	P	LDO Output that Powers LSFET Driver and Internal Circuits. Internally, the REGN pin is connected to the anode of the bootstrap diode. Connect a 4.7μF (10V rating) ceramic capacitor from REGN pin to GND. The capacitor should be placed close to the IC. The output is typically 4.5V to 5V.
23	PMID	DO	PMID Pin. PMID is the actual higher voltage port of converter (buck or boost) and is connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Connect an 8.2μF ceramic capacitor from PMID pin to GND. It is the proper point for decoupling of high frequency switching currents.
Exposed Pad	—	P	Thermal Pad and Ground Reference. It is the ground reference for the device and also the thermal pad to conduct heat from the device (not suitable for high current return). Tie externally to the PCB ground plane (GND). Thermal vias under the pad are needed to conduct the heat to the PCB ground planes.

NOTE:

1. AI = Analog Input, AO = Analog Output, AIO = Analog Input and Output, DI = Digital Input, DO = Digital Output, DIO = Digital Input and Output, P = Power.

ELECTRICAL CHARACTERISTICS

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, Full = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Quiescent Currents							
Battery Discharge Current (BAT, SW, SYS) in Buck Mode	$I_{BAT\_VBUS\_lkg}$	V_{BAT} = 4.2V, V_{VBUS} < V_{VBUS_UVLOZ}, leakage between BAT and VBUS, BATFET in on-state	Full		0.1	1	μA
Battery Discharge Current (BAT) in Buck Mode	I_{BAT}	HIZ mode, no VBUS, BATFET disabled (BATFET_DIS = 1), battery monitor disabled	Full		10	20	
Battery Discharge Current (BAT, SW, SYS)	I_{BAT}	V_{BAT} = 4.5V, HIZ mode, no VBUS, BATFET enabled (BATFET_DIS = 0), battery monitor disabled	Full		20	40	
Input Supply Current (VBUS) in Buck Mode when HIZ Mode is Enabled	I_{VBUS_HIZ}	V_{VBUS} = 5V, HIZ mode, no battery, battery monitor disabled	Full		25	40	μA
		V_{VBUS} = 12V, HIZ mode, no battery, battery monitor disabled	Full		50	70	
Input Supply Current (VBUS) in Buck Mode	I_{VBUS}	V_{VBUS} > V_{VBUS_UVLOZ}, V_{VBUS} > V_{BAT}, converter not switching	Full		1.7	3	mA
		V_{BAT} = 3.2V, I_{SYS} = 0A, V_{VBUS} > V_{BAT}, V_{VBUS} > V_{VBUS_UVLOZ}, converter switching	+25℃		3		
		V_{BAT} = 3.8V, I_{SYS} = 0A, V_{BUS} > V_{BAT}, V_{VBUS} > V_{VBUS_UVLOZ}, converter switching	+25℃		3		
Battery Discharge Current in Boost Mode	I_{BOOST}	V_{BAT} = 4.2V, I_{VBUS} = 0A, converter switching	+25℃		5		mA
VBUS Pin and BAT Pin Power-Up							
VBUS Operating Range	V_{VBUS_OP}	V_{VBUS} rising	Full	3.9		14	V
VBUS UVLO to Have Active I²C (with No Battery)	V_{VBUS_UVLOZ}		Full	3.6			V
Sleep Mode Falling Threshold	V_{SLEEP}		+25℃	15	70	125	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}		+25℃	150	200	260	mV
VBUS Over-Voltage Rising Threshold	V_{ACOV_RISE}		Full	14.6	15.2	15.8	V
VBUS Over-Voltage Falling Threshold	V_{ACOV_FALL}		Full	14	14.7	15.4	V
BAT Voltage to Have Active I²C (No Source on VBUS)	V_{BAT_UVLOZ}	V_{BAT} rising	Full	2.65			V
BAT Depletion Falling Threshold	$V_{BAT\_DPL\_FALL}$	V_{BAT} falling	Full	2.05	2.25	2.45	V
BAT Depletion Rising Threshold	$V_{BAT\_DPL\_RISE}$	V_{BAT} rising	Full	2.2	2.5	2.75	V
Bad Adapter Detection Threshold	$V_{VBUSMIN}$		+25℃		3.75		V
Bad Adapter Detection Current (Internal Current Source)	I_{BAD_SRC}	Source current from VBUS to GND	+25℃		30		mA
Power Path Management							
System Regulation Voltage	V_{SYS}	I_{SYS} = 0A, V_{BAT} > V_{SYS_MIN}, BATFET_DIS = 1	+25℃		V_{BAT} + 50mV		V
		I_{SYS} = 0A, V_{BAT} < V_{SYS_MIN}, BATFET_DIS = 1	+25℃		V_{SYS_MIN} + 150mV		
Minimum DC System Voltage Output	V_{SYS_MIN}	I_{SYS} = 0A, V_{BAT} < SYS_MIN[2:0] = 101 (3.5V)	Full	3.5	3.65		V
Maximum DC System Voltage Output	V_{SYS_MAX}	I_{SYS} = 0A, V_{BAT} = 4.35V, V_{SYS_MIN} = 3.5V	Full		4.4	4.5	V
Top Reverse Blocking MOSFET On-Resistance between VBUS and PMID - Q1	R_{ON_RBFET}		+25℃		27	35	mΩ
Top Switching MOSFET On-Resistance between PMID and SW - Q2	R_{ON_HSFET}		+25℃		32	38	mΩ
Bottom Switching MOSFET On-Resistance between SW and GND - Q3	R_{ON_LSFET}		+25℃		20	25	mΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, Full = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
BATFET forward Voltage in Supplement Mode	V_{FWD}	BAT discharge current 10mA	+25℃		30		mV
Battery Charger							
Charge Voltage Program Range	$V_{BAT\_REG\_RANGE}$		Full	3.84		4.608	V
Typical Charge Voltage Step	$V_{BAT\_REG\_STEP}$		+25℃		16		mV
Charge Voltage Setting	V_{BAT_REG}	VREG[5:0] = 010111 (4.208V)	+25℃	4.191	4.208	4.225	V
			Full	4.182	4.208	4.234	
		VREG[5:0] = 100000 (4.352V)	+25℃	4.330	4.350	4.370	
			Full	4.319	4.350	4.381	
Typical Fast Charging Current Regulation Range	$I_{CHG\_REG\_RANGE}$		Full	0		5120	mA
Typical Fast Charging Current Regulation Step	$I_{CHG\_REG\_STEP}$		+25℃		64		mA
Fast Charging Current Regulation Setting	I_{CHG_REG}	V_{BAT} = 3.8V, I_{CHG} = 128mA	+25℃	85	145	220	mA
		V_{BAT} = 3.8V, I_{CHG} = 256mA	+25℃	215	280	355	
		V_{BAT} = 3.8V, I_{CHG} = 1792mA	+25℃	1706	1778	1850	
Battery LOWV Falling Threshold	$V_{BATLOWV\_FALL}$	Fast charging to pre-charge, BATLOWV = 1	Full	2.65	2.8	2.9	V
Battery LOWV Rising Threshold	$V_{BATLOWV\_RISE}$	Pre-charge to fast charging, BATLOWV = 1, (Typical 200mV hysteresis)	Full	2.9	3	3.06	V
Pre-Charge Current Range	I_{PRECHG_RANGE}		Full	64		1024	mA
Typical Pre-Charge Current Step	I_{PRECHG_STEP}		+25℃		64		mA
Pre-Charge Current Regulation Setting	I_{PRECHG}	V_{BAT} = 2.6V, I_{PRECHG} = 256mA	+25℃	190	265	350	mA
Termination Current Range	I_{TERM_RANGE}		Full	64		1024	mA
Typical Termination Current Step	I_{TERM_STEP}		+25℃		64		mA
Termination Current Regulation Setting	I_{TERM}	I_{TERM} = 256mA	+25℃	215	265	315	mA
Battery Short Voltage	V_{SHORT}	V_{BAT} falling	+25℃		2.05		V
Battery Short Voltage Hysteresis	V_{SHORT_HYS}	V_{BAT} rising	+25℃		150		mV
Battery Short Current	I_{SHORT}	V_{BAT} < 2.2V	+25℃		50		mA
Recharge Threshold below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, VRECHG = 0 (100mV)	+25℃		100		mV
		V_{BAT} falling, VRECHG = 1 (200mV)	+25℃		200		
Battery Discharge Load Current	I_{BAT_LOAD}	V_{BAT} = 4.2V	+25℃		15		mA
System Discharge Load Current	I_{SYS_LOAD}	V_{SYS} = 4.2V	+25℃		20		mA
BAT-SYS MOSFET On-Resistance	$R_{ON\_BAT-SYS}$		+25℃		15	20	mΩ
Input Voltage and Current Regulation							
Input Voltage Regulation Range	V_{INDPM_RANGE}		Full	3.9		15.3	V
Typical Input Voltage Regulation Step	V_{INDPM_STEP}		+25℃		100		mV
Input Voltage Regulation Accuracy	V_{INDPM_ACC}	V_{INDPM} = 4.4V, 9V	Full	-3		3	%
Input Current Regulation Range	I_{INLIM_RANGE}		Full	100		4900	mA
Typical Input Current Regulation Step	I_{INLIM_STEP}		+25℃		100		mA
Input Current 100mA Regulation Accuracy	$I_{INLIM100\_ACC}$	USB100, IINLIM[5:0] = 000000 (100mA), V_{BUS} = 5V, current pulled from SW	+25℃		100		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, Full = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Current Regulation Accuracy	I_{INLIM_ACC}	USB500, IINLIM[5:0] = 000100 (500mA), V_{BUS} = 5V, current pulled from SW	+25℃	455		545	mA
		USB900, IINLIM[5:0] = 001000 (900mA), V_{BUS} = 5V, current pulled from SW	+25℃	800		1000	
		Adapter 1.5A, IINLIM[5:0] = 001110 (1500mA), V_{BUS} = 5V, current pulled from SW	+25℃	1260		1670	
Input Current Regulation during System Start-Up Sequence	I_{IN_START}	V_{SYS} = 2.2V, I_{INLIM} ≥ 200mA	+25℃		200		mA
I_{INMAX} = K_{ILIM}/R_{ILIM}	K_{ILIM}	Input current regulation by ILIM pin = 1.5A	+25℃	1400	1700	2000	A × Ω
BAT Pin Over-Voltage and Over-Current Protections							
Battery Over-Voltage Threshold	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{BAT_REG}	+25℃		104		%
Battery Over-Voltage Hysteresis	$V_{BAT\_OVP\_HYST}$	V_{BAT} falling, as percentage of V_{BAT_REG}	+25℃		2		%
System Over-Current Threshold	$I_{BAT\_FET\_OCP}$		+25℃	9			A
Thermal Regulation and Thermal Shutdown							
Junction Temperature Regulation Threshold	T_{REG}	Temperature increasing, TREG[1:0] = 11 (120℃)	Full		120		℃
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature rising	Full		160		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYS}	Temperature falling	Full		30		℃
PWM							
PWM Switching Frequency, and Digital Clock	f_{SW}	Oscillator frequency	+25℃	1.4	1.5	1.6	MHz
Maximum PWM Duty Cycle	D_{MAX_BUCK}	Buck mode	+25℃		97		%
	D_{MAX_BOOST}	Boost mode	+25℃		93		
Boost Mode Operation							
Boost Mode Regulation Voltage Range	$V_{OTG\_REG\_RANGE}$		Full	4.55		5.55	V
Typical Boost Mode Regulation Voltage Step	$V_{OTG\_REG\_STEP}$		+25℃		64		mV
Boost Mode Regulation Voltage Accuracy	$V_{OTG\_REG\_ACC}$	I_{VBUS} = 0A, BOOSTV[3:0] = 0111 (4.998V)	Full	-3		3	%
Exit Boost Mode Due to Low Battery Voltage	$V_{BATLOWV\_OTG}$	V_{BAT} falling, MIN_BAT_SEL = 0	Full	2.67		2.89	V
		V_{BAT} falling, MIN_BAT_SEL = 1	Full	2.47		2.69	
Minimum Battery Voltage to Enter Boost Mode	$V_{OTG\_BAT\_EN}$	V_{BAT} rising, MIN_BAT_SEL = 0	Full	2.9		3.06	V
		V_{BAT} rising, MIN_BAT_SEL = 1	Full	2.7		2.86	
Boost Mode Output Current Range	I_{OTG_OCP}		Full	1.2		4	A
Boost Mode Reverse Blocking FET (RBFET) Over-Current Protection Accuracy	$I_{OTG\_OCP\_ACC}$	BOOST_LIM[2:0] = 000 (1.2A)	+25℃		1.2		A
Boost Mode Over-Voltage Threshold	V_{OTG_OVP}	Rising threshold	Full	5.85	6		V
REGN LDO							
REGN LDO Output Voltage	V_{REGN}	V_{VBUS} = 9V, I_{REGN} = 40mA	Full	4.85	5	5.1	V
		V_{VBUS} = 5V, I_{REGN} = 20mA	Full	4.75	4.85		
REGN LDO Current Limit	I_{REGN}	V_{VBUS} = 9V, V_{REGN} = 3.8V	Full	60			mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{VBUS_UVLOZ} < V_{VBUS} < V_{ACOV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, Full = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

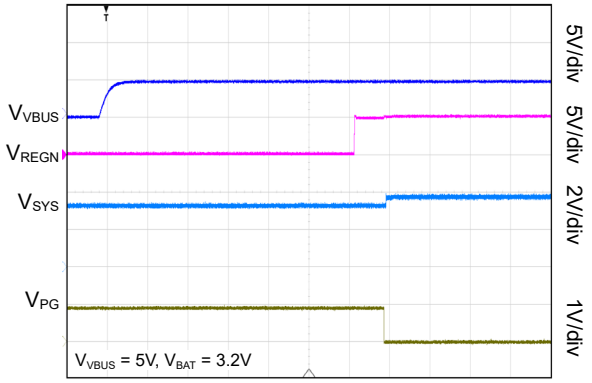
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Logic I/O Pin Characteristics (OTG, nCE, PSEL and nQON)							
Input High Threshold	V_{IH}		Full	1			V
Input Low Threshold	V_{IL}		Full			0.2	V
High-Level Leakage Current	I_{IN_BIAS}	Pull up rail 1.8V	Full			1	μA
Internal nQON Pull-Up	V_{QON}	Battery only mode	+25℃		0.85		V
		V_{VBUS} = 9V	+25℃		0.85		
		V_{VBUS} = 5V	+25℃		0.85		
Internal nQON Pull-Up Resistance	R_{QON}		+25℃		200		kΩ
Logic I/O Pin Characteristics (nINT, STAT and nPG)							
Output Low Threshold	V_{OL}	Sink current = 5mA, sink current	Full			0.3	V
High-Level Leakage Current	I_{OUT_BIAS}	Pull up rail 1.8V	Full			1	μA
I²C Interface (SCL and SDA)							
Input High Threshold, SCL and SDA	V_{IH}	Pull up rail 1.8V	Full	1			V
Input Low Threshold	V_{IL}	Pull up rail 1.8V	Full			0.2	V
Output Low Threshold	V_{OL}	Sink current = 5mA, sink current	Full			0.3	V
High-Level Leakage Current	I_{BIAS}	Pull up rail 1.8V	Full			1	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
V_{VBUS}/V_{BAT} Power-Up							
Bad Adapter Detection Duration	t_{BADSRC}		+25℃		30		ms
BAT Over-Voltage Protection							
Battery Over-Voltage Deglitch Time to Disable Charge	t_{BATOVP}		+25℃		0.1		μs
Battery Charger							
Recharge Deglitch Time	t_{RECHG}		+25℃		15		ms
Current Pulse Control							
Current Pulse Control Stop Pulse	t_{PUMPX_STOP}		+25℃	380		540	ms
Current Pulse Control Long On Pulse	t_{PUMPX_ON1}		+25℃	260		360	ms
Current Pulse Control Short On Pulse	t_{PUMPX_ON2}		+25℃	55		110	ms
Current Pulse Control Off Pulse	t_{PUMPX_OFF}		+25℃	55		110	ms
Current Pulse Control Stop Start Delay	t_{PUMPX_DLY}		+25℃	85		145	ms
nQON and Ship Mode Timing							
nQON Low Time to Turn on BATFET and to Exit Ship Mode	$t_{SHIPMODE}$		+25℃	0.9	1	1.2	s
nQON Low Time to Enable Full System Reset	t_{QON_RST}		+25℃	14.5	16	18.5	s
BATFET off Time during Full System Reset	t_{BATFET_RST}		+25℃	210	250	300	ms
Enter Ship Mode Delay	t_{SM_DLY}		+25℃		12.5		s
I²C Interface							
SCL Clock Frequency	f_{SCL}		+25℃		400		kHz
Digital Clock and Watchdog Timer							
Digital Low Power Clock	f_{LPDIG}	REGN LDO disabled	+25℃		30		kHz
Digital Clock	f_{DIG}	REGN LDO enabled	+25℃	1400	1500	1600	kHz
Watchdog Reset Time	t_{WDT}	WATCHDOG[1:0] = 11 (160s), REGN LDO disabled	+25℃	150	160		s
		WATCHDOG[1:0] = 11 (160s), REGN LDO enabled	+25℃	150	160		

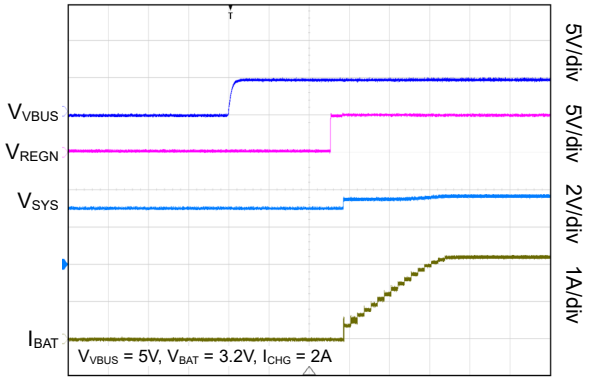
TYPICAL PERFORMANCE CHARACTERISTICS

VBUS Power-Up with Charge Disable (V_{BAT} = 3.2V)



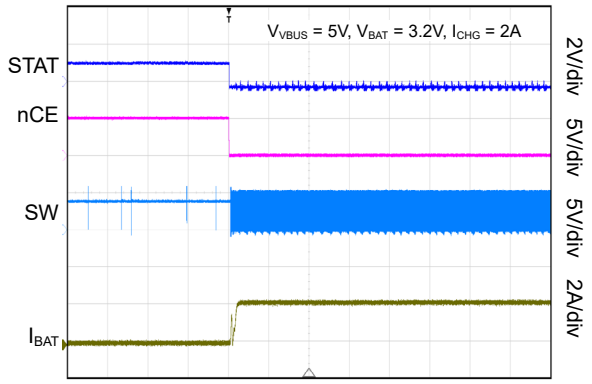
Time (40ms/div)

VBUS Power-Up with Charge Enable (V_{BAT} = 3.2V)



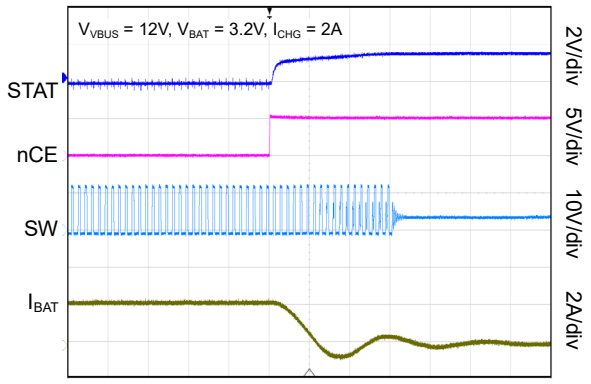
Time (100ms/div)

Charge Enable



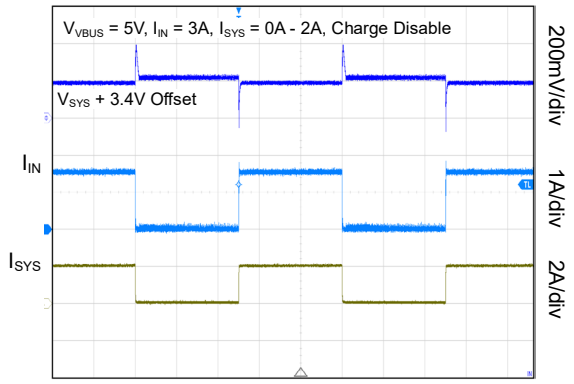
Time (400μs/div)

Charge Disable



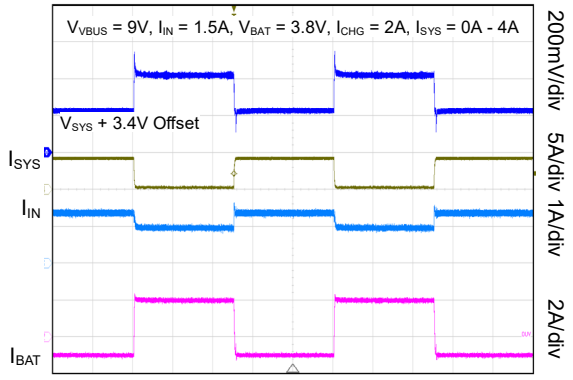
Time (4μs/div)

Input Current DPM Response without Battery



Time (2ms/div)

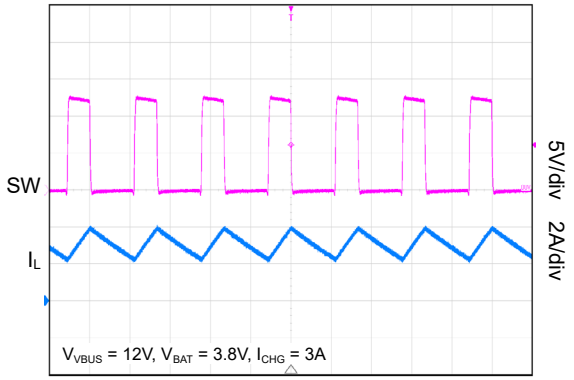
Load Transient During Supplement Mode



Time (2ms/div)

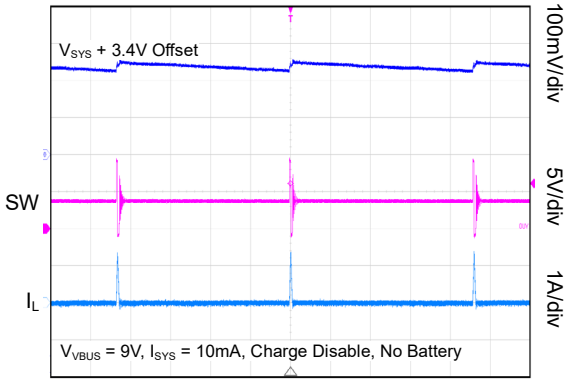
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PWM Switching Waveform



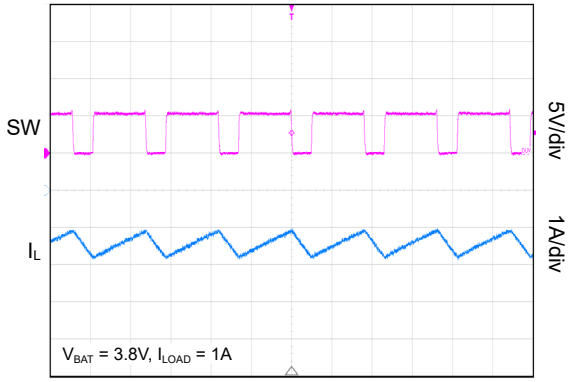
Time (400ns/div)

PFM Switching Waveform



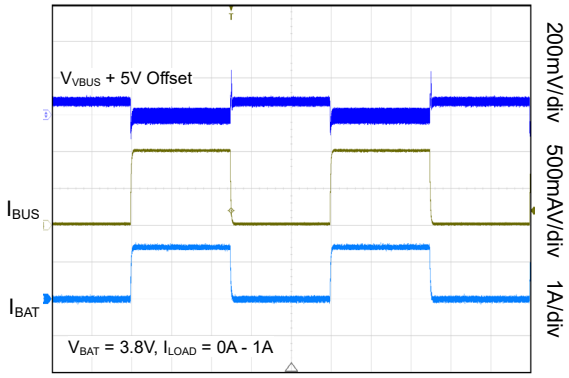
Time (8μs/div)

Boost Mode Switching Waveform



Time (400ns/div)

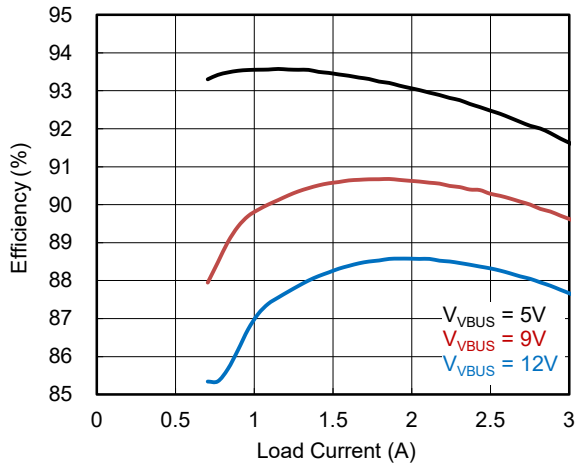
Boost Mode Load Transient



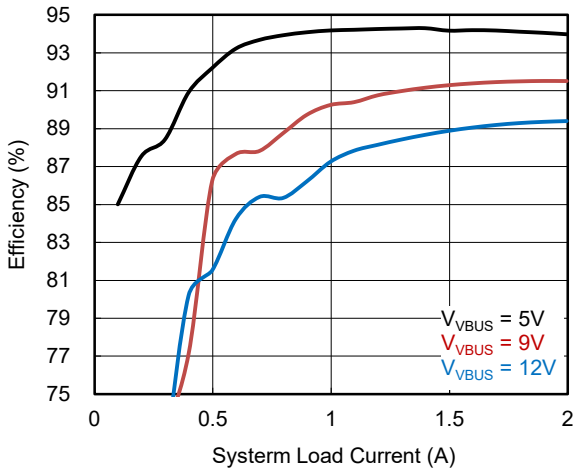
Time (4ms/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

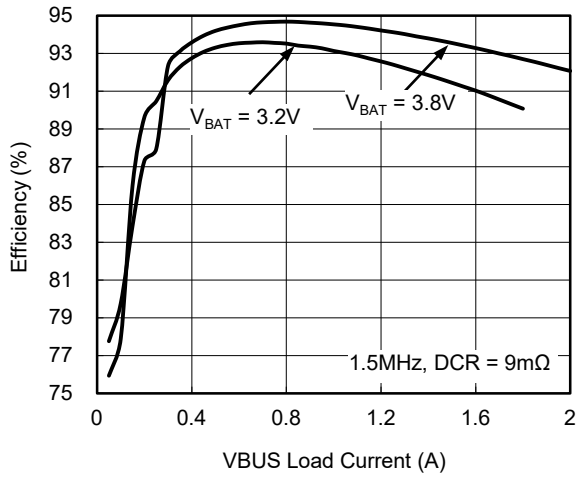
Charge Efficiency vs. Load Current



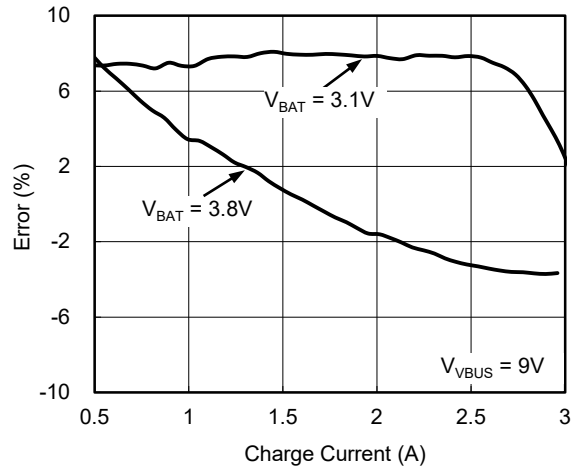
System Light Load Efficiency vs. System Light Load Current



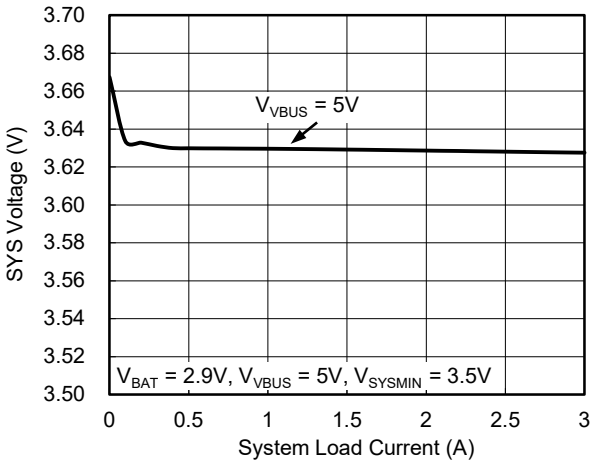
Boost Mode Efficiency vs. VBUS Load Current



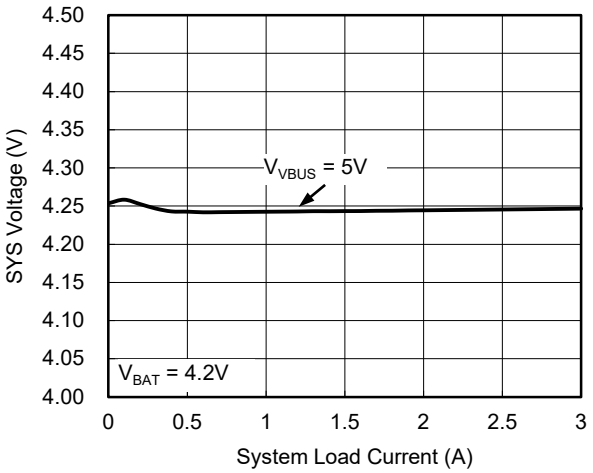
Charge Current Accuracy vs. Charge Current



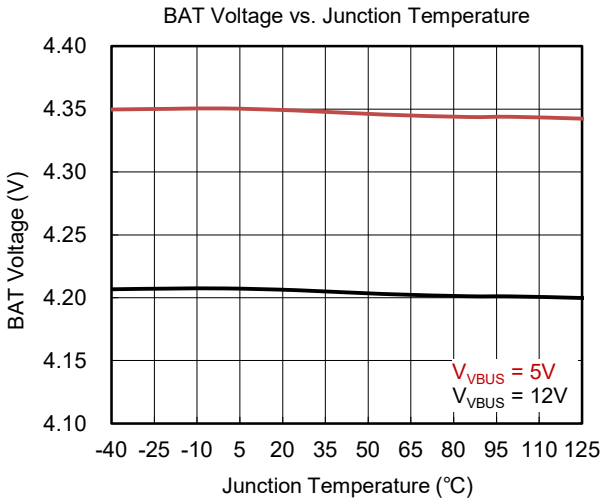
SYS Voltage Regulation vs. System Load Current

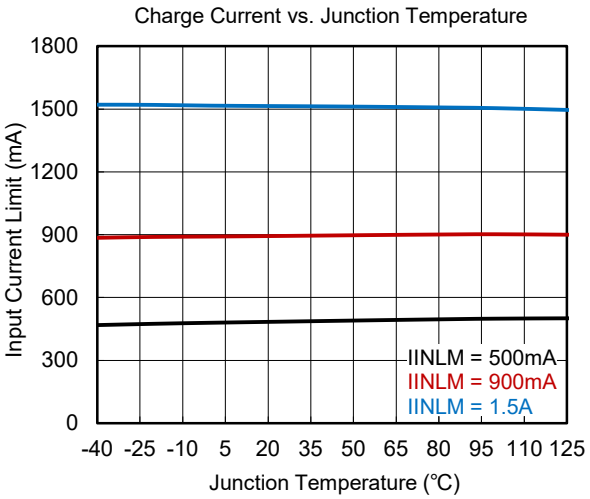


SYS Voltage Regulation vs. System Load Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)





TYPICAL APPLICATION CIRCUIT

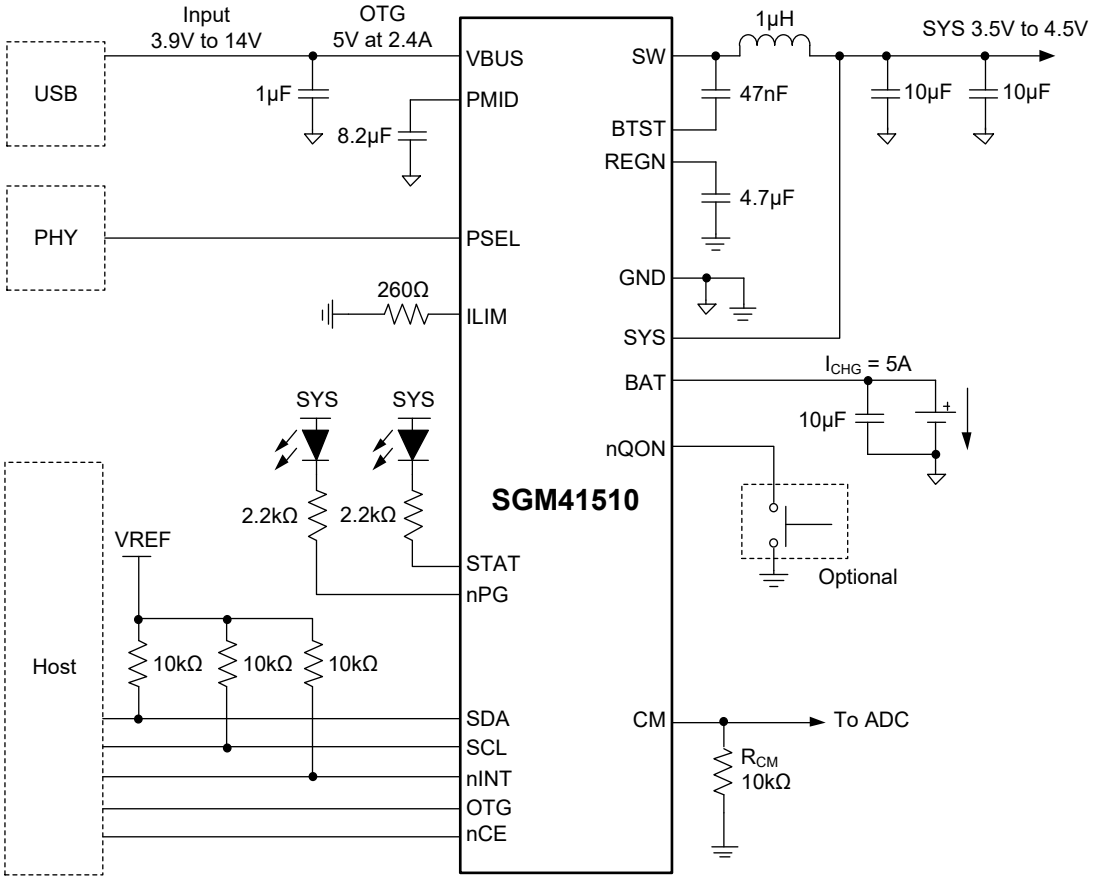


Figure 1. SGM41510 with PSEL Interface and USB On-the-Go (OTG)

FUNCTIONAL BLOCK DIAGRAM

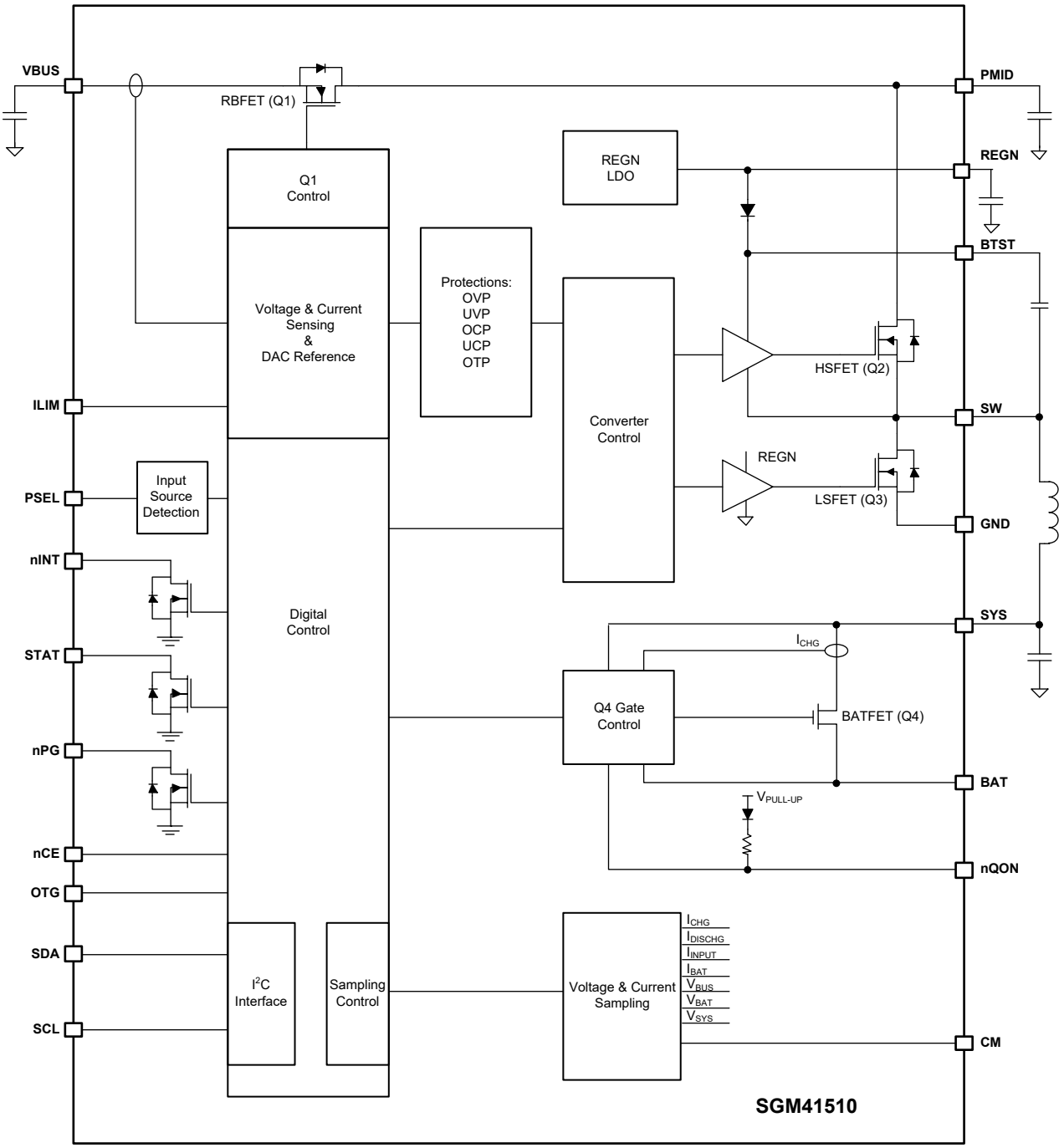


Figure 2. SGM41510 Block Diagram

DETAILED DESCRIPTION

The SGM41510 is a power management and charger device for applications such as cell phones and tablets that use high capacity single-cell Li-Ion or Li-polymer batteries. The SGM41510 is capable to operate with input voltages from 3.9V up to 14V. Automatic power path selection to power the system (SYS) from the input source (VBUS), battery (BAT), or both, is another feature of the device. Battery charge current is programmable and can reach to a maximum of 5A (charge). In the boost mode, the battery voltage is boosted to power the VBUS pin (2.4A TYP) when it is a power receiving node (USB OTG) that is typically regulated to 4.998V.

The device may operate in several different modes:

In HIZ mode, the VBUS and input source are disconnected from power circuit by turning the reverse blocking FET (Q1) off. In this mode, internal REGN LDO, converter switches and some other parts of the internal circuit remain off to save the battery while it is supplying DC power to the system through BATFET.

In the sleep mode the switching is stopped. The charger goes to the sleep mode when the input source voltage (V_{VAC}) is not high enough for charging the battery. In other words, V_{VAC} is smaller than V_{BAT} + V_{SLEEP} (where V_{SLEEP} is a small threshold) and buck converter is not able to charge, even at its maximum duty cycle. The boost may also go to the sleep mode if similar issue happens in the reverse direction (when V_{VAC} is almost equal or smaller than V_{BAT}).

In supplement mode, the input source power is not enough to supply system demanded power and the battery is assisted by discharging to the system in parallel, providing the deficit.

Power-On-Reset (POR)

The internal circuit of the device is powered from the greater voltage between V_{VBUS} and V_{BAT}. When the voltage of the selected source goes above its UVLO level (V_{VBUS} > V_{VBUS_UVLOZ} or V_{BAT} > V_{BAT_UVLOZ}) a POR happens and activates the sleep comparator, battery depletion comparator and BATFET driver. Upon activation, the I²C interface will also be ready for communication and all registers reset to their default values. The host can access all registers after POR.

Power-Up from Battery Only (No Input Source)

When only the battery is presented as a source and its voltage is above depletion threshold ($V_{BAT\_DPL\_RISE}$), the BATFET turns on and connects the battery to the system. The quiescent current is minimum because the REGN LDO remains off. Conduction losses are also low due to small R_{DSON} of BATFET. Low losses help to extend the battery run time. There is no battery temperature protection when battery is discharging to the system (no charging or boosting).

The discharge current through BATFET is continuously monitored. In the supplement mode, if a system overload (or short) occurs (I_{BAT} > I_{BATFET_OCP}), the BATFET is turned off immediately and BATFET_DIS bit is set to 1. The BATFET will not enable until the input source is applied or one of the **BATFET Enable Mode (Exit Ship Mode)** methods (explained later) is used to activate the BATFET.

Power-Up Process from the Input Source

Upon connection of an input source (VBUS), its voltage is checked to turn on the internal REGN LDO regulator and the bias circuits (no matter if the battery is present or not). The input current limit is determined and set before the buck converter is started when AUTO_DPDM_EN bit is set. The sequences of actions when VBUS as input source is powered up are:

1. REGN LDO power-up.
2. Poor source detection (qualification).
3. Input source type detection. (Based on PSEL input. It is used to set the default input current limit (IINLIM[5:0]).)
4. Setting of the input voltage limit threshold (VINDPM threshold).
5. DC/DC converter power-up.

Details of the power-up steps are explained in the following sections.

DETAILED DESCRIPTION (continued)

REGN LDO Power-Up

The REGN low dropout regulator powers the internal bias circuits, HSFET and LSFET gate drivers. The STAT pin can also be pulled up to REGN. The REGN enables when the following 2 conditions are satisfied and remain valid for a 220ms delay time, otherwise the device stays in high impedance mode (HIZ) with REGN LDO off.

1. $V_{VBUS} > V_{VBUS\_UVLOZ}$.
2. $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$ (in buck mode) or $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in boost mode).

In HIZ state, the VBUS source is disconnected (reverse blocking FET or Q1 is turned off) and the quiescent current drawn from VBUS is very small (less than I_{VBUS_HIZ}). System is only powered by the battery in HIZ mode.

Poor Source Detection (Qualification)

When REGN LDO is powered, the input source (adaptor) is checked for its type and current capacity. To start the buck converter, the input (VBUS) must meet the following conditions:

1. $V_{VBUS} < V_{ACOV}$.
2. $V_{VBUS} > V_{VBUS\_MIN}$ during t_{BADSRC} test period (30ms TYP) in which the I_{BAD_SRC} (30mA TYP) current is pulled from VBUS.

If the test is failed, the conditions are repeatedly checked every two seconds. As soon as the input source passes qualification, the VBUS_GD bit in status register is set to 1 and a pulse is sent to the nINT pin to inform the host. Type detection will start as next step.

Input Source Type Detection

The input source detection will run through the PSEL pin when AUTO_DPDM_EN bit is set while REGN LDO is powered and after the VBUS_GD bit is set. The input current limit of the SGM41510 is sets based on the state of PSEL pin. A pulse is sent to nINT pin to inform the host when the input source type detection is completed. Some registers and pins are also updated as detailed below:

1. Input current limit register (the value in the IINLIM[5:0]) is changed to set current limit.
2. PG_STAT (power good) bit is set.
3. VBUS_STAT[2:0] register is updated to indicate USB or adaptor input source types.

The host can over-write IINLIM[5:0] register to change the input current limit if needed. The charger input current is always limited by the IINLIM[5:0] register or ILIM pin at all-time.

When AUTO_DPDM_EN is disabled, the input source type detection is bypassed. The input current limit (IINLIM[5:0]) register and VBUS_STAT[2:0] register are unchanged from previous values.

Input Current Limit by PSEL

PSEL pin interfaces with USB physical layer (PHY) for input current limit setting. The USB PHY device output is used to detect if the input is a USB host or a charging port. To implement USB100 in the system, the host can enter HIZ mode by setting EN_HIZ bit after 2min charging with 500mA input current limit. In the default mode, IINLIM[5:0] is updated automatically by PSEL value in real time as given in Table 1.

Force Detection of Input Current Limit

The host can set FORCE_DPDM bit to 1 in host mode to force the device to run. And the FORCE_DPDM bit returns to 0 by itself and input result is updated after the detection is completed .

Setting of the Input Voltage Limit Threshold (VINDPM Threshold)

The device supports a wide range of input voltage limit (3.9V to 14V) for high voltage charging and provides to set input voltage limit (VINDPM[6:0]) threshold to facilitate autonomous detection.

1. Run absolute VINDPM (FORCE_VINDPM = 1) (default).
By setting FORCE_VINDPM bit to 1, VINDPM[6:0] register is writable and allows host to set the absolute threshold of VINDPM function.

2. Close VINDPM (FORCE_VINDPM = 0).
When FORCE_VINDPM bit is 0, the absolute VINDPM threshold setting is disabled. The VINDPM[6:0] register is read only.

Table 1. Input Current Limit Setting from PSEL

Input Detection	PSEL Pin	Input Current Limit (I_{INLIM})	VBUS_STAT[2:0]
USB Host SDP (USB500)	High	500mA	001
Adapter	Low	4900mA	010

DETAILED DESCRIPTION (continued)

DC/DC Converter Power-Up

The 1.5MHz switching converter composed of LSFET and HSFET is enabled and can start switching when the input current limit is set. Converter is initiated with a soft start when the system voltage is ramped up. The input current is limited to 200mA or IINLIM[5:0], whichever is smaller, if SYS voltage is less than 2.2V, otherwise the limit is set by ILIM pin and IINLIM[5:0] register.

The BATFET remains on to charge the battery if the battery charging function is enabled, otherwise BATFET turns off.

The actual input current limit used by the dynamic power management is set by IINLIM[5:0] register. In addition, the current limit is clamped by ILIM pin unless EN_ILIM bit is 0 to disable ILIM pin function.

The battery charger deploys a highly efficient 1.5MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load for higher efficiency when battery voltage is below the minimum system voltage or charging is disabled. During PFM mode, the switching duty cycle is set by the ratio of SYS and VBUS.

Boost Mode

The SGM41510 supports USB On-The-Go. The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. When a load device is connected to the USB port, the converter can operate as a step-up synchronous converter (boost mode) to supply power from the battery to that load. The boost mode output current is limited up to 2.4A (default limit) and adjustable up to 4A, but the actual current is related to battery voltage and thermal dissipation conditions. Converter will be set to boost mode if at least 30ms is passed from enabling this mode (OTG pin is high and OTG_CONFIG bit = 1) and the following conditions are satisfied:

1. $V_{BAT} > V_{BATLOWV\_OTG}$.
2. $V_{VBUS} < V_{BAT} + V_{SLEEP}$ (in sleep mode).

In boost mode, the device employs a 500kHz or 1.5MHz (set by BOOST_FREQ bit) step-up switching regulator based on system requirements. To avoid frequency change during boost mode operations, write to boost frequency configuration bit (BOOST_FREQ) is ignored when OTG_CONFIG is enabled.

During boost mode, the status register VBUS_STAT[2:0] bits are set to 111, the V_{VBUS} output is 4.998V by default (selectable through BOOSTV[3:0] register) and the output current can reach up to 4A, selected through I²C (BOOST_LIM[2:0] register). The boost output is maintained when V_{BAT} is above $V_{BATLOWV\_OTG}$ threshold.

Host Mode and Default Mode Operation with the Watchdog Timer

After a power on reset, the device starts in default mode (standalone) with all registers reset as if the watchdog timer is expired. When the host is in sleep mode or there is no host, the device stays in the default mode in which the SGM41510 operates like an autonomous charger. The battery is charged for 12 hours (default value for the fast charging safety timer). Then the charge stops while buck converter continues to operate to power the system load. In this mode the PSEL pin directly affects the IINLIM[5:0] register in real time and WATCHDOG_FAULT bit is high.

Most of the flexibility features of the SGM41510 become available in the host mode when the device is controlled by a host with I²C. By setting the WD_RST bit to 1, the charger mode changes from default mode to host mode. In this mode the WATCHDOG_FAULT bit is low and all device parameters can be programmed by the host. To prevent device watchdog reset that results in going back to default mode, the host must either disable the watchdog timer by setting WATCHDOG[1:0] = 00, or it must consistently reset the watchdog timer before expiry by writing 1 to WD_RST to prevent WATCHDOG_FAULT bit to be set. Every time a 1 is written to the WD_RST, the watchdog timer will restart counting. Therefore, it should be reset again before overflow (expiry) to keep the device in the host mode. If the watchdog timer expires (WATCHDOG_FAULT bit = 1), the device returns to default mode and all registers are reset to their default values except for IINLIM[5:0], VINDPM[6:0], BATFET_RST_EN, BATFET_DLY and BATFET_DIS bits that keep their values unchanged.

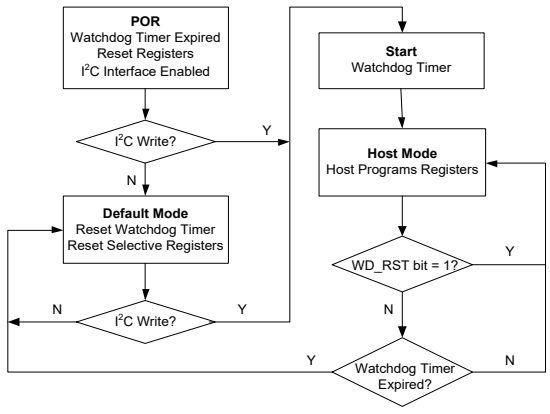


Figure 3. Watchdog Timer Flow Chart

DETAILED DESCRIPTION (continued)

Battery Charging Management

The SGM41510 is designed for charging single-cell Li-Ion or Li-polymer batteries with a charge current up to 5A (MAX). The battery connection switch (BATFET) is in the charge or discharge current path features low on-resistance (15mΩ) to allow high efficiency and low voltage drop.

Charging Cycle in Autonomous Mode

Charging is enabled if CHG_CONFIG = 1 and nCE pin is pulled low. In default mode, the SGM41510 runs a charge cycle with the default parameters itemized in Table 2. At any moment, the host can be controlled by changing to host mode.

Table 2. Charging Parameter Default Setting

Default Mode	SGM41510
Charging Voltage (VREG)	4.208V
Charging Current (I_{CHG_REG})	2.048A
Pre-Charge Current (I_{PRECHG})	128mA
Termination Current (I_{TERM})	256mA
Safety Timer	12 hours

Start a New Charging Cycle

If the converter can start switching and all the following conditions are satisfied a new charge cycle starts:

- Safety timer fault is not asserted.
- BATFET is not forced off. (BATFET_DIS bit = 0).
- Charging enabled (3 conditions: CHG_CONFIG bit = 1, ICHG[6:0] register is not 0mA and nCE pin is low).
- Battery voltage is below the programmed full charge level (V_{REGN}).

A new charge cycle starts automatically if battery voltage falls below the recharge threshold level (V_{REG} - 100mV or V_{REG} - 200mV configured by VRECHG bit). Also, if the charge cycle is completed, a new charging cycle can be initiated by toggling of the nCE pin or CHG_CONFIG bit.

Normally a charge cycle terminates when the charge voltage is above the recharge threshold level and the charging current falls below the termination threshold if the device is not in thermal regulation or Dynamic Power Management (DPM) mode.

Charge Status Report

STAT is an open-drain output pin that reports the status of charge and can drive an LED for indication: a low indicates charging is in progress, a high shows charging is completed or disabled and alternating low/high (blinking) shows a charging fault. The STAT may be disabled (keep the open drain switch off) by setting STAT_DIS bit = 1.

The CHRG_STAT[1:0] status register reports the present charging phase and status by two bits: 00 = charging disabled, 01 = in pre-charge, 10 = in fast charging (constant current mode or constant voltage mode) and 11 = charging completed.

A negative pulse is sent on nINT pin to inform the host when a charging cycle is completed.

Battery Charging Profile

The SGM41510 features a full battery charging profile with three phases. In the beginning of the cycle the battery voltage (V_{BAT}) is tested, and appropriate current and voltage regulation levels are selected as shown in Table 3. Depending on the detected status of the battery, the proper phase is selected to start or for continuation of the charging cycle. The phases are: preconditioning, constant current and constant voltage.

Table 3. Charging Current Setting Based on VBAT

V_{BAT}	Selected Charging Current	Default Value in the Register	CHRG_STAT[1:0]
< 2.2V	I_{SHORT}	-	01
2.2V to 3V	I_{PRECHG}	128mA	01
> 3V	I_{CHG}	2048mA	10

Note that in the DPM or thermal regulation modes, normal charging functions are temporarily modified: The charge current will be less than the value in the register; termination is disabled, and the charging safety timer is slowed down by counting at half clock rate.

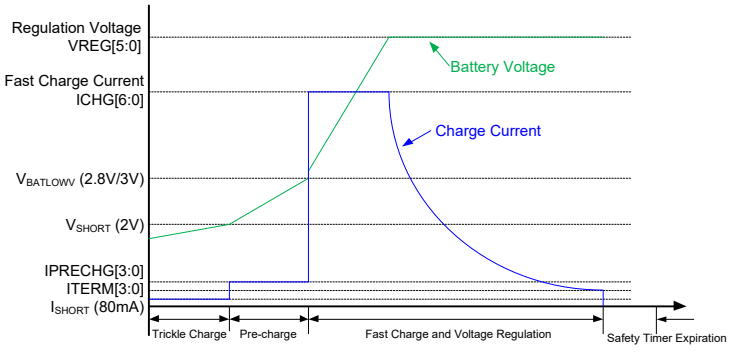


Figure 4. Battery Charging Profile

DETAILED DESCRIPTION (continued)

Termination

A charge cycle is terminated when the battery voltage is above the recharge threshold and the current falls below the programmed termination current. Unless there is a high power demand for system and need to operate in supplement mode, the BATFET turns off at the end of the charge cycle. Even after termination, the buck converter continues to operate to supply power to the system.

CHRG_STAT[1:0] is set to 11 and a negative pulse is sent to nINT pint after termination.

If the charger is regulating input current or input voltage or junction temperature instead of charge current, termination will be temporarily prevented. EN_TERM bit is termination control bit and can be set to 0 to disable termination before it happens.

Resistance Compensation (IRCOMP)

For high current charging system, resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charge time. To speed up the charging cycle, the device provides resistance compensation (IRCOMP) feature which can extend the constant current charge time to deliver maximum power to battery.

The device allows the host to compensate for the resistance by increasing the voltage regulation set point based on actual charge current and the resistance as shown below. For safe operation, the host should set the maximum allowed regulation voltage register (VCLAMP[2:0]) and the minimum resistance compensation (BAT COMP[2:0]).

$$V_{REG\_ACTUAL} = V_{REG} + Min(I_{CHRG\_ACTUAL} \times BAT\ COMP, V_{CLAMP}) \quad (1)$$

Battery Monitor

The device provides a CM pin for monitoring charge/discharge/battery/input current, and also for monitoring input/battery/system (VBUS, BAT, SYS) voltages. This is decided by CM_OUT[2:0] register in REG15 and allowed when CONV_START in REG02 is set to 1 only.

The CM pin needs to connect to GND through an external resistor R_{CM}, 10kΩ or 5kΩ is recommended for normal applications.

When CM pin is used for monitoring input current (current of VBUS when the device is operating in buck mode), or charge current (current of SYS + BAT when the device is operating in buck mode) or discharge current (current of VBUS when the device is operating in boost mode), 1/40000 of the monitored current flows through the resistor (I_{CM}). Then the voltage of CM (V_{CM}) pin when monitoring a kind of current (I_M) can be followed by Equation 2 and Equation 3.

$$V_{CM} = R_{CM} \times I_{CM} \quad (2)$$

$$I_{CM} = I_M/40000 \quad (3)$$

When CM pin is used for monitoring the BAT current (I_{BAT}), 1/40000 of the BAT current with 160μA DC offset flows through the resistor. Then V_{CM} can be followed by Equation 2 and Equation 4.

$$I_{CM} = 160\mu A \pm (I_{BAT}/40000) \quad (4)$$

where:

Direction of buck mode indicates a positive value;
Direction of boost mode indicates a negative value.

When CM pin is used for monitoring BAT/SYS/VBUS voltage, the V_{CM} is equal to 1/2 of BAT/SYS voltage and 1/10 of VBUS voltage.

$$V_{CM} = V_{BAT}/2 \quad (5)$$

$$V_{CM} = V_{SYS}/2 \quad (6)$$

$$V_{CM} = V_{BUS}/2 \quad (7)$$

DETAILED DESCRIPTION (continued)

Safety Timer

Abnormal battery conditions may result in prolonged charge cycles. An internal safety timer is considered to stop charging in such conditions. If the safety time is expired, CHRG_FAULT[1:0] bits are set to 11 and a negative pulse is sent to nINT pin. By default the charge time limit is 4 hours if the battery voltage does not rise above $V_{BATLOWV}$ threshold and 12 hours if it goes above $V_{BATLOWV}$. This feature is optional and can be disabled by clearing EN_TIMER bit. The 12 hours limit can also be reduced by setting CHG_TIMER[1:0] bits through I²C.

The safety timer counts at half clock rate when charger is running under input voltage regulation, input current regulation or thermal regulation because in these conditions, the actual charge current is likely to be less than the register setting. As an example, if the safety timer is set to 5 hours and the charger is regulating the input current (IINLIM_STAT bit = 1) in the whole charging cycle, the actual safety time will be 10 hours. Clearing the TMR2X_EN bit will disable the half clock rate feature.

The safety timer is paused if a fault occurs and charging is suspended. It will resume once the fault condition is removed. If charging cycle is stopped by a restart or by toggling nCE pin or CHG_CONFIG bit, the timer resets and restarts a new timing.

Narrow Voltage DC (NVDC) Architecture

The SGM41510 features an NVDC design using the BATFET that connects the system and battery. By using the linear region of the BATFET, the charger regulates the system bus voltage (SYS pin) above the minimum setting using buck converter even if the battery voltage is very low. MOSFET linear mode allows for the large voltage difference between SYS and BAT pins to appear as V_{DS} across the switch while conducting and charging battery. SYS_MIN[2:0] register sets the minimum system voltage (default 3.5V). If the system is in minimum system voltage regulation, VSYS_STAT bit is set.

The BATFET operates in linear region when the battery voltage is below the minimum system voltage setting. The system voltage is regulated to 150mV (TYP) above the minimum system voltage setting. The battery gradually gets charged and its voltage rises above the minimum system voltage and lets BATFET to change from linear mode to fully turned-on switch such that the voltage difference between the system and battery is the small V_{DS} of fully on BATFET.

The system voltage is always regulated to 50mV (TYP) above the battery voltage if:

1) The charging is terminated or
2) Charging is disabled and the battery voltage is above the minimum system voltage setting.

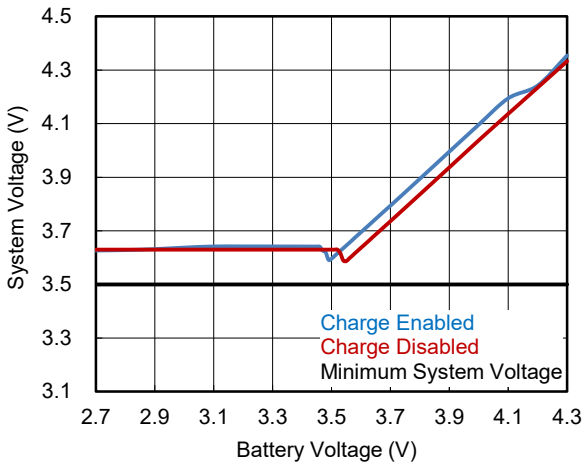


Figure 5. System Voltage vs. Battery Voltage

Dynamic Power Management (DPM)

The SGM41510 features a dynamic power management (DPM). To implement DPM the device always monitors, the input current and voltage to regulate power demand from the source and avoid input adapter overloading or to meet the maximum current limits specified in the USB specs. Overloading an input source may results in either current trying to exceed the input current limit (I_{INLIM}) or the voltage tending to fall below the input voltage limit (V_{INDPM}). With DPM, the device keeps the V_{SYS} regulated to its minimum setting by reducing the battery charge current adequately such that the input parameter (voltage or current) does not exceed the limit. In other words, charge current is reduces to satisfy $I_{IN} \le I_{INLIM}$ or $V_{IN} \ge V_{INDPM}$ whichever occurs first. DPM can be either an I_{IN} type (IINLIM) or V_{IN} type (VINDPM) depending on which limit is reached.

Changing to the supplement mode may be required if the charge current is decreased and reached to zero, but the input is still overloaded. In this case the charger reduces the system voltage below the battery voltage to allow operation in the supplement mode and provide a portion of system power demand from the battery through the BATFET.

The IINLIM_STAT or VINDPM_STAT status bits are set during an IINLIM or VINDPM respectively. Figure 6 summarizes the DPM behavior (IINLIM type) for a design example with a 9V/1.2A adapter, 3.2V battery, 2.8A charge current setting and 3.4V minimum system voltage setting.

DETAILED DESCRIPTION (continued)

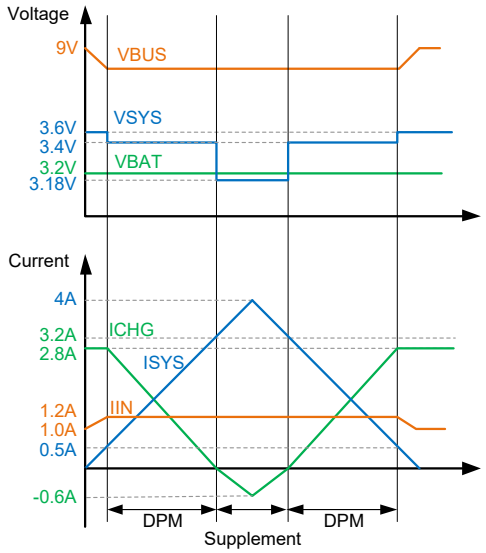


Figure 6. Input, Battery and System Voltage and Currents in DPM

Supplement Mode

If the system voltage drops below the battery voltage, the BATFET gradually starts to turn on. The threshold margin is 150mV if V_{SYS_MIN} setting is less than V_{BAT} and 45mV if V_{SYS_MIN} setting is larger than V_{BAT}. At low discharge currents, the BATFET gate voltage is regulated (R_{DS} modulation) such that the BATFET V_{DS} stays at 30mV. At higher currents, the BATFET will turn fully on (reaching its lowest R_{DSON}). From this point, increasing the discharge current will linearly increase the BATFET V_{DS} (determined by $R_{DSON} \times I_D$). Use of the MOSFET linear mode at lower currents prevents swinging oscillation of entering and exiting the supplement mode.

BATFET gate regulation V-I characteristics is shown in Figure 7. If the battery voltage falls below its minimum depletion, the BATFET turns off and exits supplement mode.

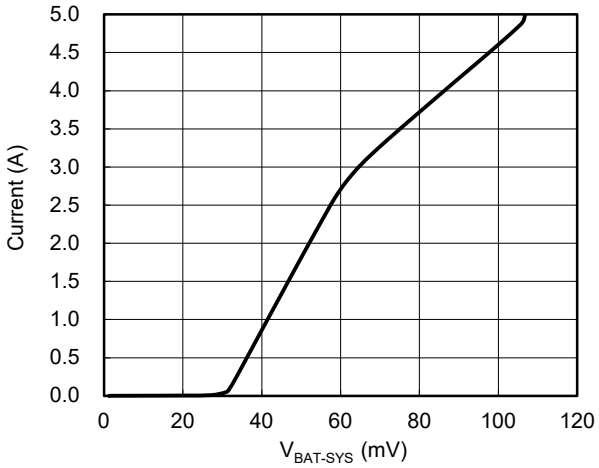


Figure 7. BATFET Gate Regulation V-I Curve

BATFET Control for System Power Reset and Ship Mode

Ship Mode (BATFET Disable)

Ship mode is usually used when the system is stored or in idle state for a long time or is in shipping. In such conditions, it is better to completely disconnect battery and make system voltage zero to minimize the leakage and extend the battery life. To enter ship mode, the BATFET has to be forced off by setting BATFET_DIS bit. The BATFET turns off immediately if BATFET_DLY bit is 0, or turns off after a t_{SM_DLY} delay (12.5 seconds) if BATFET_DLY is set.

Exit Ship Mode (BATFET Enable)

To exit the ship mode and enable the BATFET one of the following can be applied:

With no input power (no operating VBUS):

1. Connect the adapter to the input with a valid voltage to the VBUS input.
2. Pull nQON pin from logic high to low to enable BATFET for example by shorting nQON to GND. The negative pulse width should be at least a $t_{SHIPMODE}$ (1s TYP) for deglitching.

With the chip already powered by VBUS:

3. Clear BATFET_DIS bit using host and I²C.
4. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0).
5. Apply a negative pulse to nQON (same as 2).

Full System Reset with BATFET Using nQON

When the input source is not present, the BATFET can act as a load on/off switch between the system and battery. This feature can be used to apply a power-on reset to the system. Host can toggle BATFET_DIS bit to cycle power off/on and reset the system. A push-button connected to nQON pin or a negative pulse can also be used to manually force a system power cycle when BATFET is ON (BATFET_DIS bit = 0). For this function, a negative logic pulse with a minimum width of t_{QON_RST} (16s TYP) must be applied to the nQON pin that results in a temporary BATFET turn off for t_{BATFET_RST} (250ms TYP) that automatically turns on afterward. This functionality can be disabled by setting BATFET_RST_EN bit to 0.

In summary the nQON pin controls BATFET and system reset in two different ways:

1. Enable BATFET: Applying an nQON logic high to low transition with longer than $t_{SHIPMODE}$ deglitch time (negative pulse) turns on BATFET to exit ship mode (Figure 8 left).

DETAILED DESCRIPTION (continued)

2. Reset BATFET: By applying a logic low for a duration of at least t_{QON_RST} to nQON pin while VBUS is not powered and BATFET is allowed to turn on (BATFET_DIS bit = 0), the BATFET turns off for t_{BATFET_RST} and then it is re-enabled resulting in a system power-on-reset. This function can be disabled by clearing BATFET_RST_EN bit (Figure 8 right).

A typical push button circuit for nQON is given in Figure 9.

Status Outputs Pins (nPG, STAT and nINT)

Power Good Indication (nPG Pin and PG_STAT Bit)

When a good input source is connected to VBUS and input type is detected, the PG_STAT status bit goes high and the nPG pin goes low. A good input source is detected if all following conditions on V_{VBUS} are satisfied and input type detection is completed:

- V_{VBUS} is in the operating range: $V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VACOV}$.
- Device is not in sleep mode: $V_{VBUS} > V_{BAT} + V_{SLEEP}$.
- Input source is not poor: $V_{VBUS} > V_{VBUSMIN}$ (3.75V TYP) when I_{BAD_SRC} (30mA TYP) loading is applied. (Poor source detection.)
- Completed input source type detection.

Charge Status (STAT Pin)

Charging state is indicated with the open-drain STAT pin as explained in Table 4. This pin is able to drive an LED (see Figure 1). The STAT pin function can be disabled by setting STAT_DIS bit.

Table 4. STAT Pin Function

Charging State	STAT Indicator
Charging battery (or recharge)	Low (LED ON)
Charge complete	High (LED OFF)
Charging is disabled or in sleep mode	High (LED OFF)
Charge is suspended due to input over-voltage, timer faults or input or system over-voltage	1Hz Blinking

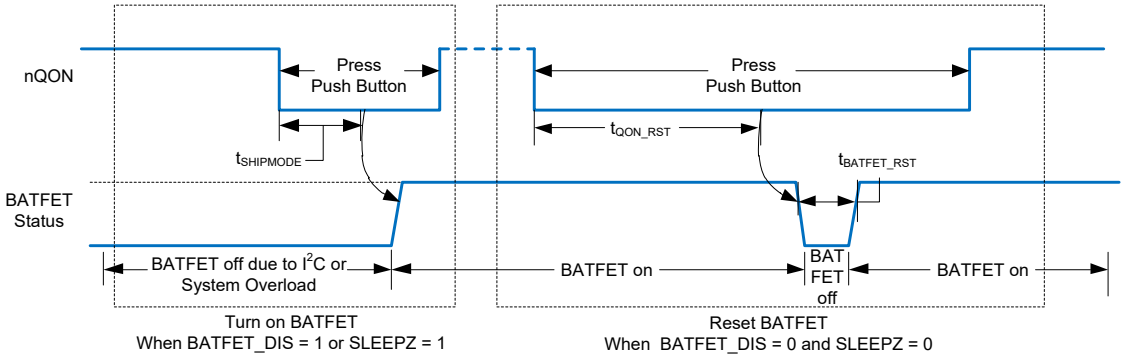


Figure 8. Left: nQON Timing to Exit Ship Mode (Enable BATFET), Right: System Power Reset (BATFET Temporarily Off)

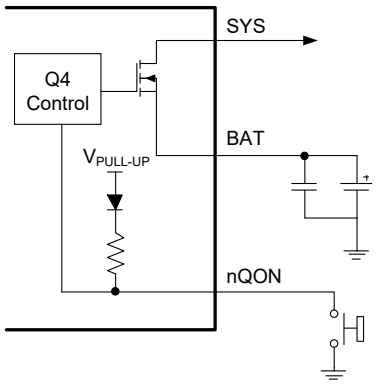


Figure 9. nQON Push Button Circuit

DETAILED DESCRIPTION (continued)

nINT Interrupt Output Pin

When a new update occurs in the charger states, a 256μs negative pulse is sent through the nINT pin to interrupt the host. The host may not continuously monitor the charger device and by receiving the interrupt it can react and check the charger situation on time.

The following events can generate an interrupt pulse:

1. All faults reflected in REG0C register (watchdog, boost overload, charge faults and battery over-voltage).
2. Charging completed.
3. PSEL identified a connected source (USB or adapter). (Through PSEL or DPDM detection, with OTG pin.)
4. Input source voltage entered the "input good" range:
   a) V_{VBUS} exceeded V_{BAT} (not in sleep mode).
   b) V_{VBUS} came below V_{VACOV}.
   c) V_{VBUS} remained above $V_{VBUSMIN}$ (3.75V TYP) when I_{BAD_SRC} (30mA TYP) load current is applied.
5. Input removed or out of the "input good" range.
6. A DPM event (VINDPM or IINLIM) occurred (a maskable interrupt).

Once a fault happens, the INT pulse is asserted once and the fault bits are updated in REG0C. Fault status is not reset in the register until the host reads it. A new fault will not assert a new INT pulse until the host reads REG0C and all the previous faults are cleared. Therefore in order to read the current time faults the host must read REG0C two times consecutively. The first read returns the history of the fault register status (from the time of the last read or reset) and the second one checks the current active faults.

REG0C does not support multi-read and multi-write as will be explained later.

Current Pulse Control Protocol

The device provides the control to generate the VBUS current pulse protocol to communicate with adjustable high voltage adapter in order to signal adapter to increase or decrease output voltage. To enable the interface, the EN_PUMPX bit must be set. Then the host can select the increase/decrease voltage pulse by setting one of the PUMPX_UP or PUMPX_DN bit (but not both) to start the VBUS current pulse sequence. During the current pulse sequence, the PUMPX_UP and PUMPX_DN bits are set to indicate pulse sequence is in progress and the device pulses the input current limit between current limit set forth by IINLIM[5:0] register and the 100mA current limit. When the pulse sequence is completed, the input current limit is returned to the value set by IINLIM[5:0] register and the PUMPX_UP or PUMPX_DN bit is cleared. In addition, the EN_PUMPX can be cleared during the current pulse sequence to terminate the sequence and force charger to return to input current limit as set forth by the IINLIM[5:0] register immediately. When EN_PUMPX bit is low, write to PUMPX_UP and PUMPX_DN bits would be ignored and have no effect on VBUS current limit.

Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (8)$$

The actual input current limit is the lower value between ILIM setting and register setting (IINLIM[5:0]). For example, if the register setting is 111111 for 3.25A, and ILIM has a 260Ω resistor (K_{ILIM} = 390 MAX) to ground for 1.5A, the input current limit is 1.5A. ILIM pin can be used to set the input current limit rather than the register settings when EN_ILIM bit is set. The device regulates ILIM pin at 0.8V. If ILIM voltage exceeds 0.8V, the device enters input current regulation (refer to dynamic power management section).

The ILIM pin can also be used to monitor input current when EN_ILIM is enabled. The voltage on ILIM pin is proportional to the input current. As shown in Equation 9, the ILIM pin can be used to monitor the input current.

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \quad (9)$$

For example, if ILIM pin is set with 260Ω resistor, and the ILIM voltage is 0.4V, the actual input current 0.615A - 0.75A (based on K_{ILIM} specified). If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8V. If ILIM pin is short, the input current limit is set by the register.

The ILIM pin function can be disabled by setting EN_ILIM bit to 0. When the pin is disabled, both input current limit function and monitoring function are not available.

SGM41510 Protection Features

Monitoring of Voltage and Current

During the converter operation, the input and system voltages (VBUS and VSYS) and switch currents are constantly monitored to assure safe operation of the device in both buck and boost modes, as will be explained below.

DETAILED DESCRIPTION (continued)

Buck Mode Voltage and Current Monitoring

1. Input Over-Voltage (ACOV)

The input voltage for buck mode operation is V_{VBUS_OP}. The device supports different OVP thresholds by VBUS_OV[2:0] register in REG15. If VBUS voltage exceeds VACOV, the device stops switching immediately. During input over-voltage event (ACOV), the CHRG_FAULT[1:0] bits in fault register (REG0C) are set to 01 and an INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage falls below the OVP threshold.

2. System Over-Voltage (SYSOVP)

During a system load transient, the device clamps the system voltage to protect the system components from over-voltage. The SYSOVP over-voltage limit threshold is 350mV + V_{SYSMIN} (programmed minimum system regulation voltage + 350mV). Once a SYSOVP occurs, switching stops to clamp any overshoot and a 30mA sink current is applied to SYS to pull the voltage down.

Boost Mode Voltage and Current Monitoring

In boost mode the RBFET (reverse blocking) and LSFET (low-side switch) FET currents and VBUS voltage are monitored for protection.

1. Over-Current on VBUS

The charger device closely monitors the RBFET (Q1), and LSFET (Q3) current to ensure safe boost mode operation. During over-current, the device will operate in hiccup mode to provide protection when the output current exceeds I_{OTG_OCP}. While in hiccup mode cycle, the device turns off RBFET for $t_{OTG\_OCP\_OFF}$ (30ms TYP) and turns on RBFET for $t_{OTG\_OCP\_ON}$ (250μs TYP) in an attempt to restart. If the over-current condition is removed, the boost converter returns to normal operation. When over-current condition continues to exist, the device repeats the hiccup cycle until over-current condition is removed. When over-current condition is detected, the fault register BOOST_FAULT bit is set high to indicate the fault in boost operation. An INT pulse is also asserted to the host.

2. Output Over-Voltage Protection for VBUS

When the VBUS voltage rises above regulation and exceeds V_{OTG_OVP}, over-voltage protection stops switching and device exits the boost mode (the OTG_CONFIG bit clears). The BOOST_FAULT bit is set high to indicate the fault and an INT pulse is asserted to the host.

SGM41510 Thermal Regulation and Shutdown

Buck Mode Thermal Protections

Internal junction temperature (T_J) is always monitored to avoid overheating. A limit of 120℃ is considered for maximum IC surface temperature in buck mode and if T_J intends to exceed this level, the device reduces the charge current to keep maximum temperature limited to 120°C (thermal regulation mode) and sets the THERM_STAT bit to 1. The wide thermal regulation range from 60℃ to 120℃ allows the user to optimize the system thermal performance. As expected, the actual charging current is usually lower than programmed value during thermal regulation. Therefore, the safety timer runs at half clock rate and charge termination is disabled during thermal regulation.

If the temperature exceeds T_{SHUT} (150℃), thermal shutdown protection arise in which the converter and BATFET are turned off, CHRG_FAULT[1:0] bits are set to 10 in the fault register and an INT pulse is sent.

When the device recovers and T_J falls below the hysteresis band of T_{SHUT_HYS} (20℃ under T_{SHUT}), the converter and BATFET resume automatically.

Boost Mode Thermal Protections

Similar to buck mode, T_J is monitored in boost mode for thermal shutdown protection. If junction temperature exceeds T_{SHUT} (150℃), BATFET will turn off and the boost mode will be disabled (OTG_CONFIG bit clears). BATFET will resume If T_J falls below the hysteresis band of T_{SHUT_HYS} (20℃ under T_{SHUT}). Boost can recover again by re-enabling OTG_CONFIG bit by host.

Battery Protections

Battery Over-Voltage Protection (BATOVP)

The over-voltage limit for the battery is 4% above the battery regulation voltage setting. In case of a BATOVP, charging stops right away, the BAT_FAULT bit is set to 1 and an INT pulse is sent.

Battery Over-Discharge Protection

If battery discharges too much and V_{BAT} falls below the depletion level ($V_{BAT\_DPL\_FALL}$), the device turns off BATFET to protect battery. This protection is latched and is not recovered until an input source is connected to the VBUS pin. When an input source is plugged in, the BATFET turns on. In such condition, the battery will start charging with the small I_{SHORT} current (80mA TYP) first as long as $V_{BAT} < V_{SHORTZ}$. When battery voltage is increased and $V_{SHORTZ} < V_{BAT} < V_{BATLOW}$, the charge current will increase to the pre-charge current level programmed in the IPRECHG[3:0] register.

Battery Over-Current Protection for System

If its current limit is exceeded due to a short or large overload on the system ($I_{BAT} > I_{BATOP}$), the BATFET will latch off. To reset this latch-off and enable BATFET, the "Exit Ship Mode" procedure must be followed.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM41511 parameters and get status reports. I²C is well known 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM41510 operates as a slave device with address 0x6B. It has twelve 8-bit registers, numbered from REG00 to REG15. A register read beyond REG15 (0x15) returns 0xFF.

Physical Layer

The SGM41510 supports I²C standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s) communication speeds. Bus lines are pulled high by weak current source or pull-up resistors are in logic high state with no clocking when the bus is free. The SDA and SCL pins are open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 10. All transactions begin by the master who applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

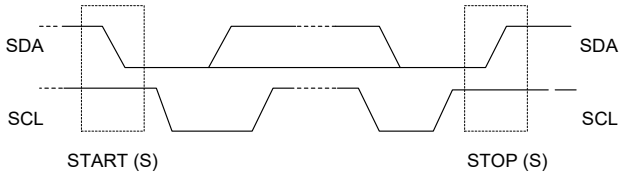


Figure 10. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the HIGH period of the clock. The state of the SDA can only change when the clock (SCL) is LOW. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 11.

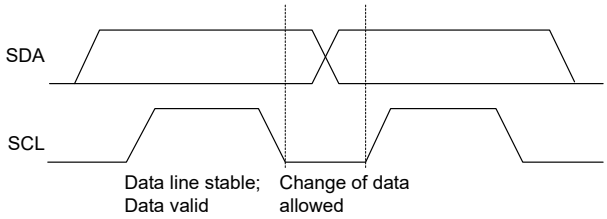


Figure 11. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. Figure 12 shows the byte transfer process with I²C interface.

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter an acknowledge bit is replied by the receiver as ninth bit. With the acknowledge bit the receiver informs the transmitter that the byte was received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including for the acknowledge ninth bit, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse and the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address and then without a stop condition another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

DETAILED DESCRIPTION (continued)

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is also a WRITE sending the register address that is supposed to be accesses in the next byte(s).

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 14 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, that will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 15), it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until a NAK is sent by master. A STOP must be sent by master in any case to end the transaction.

In the figures, the data blocks with gray background show the bits sent by master and the white background represent data bits sent by slave. If the register address is not defined, the device replies with NCK and goes back to the I²C slave idle state.

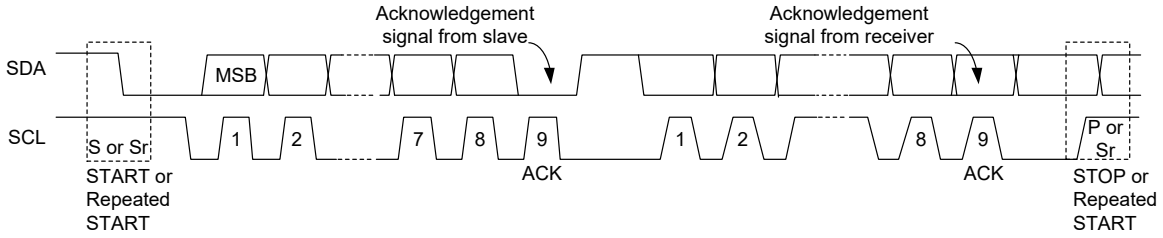


Figure 12. Data Transfer on the I²C Bus

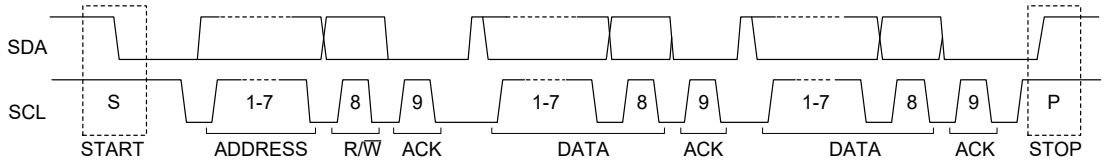


Figure 13. A Complete Data Transfer Transaction

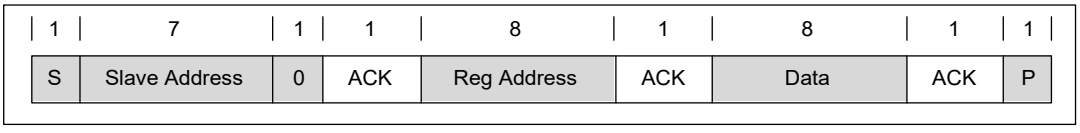


Figure 14. A Single Write Transaction

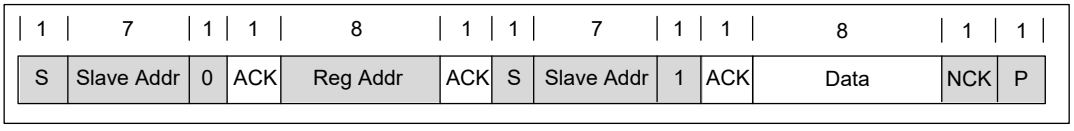


Figure 15. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM41510 for REG00 through REG14 registers, except for REG0C as explained in Figure 16 and Figure 17. REG09 (fault register), is skipped in multi-read/writes. In the multi-write, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (whose address is already written to the slave), the master replies with an ACK to ask the slave for sending the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues an STOP condition.

REG0C is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG0C reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG0C for the second time. In addition, REG0C does not support multi-read and multi-write.

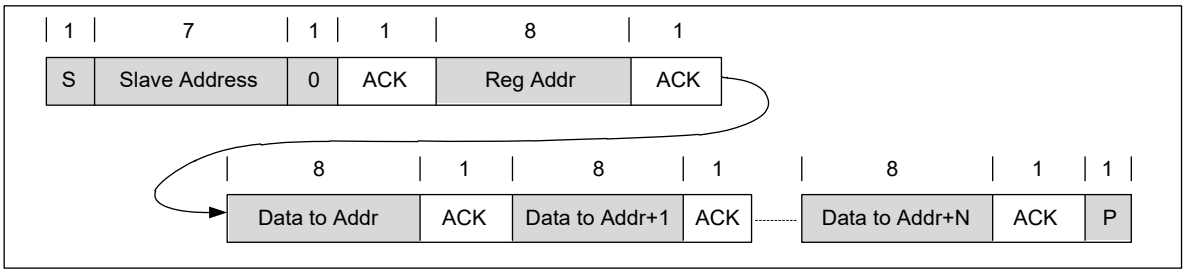


Figure 16. A Multi-Write Transaction

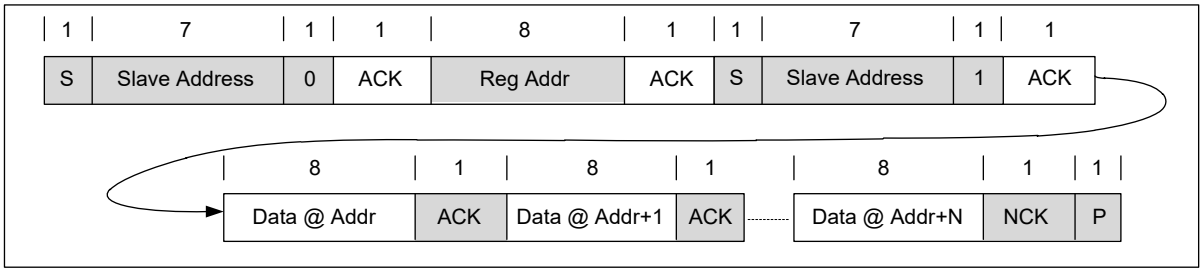


Figure 17. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address: 0x6B

R/W: Read/Write bit(s).
R: Read only bit(s).
PORV: Power-On-Reset value.
n: Parameter code formed by the bits as an unsigned binary number.

REG00

Register address: 0x00; R/W
PORV = 01000100

Table 5. REG00 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	EN_HIZ	Enable HIZ Mode 0 = Disable (default) 1 = Enable		0	R/W	REG_RST or Watchdog
D[6]	EN_ILIM	Enable ILIM Pin 0 = Disable 1 = Enable (default)	Enable ILIM pin (1).	1	R/W	REG_RST or Watchdog
D[5:0]	IINLIM[5:0]	IINLIM[5] 1 = 3200mA	Input Current Limit Value (n: 6 bits): = 100 + 100n (mA) (n ≤ 48) Offset: 100mA Range: 100mA (000000) - 4.9A (110000) Default: 000100 (500mA) Actual input current limit is the lower of I²C or ILIM pin. The IINLIM[5:0] register is changed automatically after input source detection is completed. PSEL = High (USB500) = 500mA PSEL = Low = 4900mA	000100	R/W	REG_RST
		IINLIM[4] 1 = 1600mA				
		IINLIM[3] 1 = 800mA				
		IINLIM[2] 1 = 400mA				
		IINLIM[1] 1 = 200mA				
		IINLIM[0] 1 = 100mA				

REG01

Register address: 0x01; R
PORV = 00000110

Table 6. REG01 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	Reserved	Always Read 00000110	REG01 is reserved. All the data wrote in will be ignored, and the default can be read.	0000 0110	R	REG_RST

REGISTER MAPS (continued)

REG02

Register address: 0x02; R/W

PORV = 00010001

Table 7. REG02 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	CONV_START	CM Sampling Start Control for External ADC 0 = CM sampling not active (default) 1 = CM sampling permit		0	R/W	REG_RST or Watchdog
D[6]	Reserved	Reserved (default = 0)		0	R/W	REG_RST or Watchdog
D[5]	BOOST_FREQ	Boost Mode Frequency Selection 0 = 1.5MHz (default) 1 = 500kHz	Write to this bit is ignored when OTG_CONFIG is enabled.	0	R/W	REG_RST
D[4:2]	Reserved	Reserved (default = 100)		1	R/W	REG_RST
				0	R/W	REG_RST
				0	R/W	REG_RST
D[1]	FORCE_DPDM	Force Input Detection 0 = Not in PSEL detection (default) 1 = Force PSEL detection		0	R/W	REG_RST or Watchdog
D[0]	AUTO_DPDM_EN	Automatic Input Detection Enable 0 = Disable PSEL detection when VBUS is plugged-in 1 = Enable PSEL detection when VBUS is plugged-in (default)		1	R/W	REG_RST

REG03

Register address: 0x03; R/W

PORV = 00011010

Table 8. REG03 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	BAT_LOADEN	Battery Load (I_{BAT_LOAD}) Enable 0 = Disabled (default) 1 = Enabled		0	R/W	REG_RST or Watchdog
D[6]	WD_RST	I²C Watchdog Timer Reset 0 = Normal (default) 1 = Reset (back to 0 after timer reset)	Watchdog Timer Reset Control Bit. Write 1 to this bit to avoid watchdog expiry. WD_RST resets to 0 after watchdog timer reset (expiry).	0	R/W	REG_RST or Watchdog
D[5]	OTG_CONFIG	Enable OTG 0 = OTG disable (default) 1 = OTG enable	This bit has priority over charge enable in the CHG_CONFIG.	0	R/W	REG_RST or Watchdog
D[4]	CHG_CONFIG	Enable Battery Charging 0 = Charge disable 1 = Charge enable (default)	Battery charging is enabled when CHG_CONFIG = 1 and nCE pin is driven low.	1	R/W	REG_RST or Watchdog
D[3:1]	SYS_MIN[2:0]	Minimum System Voltage 000 = 3.0V 001 = 3.1V 010 = 3.2V 011 = 3.3V 100 = 3.4V 101 = 3.5V (default) 110 = 3.6V 111 = 3.7V	Minimum System Voltage Value. Offset: 3.0V Range: 3.0V (000) - 3.7V (111) Default: 3.5V (101)	101	R/W	REG_RST
D[0]	MIN_BAT_SEL	Minimum Battery Voltage (Falling) to Exit Boost Mode 0 = 2.8V V_{BAT} falling (default) 1 = 2.6V V_{BAT} falling		0	R/W	REG_RST or Watchdog

REGISTER MAPS (continued)

REG04

Register address: 0x04; R/W

PORV = 00100000

Table 9. REG04 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	EN_PUMPX	Current Pulse Control Enable 0 = Disable (default) 1 = Enable (PUMPX_UP and PUMPX_DN)		0	R/W	REG_RST or Watchdog
D[6:0]	ICHG[6:0]	ICHG[6] 1 = 4096mA	Fast Charging Current Value (n: 7 bits): = 64n (mA) (n ≤ 79) Offset: 0mA Range: 0mA (0000000) - 5056mA (1001111) Default: 2048mA (0100000) Notes: I_{CHG} = 000000 (0mA) disables charge. I_{CHG} > 1001111 (5056mA) is clamped to register value 1001111 (5056mA).	0	R/W	REG_RST or Watchdog
		ICHG[5] 1 = 2048mA		1	R/W	
		ICHG[4] 1 = 1024mA		0	R/W	
		ICHG[3] 1 = 512mA		0	R/W	
		ICHG[2] 1 = 256mA		0	R/W	
		ICHG[1] 1 = 128mA		0	R/W	
		ICHG[0] 1 = 64mA		0	R/W	

REG05

Register address: 0x05; R/W

PORV = 00010011

Table 10. REG05 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:4]	IPRECHG[3:0]	IPRECHG[3] 1 = 512mA	Pre-Charge Current Limit (n: 4 bits): = 64 + 64n (mA) Offset: 64mA Range: 64mA (0000) - 1024mA (1111) Default: 128mA (0001)	0	R/W	REG_RST or Watchdog
		IPRECHG[2] 1 = 256mA		0	R/W	
		IPRECHG[1] 1 = 128mA		0	R/W	
		IPRECHG[0] 1 = 64mA		1	R/W	
D[3:0]	ITERM[3:0]	ITERM[3] 1 = 512mA	Termination Current Limit (n: 4 bits): = 64 + 64n (mA) Offset: 64mA Range: 64mA (0000) - 1024mA (1111) Default: 256mA (0011)	0	R/W	REG_RST or Watchdog
		ITERM[2] 1 = 256mA		0	R/W	
		ITERM[1] 1 = 128mA		1	R/W	
		ITERM[0] 1 = 64mA		1	R/W	

REGISTER MAPS (continued)

REG06

Register address: 0x06; R/W

PORV = 01011110

Table 11. REG06 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:2]	VREG[5:0]	VREG[5] 1 = 512mV	Charge Voltage Limit (n: 6 bits): = 3840 + 16n (mV) if (n ≤ 48) Offset: 3.840V Range: 3.840V (000000) - 4.608V (110000) Default: 4.208V (010111) Note: V_{REG} > 110000 (4.608V) is clamped to register value 110000 (4.608V).	0	R/W	REG_RST or Watchdog
		VREG[4] 1 = 256mV		1	R/W	
		VREG[3] 1 = 128mV		0	R/W	
		VREG[2] 1 = 64mV		1	R/W	
		VREG[1] 1 = 32mV		1	R/W	
		VREG[0] 1 = 16mV		1	R/W	
D[1]	BATLOWV	Battery Pre-Charge to Fast Charging Threshold 0 = 2.8V 1 = 3.0V (default)	Default: 3.0V (1) V_{BAT} rising. V_{BAT} falling, $V_{BATLOWV\_FALL}$ = 2.8V; V_{BAT} rising, $V_{BATLOWV\_RISE}$ = 3.0V.	1	R/W	REG_RST or Watchdog
D[0]	VRECHG	Battery Recharge Threshold (below Charge Voltage Limit) 0 = 100mV below VREG[5:0] (default) 1 = 200mV below VREG[5:0]		0	R/W	REG_RST or Watchdog

REG07

Register address: 0x07; R/W

PORV = 10011101

Table 12. REG07 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	EN_TERM	Charging Termination Enable 0 = Disable 1 = Enable (default)		1	R/W	REG_RST or Watchdog
D[6]	STAT_DIS	STAT Pin Enable 0 = Enable STAT pin function (default) 1 = Disable STAT pin function		0	R/W	REG_RST or Watchdog
D[5:4]	WATCHDOG[1:0]	Watchdog Timer Setting 00 = Disable watchdog timer 01 = 40s (default) 10 = 80s 11 = 160s	Expiry time of the watchdog timer if it is not reset.	01	R/W	REG_RST or Watchdog
D[3]	EN_TIMER	Charging Safety Timer Enable 0 = Disable 1 = Enable (default)		1	R/W	REG_RST or Watchdog
D[2:1]	CHG_TIMER[1:0]	Charging Safety Timer Setting 00 = 5hrs 01 = 8hrs 10 = 12hrs (default) 11 = 20hrs		10	R/W	REG_RST or Watchdog
D[0]	Reserved	Reserved (default = 1)		1	R/W	REG_RST or Watchdog

REGISTER MAPS (continued)

REG08

Register address: 0x08; R/W

PORV = 00000011

Table 13. REG08 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:5]	BAT COMP[2:0]	BAT COMP[2] 1 = 80mΩ	IR Compensation Resistor Setting Range: 0mΩ (000)- 140mΩ (111) Default: 0Ω (000) (i.e. Disable IR Comp)	0	R/W	REG_RST or Watchdog
		BAT COMP[1] 1 = 40mΩ		0	R/W	
		BAT COMP[0] 1 = 20mΩ		0	R/W	
D[4:2]	VCLAMP[2:0]	VCLAMP[2] 1 = 128mV	IR Compensation Voltage Clamp above VREG[5:0] V_{CLAMP} (n: 3 bits): = 32n (mV) Offset: 0mV Range: 0mV (000) - 224mV (111) Default: 0mV (000)	0	R/W	REG_RST or Watchdog
		VCLAMP[1] 1 = 64mV		0	R/W	
		VCLAMP[0] 1 = 32mV		0	R/W	
D[1:0]	TREG[1:0]	Thermal Regulation Threshold 00 = 60℃ 01 = 80℃ 10 = 100℃ 11 = 120℃ (default)		11	R/W	REG_RST or Watchdog

REG09

Register address: 0x09; R/W

PORV = 01000100

Table 14. REG09 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	Reserved	Reserved (default = 0)		0	R/W	REG_RST or Watchdog
D[6]	TMR2X_EN	Safety Timer Setting during DPM or Thermal Regulation 0 = Disable 1 = Safety timer slow down by 2× during input DPM or thermal regulation (default)		1	R/W	REG_RST or Watchdog
D[5]	BATFET_DIS	Force BATFET Off to Enable Ship Mode 0 = Allow BATFET turn on (default) 1 = Force BATFET off		0	R/W	REG_RST
D[4]	Reserved	Reserved (default = 0)		0	R/W	REG_RST or Watchdog
D[3]	BATFET_DLY	BATFET Turn-Off Delay Control 0 = Turn off BATFET immediately (default) 1 = Turn off BATFET after t_{SM_DLY} delay	BATFET_DIS bit is set.	0	R/W	REG_RST
D[2]	BATFET_RST_EN	BATFET Full System Reset Enable 0 = Disable BATFET reset 1 = Enable BATFET reset (default)		1	R/W	REG_RST
D[1]	PUMPX_UP	Current Pulse Control Voltage up Enable 0 = Disable (default) 1 = Enable	This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed.	0	R/W	REG_RST or Watchdog
D[0]	PUMPX_DN	Current Pulse Control Voltage down Enable 0 = Disable (default) 1 = Enable	This bit is can only be set when EN_PUMPX bit is set and returns to 0 after current pulse control sequence is completed.	0	R/W	REG_RST or Watchdog

REGISTER MAPS (continued)

REG0A

Register address: 0x0A; R/W

PORV = 01110011

Table 15. REG0A Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:4]	BOOSTV[3:0]	BOOSTV[3] 1 = 512mV	Boost Mode Voltage Regulation (n: 4 bits): = 4.55 + 0.064n (V) Offset: 4.55V Range: 4.55V (0000) - 5.51V (1111) Default:4.998V (0111)	0	R/W	REG_RST or Watchdog
		BOOSTV[2] 1 = 256mV		1	R/W	
		BOOSTV[1] 1 = 128mV		1	R/W	
		BOOSTV[0] 1 = 64mV		1	R/W	
D[3]	PFM_OTG_DIS	PFM Allowed in Boost Mode 0 = Allow PFM in boost mode (default) 1 = Disable PFM in boost mode		0	R/W	REG_RST
D[2:0]	BOOST_LIM[2:0]	Boost Mode Current Limit 000 = 1.2A 001 = 1.6A 010 = 2A 011 = 2.4A (default) 100 = 2.8A 101 = 3.2A 110 = 3.6A 111 = 4A	Range: 1.2A (000) - 4A (111) Default: 2.4A (011) Note: Higher than 2.4A requires higher battery voltage and better thermal dissipation conditions.	0	R/W	REG_RST or Watchdog
				1	R/W	
				1	R/W	

REG0B

Register address: 0x0B; R

PORV = xxxxxxxx

Table 16. REG0B Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE	RESET BY
D[7:5]	VBUS_STAT[2:0]	VBUS Status Register 000 = No input 001 = USB host SDP (500mA)→ PSEL high 010 = Adapter (4.9A) → PSEL low 111 = OTG Other values are Reserved. Current limit value is reported in IINLIM[5:0] register.	x	R	NA
			x	R	
			x	R	
D[4:3]	CHRG_STAT[1:0]	Charging Status 00 = Charge disable 01 = Pre-charge (V_{BAT} < V_{BATLOW}) 10 = Fast charging 11 = Charging terminated	x	R	NA
			x	R	
D[2]	PG_STAT	Input Power Good Status 0 = Input power source is not good 1 = Input power source is good	x	R	NA
D[1]	Reserved		x	R	NA
D[0]	VSYS_STAT	System Voltage Regulation Status 0 = Not in VSYSMIN regulation (V_{BAT} > V_{SYS_MIN}) 1 = In VSYSMIN regulation (V_{BAT} < V_{SYS_MIN})	x	R	NA

REGISTER MAPS (continued)

REG0C

Register address: 0x0C; R

PORV = xxxxxxxx

Table 17.REG0C Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	WATCHDOG_FAULT	Watchdog Fault Status 0 = Normal 1 = Watchdog timer expired		x	R	NA
D[6]	BOOST_FAULT	Boost Mode Fault Status 0 = Normal 1 = VBUS overloaded in OTG, or VBUS OVP, or battery voltage too low (any condition that prevents boost starting function)		x	R	NA
D[5:4]	CHRG_FAULT[1:0]	Charge Fault Status 00 = Normal 01 = Input fault (VBUS > V_{ACOV} or V_{BAT} < V_{VBUS} < 3.8V) 10 = Thermal shutdown 11 = Charge safety timer expired		x	R	NA
D[3]	BAT_FAULT	Battery Fault Status 0 = Normal 1 = Battery over-voltage (V_{BAT} > V_{BAT_OVP})		x	R	NA
D[2:0]	Reserved			x	R	NA

REG0D

Register address: 0x0D; R/W

PORV = 10010010

Table 18. REG0D Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	FORCE_VINDPM	VINDPM Threshold Setting 0 = Close V_{INDPM} threshold 1 = Run absolute V_{INDPM} threshold (default)	Note: Register is reset to default value when input source is plugged in.	1	R/W	REG_RST
D[6:0]	VINDPM[6:0]	VINDPM[6] 1 = 6400mV	Absolute VINDPM Threshold (n: 7 bits): = 2.6V + 0.1n (V) Offset: 2.6V Range: 3.9V (0001101) - 15.3V (1111111) Default: 4.4V (0010010) Notes: VINDPM[6:0] < 0001101 (3.9V) is clamped to register value 0001101 (3.9V). Register is read only when FORCE_VINDPM = 0. Register can be R/W when FORCE_VINDPM = 1 Register is reset to default value when input source is plugged in.	0	R/W	REG_RST
		VINDPM[5] 1 = 3200mV		0	R/W	
		VINDPM[4] 1 = 1600mV		1	R/W	
		VINDPM[3] 1 = 800mV		0	R/W	
		VINDPM[2] 1 = 400mV		0	R/W	
		VINDPM[1] 1 = 200mV		1	R/W	
		VINDPM[0] 1 = 100mV		0	R/W	

REGISTER MAPS (continued)

REG0E

Register address: 0x0E; R

PORV = xxxxxxxx

Table 19. REG0E Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE	RESET BY
D[7]	THERM_STAT	Thermal Regulation Status 0 = Not in thermal regulation 1 = In thermal regulation	x	R	NA
D[6:0]	Reserved		x	R	NA

REG0F

Register address: 0x0F; R

PORV = xxxxxxxx

Table 20. REG0F Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	Reserved	Always Read 00000000		x	R	NA

REG10

Register address: 0x10; R

PORV = xxxxxxxx

Table 21. REG10 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	Reserved	Always Read 00000000		x	R	NA

REG11

Register address: 0x11; R

PORV = xxxxxxxx

Table 22. REG11 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7]	VBUS_GD	Good Input Source Detected 0 = No VBUS attached 1 = VBUS attached		x	R	NA
D[6:0]	Reserved			x	R	NA

REG12

Register address: 0x12; R

PORV = xxxxxxxx

Table 23. REG12 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:0]	Reserved	Always Read 00000000		x	R	NA

REGISTER MAPS (continued)

REG13

Register address: 0x13; R

PORV = xxxxxxxx

Table 24. REG13 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE	RESET BY
D[7]	VINDPM_STAT	Input Voltage Regulation (Dynamic Power Management) 0 = Not in VINDPM 1 = In VINDPM	x	R	NA
D[6]	IINLIM_STAT	Input Current Regulation (Dynamic Power Management) 0 = Not in IINLIM 1 = IINLIM	x	R	NA
D[5:0]	Reserved		x	R	NA

REG14

Register address: 0x14; R/W, R

PORV = 0xxxxxxx

Table 25. REG14 Register Details

BITS	BIT NAME	DESCRIPTION	PORV	TYPE	RESET BY
D[7]	REG_RST	Register Reset 0 = Keep current register setting (default) 1 = Reset R/W bits of all Registers to default and reset safety timer (It also resets itself to 0 after register reset is completed.)	0	R/W	NA
D[6]	Reserved	Reserved (always reads 0)	x	R	NA
D[5:3]	PN[2:0]	Part ID 000 = SGM41510	x	R	NA
			x	R	NA
			x	R	NA
D[2]	Reserved	Reserved (always reads 0)	x	R	NA
D[1:0]	DEV_REV[1:0]	Device Revision: 00	x	R	NA
			x	R	NA

REG15

Register address: 0x15; R/W

PORV = 00001100

Table 26. REG15 Register Details

BITS	BIT NAME	DESCRIPTION	COMMENT	PORV	TYPE	RESET BY
D[7:5]	CM_OUT[2:0]	000 = DC offset current (160μA) (default) 001 = 1/40000 charge current 010 = 1/40000 discharge current 011 = 1/40000 BAT current with DC offset 100 = 1/40000 input current 101 = 1/2 BAT voltage 110 = 1/2 SYS voltage 111 = 1/10 VBUS voltage	These bits can only be set when CONV_START is set to 1.	0	R/W	REG_RST or Watchdog
				0	R/W	
				0	R/W	
D[4:2]	VBUS_OV[2:0]	VBUS_OV[2] 1 = 6.4V	Input Over-Voltage Offset: 10.3V Range: 10.3V (000) – 15.1V (011) Default: 15.1V (011)	0	R/W	REG_RST or Watchdog
		VBUS_OV[1] 1 = 3.2V		1	R/W	
		VBUS_OV[0] 1 = 1.6V		1	R/W	
D[1:0]	SP[1:0]	(default 00)	Reserved bits for extra requirement	00	R/W	REG_RST

APPLICATION INFORMATION

A typical application includes the SGM41510 as an I²C controlled power path management device and a single-cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

Detailed Design Procedure

Inductor Selection

The 1.6MHz switching frequency allows the use of small inductor and capacitor values. Maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the peak to peak ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\ I_{RIPPLE} \quad (3)$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{VBUS} \times D \times (1-D)}{f_S \times L} \quad (4)$$

The maximum inductor ripple current occurs when the duty cycle (D) is around 0.5. In a practical design, usually the inductor peak to peak current ripple is selected in the range between 20% to 40% of the maximum (charging) current as a trade-off between inductor size and efficiency.

Input Capacitor

Input capacitance must have enough rms ripple current rating to absorb (decouple) the input switching ripple current (I_{CIN}). In worst case the RMS ripple current is half of the DC charging current (I_{CHG}) occurring when duty cycle is around 50%. If the converter does not operate at V_{BAT}/V_{VBUS}≈50% duty cycle, then the worst-case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by Equation 5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (5)$$

Low ESR ceramic capacitors such as X7R or X5R are preferred for input decoupling capacitor and should be placed close to the drain of the high-side and source of the low-side MOSFETs. For SGM41510 C_{IN} can be placed across PMID and GND pins close to the chip. Voltage rating of the capacitor must be at least 25% higher than the normal input voltage to minimize voltage derating. A rating of 25V or higher is preferred for a 15V input voltage.

For 3A to 4A charger a C_{IN} capacitance of 22μF is suggested.

Output Capacitor

The output capacitance on the system must have enough rms (ripple) current rating to absorb the inductor switching ripple and provide system transient current demands. I_{COUT} (C_{OUT} rms current) can be calculated by:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

And the output voltage ripple can be calculated by:

$$\Delta V_O = \frac{V_{OUT}}{8LC_{OUT}f_S^{\ 2}}\left(1 - \frac{V_{OUT}}{V_{VBUS}}\right) \quad (7)$$

Increasing L or C_{OUT} (of the LC filter) can reduce the ripple.

The charger device has internal loop compensation optimized for above 20μF ceramic output capacitance. A 10V, X7R (or X5R) ceramic capacitor is recommended for the output.

Note that even though the design is based on buck mode operation, it is good for boost mode too, because only the direction of currents is reversed and switches are bidirectional.

Power Supply Recommendations

In order to provide an output voltage on SYS, the SGM41510 device requires either an input power supply between 3.9V to 14.2V with at least 100mA current rating connected to VBUS; or, a single-cell Li-Ion battery with voltage higher than $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 3A in order for the buck converter of the charger to provide maximum output power to SYS.

APPLICATION INFORMATION (continued)

Layout Guidelines

The switching node (SW) creates very high frequency noises several times higher than f_{SW} (1.6MHz) due to sharp rise and fall times of the voltage and current in the switches. To reduce the ringing issues and noise generation, proper layout is important to minimize the current path impedance and loop area. A graphical guideline for the current loops and their frequency content is provided in Figure 18. The following considerations can help making a better layout.

1. Place the input capacitor between PMID and GND pins as close as possible to the chip with shortest copper connections (avoid vias).

2. Connect one pin of the inductor as close as possible to the SW pin of the device and minimize the copper area of SW node to reduce capacitive coupling from SW area to nearby signal traces. This decreases the noise induced through parasitic stray capacitances and displacement currents to other conductors. SW connection should be wide enough to carry the charging current. Keep other signals and traces away from SW if possible.

3. Place output capacitor GND pin as close as possible to the GND pin of the device and the GND pin of input capacitor C_{IN}. It is better to avoid using vias for these connections and keep the high frequency currents paths very short and on the same layer GND plane with smallest HF current loop area. A GND copper layer under the component layer helps reducing noise emissions. Pay attention to the DC current and ac currents paths in the layout and keep them short and decoupled as much as possible.

4. For analog signals, it is better to use a separate analog ground (AGND) branched only at one point from GND pin. To avoid high current flow through the AGND path, it should be connected to GND only at one point (preferably the GND pin and thermal pad of the device). Alternatively a 0Ω resistor can be used to tie analog ground to power ground.

6. Place decoupling capacitors right next to the IC pins with shortest possible trace connections.

7. It is critical to solder the exposed thermal pad of the package to the PCB ground planes. Ensure that there are enough thermal vias directly under the IC, connecting to the ground plane on the other layers for better heat dissipation and cooling of the device.

8. Ensure that the number and sizes of vias provide enough copper for a given current path. Remember that vias usually have some parasitic inductance and resistance.

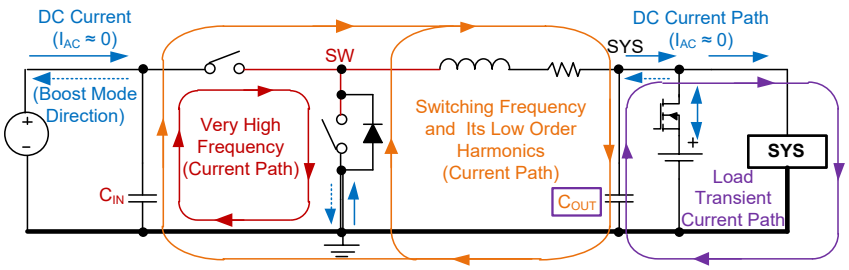


Figure 18. The Paths and Loops Carrying Very High Frequency, High Frequency and DC Currents (for Layout Design Consideration)

REVISION HISTORY

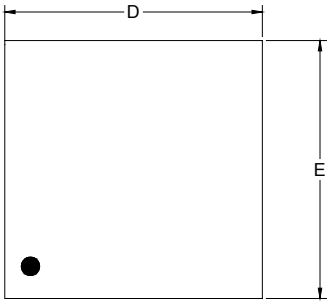
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

JUNE 2021 – REV.A to REV.A.1	Page
Updated Byte Format section	26

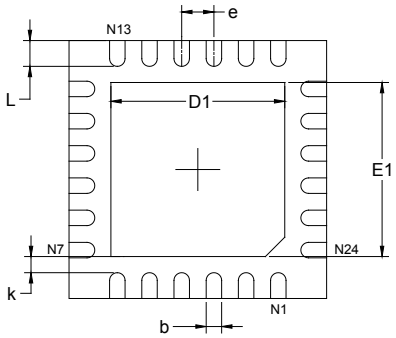
Changes from Original (SEPTEMBER 2020) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

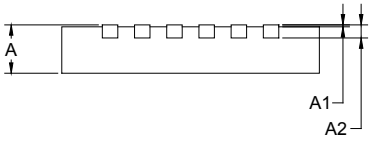
TQFN-4×4-24L



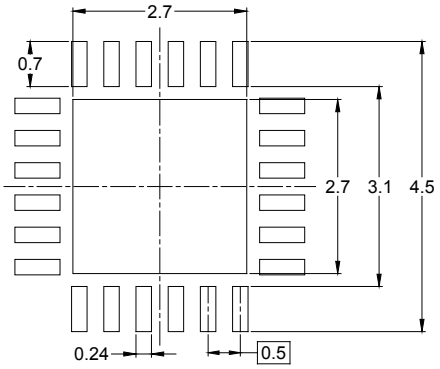
TOP VIEW



BOTTOM VIEW



SIDE VIEW

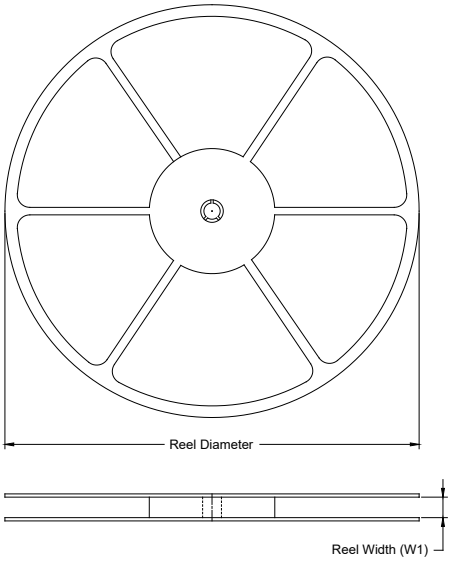


RECOMMENDED LAND PATTERN (Unit: mm)

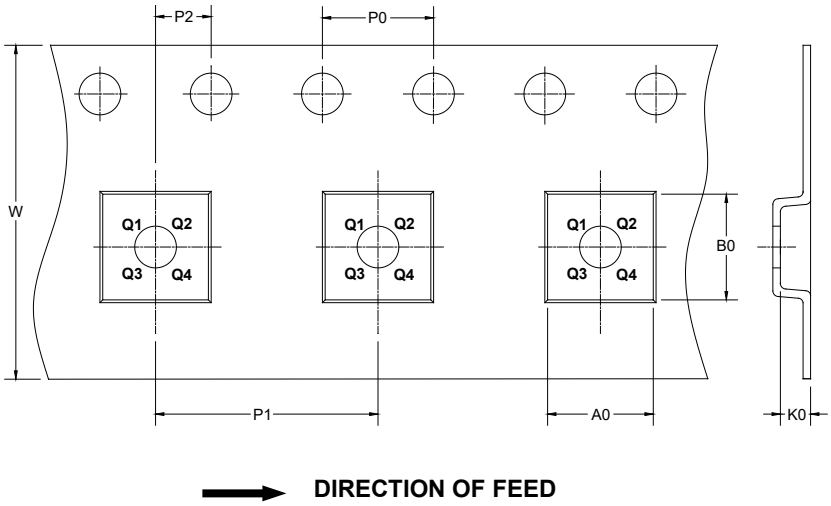
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	3.900	4.100	0.154	0.161
D1	2.600	2.800	0.102	0.110
E	3.900	4.100	0.154	0.161
E1	2.600	2.800	0.102	0.110
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



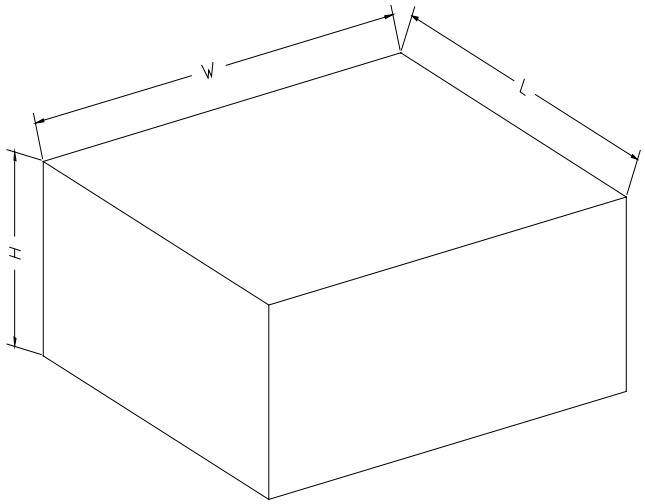
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-24L	13″	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002