SGM890BxQ
Voltage Detector with Separated Sense Pin and Delay Capacitor Pin

GENERAL DESCRIPTION

The SGM890BxQ is a low-power and high-accuracy voltage detector. The adjustable threshold is 1.0V and 3.0V, which greatly provides application flexibility.

Since the sense pin (VSEN) of the device is separated from the power supply pin, it can monitor other power supplies. And when the monitored power supply voltage drops to 0V, the device can also maintain the detection state.

In addition, the C_D pin of SGM890BxQ has an external capacitor connected to GND, which can adjust the release delay time. Consequently delay time can be set to more than 1s when the delay capacitor (C_D) is 1μF. The device is very suitable for applications in power sequencing, reset sequencing and power switching.

This device is AEC-Q100 qualified (Automotive Electronics Council Standard Q100 Grade 1) and the use of this device is suitable for automotive applications.

The SGM890BxQ is available in a Green SOT-23-5 package. It operates over the -40℃ to +125℃ temperature range.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Operating Voltage Range: 1V to 6V**
- **High Accuracy Detection: ±1% (TYP)**
- **Low Power Consumption: 0.4μA (TYP) at V_{IN} = 1V**
- **Detection Voltage: 1.0V and 3.0V**
- **Detection Voltage Temperature Coefficient: ±60ppm/℃ (TYP)**
- **Adjustable Release Delay Time**
- **Sense Pin Separates from Power Supply**
- **N-Channel Open-Drain Output**
- **Available in a Green SOT-23-5 Package**

APPLICATIONS

Power Sequencing and Reset Sequencing
Power Switching
Automotive Equipment
Portable Equipment
Computers/Servers

TYPICAL APPLICATION

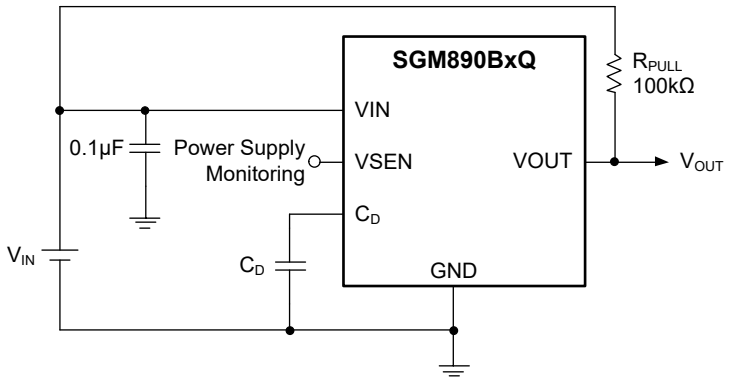


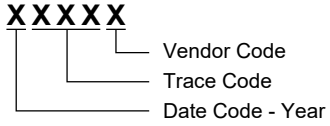
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	DETECTION VOLTAGE (V)	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM890B-1.0Q	1.0	SOT-23-5	-40℃ to +125℃	SGM890B-1.0QN5G/TR	0ZU XXXXX	Tape and Reel, 3000
SGM890B-3.0Q	3.0	SOT-23-5	-40℃ to +125℃	SGM890B-3.0QN5G/TR	0NY XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range, V_{IN} ..... GND - 0.3V to 7V
Output Current, I_{OUT} 30mA
Output Voltage Range, V_{OUT} ..... GND - 0.3V to 7V
VSEN Pin Voltage Range, V_{SEN} ..... GND - 0.3V to 7V
C_D Pin Voltage Range, V_{CD} ..... GND - 0.3V to V_{IN} + 0.3V
C_D Pin Current, I_{CD} 5mA
Package Thermal Resistance
SOT-23-5, θ_{JA} ..... 152.8℃/W
SOT-23-5, θ_{JB} ..... 41.9℃/W
SOT-23-5, θ_{JC} ..... 66.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±1500V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Operating Ambient Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

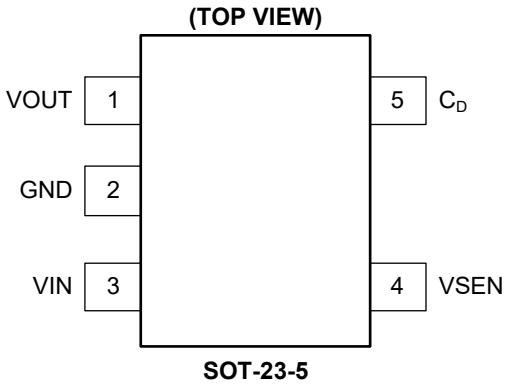
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

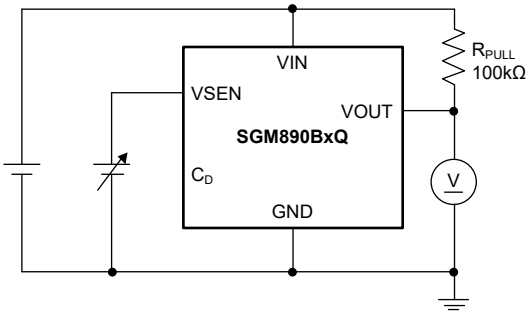
PIN	NAME	FUNCTION
1	VOUT	Active-Low Output Pin.
2	GND	Ground.
3	VIN	Supply Voltage Pin.
4	VSEN	Sense Pin.
5	C_D	Adjustable Delay Capacitor Pin.

ELECTRICAL CHARACTERISTICS

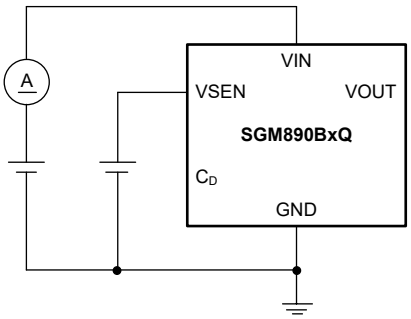
(T_A = -40℃ to +125℃, typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage	V_{IN}			1		6	V
Detection Voltage	V_{DET}	V_{IN} = 1V to 6V, R_{PULL} = 100kΩ, SGM890B-1.0Q	T_A = +25℃	0.990	1.0	1.010	V
			T_A = -40℃ to +125℃	0.980	1.0	1.020	V
		V_{IN} = 1V to 6V, R_{PULL} = 100kΩ, SGM890B-3.0Q	T_A = +25℃	2.970	3.0	3.030	V
			T_A = -40℃ to +125℃	2.940	3.0	3.060	V
Hysteresis Voltage	V_{HYS}	V_{IN} = 1V to 6V, R_{PULL} = 100kΩ, SGM890B-1.0Q		0.020	0.050	0.080	V
		V_{IN} = 1V to 6V, R_{PULL} = 100kΩ, SGM890B-3.0Q		0.078	0.150	0.222	V
Detection Voltage Line Regulation	$\Delta V_{DET}/(\Delta V_{IN} \times V_{DET})$	V_{IN} = 1V to 6V, R_{PULL} = 100kΩ (Test Circuit 1)			±0.03		%/V
Detection Voltage Temperature Coefficient	$\Delta V_{DET}/(\Delta T_A \times V_{DET})$	R_{PULL} = 100kΩ (Test Circuit 1)			±60	±150	ppm/℃
Supply Current	I_{CC}	(Test Circuit 2)	V_{IN} = 1V		0.4	0.9	μA
			V_{IN} = 3V		0.5	1.5	
			V_{IN} = 6V		0.7	1.7	
Output Current	I_{OUT}	V_{SEN} = 0V, V_{DS_NCH} = 0.5V (N-channel) (Test Circuit 3)	V_{IN} = 1V	0.09	0.8		mA
			V_{IN} = 2V	7.5	12.0		
			V_{IN} = 3V	11.5	17.5		
			V_{IN} = 4V	13.5	20.5		
			V_{IN} = 5V	15.0	22.0		
			V_{IN} = 6V	16.0	23.0		
Leakage Current	I_{LEAK}	V_{IN} = V_{SEN} = V_{OUT} = 6V, C_D: Open (Test Circuit 3)			0.001	2.0	μA
Sense Resistance	R_{SEN}	V_{SEN} = 5V, V_{IN} = 0V (Test Circuit 4)		21	28	34	MΩ
Delay Resistance	R_{DELAY}	V_{SEN} = 6V, V_{IN} = 5V, V_{CD} = 0V (Test Circuit 5)		1.65	2.2	2.75	MΩ
Delay Capacitance Pin Sink Current	I_{CD}	V_{CD} = 0.5V, V_{IN} = 1V (Test Circuit 5)		50	230	420	μA
Delay Capacitance Pin Threshold Voltage	V_{TCD}	V_{SEN} = 6V, R_{PULL} = 100kΩ (Test Circuit 6)	V_{IN} = 1.0V	0.4	0.5	0.7	V
			V_{IN} = 6.0V	2.9	3.0	3.2	
Detection Delay Time	t_{DF0}	V_{IN} = 6.0V, V_{SEN} = 1.5 × V_{DET} to 0V, C_D: Open, R_{PULL} = 100kΩ (Test Circuit 7)			30	90	μs
Release Delay Time	t_{DR0}	V_{IN} = 6.0V, V_{SEN} = 0V to 1.5 × V_{DET}, C_D: Open, R_{PULL} = 100kΩ (Test Circuit 7)			60	150	μs

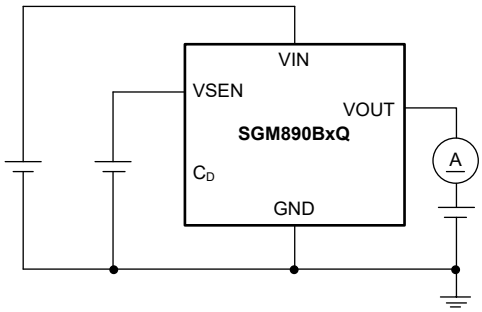
TEST CIRCUITS



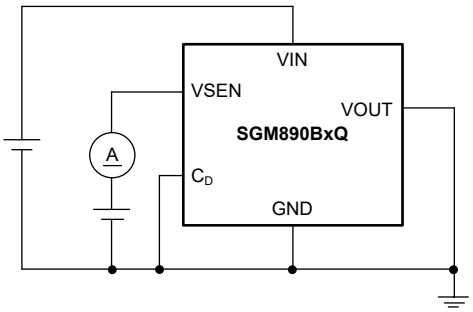
Test Circuit 1



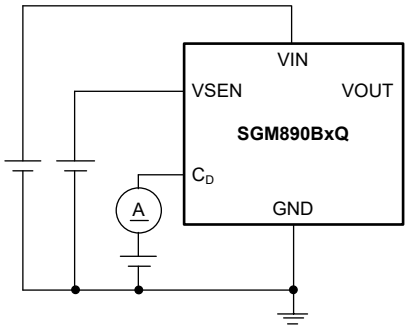
Test Circuit 2



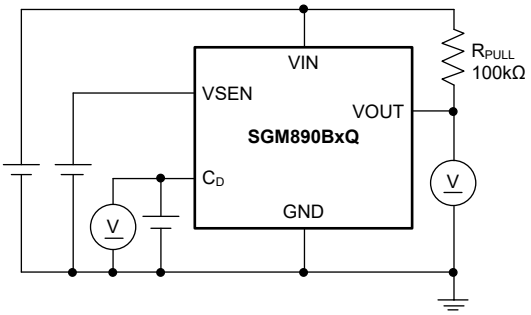
Test Circuit 3



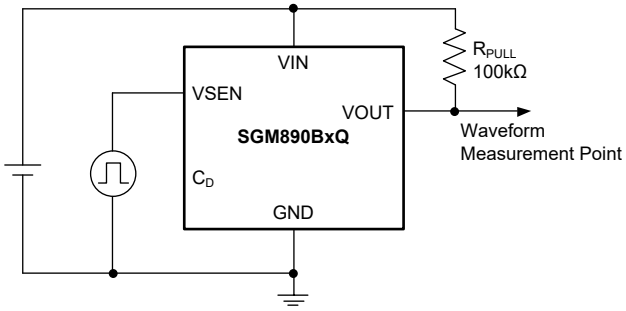
Test Circuit 4



Test Circuit 5



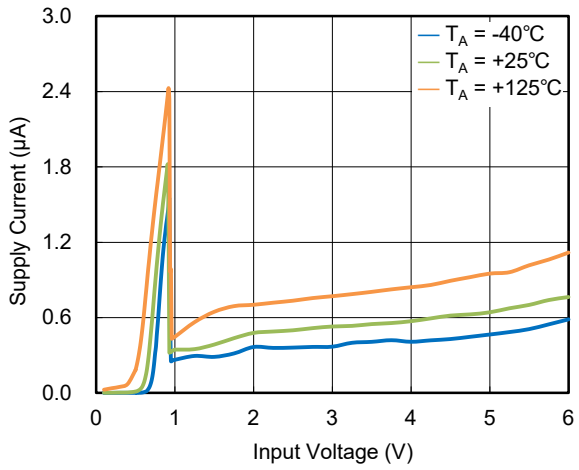
Test Circuit 6



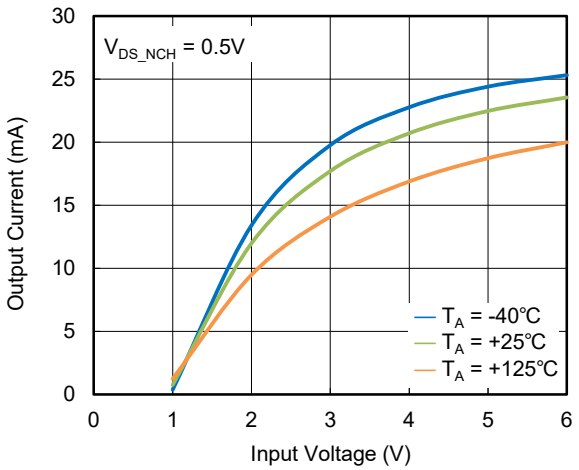
Test Circuit 7

TYPICAL PERFORMANCE CHARACTERISTICS

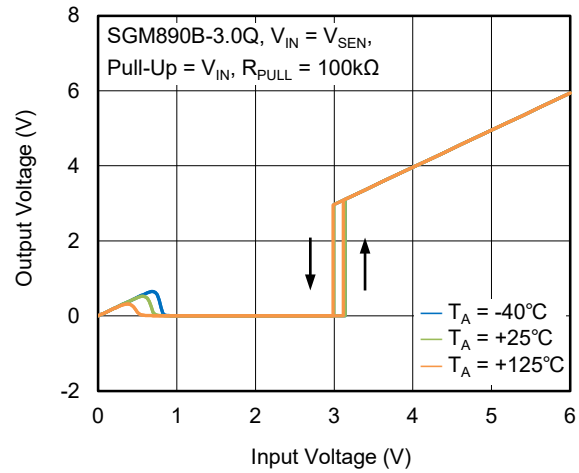
Supply Current vs. Input Voltage



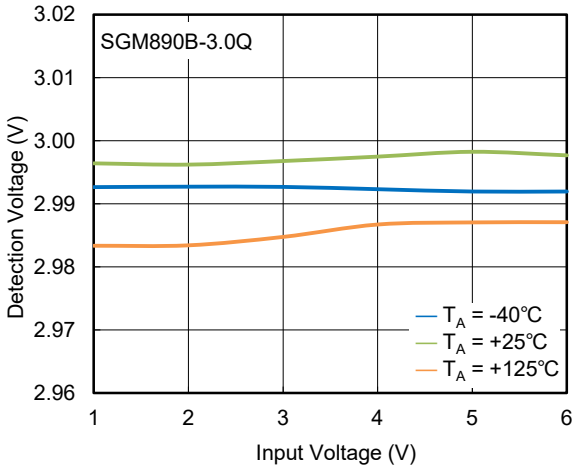
Output Current vs. Input Voltage



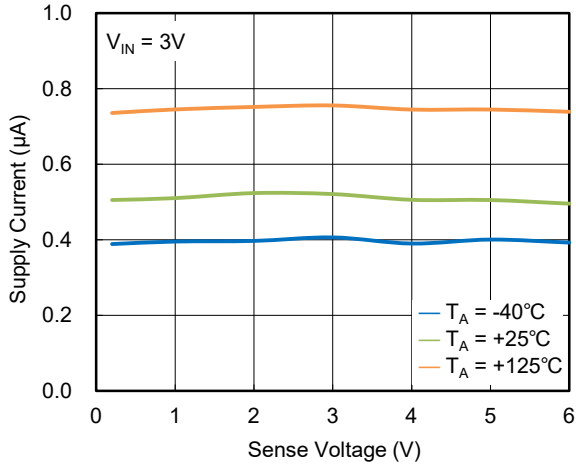
Output Voltage vs. Input Voltage



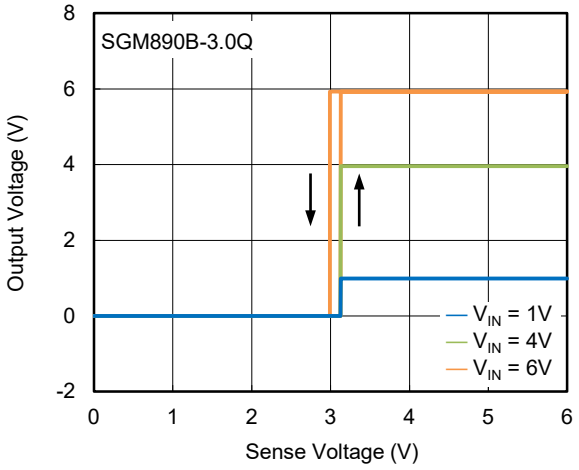
Detection Voltage vs. Input Voltage



Supply Current vs. Sense Voltage

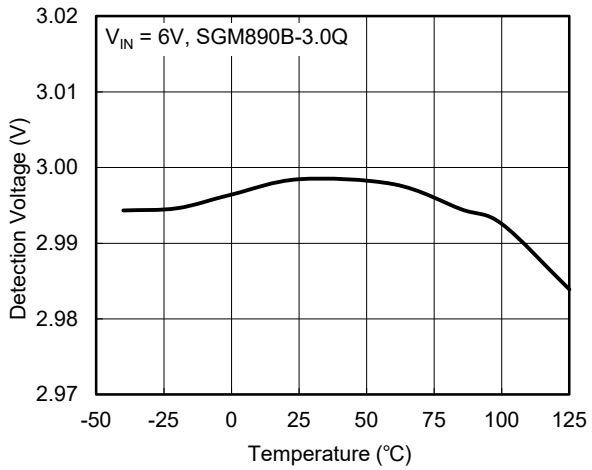


Output Voltage vs. Sense Voltage

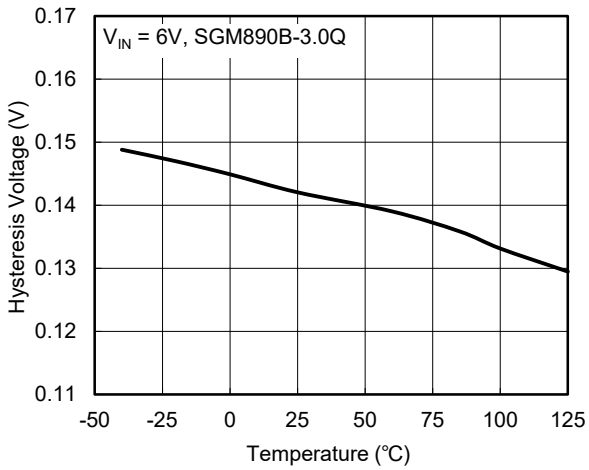


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

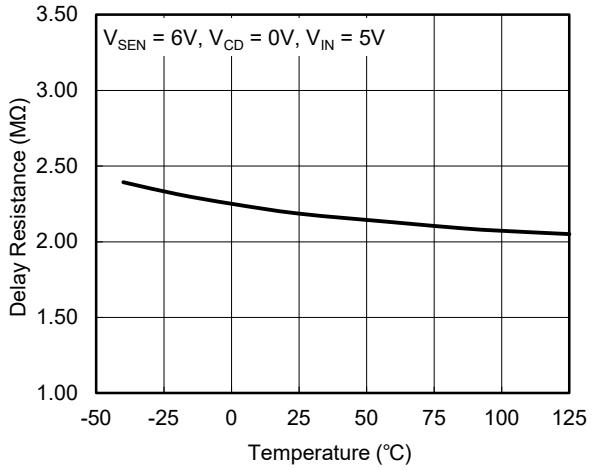
Detection Voltage vs. Temperature



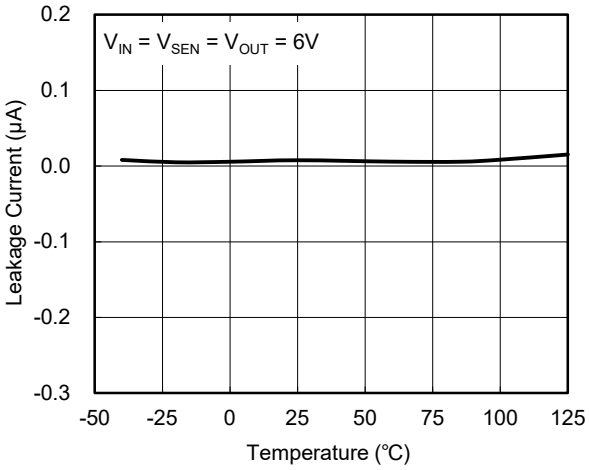
Hysteresis Voltage vs. Temperature



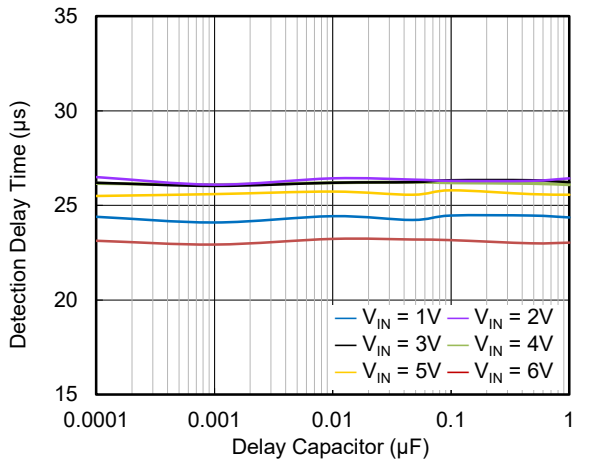
Delay Resistance vs. Temperature



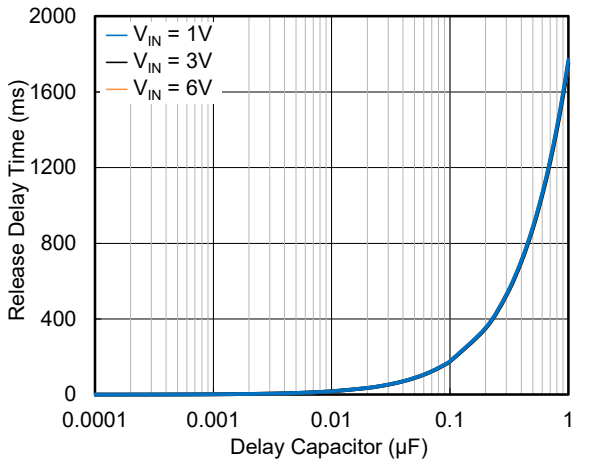
Leakage Current vs. Temperature



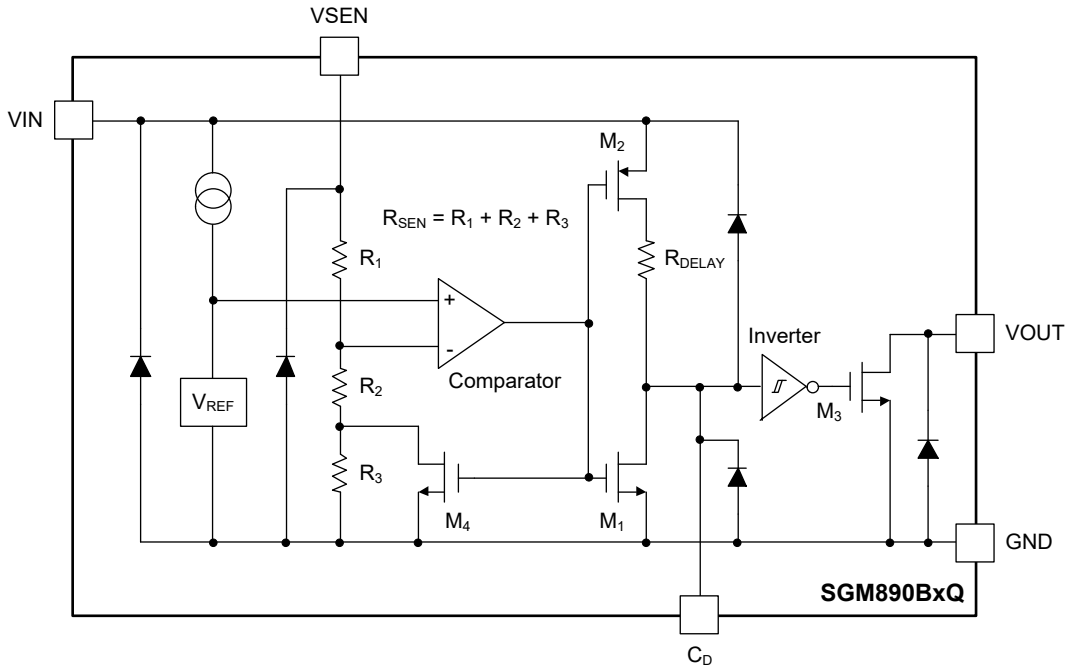
Detection Delay Time vs. Delay Capacitance



Release Delay Time vs. Delay Capacitance



FUNCTIONAL BLOCK DIAGRAM



NOTE: Diodes inside the circuits are ESD protection diodes and parasitic diodes.

Figure 2. SGM890BxQ Block Diagram

DETAILED DESCRIPTION

Typical Application

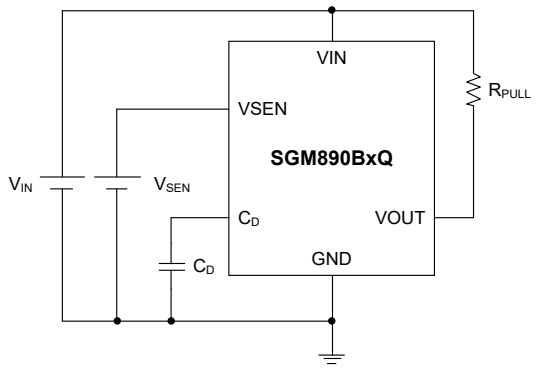


Figure 3. Typical Application Circuit of SGM890BxQ

The output voltage (V_{OUT}) transition, the delay capacitance (C_D) charge and discharge are determined by the status of power supply and the sense pin voltage (V_{SEN}). Figure 4 is the timing chart of Figure 3. It may go through seven processes, and below words are shown as the description of the sequence.

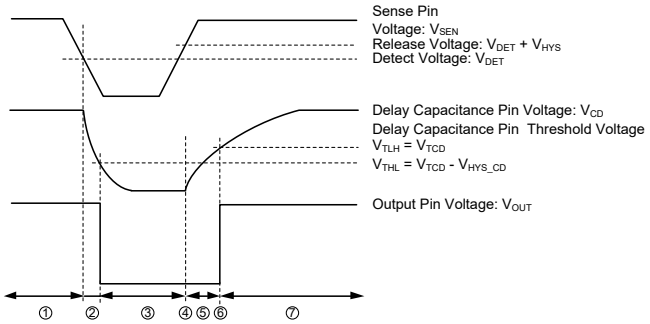


Figure 4. Timing Chart

① Default Status before V_{IN} Falling

In original state, the delay capacitance voltage (V_{CD}) is charged to the input voltage (V_{IN}), which ranges from 1V to 6V.

In the beginning, V_{SEN} is larger than the detection voltage (V_{DET}) plus the hysteresis (V_{HYS}). While V_{SEN} starts dropping but still larger than V_{DET}, V_{OUT} keeps the high level (= V_{IN}).

NOTE: The high level voltage is determined by the power rail to which the pull-up resistor at V_{OUT} is connected.

② Triggered V_{DET} while V_{SEN} Falling

When V_{SEN} drops below V_{DET}, an N-ch transistor (M_1) is turned on to discharge the delay capacitor.

An internal inverter connected to the C_D pin is used as a comparator, where the high threshold $V_{TLH} = V_{TCD}$ and low-level threshold $V_{THL} = V_{TCD} - V_{HYS\_CD}$. Once V_{CD} drops to V_{THL}, the inverter state is toggled and V_{OUT} turns to logic low (= GND).

③ V_{OUT} Keeps Low until V_{SEN} Rises

V_{CD} is fully discharged to GND and V_{SEN} is below V_{DET}. Hence, V_{OUT} keeps logic low unless V_{SEN} increases to $V_{DET} + V_{HYS}$ again.

④ V_{SEN} Rising up to $V_{DET} + V_{HYS}$

The N-channel transistor (M_1) for the delay capacitance discharge will be turned off, and the delay capacitance will be charged via a delay resistor (R_{DELAY}), when V_{SEN} turns to be larger than $V_{DET} + V_{HYS}$.

⑤ C_D is Charged when V_{SEN} Keeps High

Once V_{CD} is above V_{TCD}, when V_{SEN} increases to $V_{DET} + V_{HYS}$ or higher, the C_D capacitor is charged with the time constant determined by R_{DELAY} and C_D. Thus, the release delay time (t_{DR}) can be given as:

$$t_{DR} = R_{DELAY} \times C_D \times 0.79 \quad (1)$$

where R_{DELAY} is 2.2MΩ (TYP).

Take C_D = 0.68μF as an example, t_{DR} is:

$$2.2 \times 10^6 \times 0.68 \times 10^{-6} \times 0.79 = 1182 \text{ (ms)}$$

NOTE: Because the time described in ③ is very short, t_{DR} may be relatively short when V_{CD} is not strictly discharged to GND.

⑥ V_{OUT} Goes High when C_D is Charged Full

When the C_D pin voltage reaches the C_D pin rising logic threshold voltage (= V_{TCD}), the inverter output will be inverted. As a result, V_{OUT} changes into the high level (= V_{IN}). The release delay time without C_D (t_{DR0}) is defined as time which ranges from $V_{SEN} = V_{DET} + V_{HYS}$ to the V_{OUT} of high level with unconnected C_D pin.

⑦ V_{OUT} Keeps High when $V_{SEN} > V_{DET}$

The C_D pin is charged until the V_{CD} increases to the input voltage level, when the sense pin voltage is higher than the detection voltage ($V_{SEN} > V_{DET}$). Therefore, V_{OUT} maintains the high level (= V_{IN}).

DETAILED DESCRIPTION (continued)

The V_{OUT} status is determined by the V_{SEN} and V_{CD}. A summary table of transitions about V_{OUT} is shown below.

Table 1. Function Chart

V_{SEN}	V_{CD}	Transition of V_{OUT} Condition (1)		
		①	⇒	②
L	L	L	⇒	L
	H			
	L	H		
	H			
H	L	L	⇒	L
	H		⇒	H
	L	H	⇒	
	H			

NOTE:
1. V_{OUT} transits from condition ① to ② because of the combination of V_{SEN}, V_{CD} and V_{IN}. V_{IN} should exceed the lowest operation voltage.

Examples:

(1). V_{OUT} ranges from 'L' to 'H' in the case of V_{SEN} = 'H' ($V_{SEN} \geq V_{DET} + V_{HYS}$), V_{CD} = 'H' ($V_{CD} \geq V_{TCD}$) while V_{OUT} is 'L'.

(2). V_{OUT} maintains 'H' when V_{CD} ranges from 'H' to 'L' ($V_{CD} \leq V_{TCD} - V_{HYS\_CD}$), V_{SEN} = 'H' and V_{CD} = 'L' when V_{OUT} becomes 'H' in example (1).

The release delay time is adjustable by the external capacitor C_D. The t_{DR} values for common ideal capacitors are shown below.

Table 2. Release Delay Time Chart

Delay Capacitance (C_D) (μF)	Release Delay Time (t_{DR}) (TYP) (ms)
0.010	17.4
0.022	38.2
0.047	81.7
0.100	174
0.220	382
0.470	817
1.000	1740

NOTE: The t_{DR} values above are calculated by the Equation 1.

APPLICATION INFORMATION

1. Do not exceed the absolute maximum ratings. For temporary transitional voltage drop or voltage rising phenomenon, the IC may fail if the rated value is exceeded.

2. Be careful with the input pin voltage at IC side. It may be affected by the resistor between the power supply and IC, and input operation current. The IC cannot operate correctly once the input pin voltage at IC side is smaller than the minimum operating voltage.

3. If the voltage to be sensed is lower than 1V, please apply different voltage to VIN and V_{SEN}, and apply voltage higher than 1V to VIN.

4. Pay attention to errors that might be caused by the input voltage variations. To solve this problem, a decouple capacitor is needed (e.g. 0.1μF or larger).

5. In case of fast VIN drop condition from 6V to 0V at release condition with a capacitor connected to the C_D pin, please place a Schottky barrier diode between the VIN pin and the C_D pin (see Figure 5).

6. The output pin of SGM890BxQ is an open-drain NMOS. Consequently, the V_{OUT} voltage at detection and release condition is determined by resistance of a pull-up resistor and ON/OFF resistance of the NMOS. Choose suitable resistance of the pull-up resistor according to Figure 6.

During detection, the formula is given as:

$$V_{OUT} = V_{PULL}/(1 + R_{PULL}/R_{ON}) \quad (2)$$

where:
V_{PULL} is the pull-up voltage.
R_{ON} (1) is the on-resistance of N-channel driver M_3 that can be calculated as V_{DS_NCH}/I_{OUT} from electrical characteristics.

For example, when R_{ON} (2) = $0.5/(0.8 \times 10^{-3}) = 625\Omega$ (MIN) at V_{IN} = 1V, V_{PULL} = 3V and $V_{OUT} \leq 0.1$V at detection, R_{PULL} can be calculated as follows:

$R_{PULL} = (V_{PULL}/V_{OUT} - 1) \times R_{ON} = (3/0.1 - 1) \times 625 \approx 18k\Omega$

APPLICATION INFORMATION (continued)

In this case, R_{PULL} should be selected higher than or equal to 18kΩ in order to keep the output voltage less than 0.1V during detection.

NOTES:

1. R_{ON} is bigger when V_{IN} is smaller.
2. For calculation, choose the minimum V_{IN} value among the input voltage range.

During releasing, the formula is given as:

$$V_{OUT} = V_{PULL}/(1 + R_{PULL}/R_{OFF}) \quad (3)$$

where:

V_{PULL} is the pull-up voltage.

R_{OFF} is the off-resistance of N-channel driver M_3 that is 15MΩ (MIN) when the driver is off (as to V_{OUT}/I_{LEAK}).

For example, when V_{PULL} = 6V and V_{OUT} ≥ 5.99V, R_{PULL} can be calculated as follows:

$R_{PULL} = (V_{PULL}/V_{OUT} - 1) \times R_{OFF} = (6/5.99 - 1) \times 15 \times 10^6 \approx 25k\Omega$

It is recommended to select the R_{PULL} smaller or equal to 25kΩ so that the output voltage can be higher than 5.99V during releasing.

7. SGMICRO is committed to product improvement and reliability. Users are required to incorporate fail-safe designs and post-aging protection treatment in their systems.

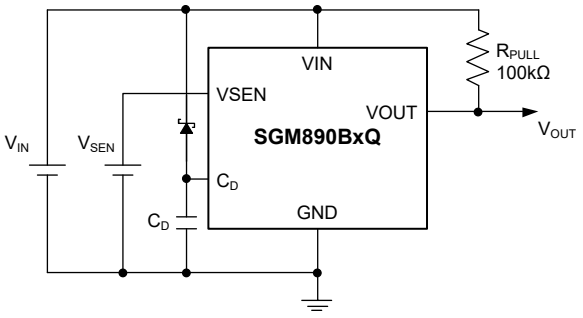
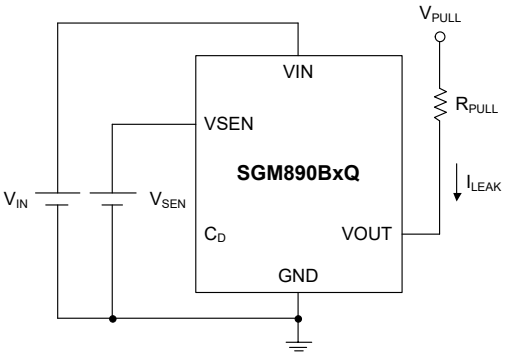


Figure 5. Circuit Example with C_D Pin Connected to a Schottky Barrier Diode of SGM890BxQ



NOTE: $R_{OFF} = V_{OUT}/I_{LEAK}$.

Figure 6. Circuit Example of SGM890BxQ

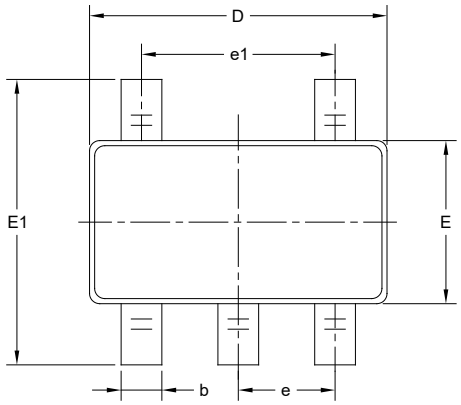
REVISION HISTORY

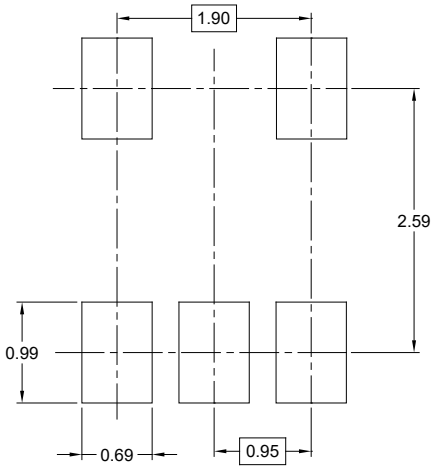
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

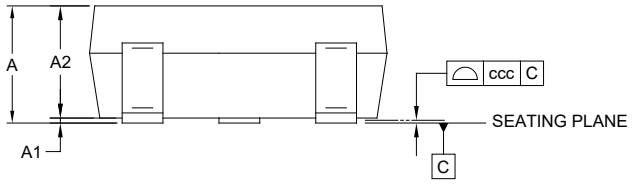
PACKAGE OUTLINE DIMENSIONS

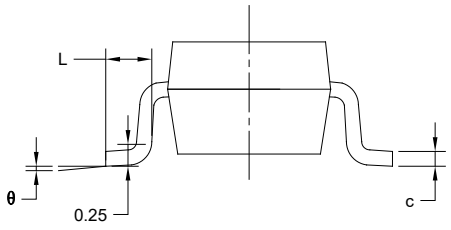
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



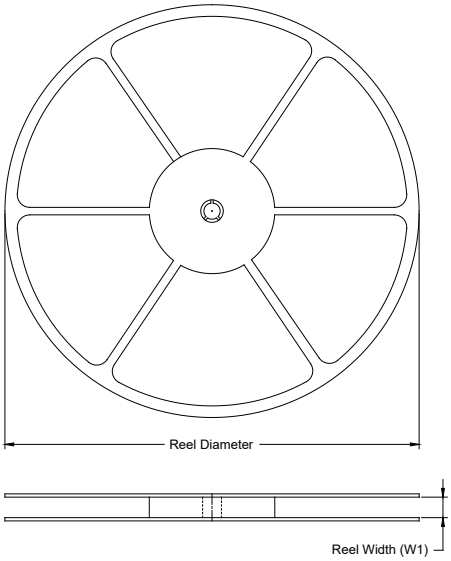


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

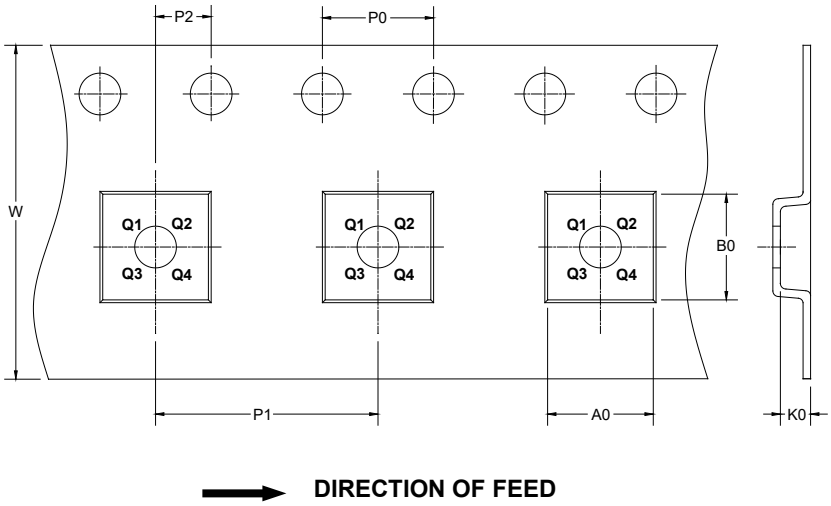
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

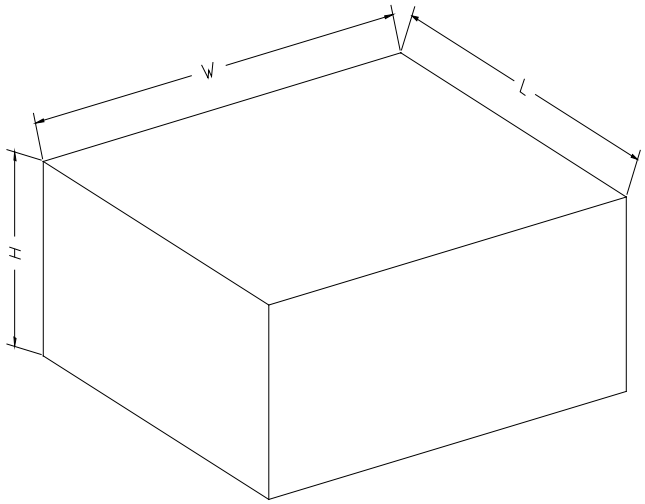
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002