SGM8969-1/SGM8969-2

1.1mA, 50MHz, High Precision, Rail-to-Rail I/O, Low Noise, G ≥ 10 Stable CMOS Operational Amplifiers

GENERAL DESCRIPTION

The SGM8969-1/2 are a family of single and dual rail-to-rail input and output operational amplifiers, which are optimized for low voltage, low noise and high precision operation. These devices can operate from 1.8V to 5.5V single supply, while consuming only 1.1mA quiescent current per amplifier at 5.5V.

The SGM8969-1/2 feature a 240μV maximum input offset. They exhibit a high gain-bandwidth product of 50MHz and a slew rate of 20V/μs. These specifications make the operational amplifiers appropriate for various applications.

The SGM8969-1 is available in a Green SOT-23-5 package. The SGM8969-2 is available in Green SOIC-8 and TDFN-3×3-8L packages. They are specified over the extended industrial temperature range (-40℃ to +125℃).

FEATURES

- **Input Offset Voltage: 240μV (MAX)**
- **High Gain-Bandwidth Product: 50MHz**
- **High Slew Rate: 20V/μs**
- **Settling Time to 0.1% with 2V Step: 500ns**
- **Overload Recovery Time: 50ns**
- **Low Noise: 8nV/$\sqrt{Hz}$ at 10kHz**
- **Gain 10 Stable**
- **Rail-to-Rail Input and Output**
- **Supply Voltage Range: 1.8V to 5.5V**
- **Input Voltage Range: -0.1V to 5.6V with V_S = 5.5V**
- **Low Power: 1.1mA/Amplifier (TYP) Supply Current**
- **-40℃ to +125℃ Operating Temperature Range**
- **Small Packaging:**
  SGM8969-1 Available in a Green SOT-23-5 Package
  SGM8969-2 Available in Green SOIC-8 and TDFN-3×3-8L Packages

APPLICATIONS

Sensor
Audio
Active Filter
A/D Converter
Communication
Test Equipment
Cellular and Cordless Phone
Laptop and PDA
Photodiode Amplification
Battery-Powered Instrumentation

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8969-1	SOT-23-5	-40℃ to +125℃	SGM8969-1XN5G/TR	MB8XX	Tape and Reel, 3000
SGM8969-2	SOIC-8	-40℃ to +125℃	SGM8969-2XS8G/TR	SGM 89692XS8 XXXXX	Tape and Reel, 4000
	TDFN-3×3-8L	-40℃ to +125℃	SGM8969-2XTDB8G/TR	SGM 89692DB XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XX = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

SOT-23-5

YYY X X
- X — Date Code - Week
- X — Date Code - Year
- YYY — Serial Number

SOIC-8/TDFN-3×3-8L

X XXX X
- X — Vendor Code
- XXX — Trace Code
- X — Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 6V
Input Common Mode Voltage Range
.... $(-V_S) - 0.3V$ to $(+V_S) + 0.3V$
Junction Temperature .... +150℃
Storage Temperature Range .... -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility
HBM 7000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range .... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

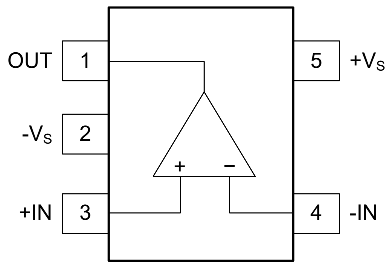
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

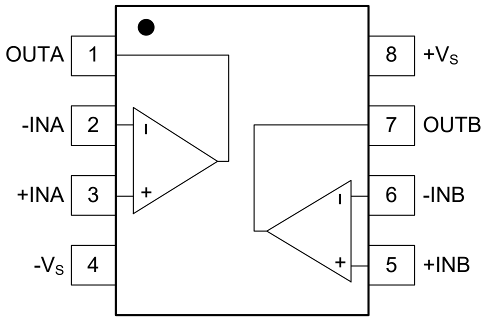
PIN CONFIGURATIONS

SGM8969-1 (TOP VIEW)



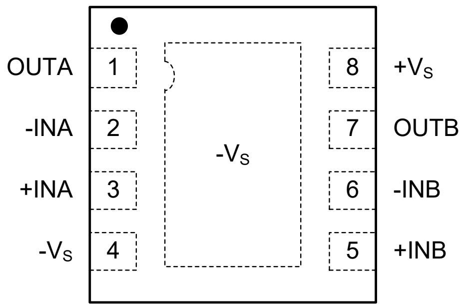
SOT-23-5

SGM8969-2 (TOP VIEW)



SOIC-8

SGM8969-2 (TOP VIEW)



TDFN-3×3-8L

NOTE: For TDFN-3×3-8L package, connect exposed pad to $-V_S$.

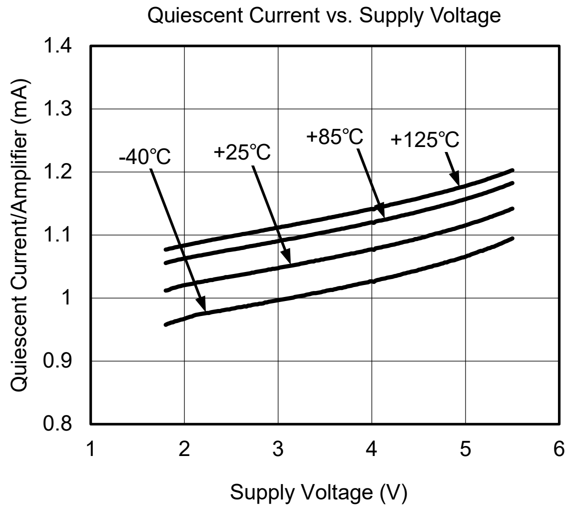
ELECTRICAL CHARACTERISTICS

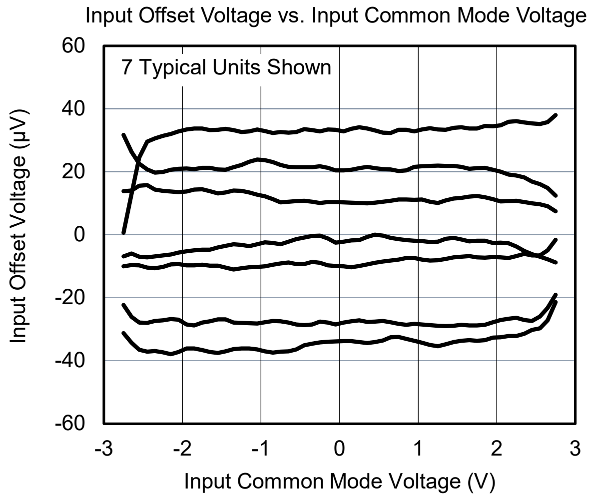
(At T_A = +25℃, V_S = 1.8V to 5.5V or ±0.9V to ±2.75V, V_{CM} = V_S/2 and R_L = 10kΩ connected to V_S/2, Full = -40℃ to +125℃, unless otherwise noted.)

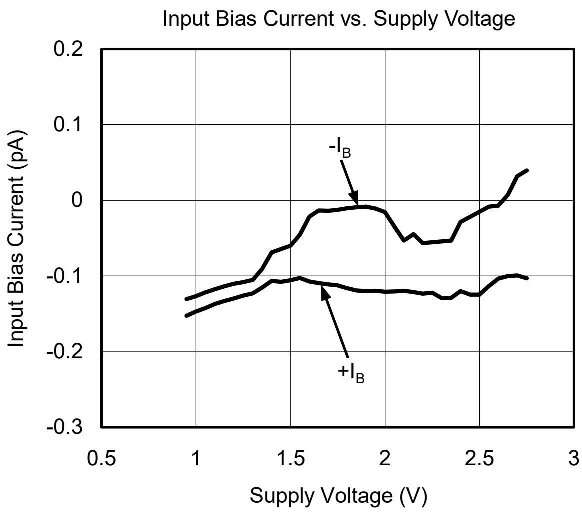
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}		+25℃		50	240	μV
			Full			750	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	V_S = ±2.75V	Full		1		μV/℃
Input Bias Current	I_B		+25℃		6	120	pA
			Full			4000	
Input Offset Current	I_{OS}		+25℃		6	120	pA
			Full			1000	
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S)$ - 0.1		$(+V_S)$ + 0.1	V
Common Mode Rejection Ratio	CMRR	V_S = 5.5V, V_{CM} = -0.1V to 5.6V	+25℃	84	102		dB
			Full	81			
		V_S = 1.8V, V_{CM} = -0.1V to 1.9V	+25℃	76	95		
			Full	73			
Open-Loop Voltage Gain	A_{OL}	V_S = ±0.9V, R_L = 1kΩ, $(-V_S)$ + 0.25V < V_{OUT} < $(+V_S)$ - 0.25V	+25℃	91	117		dB
			Full	88			
		V_S = ±2.75V, R_L = 1kΩ, $(-V_S)$ + 0.25V < V_{OUT} < $(+V_S)$ - 0.25V	+25℃	102	128		
			Full	99			
		V_S = ±0.9V, R_L = 10kΩ, $(-V_S)$ + 0.15V < V_{OUT} < $(+V_S)$ - 0.15V	+25℃	94	118		
			Full	91			
		V_S = ±2.75V, R_L = 10kΩ, $(-V_S)$ + 0.15V < V_{OUT} < $(+V_S)$ - 0.15V	+25℃	102	127		
			Full	99			
Output Characteristics							
Output Voltage Swing from Rail	V_{OUT}	V_S = 5.5V, R_L = 1kΩ	+25℃		60	75	mV
			Full			80	
		V_S = 5.5V, R_L = 10kΩ	+25℃		12	18	
			Full			20	
Output Current (I_{OUT})	I_{OUT}	V_S = 5.5V	+25℃	30	50		mA
			Full	12			
Power Supply							
Operating Voltage Range	V_S		Full	1.8		5.5	V
Power Supply Rejection Ratio	PSRR	V_S = 1.8V to 5.5V, V_{CM} = $(-V_S)$ + 0.5V	+25℃	89	106		dB
			Full	86			
Quiescent Current/Amplifier	I_Q	I_{OUT} = 0	+25℃		1.1	1.55	mA
			Full			1.6	
Dynamic Performance							
Gain-Bandwidth Product	GBP	V_S = 5V	+25℃		50		MHz
Phase Margin	φ_O	V_S = 5V	+25℃		60		°
Slew Rate	SR	V_S = 5V, G = +10, 2V output step	+25℃		20		V/μs
Settling Time to 0.1%	t_S	V_S = 5V, G = +10, 2V output step	+25℃		500		ns
Overload Recovery Time		V_S = 5V, V_{IN} × G = V_S	+25℃		50		ns
Noise Performance							
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		20		$nV/\sqrt{Hz}$
		f = 10kHz	+25℃		8		

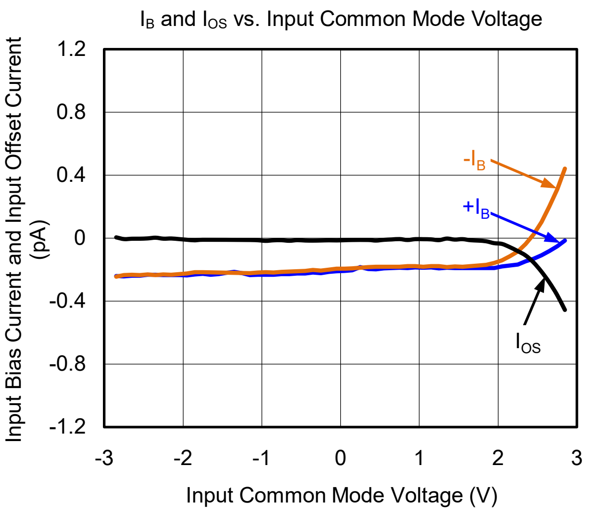
TYPICAL PERFORMANCE CHARACTERISTICS

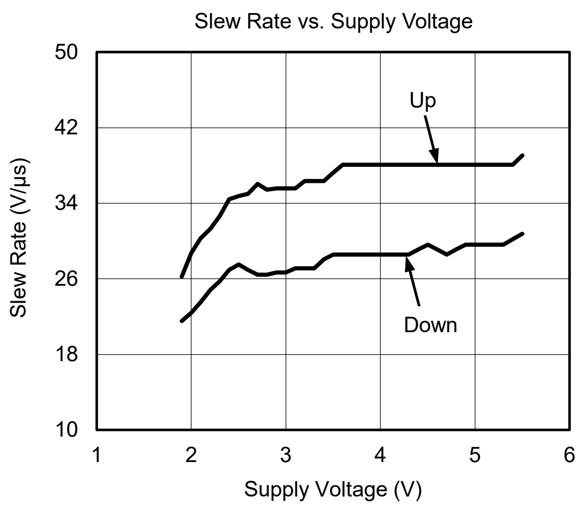
At T_A = +25℃, V_S = ±2.75V and R_L = 10kΩ, unless otherwise noted.

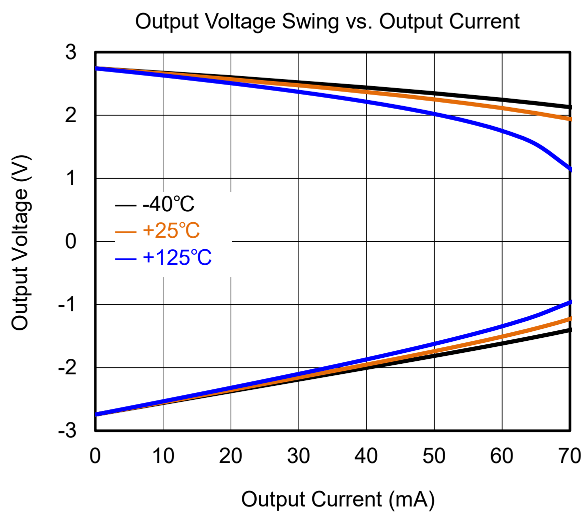






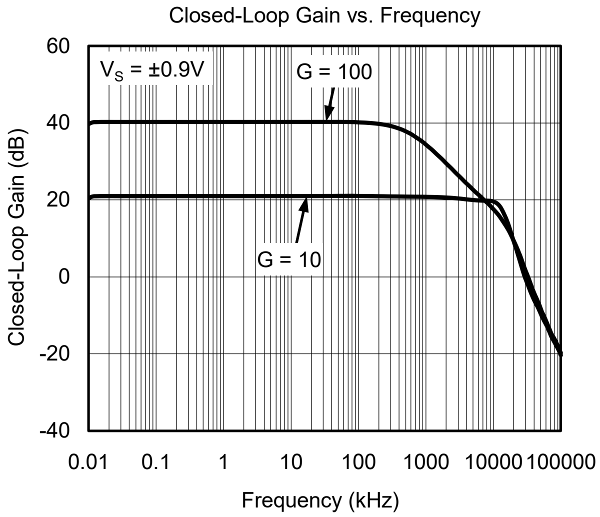


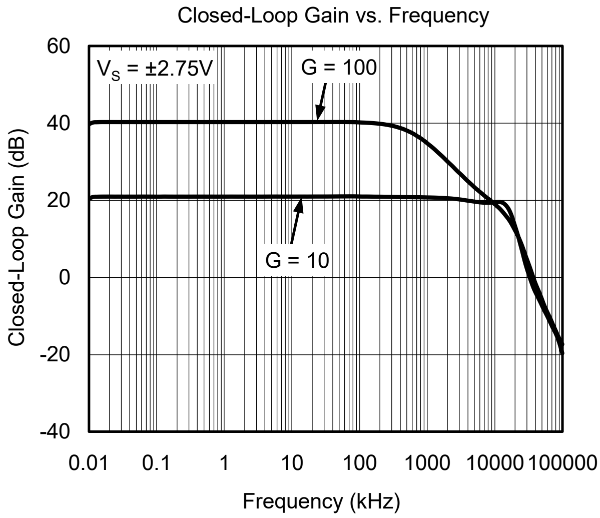


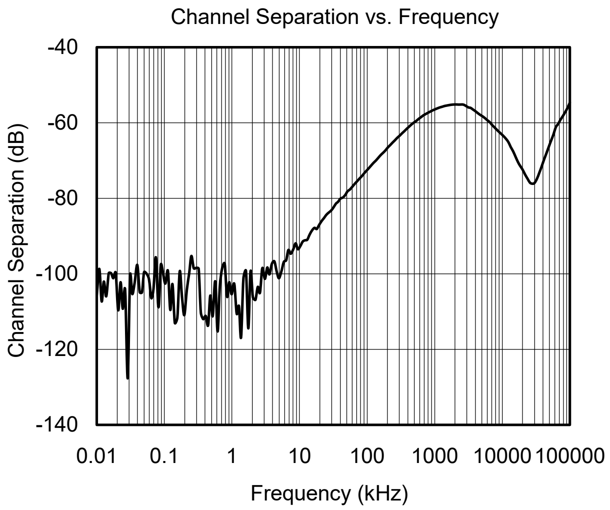


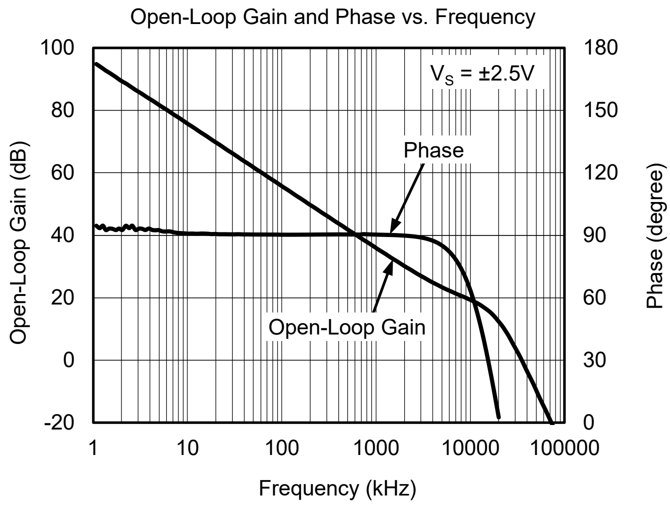
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

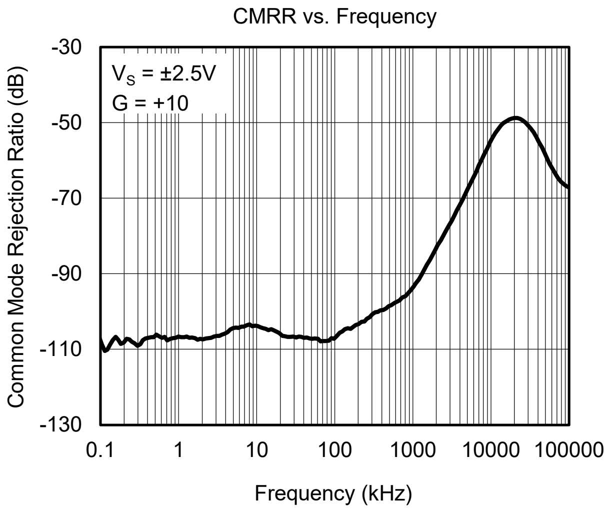
At T_A = +25℃, V_S = ±2.75V and R_L = 10kΩ, unless otherwise noted.

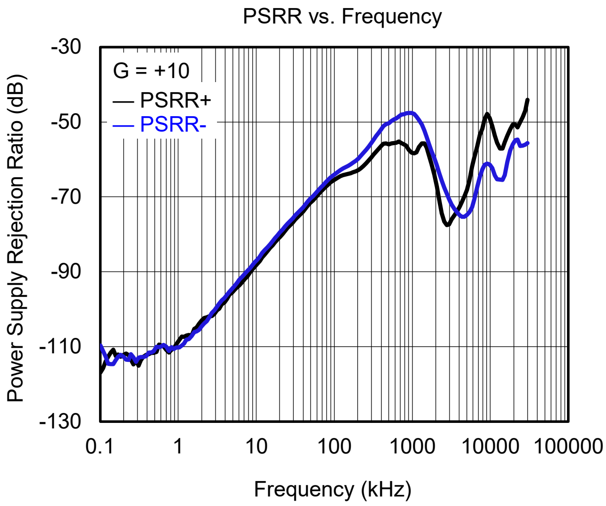






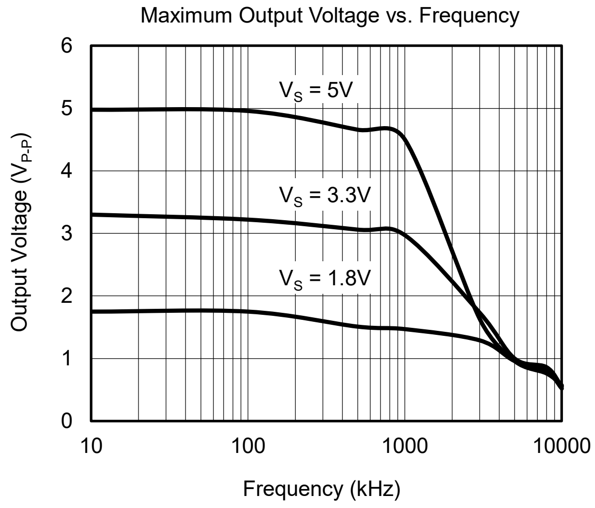


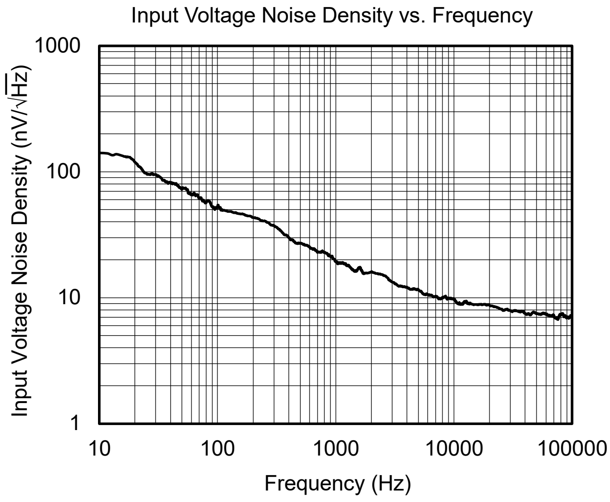


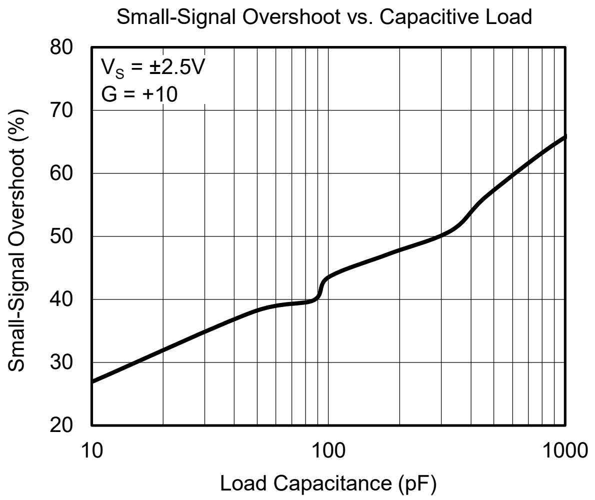


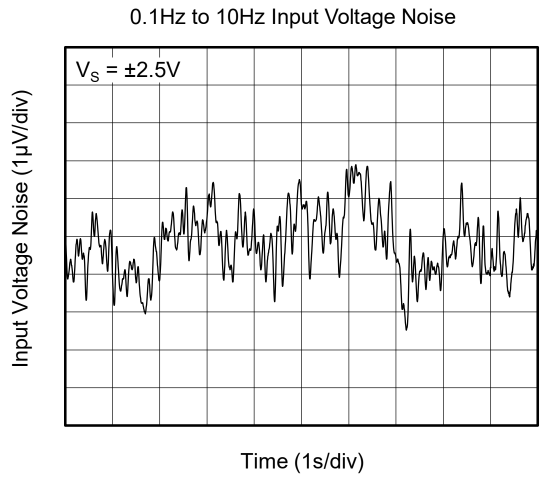
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

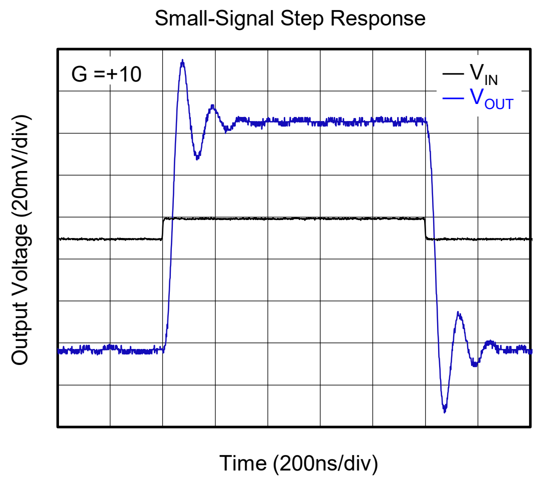
At T_A = +25℃, V_S = ±2.75V and R_L = 10kΩ, unless otherwise noted.

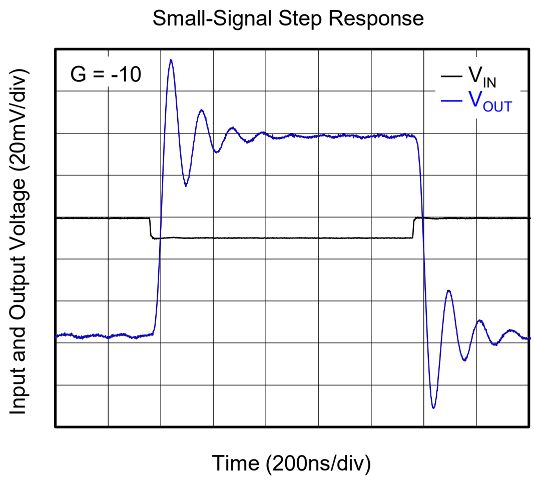








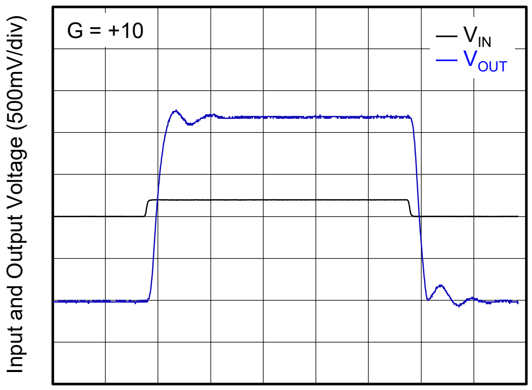




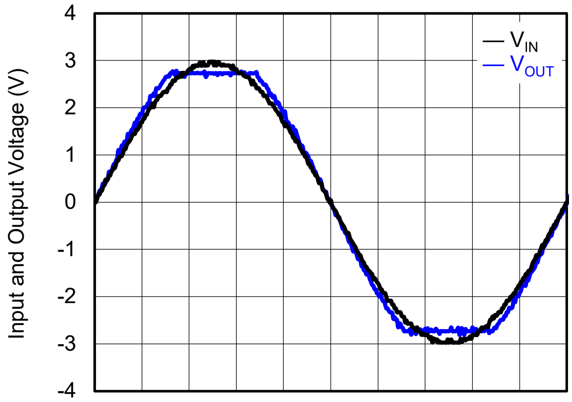
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±2.75V and R_L = 10kΩ, unless otherwise noted.

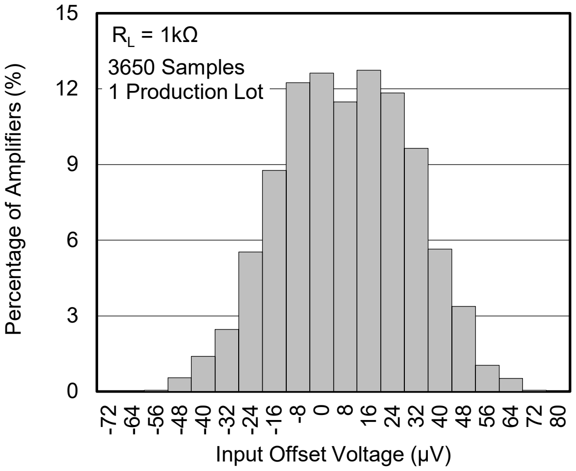
Large-Signal Step Response



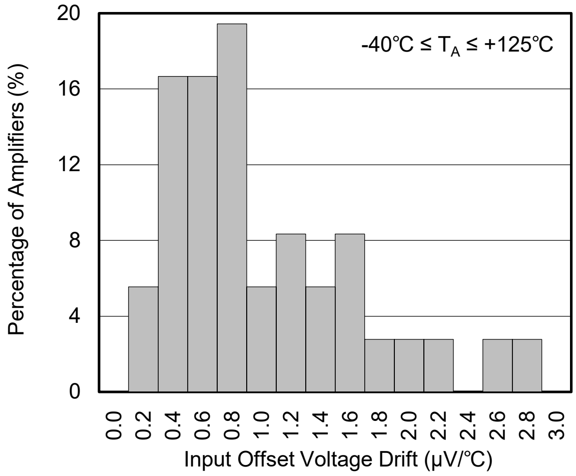
No Phase Reversal



Input Offset Voltage Production Distribution



Input Offset Voltage Drift Distribution



APPLICATION INFORMATION

Rail-to-Rail Input

When SGM8969-1/2 work at the power supply between 1.8V and 5.5V, the input common mode voltage range is from (-V_S) - 0.1V to (+V_S) + 0.1V. In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage not to exceed the rails.

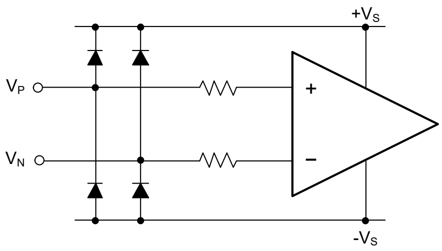


Figure 1. Input Equivalent Circuit

Input Current-Limit Protection

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 2, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is that it contributes thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

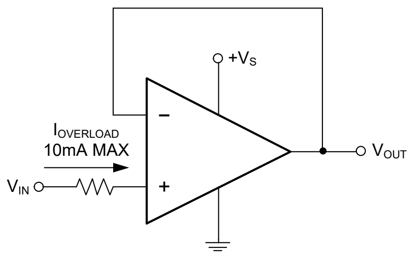


Figure 2. Input Current-Limit Protection

Rail-to-Rail Output

The SGM8969-1/2 support rail-to-rail output operation. In single power supply application, for example, when +V_S = 5.5V, -V_S = GND, 10kΩ load resistor is tied from OUT pin to V_S/2, the typical output swing range is from 0.012V to 5.488V.

Driving Capacitive Loads

The SGM8969-1/2 are designed for gain 10 stable for capacitive load up to 470pF. If greater capacitive load must be driven in application, the circuit in Figure 3 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

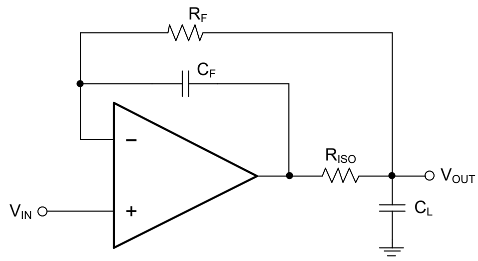


Figure 3. Circuit to Drive Heavy Capacitive Load

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design, besides of input signal noise, the power supply is one of important source of noise to the amplifiers through +V_S and -V_S pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 4. The ceramic capacitors should be placed as close as possible to +V_S and -V_S power supply pins.

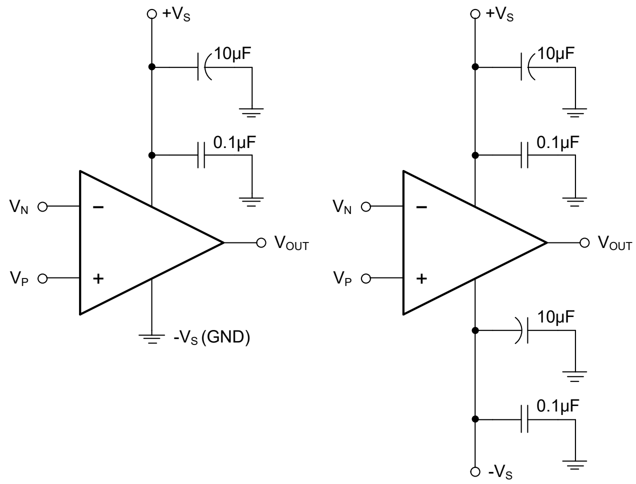


Figure 4. Amplifier Power Supply Bypassing

APPLICATION INFORMATION (continued)

Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

Typical Application Circuits

Difference Amplifier

The circuit in Figure 5 is a design example of classical difference amplifier. If $R_4/R_3 = R_2/R_1$, then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

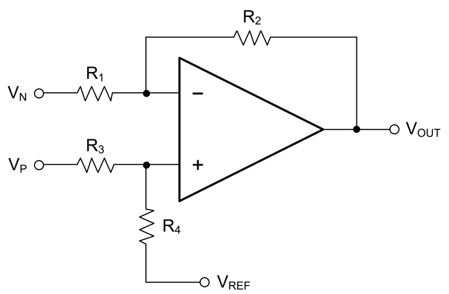


Figure 5. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 6 is a design example of high input impedance difference amplifier, the added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 5.

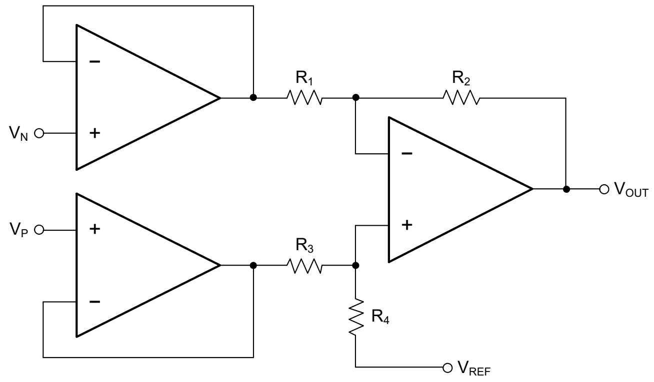


Figure 6. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The circuit in Figure 7 is a design example of active low-pass filter, the DC gain is equal to $-R_2/R_1$ and the -3dB corner frequency is equal to $1/2\pi R_2C$. In this design, the filter bandwidth must be less than the bandwidth of the amplifier, the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

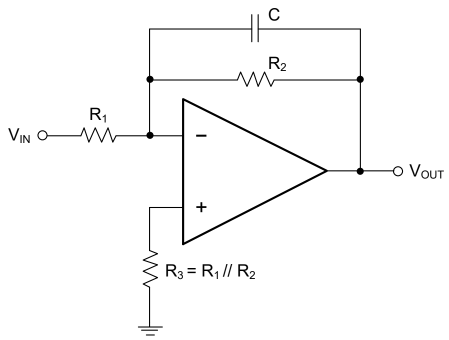


Figure 7. Active Low-Pass Filter

REVISION HISTORY

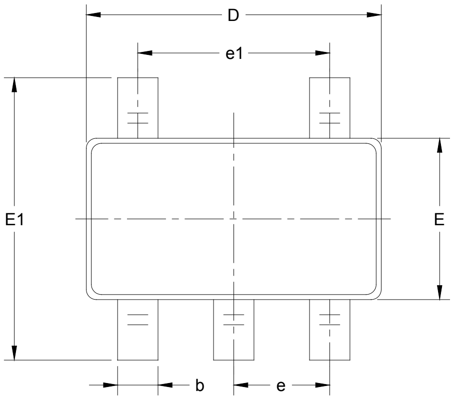
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

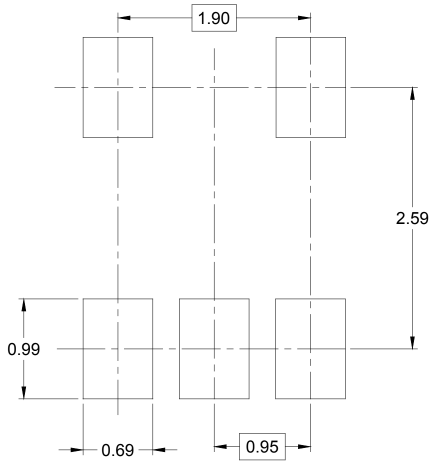
MAY 2020 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	4
Updated Typical Performance Characteristics section	8

Changes from Original (DECEMBER 2019) to REV.A	Page
Changed from product preview to production data	All

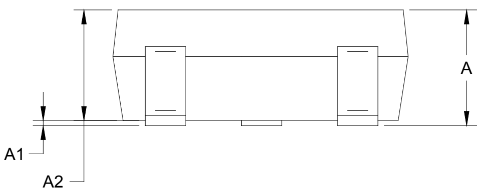
PACKAGE OUTLINE DIMENSIONS

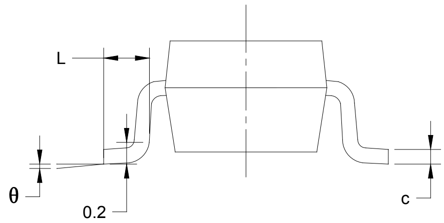
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)

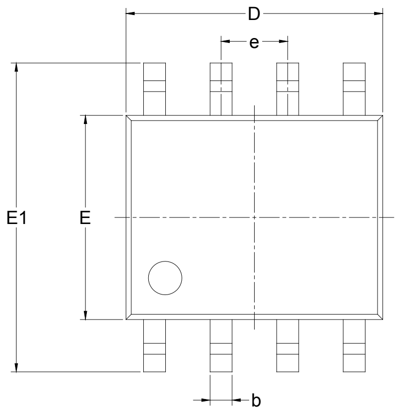


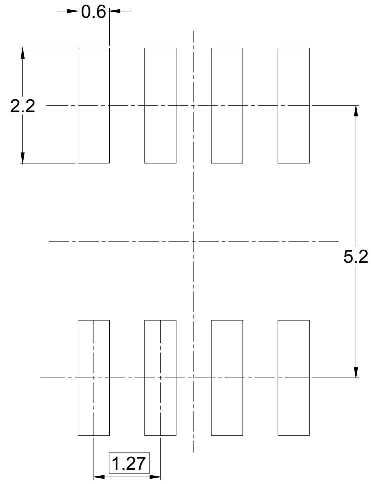


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

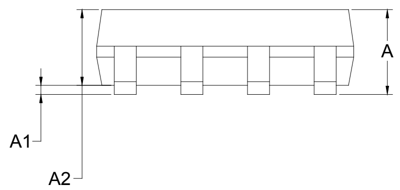
PACKAGE OUTLINE DIMENSIONS

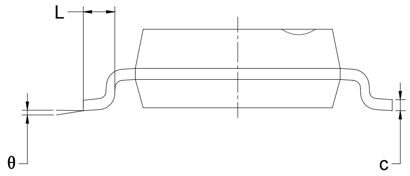
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

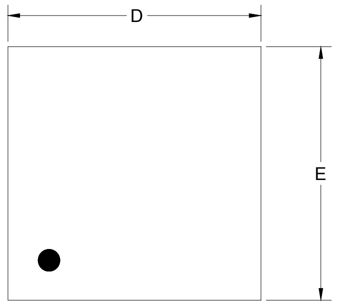




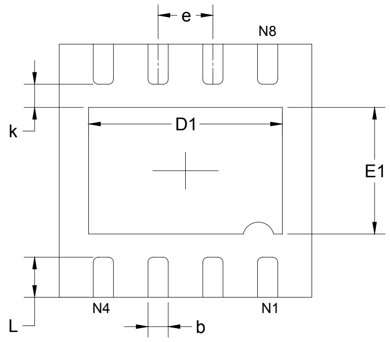
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

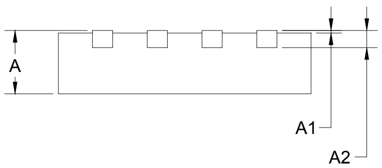
TDFN-3×3-8L



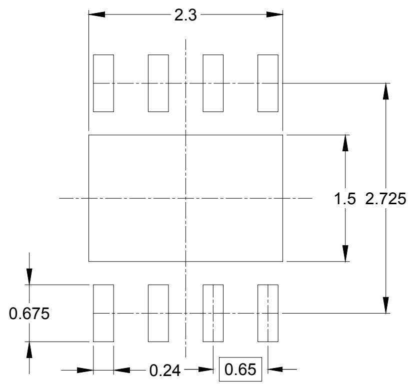
TOP VIEW



BOTTOM VIEW



SIDE VIEW

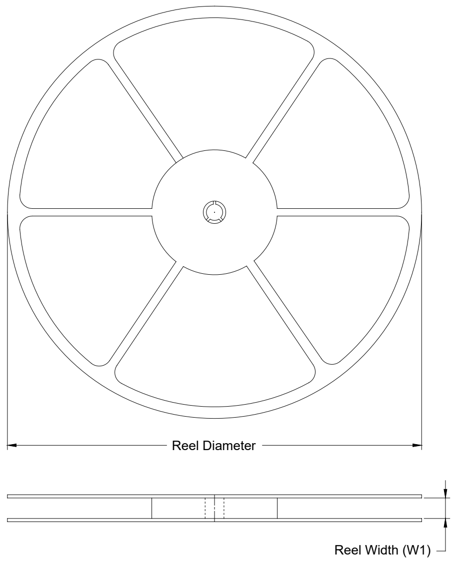


RECOMMENDED LAND PATTERN (Unit: mm)

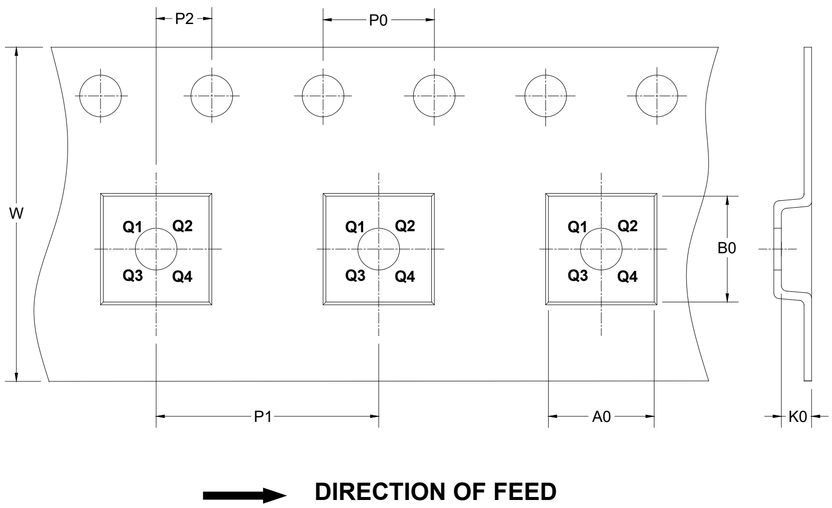
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.200	2.400	0.087	0.094
E	2.900	3.100	0.114	0.122
E1	1.400	1.600	0.055	0.063
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.650 TYP		0.026 TYP	
L	0.375	0.575	0.015	0.023

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



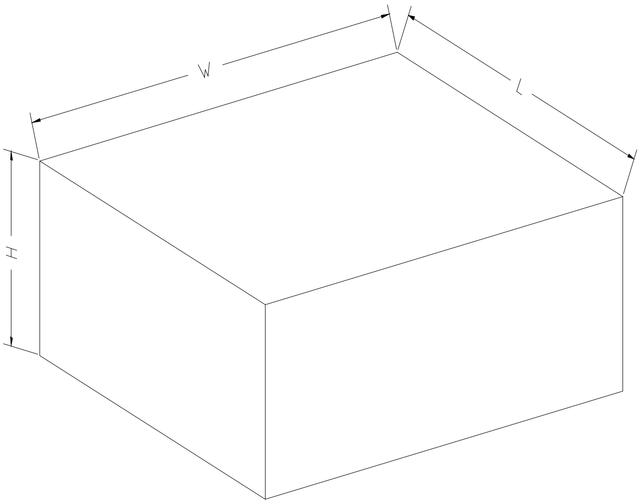
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-8L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002