SGM829S
Microprocessor Supervisory Circuit with Programmable Delay Time

GENERAL DESCRIPTION

The SGM829S family can monitor system voltages from 1.8V to 5V. When the V_{DD} voltage falls below the preset threshold (V_{ITL}) or the manual reset (nMR) pin is driven low, the open-drain nRESET output is asserted. After the V_{DD} voltage and nMR voltage return higher than their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

The SGM829S uses a precision reference to achieve 1% threshold accuracy. The fixed reset timeout period can be set to 0.25ms by leaving the SRT pin open. The programmable reset timeout period can be set from 1.25ms to 10s through an external capacitor connected to the SRT pin. Low quiescent current makes the SGM829S very suitable for battery-powered applications.

The SGM829S is available in a Green SOT-23-5 package.

FEATURES

- **Adjustable Reset Timeout Period: 1.25ms to 10s**
- **Low Quiescent Current: 0.8μA (TYP)**
- **High Threshold Accuracy: 1% (TYP)**
- **Factory-Set Detection Voltages: 1.8V to 5V**
- **Manual Reset (nMR) Input**
- **Open-Drain nRESET Output**
- **Available in a Green SOT-23-5 Package**

APPLICATIONS

Computers
Portable Equipment
Intelligent Instruments
Microprocessor Systems
Critical μP Power Monitoring

TYPICAL APPLICATION

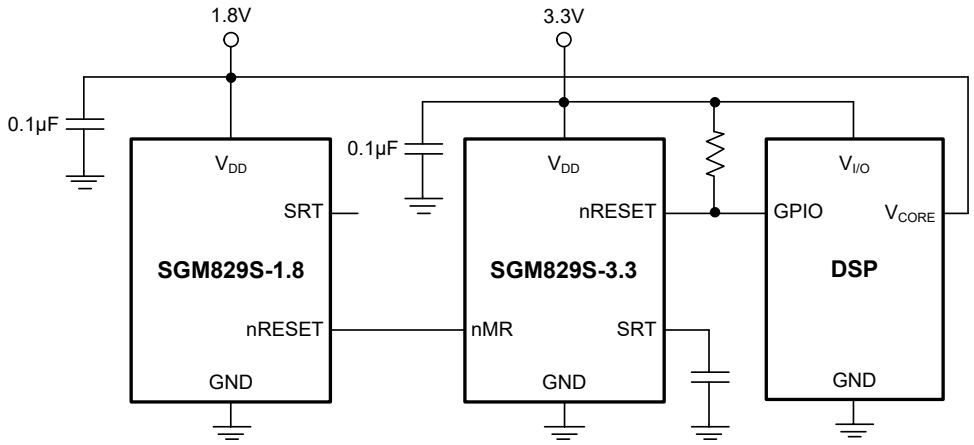


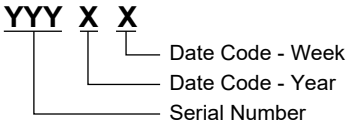
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	THRESHOLD VOLTAGE (V_{ITL}) (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM829S-1.8	1.67	SOT-23-5	SGM829S-1.8XN5G/TR	0L2XX	Tape and Reel, 3000
SGM829S-1.9	1.77	SOT-23-5	SGM829S-1.9XN5G/TR	0LWXX	Tape and Reel, 3000
SGM829S-2.5	2.33	SOT-23-5	SGM829S-2.5XN5G/TR	0LXXX	Tape and Reel, 3000
SGM829S-2.7	2.52	SOT-23-5	SGM829S-2.7XN5G/TR	0LYXX	Tape and Reel, 3000
SGM829S-2.9	2.7	SOT-23-5	SGM829S-2.9XN5G/TR	0LZXX	Tape and Reel, 3000
SGM829S-3.0	2.79	SOT-23-5	SGM829S-3.0XN5G/TR	0GPXX	Tape and Reel, 3000
SGM829S-3.3	3.07	SOT-23-5	SGM829S-3.3XN5G/TR	0M0XX	Tape and Reel, 3000
SGM829S-3.7	3.45	SOT-23-5	SGM829S-3.7XN5G/TR	0M1XX	Tape and Reel, 3000
SGM829S-4.0	3.73	SOT-23-5	SGM829S-4.0XN5G/TR	0M2XX	Tape and Reel, 3000
SGM829S-4.5	4.2	SOT-23-5	SGM829S-4.5XN5G/TR	0M3XX	Tape and Reel, 3000
SGM829S-5.0	4.65	SOT-23-5	SGM829S-5.0XN5G/TR	0L3XX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V to 7V
SRT to GND ..... -0.3V to V_{DD} + 0.3V
nRESET, nMR to GND ..... -0.3V to 7V
nRESET Pin Current 8mA
Package Thermal Resistance
SOT-23-5, θ_{JA} ..... 176.9℃/W
SOT-23-5, θ_{JB} ..... 53.4℃/W
SOT-23-5, θ_{JC} ..... 97.7℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range, V_{DD} ..... 1.65V to 6.5V
SRT Pin Voltage, V_{SRT} ..... V_{DD} (MAX)
nMR Pin Voltage, V_{nMR} ..... 0V to 6.5V
nRESET Pin Voltage, V_{nRESET} ..... 0V to 6.5V
nRESET Pin Current, I_{nRESET} ..... 0.0003mA to 5mA
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

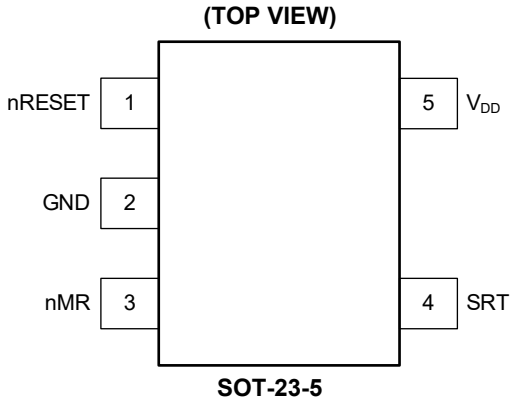
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	nRESET	O	Active-Low Reset Output Pin. nRESET remains low if the V_{DD} input is below V_{ITL} or nMR is logic low. It goes (or remains) low for the reset timeout period after the V_{DD} voltage exceeds V_{ITH} and nMR pin is driven high. It is recommended to connect a 10kΩ to 1MΩ pull-up resistor to this pin which enables the reset voltages greater than V_{DD}.
2	GND	—	Ground.
3	nMR	I	Manual Reset Input Pin. Pulling this pin (nMR) low will assert nRESET. nMR is internally pulled up to V_{DD} by a 100kΩ resistor.
4	SRT	I	Set Reset Timeout Input. Connect a capacitor between SRT and ground to set the timeout period. The pin can be left open, but it cannot be connected to V_{DD}. Determine the period as follows: T_D (μs) = (2.5 × 10^6) × C_{SRT} (μF) + 250μs.
5	V_{DD}	I	Supply Voltage. It is recommended to place a 0.1μF ceramic capacitor close to this pin.

NOTE: I: input, O: output.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.65V to 6.5V, R_{LRESET} = 100kΩ (1), T_J = -40℃ to +125℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage Range	V_{DD}		1.65		6.5	V
Supply Current (Current into V_{DD} Pin)	I_{DD}	V_{DD} = 3.3V, nRESET not asserted		0.8	1.6	μA
		V_{DD} = 6.5V, nRESET not asserted		1.1	2.3	
Low-Level Output Voltage	V_{OL}	1.3V ≤ V_{DD} < 1.8V, I_{OL} = 0.4mA			0.1	V
		1.8V ≤ V_{DD} ≤ 6.5V, I_{OL} = 1mA			0.2	
Power-On Reset Voltage	V_{POR}	V_{OL_MAX} = 0.2V, I_{nRESET} = 15μA			0.8	V
Negative-Going Input Threshold Accuracy	V_{ITL}	T_J = +25℃	-1		1	%
		T_J = -20℃ to +85℃	-1.8		1.8	
		T_J = -40℃ to +125℃	-2.2		2.2	
Positive-Going Input Threshold Accuracy	V_{ITH}	T_J = +25℃	-2		2	%
		T_J = -20℃ to +85℃	-3		3	
		T_J = -40℃ to +125℃	-3.5		3.5	
Hysteresis on V_{ITL} (2)	V_{HYS}		34 × V_{ITL}	50 × V_{ITL}	64 × V_{ITL}	mV
V_{DD} Drop to Reset Delay	t_{RP0}	Drop from V_{ITH} + 250mV to V_{ITL} - 250mV		35		μs
nMR Internal Pull-Up Resistance	R_{nMR}			100		kΩ
nMR Input	V_{IH}	Logic high	0.7 × V_{DD}			V
	V_{IL}	Logic low			0.3 × V_{DD}	
Input Capacitance, Any Pin	C_{IN}	SRT pin, V_{IN} = 0V to V_{DD}		5		pF
		Other pins, V_{IN} = 0V to 6.5V		5		
nMR Glitch Rejection	t_{nMR}			120		ns
nMR to Reset Propagation Delay	t_{MR}			150		ns
Reset Timeout Period	t_D	SRT open, V_{DD} = 1.65V to 5.5V	0.14	0.25	0.35	ms
		SRT open, V_{DD} = 1.65V to 6.5V	0.1	0.25	0.35	
		C_{SRT} = 1nF, V_{DD} = 1.65V to 5.5V	1.5	2.8	4.1	
		C_{SRT} = 1nF, V_{DD} = 1.65V to 6.5V	1.2	2.8	4.2	
SRT Source Current	I_{RAMP}			490		nA
SRT Source Threshold Voltage	$V_{TH-RAMP}$			1.205		V

NOTES:

1. R_{LRESET} is the resistor connected to the nRESET pin.
2. Guaranteed by design and not tested in production.

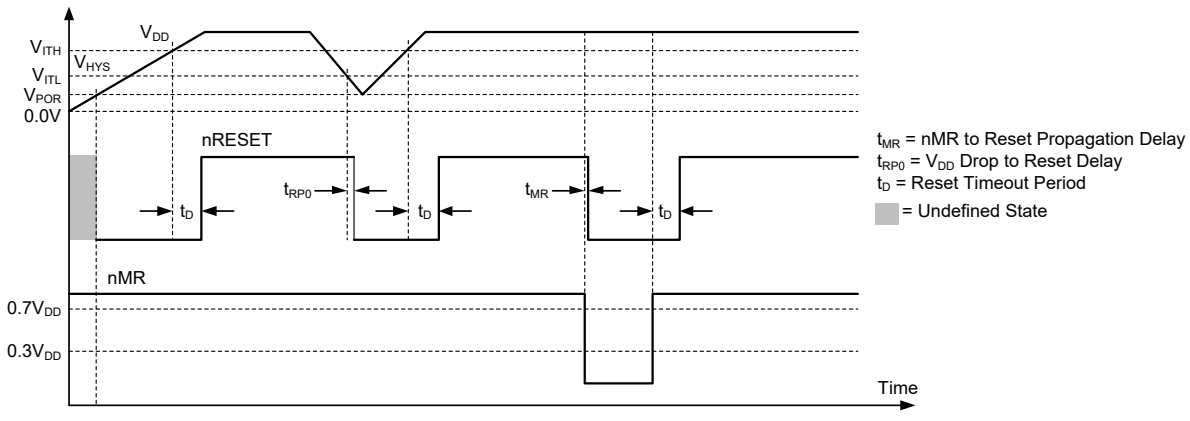
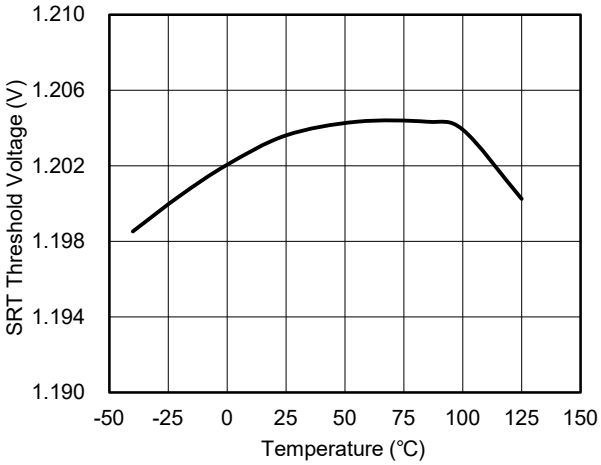


Figure 2. SGM829S Timing Diagram Showing nMR and V_{DD} Reset Timing

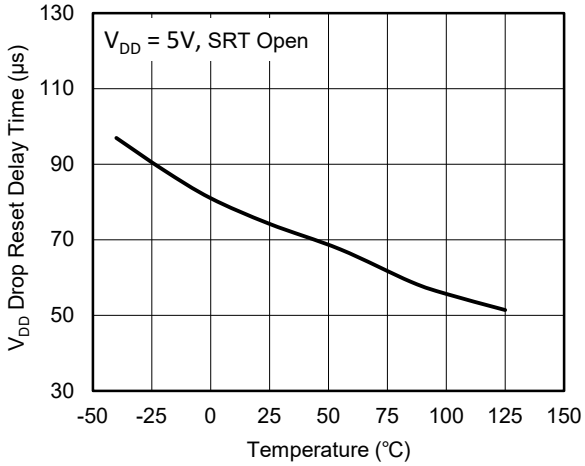
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = +25℃, unless otherwise noted.

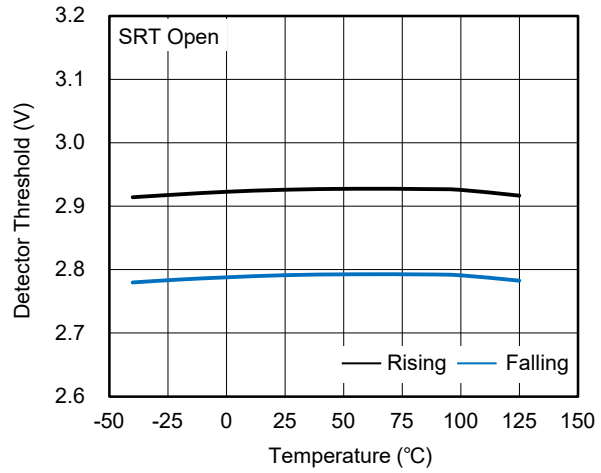
SRT Threshold Voltage vs. Temperature



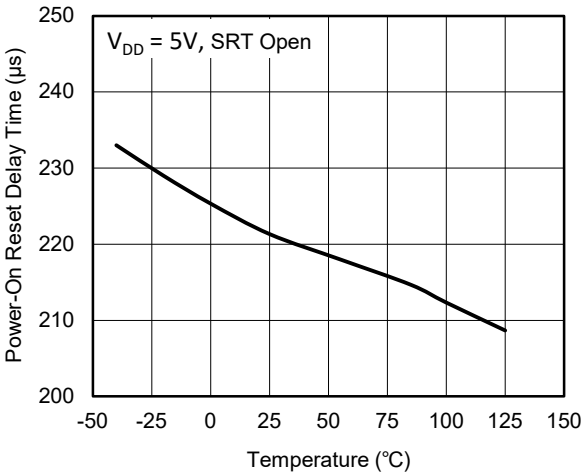
V_{DD} Drop Reset Delay Time vs. Temperature



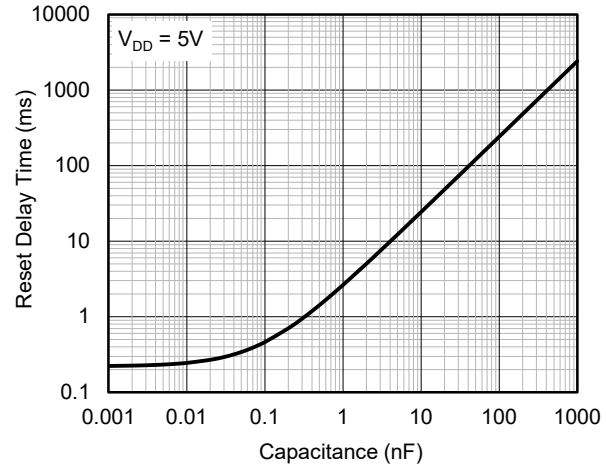
Detector Threshold vs. Temperature



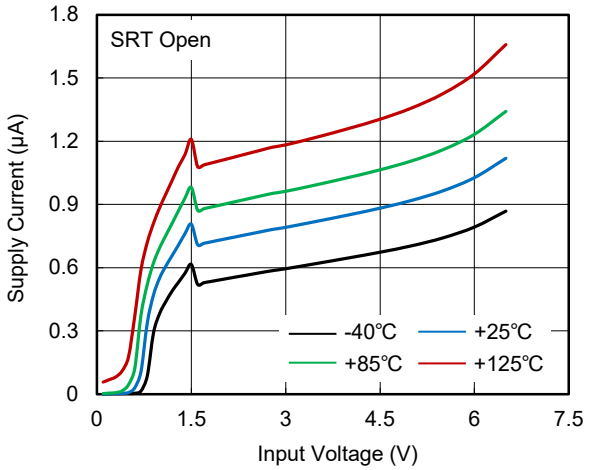
Power-On Reset Delay Time vs. Temperature



Reset Delay Time vs. Capacitance



Supply Current vs. Input Voltage



FUNCTIONAL BLOCK DIAGRAM

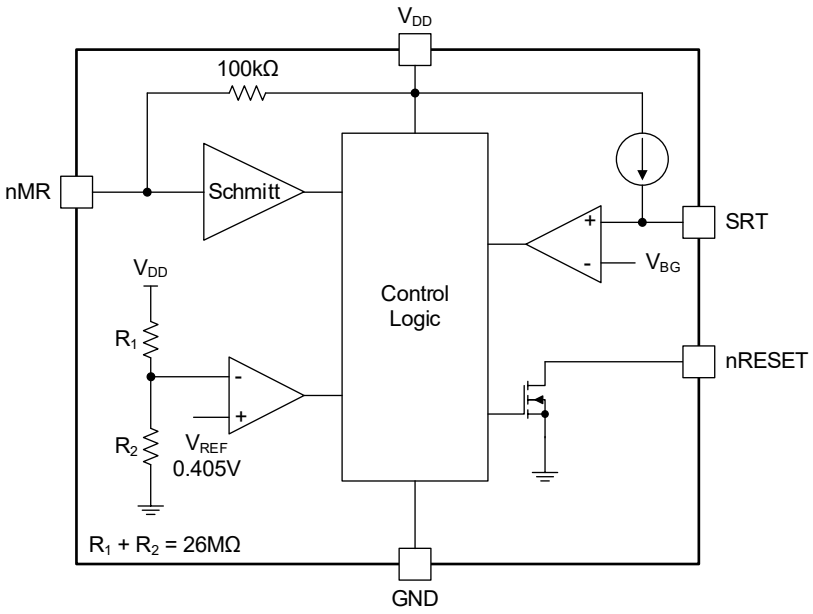


Figure 3. Block Diagram

DETAILED DESCRIPTION

When the V_{DD} voltage falls below V_{ITL} or the nMR pin is driven low, the open-drain nRESET output is asserted. After the V_{DD} and nMR voltages exceed their respective thresholds, the nRESET output remains low within the user-adjustable delay time.

Feature Description

The SGM829S device has a reset delay time adjustment function and a wide range of detection thresholds, so it can be widely used in various applications. The detection threshold voltages are factory-set from 1.8V to 5V. The reset timeout period can be set from 1.25ms to 10s through programming an external capacitor which is connected to the SRT pin.

Selecting the Reset Delay Time

When the V_{DD} voltage exceeds the V_{DD} threshold voltage, a current source will start to charge the SRT capacitor and the SRT voltage will rise. When the SRT voltage exceeds 1.205V, the nRESET voltage will change from low to high.

Therefore, there is a delay time between the point of V_{DD} reaching its threshold voltage and the nRESET active-high point. The delay time can be calculated according to the following equation:

$$T_D\,(\mu s) = (2.5 \times 10^6) \times C_{SRT}\,(\mu F) + 250\mu s \quad (1)$$

Manual Reset (nMR) Input

The manual reset (nMR) input allows the operator, test technician, or external logic circuit to initiate a reset. A logic low ($0.3 \times V_{DD}$) on nMR forces the nRESET low. After nMR returns to a logic high and the V_{DD} voltage rises above its reset threshold, nRESET is deasserted after a reset delay time period (t_D). nMR is pulled up to V_{DD} with an internal 100kΩ resistor. This pin can be left floating if nMR is not used.

Figure 4 shows how to use nMR to monitor multiple system voltages. If the logic signal does not drive nMR fully to V_{DD}, some extra current will flow into V_{DD} due to the pull-up resistor on nMR. Figure 5 shows how to use an external FET to minimize the current draw.

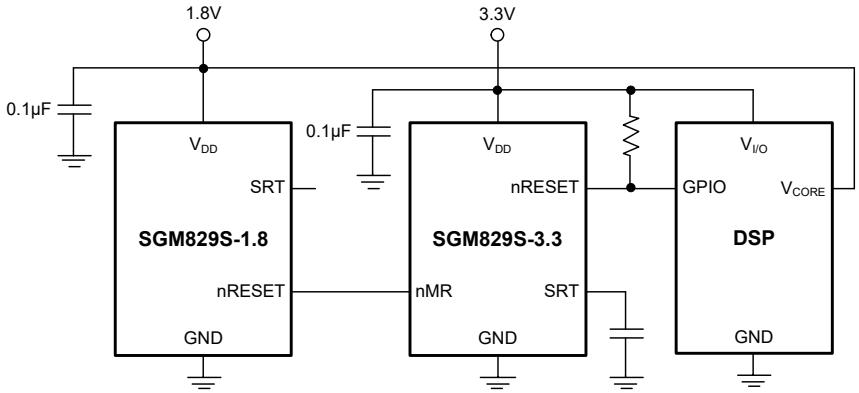


Figure 4. Monitor Multiple System Voltages Using the nMR Pin

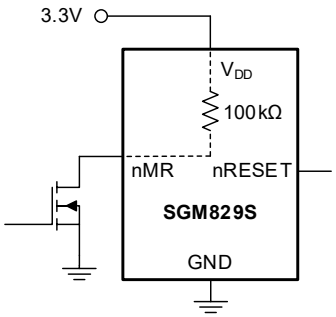


Figure 5. An External MOSFET is used to Minimize I_{DD}

DETAILED DESCRIPTION (continued)

nRESET Output

As long as V_{DD} voltage exceeds V_{ITL} and the nMR is logic high, nRESET remains high (deasserted). Either V_{DD} is lower than V_{ITL} or nMR is set low, nRESET will be low (asserted).

If nMR returns to logic high again and V_{DD} voltage exceeds V_{ITH}, nRESET will remain low for a fixed reset delay time due to the delay circuit function. As soon as the reset delay has expired, the nRESET turns into logic high. The pull-up resistor between nRESET and V_{DD} can be used to reset the microprocessor signal to obtain a voltage above V_{DD} voltage. The pull-up resistor should be no less than 10kΩ due to the limited nRESET pull-down ability.

Device Functional Modes

Table 1. Matrices of the nRESET Output

nMR	$V_{DD} > V_{ITL}$	nRESET
L	0	L
L	1	L
H	0	L
H	1	H

Normal Operation ($V_{DD} > V_{DD\_MIN}$)

When the V_{DD} voltage is higher than V_{DD_MIN}, the logic state of nRESET is determined by V_{DD} and the logic state of nMR.

• nMR high: When V_{DD} voltage is higher than 1.65V for a selected time (t_D), the nRESET logic state corresponds to V_{DD} relative to V_{ITL}.

• nMR low: nRESET is held low regardless of V_{DD} voltage in this mode.

Above Power-On Reset but Lower than V_{DD_MIN} ($V_{POR} < V_{DD} < V_{DD\_MIN}$)

When the V_{DD} voltage is lower than V_{DD_MIN} and higher than the power-on reset voltage (V_{POR}), the nRESET is asserted and driven to a low-impedance state.

Below Power-On Reset ($V_{DD} < V_{POR}$)

When the V_{DD} voltage is lower than the required voltage (V_{POR}), the nRESET voltage is undefined. In the case of nRESET pulling up to V_{DD} through a 100kΩ resistor, nRESET voltage is equal to or lower than V_{DD} voltage.

APPLICATION INFORMATION

The SGM829S requires a voltage supply within 1.65V and 6.5V. Figure 6 shows a typical application of the SGM829S-2.5 used with a 2.5V microprocessor. Normally, the nRESET output is connected to the nRESET input of the microprocessor. It is necessary to connect a 1MΩ pull-up resistor between nRESET and V_{DD} to keep the nRESET logic high if it is not asserted.

The reset delay time can be set by SRT while it depends on the requirement of microprocessor. If left it open, a typical 0.25ms of reset delay time is set.

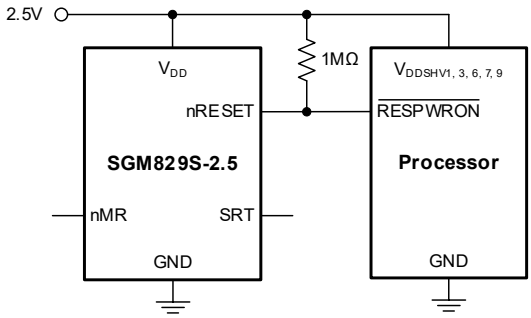


Figure 6. SGM829S Typical Application circuit with a Microprocessor

Layout Guidelines

It is recommended to connect a 0.1μF ceramic capacitor to the V_{DD} pin as close as possible. If there is no connection capacitor, minimize the parasitic capacitor to avoid a significant impact on the nRESET delay time.

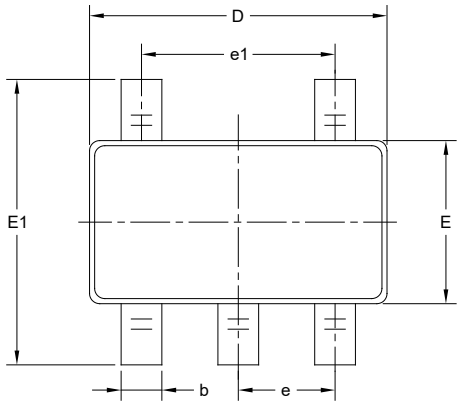
REVISION HISTORY

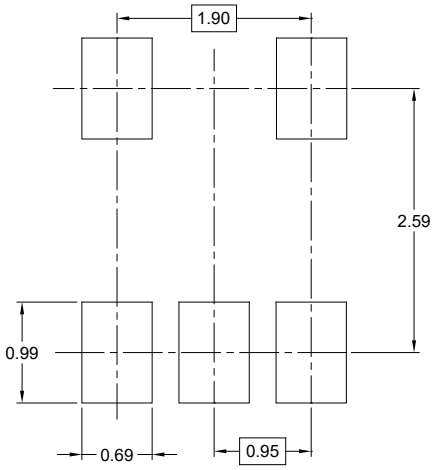
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

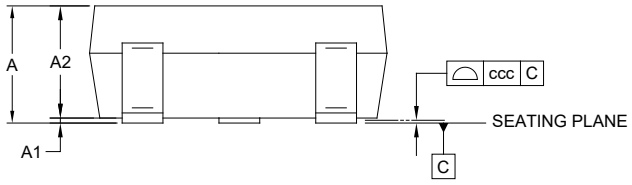
PACKAGE OUTLINE DIMENSIONS

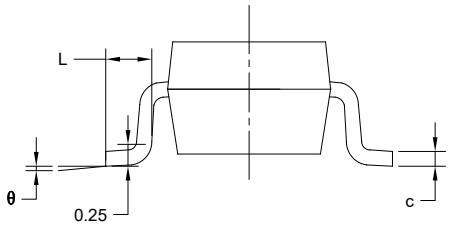
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



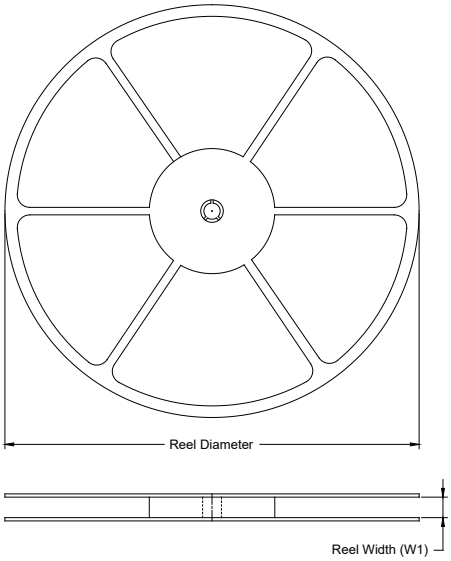


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

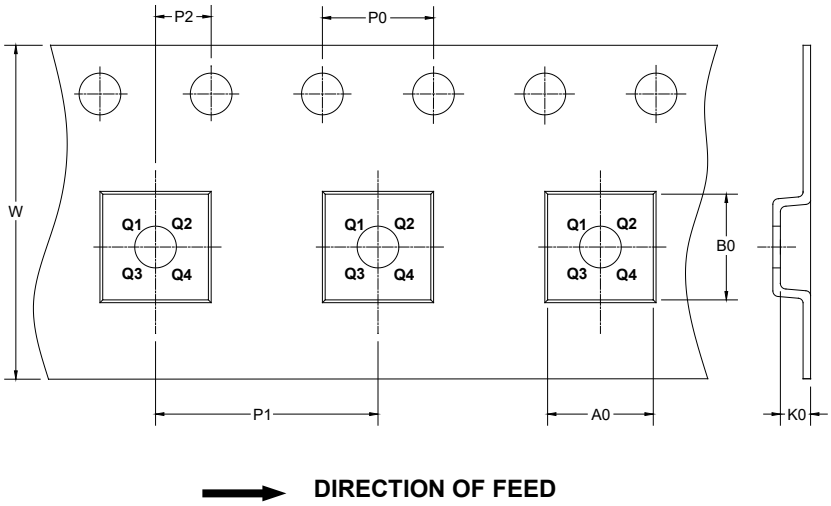
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



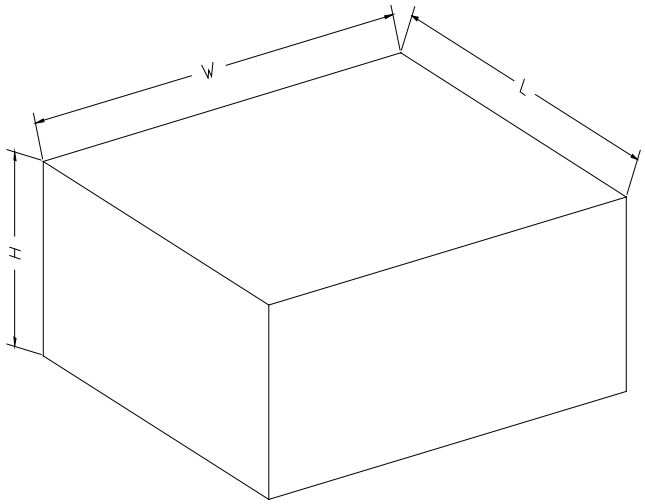
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002