SGM3843
Power Management IC for AMOLED Display

GENERAL DESCRIPTION

The SGM3843 is a PMIC (Power Management IC) designed for powering AMOLED (Active Matrix Organic LED) displays which require V_{ELVDD}, V_{ELVSS}, V_{AVDD}, V_{DVDD} and V_{VGL}.

The device integrates two Boost converters VO1 for V_{ELVDD} and VO3 for V_{AVDD}, one dual-phase inverting Buck-Boost converter VO2 for V_{ELVSS}, one single-phase inverting Buck-Boost converter VO5 for V_{VGL}, and one Buck converter VO4 for V_{DVDD}. It also integrates one negative low dropout linear regulator (LDO) VO5_LDO for V_{VGL_LDO}.

The DVDD, VGL and VGL_LDO are used for powering the DDIC (Display-Driver IC).

All output voltages of these converters can be programmed in digital steps through the I^2C interface.

The SGM3843 is available in a Green WLCSP-3.3×3.3-64B package.

FEATURES

- **2.9V to 5.0V Input Supply Voltage Range**
- **Synchronous Boost Converter VO1 (ELVDD)**
  - **4.6V to 5.0V Output Voltage with 100mV Steps**
  - **4.6V Default Output Voltage**
  - **0.65% Accuracy at 4.6V**
  - **1200mA Output Current Capability**
- **Synchronous Inverting Buck-Boost Converter VO2 (ELVSS)**
  - **-8.0V to -1.0V Output Voltage with 50mV Steps**
  - **-4.0V Default Output Voltage**
  - **1% Accuracy at -4.0V**
  - **1200mA Output Current Capability**
- **Synchronous Boost Converter VO3 (AVDD)**
  - **5.7V to 8.0V Output Voltage with 50mV Steps**
  - **7.6V Default Output Voltage**
  - **0.66% Accuracy at 7.6V**
  - **200mA Output Current Capability**
- **Synchronous Buck Converter VO4 (DVDD)**
  - **0.7V to 2.1V Output Voltage with 25mV Steps**
  - **1.05V Default Output Voltage**
  - **0.6% Initial Accuracy at 1.05V**
  - **400mA Output Current Capability**
- **Synchronous Inverting Buck-Boost Converter VO5 (VGL)**
  - **-4.0V to -12.5V Output Voltage with 100mV Steps**
  - **-7V Default Output Voltage**
  - **0.8% Accuracy at -7V**
  - **30mA Output Current Capability**
- **Low Dropout Linear Regulator VO5_LDO (VGL_LDO)**
  - **Fixed 300mV Dropout Voltage**
  - **30mA Output Current Capability**
- **Excellent Line Transient Regulation**
- **High Performance Load Regulation**
- **V_{IN} and V_{OUT} Bi-Directional Isolation**
- **I^2C Interface**
- **Under-Voltage Lockout (UVLO)**
- **All Channels Soft-Start**
- **All Channels Fast Discharge Function (FD)**
- **All Channels Short Circuit Protection (SCP)**
- **All Channels Over-Current Protection (OCP)**
- **Over-Temperature Protection (OTP)**
- **Overload Protection (OLP)**
- **Start-Up Short Detection (SSD)**
- **V_{ELVSS} Start-Up Delay: 5.7ms**
- **Short Circuit and OLP Detection Time: 1ms**
- **Available in a Green WLCSP-3.3×3.3-64B Package**

APPLICATIONS

Smartphones & Tablets

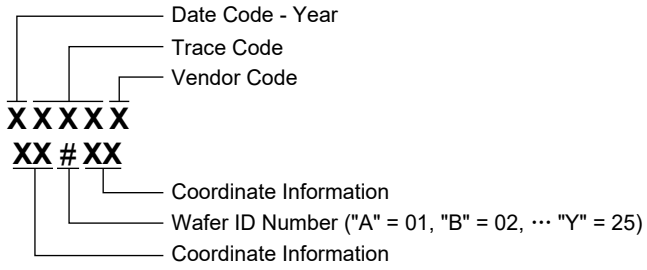
Active Matrix OLED Displays

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM3843	WLCSP-3.3×3.3-64B	-40℃ to +85℃	SGM3843YG/TR	SGM 3843YG XXXXX XX#XX	Tape and Reel, 5000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to Ground Pin)
PVIN1, PVIN2A, PVIN2B, PVIN4, PVIN5, AVIN, VO1, VO1_FB, VO4_FB ..... -0.3V to 6V
VO4_EN, VO5_EN, SDA, SCL, RESETB, VIO, PGOOD ..... -0.3V to 6V
VO2A, VO2B, VO2_FB ..... -9V to GND + 0.3V
VO5, IN_LDO, VO5_LDO ..... -15V to GND + 0.3V
SW1, SW4 ..... -0.3V to 6V
SW1, SW4 (Transient: 10ns) ..... -1V to 8V
SW3, VO3 ..... -0.3V to 10V
SW3 (Transient: 10ns) ..... -1V to 12V
SW2A, SW2B ..... -9V to 6V
SW2A, SW2B (Transient: 10ns) ..... -11V to 8V
SW5 ..... -15V to 6V
SW5 (Transient: 10ns) ..... -17V to 8V
Package Thermal Resistance
WLCSP-3.3×3.3-64B, θ_{JA} ..... 27℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Junction Temperature Range ..... -40℃ to +125℃
Operating Ambient Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

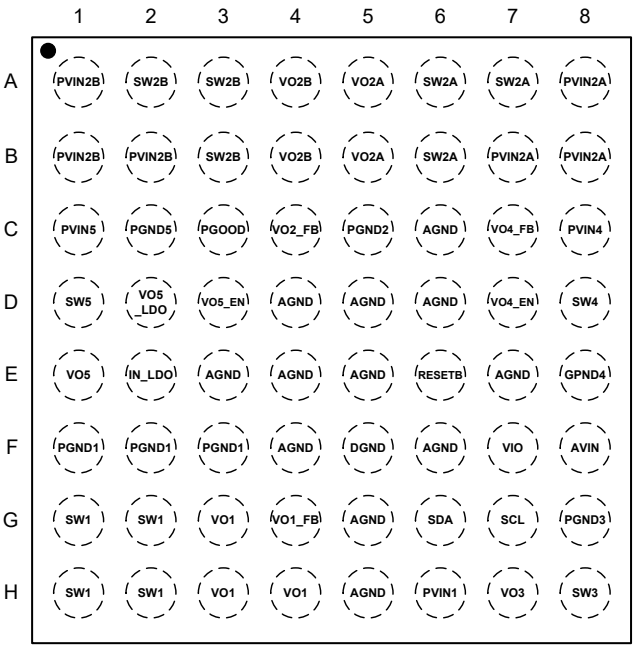
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-3.3×3.3-64B

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
A1, B1, B2	PVIN2B	I	VO2 Inverting Buck-Boost Converter B Power Supply Input Pin.
A2, A3, B3	SW2B	I/O	VO2 Inverting Buck-Boost Converter B Switching Node.
A4, B4	VO2B	O	VO2 Inverting Buck-Boost Converter B Output Pin.
A5, B5	VO2A	O	VO2 Inverting Buck-Boost Converter A Output Pin.
A6, A7, B6	SW2A	I/O	VO2 Inverting Buck-Boost Converter A Switching Node.
A8, B7, B8	PVIN2A	I	VO2 Inverting Buck-Boost Converter A Power Supply Input Pin.
C1	PVIN5	I	VO5 Inverting Buck-Boost Converter Power Supply Input Pin.
C2	PGND5	G	VO5 Power Ground.
C3	PGOOD	O	Power Good Open-Drain Output.
C4	VO2_FB	I	VO2 Inverting Buck-Boost Converter Output Sense Input.
C5	PGND2	G	VO2 Inverting Buck-Boost Converter Power Ground.
C6, D4, D5, D6, E3, E4, E5, E7, F4, F6, G5, H5	AGND	G	Analog Ground Pin.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	DESCRIPTION
C7	VO4_FB	O	VO4 Buck Converter Output Sense Input.
C8	PVIN4	I	VO4 Buck Converter Power Supply Input Pin.
D1	SW5	I/O	VO5 Inverting Buck-Boost Converter Switching Node.
D2	VO5_LDO	O	VO5 Negative Low Dropout Regulator Output.
D3	VO5_EN	I	VO5 Inverting Buck-Boost Converter Enable Pin.
D7	VO4_EN	I	VO4 Buck Converter Enable Pin.
D8	SW4	I/O	VO4 Buck Converter Switching Node.
E1	VO5	O	VO5 Inverting Buck-Boost Converter Output.
E2	IN_LDO	I	VO5 Inverting Buck-Boost Converter and LDO Power Supply Input Pin.
E6	RESETB	I	Reset Control Input Pin.
E8	PGND4	G	VO4 Buck Converter Power Ground.
F1, F2, F3	PGND1	G	VO1 Boost Converter Power Ground.
F5	DGND	G	Digital Ground Pin.
F7	VIO	I	Input Voltage Supply for I/O Circuits. Bypass this pin to AGND with at least 1μF high quality ceramic capacitor (X5R or better).
F8	AVIN	I	Analog Input Supply Pin.
G1, G2, H1, H2	SW1	I/O	VO1 Boost Converter Switching Node.
G3, H3, H4	VO1	O	VO1 Boost Converter Output.
G4	VO1_FB	I	VO1 Boost Converter Output Sense Input.
G6	SDA	I/O	I^2C Interface Data Line.
G7	SCL	I	I^2C Interface Clock Line.
G8	PGND3	G	VO3 Boost Converter Power Ground.
H6	PVIN1	I	VO1 Boost Converter Power Supply Input Pin.
H7	VO3	O	VO3 Boost Converter Output.
H8	SW3	I/O	VO3 Boost Converter Switching Node.

NOTE: I: input, O: output, I/O: input or output, G: ground.

TYPICAL APPLICATION

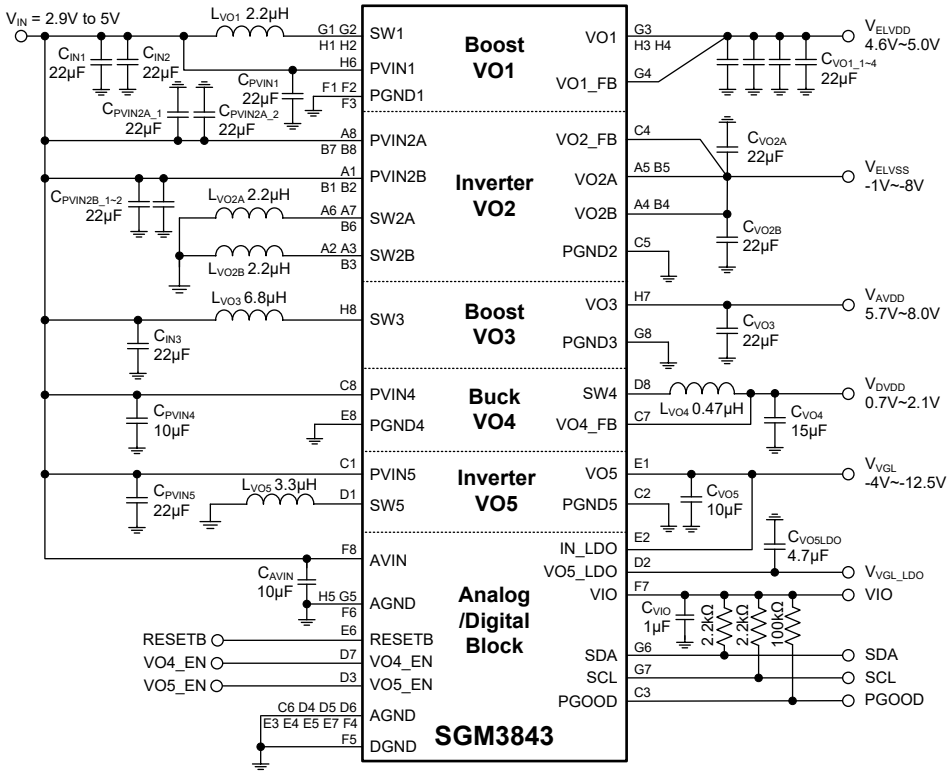


Figure 1. Typical Application Circuit

RECOMMENDED COMPONENT SELECTION

Table 1. Recommended Component Selection

Component	Value	Number	Electrical Spec	Part Number	Manufacturer
C_{IN1}, C_{IN2}, C_{IN3}, C_{PVIN1}, C_{PVIN2A_1}, C_{PVIN2A_2}, C_{PVIN2B_1}, C_{PVIN2B_2}, C_{PVIN5}, C_{VO1_1}, C_{VO1_2}, C_{VO1_3}, C_{VO1_4}, C_{VO2A} (1), C_{VO2B} (1), C_{VO3}	22μF	16	X5R, 16V, 0805	GRM219R61C226ME15L	Murata
C_{PVIN4}, C_{AVIN}	10μF	2	X5R, 16V, 0603	GRM188R61C106MA73	Murata
C_{VO4} (2)	15μF	1	X5R, 10V, 0603	C1608X5R1A156M080AC	TDK
C_{VO5}	10μF	1	X5R, 25V, 0603	GRM188R61E106MA73	Murata
C_{VIO}	1μF	1	X5R, 16V, 0603	GRM155R61C105KA12	Murata
C_{VO5LDO}	4.7μF	1	X5R, 25V, 0603	GRM188R61E475ME11	Murata
L_{VO1}, L_{VO2A}, L_{VO2B}	2.2μH	3	4A, 70mΩ, 322512	HMLQ32251B-2R2MS	Cyntec
L_{VO3}	6.8μH	1	1.1A, 275mΩ, 252012	VLS252012CX-6R8M-1	TDK
L_{VO4} (2)	0.47μH	1	2.9A, 54mΩ, 160808	TFM160808ALC-R47MTAA	TDK
L_{VO5}	3.3μH	1	1.5A, 228mΩ, 252010	1269AS-H-3R3M=P2	Murata
R_{SCL}, R_{SDA}	2.2kΩ	2			
R_{PGOOD}	100kΩ	1			

NOTES:

1. C_{VO2A} = C_{VO2B} = 2×22μF are recommended for I_{VO2} > 1A.
2. L_{VO4} = 2.2μH & C_{VO4} = 2.2μF are recommended for V_{DVDD} ≤ 1.5V application due to better efficiency.
   L_{VO4} = 0.47μH & C_{VO4} = 15μF can be used for 0.7V ≤ V_{DVDD} ≤ 2.1V application.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -4.0V, V_{VO3} = 7.6V, V_{VO4} = 1.05V, V_{VO5} = -7V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
General							
AVIN, PVIN Input Voltage Range	V_{S_VIN}			2.9		5	V
Shutdown Current into PVINx, AVIN	I_{SD}	All channels off			1.0	2.0	μA
Quiescent Current into PVINx, AVIN	I_{QON}	All channels on, no load. LPD_EN[2:0] = 000			4.3		mA
Quiescent Current into PVINx, AVIN	I_{QON}	All channels on, no load. LPD_EN[2:0] = 111			1.6		mA
AVIN Start Threshold Voltage	V_{START}	V_{IN} rising		2.2	2.36	2.5	V
AVIN Stop Threshold Voltage	V_{STOP}	V_{IN} falling		2.1	2.25	2.4	V
Thermal Shutdown Temperature	T_{SD}	Temperature rising			150		℃
Thermal Shutdown Hysteresis	ΔT_{SD}	TSD release threshold temperature = T_{SD} - ΔT_{SD}			15		℃
ELVDD Boost Converter (V_{VO1} = V_{ELVDD})							
Output Default Voltage	V_{VO1}	4.6V to 5.0V with 100mV/step, default 4.6V		4.6	4.6	5.0	V
Output Voltage Total Accuracy		V_{VO1} = 4.6V, no load	T_J = +25℃	-0.5		0.5	%
			T_J = -40℃ to +85℃	-0.65		0.65	
SW1 MOSFET On-Resistance	$R_{DS(ON)11}$	I_{DS} = 200mA			60		mΩ
SW1 MOSFET Rectifier On-Resistance	$R_{DS(ON)12}$	I_{DS} = 200mA			110		mΩ
SW1 Current Limit	I_{SW1_LIM}	Inductor valley current, T_J = +25℃		2.5	2.9	3.3	A
SW1 Switching Frequency	f_{SW1}	I_{VO1} = 100mA		1.25	1.45	1.65	MHz
Maximum Output Current	I_{VO1_MAX}	V_{IN} = 3.0V to 5.0V, T_J = +25℃		1200			mA
VO1 and FB1 Leakage	I_{LEAK_VO1}	No discharge, EL_EN = 0			0.5	1.2	μA
Short Circuit Protection Threshold in Operation	V_{VO1_FBCP}	V_{VO1} falling, percentage of nominal V_{VO1}, T_J = +25℃		78	87	94	%
Discharging Resistance	R_{DCHG_VO1}	I_{VO1} = 20mA			75		Ω
Discharge Time	t_{DVO1}				8		ms
Line Transient	$VO1_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO1} = 0mA to 300mA	Overshoot		8		mV
			Undershoot		8		
		ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO1} = 300mA to 1200mA	Overshoot		18		mV
			Undershoot		18		
Line Regulation	$VO1_{LINEREG}$	I_{VO1} = 100mA, V_{IN} = 2.9V to 5.0V			±0.014		%/V
		No load, V_{IN} = 2.9V to 5.0V			±0.014		
Output Voltage Ripple	$VO1_{RIPPLE}$	I_{VO1_VO2} = 0mA to 700mA			14		mV_{PP}
		I_{VO1_VO2} = 700mA to 1200mA			20		mV_{PP}
Load Transient	$VO1_{LOADTRA}$	ΔI_{VO1} = 10mA to 1200mA, t_R = t_F = 5ms	Overshoot		6		mV
			Undershoot		6		
Load Regulation	$VO1_{LOADREG}$	0mA ≤ I_{VO1} ≤ 1200mA, V_{IN} = 2.9V to 5.0V			3		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -4.0V, V_{VO3} = 7.6V, V_{VO4} = 1.05V, V_{VO5} = -7V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ELVSS Buck-Boost Converter (V_{VO2} = V_{ELVSS})							
Output Voltage Range	V_{VO2}	-8.0V to -1.0V with 50mV/step, default -4.0V		-8	-4	-1	V
Output Voltage Total Accuracy		V_{VO2} = -4.0V, no load	T_J = +25℃	-25		25	mV
			T_J = -40℃ to +85℃	-40		40	
SW2A MOSFET On-Resistance	$R_{DS(ON)A1}$	I_{DS} = 200mA			90		mΩ
SW2A MOSFET Rectifier On-Resistance	$R_{DS(ON)A2}$	I_{DS} = 200mA			65		mΩ
SW2B MOSFET On-Resistance	$R_{DS(ON)B1}$	I_{DS} = 200mA			90		mΩ
SW2B MOSFET Rectifier On-Resistance	$R_{DS(ON)B2}$	I_{DS} = 200mA			65		mΩ
SW2A Current Limit	I_{SW2A_LIM}	Inductor peak current, T_J = +25℃		2.85	3.6	4.45	A
SW2B Current Limit	I_{SW2B_LIM}	Inductor peak current, T_J = +25℃		2.85	3.6	4.45	A
Average Load Current Threshold with Dual-Phase	$I_{RMSA\&B}$	Load current rising			200		A
Average Load Current Threshold with Phase A Only	I_{RMSA}	Load current falling			130		A
SW2 Switching Frequency	f_{SW2}	I_{VO2} = 100mA		1.05	1.25	1.45	MHz
Maximum Output Current	I_{VO2_MAX}	V_{IN} = 3.0V to 5.0V, T_J = +25℃		1200			mA
Short Circuit Protection Threshold in Operation	V_{VO2_SCP}	V_{VO2} rising, percentage of nominal V_{VO2}, T_J = +25℃		75	83	89	%
Discharging Resistance	R_{DCHG_VO2}	I_{VO2} = 20mA			65		Ω
Discharge Time	t_{DVO2}				3.5		ms
VO2 Leakage, No Discharge	I_{LEAK_VO2}				1.3	2.7	μA
Output Voltage Ripple	$VO2_{RIPPLE}$	I_{VO1_VO2} = 0mA to 650mA, V_{VO2} = -1.0V to -8.0V			20		mV_{PP}
		I_{VO1_VO2} = 0mA to 1200mA, V_{VO2} = -1.0V to -5.0V			31		mV_{PP}
Line Transient	$VO2_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO2} = 0mA to 650mA, V_{VO2} = -1.0V to -8.0V	Overshoot		21		mV
			Undershoot		20		
		ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO2} = 650mA to 1200mA, V_{VO2} = -1.0V to -5.0V	Overshoot		22		mV
			Undershoot		20		
Line Regulation	$VO2_{LINEREG}$	I_{VO2} = 100mA, V_{IN} = 2.9V to 5.0V			±0.013		%/V
Load Transient	$VO2_{LOADTRA}$	ΔI_{VO2} = 10mA to 1200mA, V_{VO2} = -4V, t_R = t_F = 5ms	Overshoot		25		mV
			Undershoot		35		
Load Regulation	$VO2_{LOADREG}$	0mA ≤ I_{VO2} ≤ 1200mA			±0.011		%/A

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -4.0V, V_{VO3} = 7.6V, V_{VO4} = 1.05V, V_{VO5} = -7V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AVDD Boost Converter (V_{VO3} = V_{AVDD})							
Output Voltage Range	V_{VO3}	5.7V to 8.0V with 50mV/step, default 7.6V		5.7	7.6	8.0	V
Output Voltage Total Accuracy		V_{VO3} = 7.6V, no load	T_J = +25℃	-35		35	mV
			T_J = -40℃ to +85℃	-50		50	
SW3 MOSFET On-Resistance	$R_{DS(ON)31}$	I_{DS} = 200mA			430		mΩ
SW3 MOSFET Rectifier On-Resistance	$R_{DS(ON)32}$	I_{DS} = 200mA			550		mΩ
SW3 Current Limit	I_{SW3_LIM}	Inductor peak current, T_J = +25℃		0.85	1.23	1.65	A
SW3 Switching Frequency	f_{SW3}	I_{VO3} = 30mA		1.25	1.45	1.65	MHz
Maximum Output Current	I_{VO3_MAX}	V_{IN} = 3.0V to 5.0V, T_J = +25℃		200			mA
Short Circuit Protection Threshold in Operation	V_{VO3_SCP}	V_{VO3} falling, percentage of nominal V_{VO3}, T_J = +25℃		79	86	92	%
VO3 Leakage, No Discharge	I_{LEAK_VO3}				2.5	3.5	μA
Discharging Resistance	R_{DCHG_VO3}	I_{VO3} = 20mA			52		Ω
Discharge Time	t_{DVO3}				1.5		ms
Output Voltage Ripple	$VO3_{RIPPLE}$	I_{VO3} = 0mA to 200mA			32		mV_{PP}
Line Transient	$VO3_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO3} = 30mA	Overshoot		16		mV
			Undershoot		16		
Line Regulation	$VO3_{LINEREG}$	I_{VO3} = 100mA, V_{IN} = 2.9V to 5.0V			±0.011		%/V
Load Transient	$VO3_{LOADTRA}$	ΔI_{VO3} = 50mA to 100mA, t_R = t_F = 10μs, V_{IN} = 3.8V	Overshoot		43		mV
			Undershoot		43		
Load Regulation	$VO3_{LOADREG}$	0mA ≤ I_{VO3} ≤ 200mA			±0.036		%/A
DVDD Buck Converter (V_{VO4} = V_{DVDD})							
Output Voltage Range	V_{VO4}	0.7V to 2.1V with 25mV/step, default 1.05V		0.7	1.05	2.1	V
Output Voltage Total Accuracy (Initialization)		V_{VO4} = 1.05V, T_J = +25℃		-6		6	mV
Output Voltage Total Accuracy		V_{VO4} = 1.05V	T_J = +25℃	-10		10	mV
			T_J = -40℃ to +85℃	-18		18	
SW4 Current Limit	I_{SW4_LIM}	Inductor peak current, T_J = +25℃		0.8	1.2	1.6	A
SW4 MOSFET On-Resistance	$R_{DS(ON)41}$	I_{DS} = 200mA			370		mΩ
SW4 MOSFET Rectifier On-Resistance	$R_{DS(ON)42}$	I_{DS} = 200mA			220		mΩ
SW4 Switching Frequency	f_{SW4}	I_{VO4} = 400mA			2.7		MHz
Maximum Output Current	I_{DVDD_MAX}	V_{IN} = 2.9V to 5.0V, T_J = +25℃		400			mA
Discharging Resistance	R_{DCHG_VO4}	I_{VO4} = 20mA			75		Ω
VO4 Discharge Time	t_{DVO4}				2.5		ms
Output Voltage Ripple	$VO4_{RIPPLE}$				22		mV_{PP}
Line Transient	$VO4_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO4} = 200mA	Overshoot		13		mV
			Undershoot		13		
Line Regulation	$VO4_{LINEREG}$	I_{VO4} = 60mA to 100mA, V_{IN} = 2.9V to 5V			±0.021		%/V
Load Transient	$VO4_{LOADTRA}$	ΔI_{VO4} = 100mA, t_R = t_F = 10μs, V_{IN} = 2.9V to 5V	Overshoot		8		mV
			Undershoot		28		
Load Regulation	$VO4_{LOADREG}$	0mA ≤ I_{VO4} ≤ 400mA			5		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3.7V, V_{VO1} = 4.6V, V_{VO2} = -4.0V, V_{VO3} = 7.6V, V_{VO4} = 1.05V, V_{VO5} = -7V, T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VGL Buck-Boost Converter (V_{VO5} = V_{VGL})							
Output Voltage Range	V_{VO5}	-4.0V to -12.5V with 100mV/step, default -7V		-12.5	-7	-4	V
Output Voltage Total Accuracy		V_{VO5} = -7V, no load	T_J = +25℃	-0.6		0.6	%
			T_J = -40℃ to +85℃	-0.8		0.8	
SW5 Current Limit	I_{SW5_LIM}	Inductor peak current, T_J = +25℃		0.70	1.05	1.45	A
SW5 MOSFET On-Resistance	$R_{DS(ON)51}$	I_{DS} = 200mA			720		mΩ
SW5 MOSFET Rectifier On-Resistance	$R_{DS(ON)52}$	I_{DS} = 200mA			360		mΩ
SW5 Switching Frequency	f_{SW5}	I_{VO5} = 30mA		1.05	1.25	1.45	MHz
Maximum Output Current	I_{VO5_MAX}	V_{IN} = 2.9V to 5.0V, T_J = +25℃		30			mA
VO5 Short Circuit Protection	V_{VO5_SCP}	V_{VO5} rising, percentage of nominal V_{VO5}, T_J = +25℃		60	76	85	%
Short Circuit Detection Time in Operation	$t_{VO5(SCP)}$				1		ms
Discharging Resistance	R_{DCHG_VO5}	I_{VO5} = 20mA			120		Ω
VO5 Discharge Time	t_{DVO5}				2.5		ms
VO5 Leakage, No Discharge	I_{LEAK_VO5}				2.6	4	μA
Output Voltage Ripple	$VO5_{RIPPLE}$	I_{VO5} = 0mA to 30mA			34		mV_{PP}
Line Transient	$VO5_{LINETRA}$	ΔV_{IN} = 0.5V, t_R = t_F = 10μs, I_{VO5} = 0mA to 30mA	Overshoot		35		mV
			Undershoot		35		
Line Regulation	$VO5_{LINEREG}$	I_{VO5} = 5mA, V_{IN} = 2.9V to 5V			±0.011		%/V
Load Transient	$VO5_{LOADTRA}$	ΔI_{VO5} = 0mA to 10mA, V_{VO5} = -7V, t_R = t_F = 10μs	Overshoot		8		mV
			Undershoot		18		
Load Regulation	$VO5_{LOADREG}$	0mA ≤ I_{VO5} ≤ 30mA			±0.31		%/A
Negative LDO (VO5_LDO)							
Output Default Voltage	V_{VO5_LDO}				V_{VO5} + 0.3		V
Output Voltage Accuracy		V_{VO5} = -7.1V, no load	T_J = +25℃	-1.1		1.1	%
			T_J = -40℃ to +85℃	-1.2		1.2	
Load Regulation	dL_{LDO}	0mA ≤ I_{VO5_LDO} ≤ 30mA			±0.37		%/A
Line Regulation	dV_{LDO}	I_{VO5_LDO} = 5mA, V_{IN} = 2.9V to 5V			±0.013		%/V
Logic I/O Pin Characteristics (VO4_EN, VO5_EN, RESETB)							
Input High Threshold Voltage	V_{IH_S}	Input rising		1.0			V
Input Low Threshold Voltage	V_{IL_S}	Input falling				0.4	V
Logic I/O Pin Characteristics (PGOOD) – Open-Drain							
Output Logic Low Voltage	V_{OL}	At 5mA sink current				0.4	V
Logic I^2C (SDA, SCL)							
Input Logic High	V_{IH}	V_{VIO} = 1.8V ± 3%		0.7×V_{VIO}			V
Input Logic Low	V_{IL}	V_{VIO} = 1.8V ± 3%		-0.5		0.3×V_{VIO}	V
Output Logic High	V_{OH}			0.8×V_{VIO}		V_{VIO}	V
Output Logic Low	V_{OL}	At 3mA sink current		0		0.2×V_{VIO}	V

TIMING REQUIREMENTS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Short Circuit Timer					
VO1 Short Circuit Detection Time in Start-Up	$t_{VO1(SCP)}$	2	2.50	3	ms
VO1 Short Circuit Detection Time in Operation		0.8	1.0	1.3	
VO2 Short Circuit Detection Time in Start-Up	$t_{VO2(SCP)}$	5.5	6.7	7.9	
VO2 Short Circuit Detection Time in Operation		0.8	1.0	1.3	
VO3 Short Circuit Detection Time in Start-Up	$t_{VO3(SCP)}$		3.4		
VO3 Short Circuit Detection Time in Operation		0.8	1.0	1.3	
VO5 Short Circuit Detection Time in Start-Up	$t_{VO5(SCP)}$		3.4		
VO5 Short Circuit Detection Time in Operation		0.8	1.0	1.3	
Power Sequence					
VO1 Start-Up Time	t_{SS1}		3.0		ms
VO2 Start-Up Time	t_{SS2}		2.0		
VO2 Start-Up Time Delay after VO1	t_{DELAY}		2.7		
VO3 Start-Up Time	t_{SS3}		1.9		
VO4 Start-Up Time	t_{SS4}		1.0		
VO5 Start-Up Time (after VO5_EN = 1)	t_{SS5}		1.0		
VO5_LDO Start-Up Time (after VO5_EN = 1)	t_{SS5_L}		3.5		

I²C INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		FAST MODE PLUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL Clock Frequency	f_{SCL}		100	100	400		1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	4		0.6		0.26		μs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		0.5		μs
High Period of SCL Clock	t_{HIGH}	4		0.6		0.26		μs
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4.7		0.6		0.26		μs
Data Setup Time	$t_{SU;DATA}$	250		100		50		ns
Data Hold Time	$t_{HD;DATA}$	0		0		0		μs
Rising Time of SCL Clock	t_{RCL}		1000	20	300		120	ns
Falling Time of SCL Clock	t_{FCL}		300		300		120	ns
Rising Time of SDA Clock	t_{RDA}		1000	20	300		120	ns
Falling Time of SDA Clock	t_{FDA}		300		300		120	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4		0.6		0.26		μs
Bus Free Time between a STOP and a START Condition	t_{BUF}	4.7		1.3		0.5		μs
Noise Margin at LOW	V_{nL}	0.1 × V_{VIO}		0.1 × V_{VIO}		0.1 × V_{VIO}		V
Noise Margin at HIGH	V_{nH}	0.2 × V_{VIO}		0.2 × V_{VIO}		0.2 × V_{VIO}		V
Pulse Width of Spikes must be Suppressed by the Input Filter	t_{SP}	0	50	0	50	0	50	ns
Data Valid Time	t_{VD_DAT}		3.45		0.9		0.45	μs
Data Valid Acknowledge Time	t_{VD_ACK}		3.45		0.9		0.45	μs

NOTE:
1. Industry standard I²C timing characteristics are according to I²C-Bus Specification. Not tested in production.

I²C INTERFACE TIMING DIAGRAM

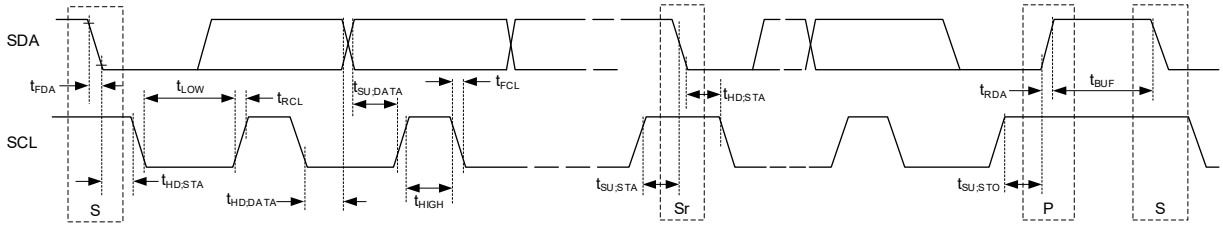
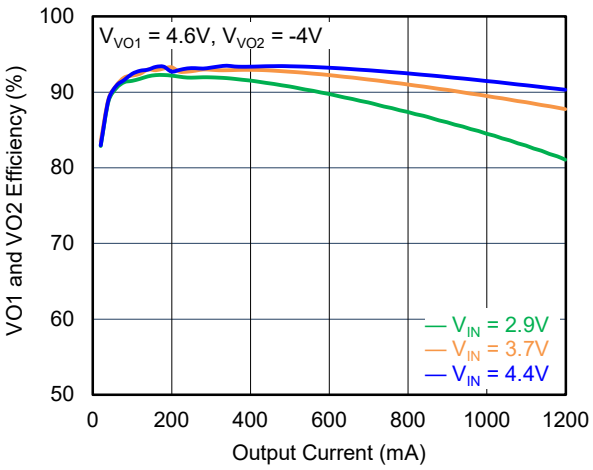


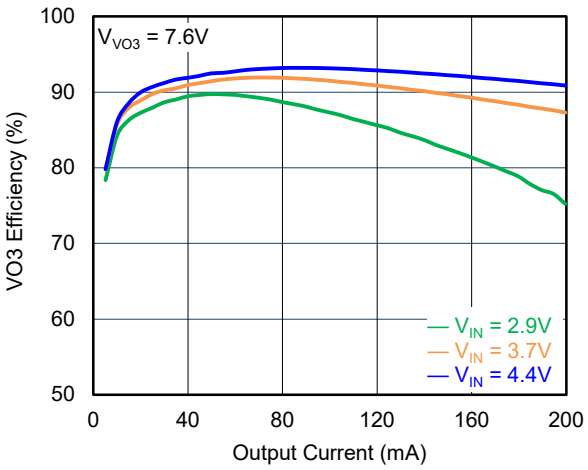
Figure 2. Serial Interface Timing for F/S-Mode

TYPICAL PERFORMANCE CHARACTERISTICS

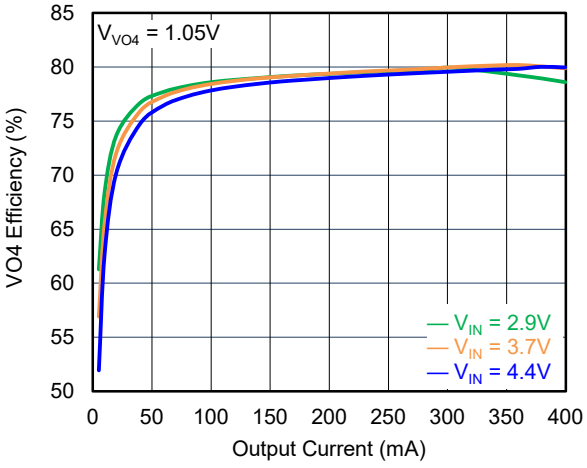
VO1 and VO2 Combined Efficiency vs. Output Current



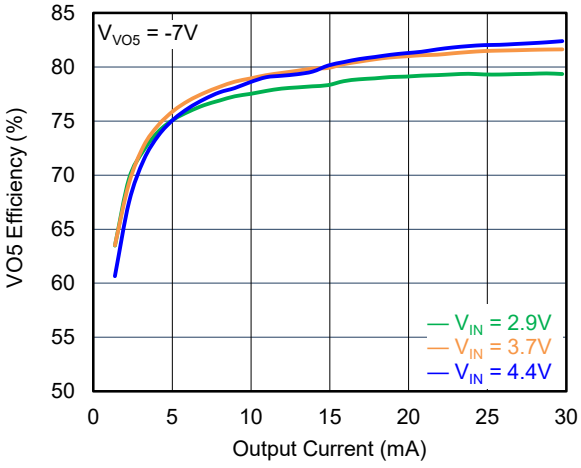
VO3 Efficiency vs. Output Current



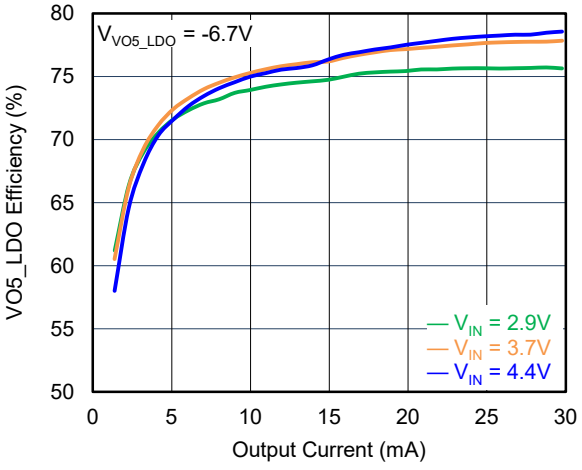
VO4 Efficiency vs. Output Current



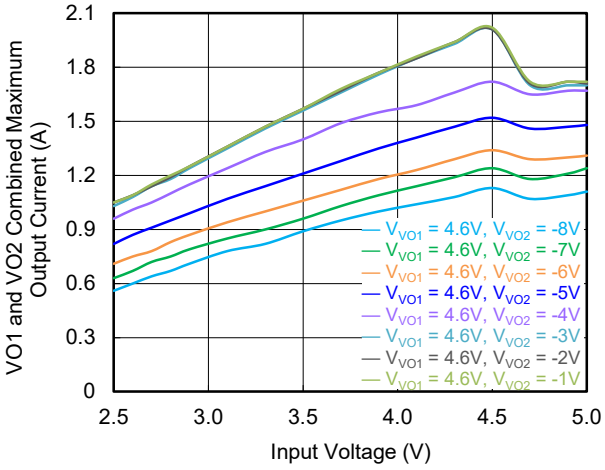
VO5 Efficiency vs. Output Current



VO5_LDO Efficiency vs. Output Current

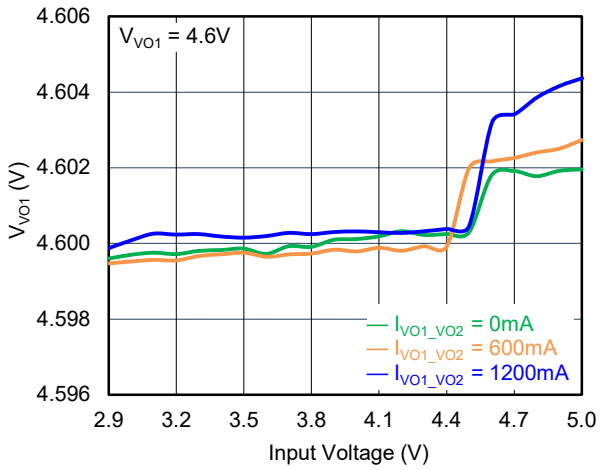


VO1 and VO2 Combined Maximum Output Current vs. Input Voltage

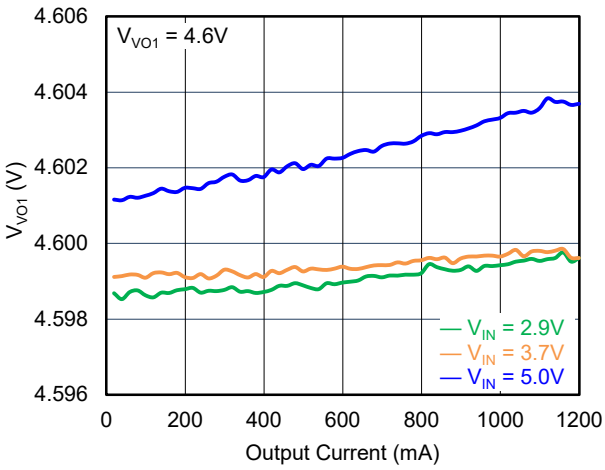


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

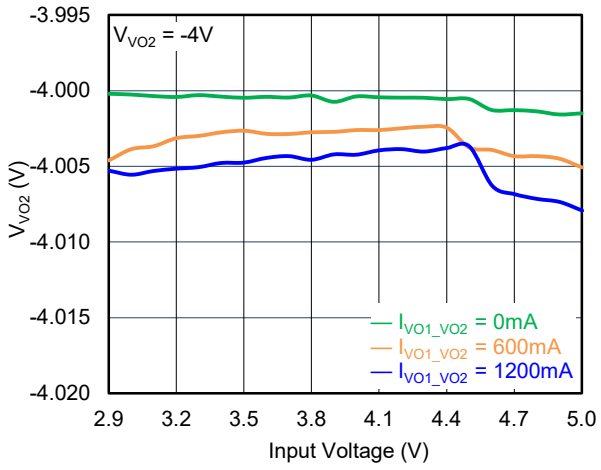
VO1 Line Regulation



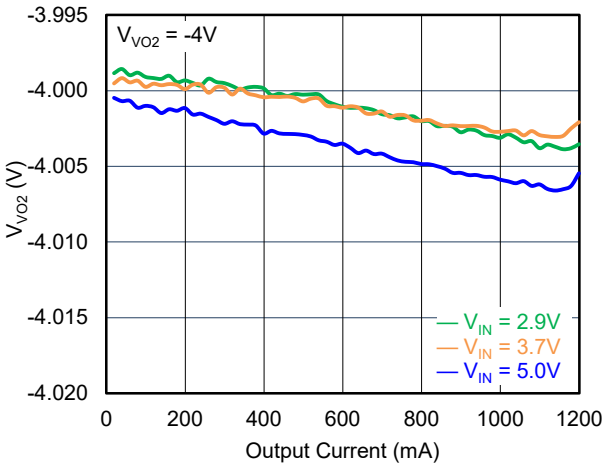
VO1 Load Regulation



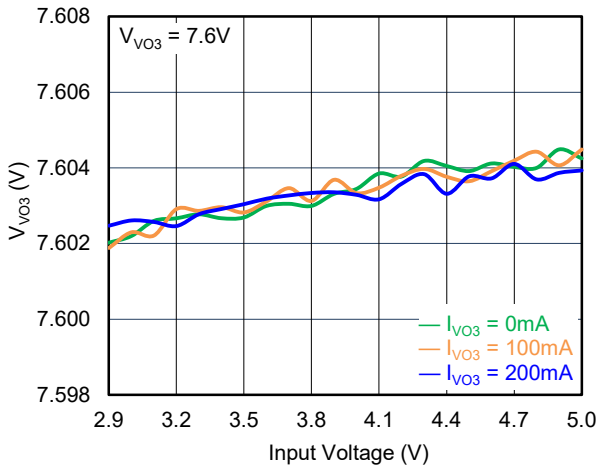
VO2 Line Regulation



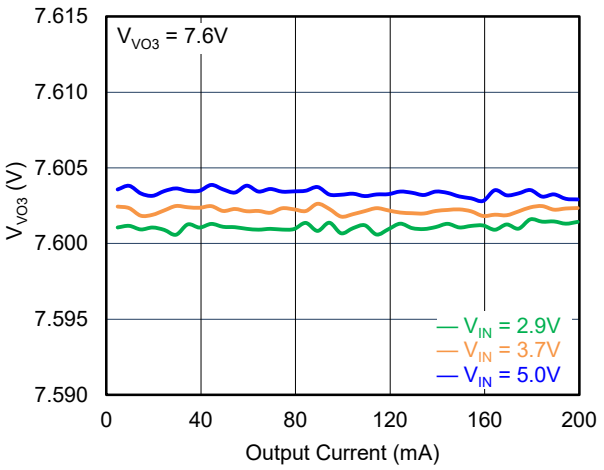
VO2 Load Regulation



VO3 Line Regulation

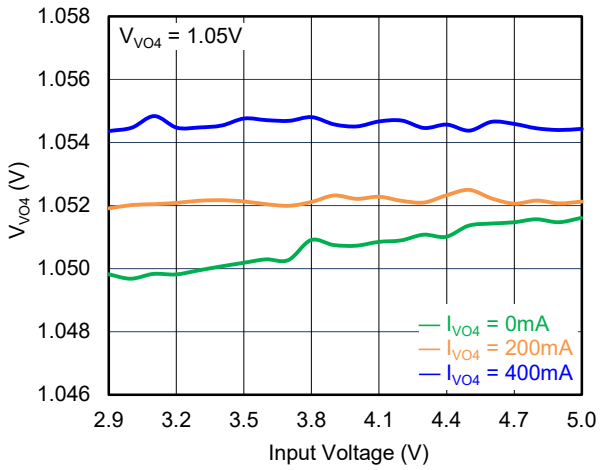


VO3 Load Regulation

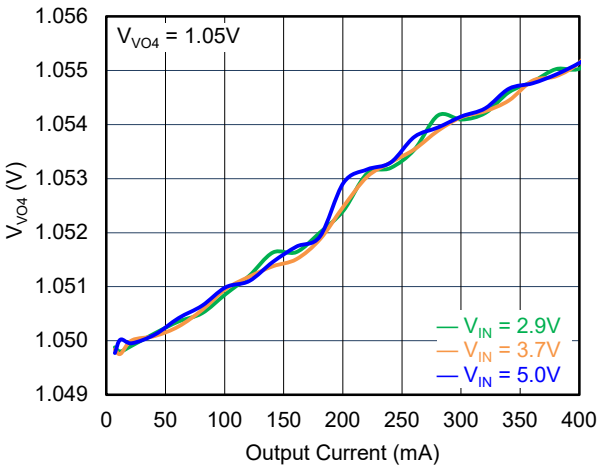


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

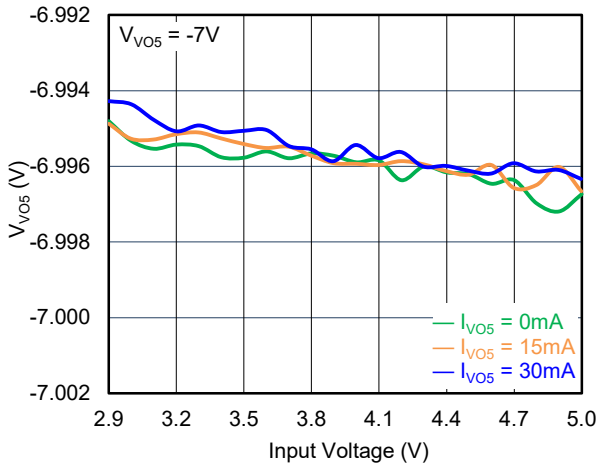
VO4 Line Regulation



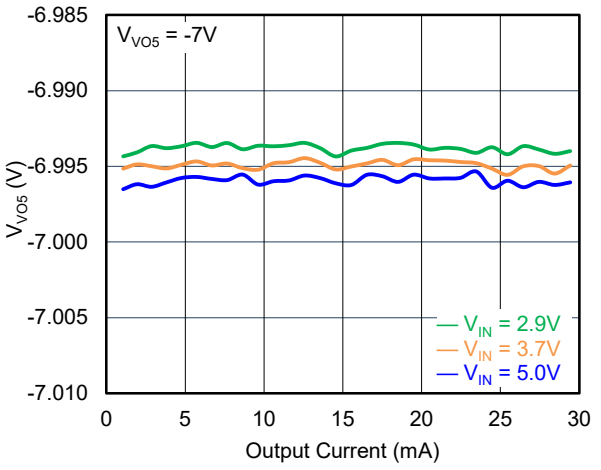
VO4 Load Regulation



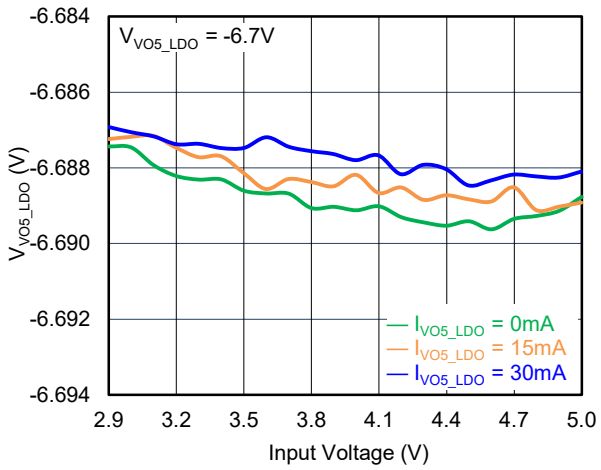
VO5 Line Regulation



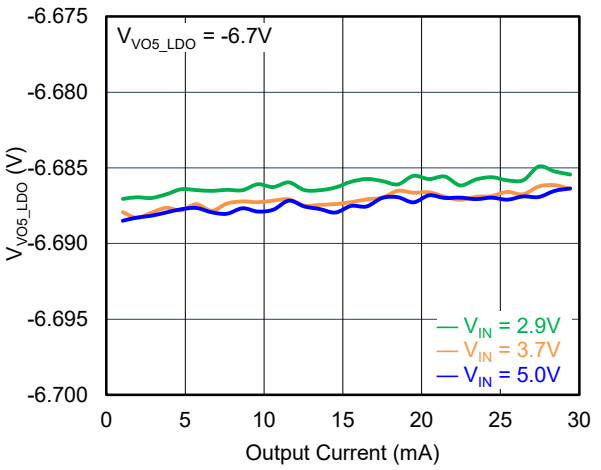
VO5 Load Regulation



VO5_LDO Line Regulation

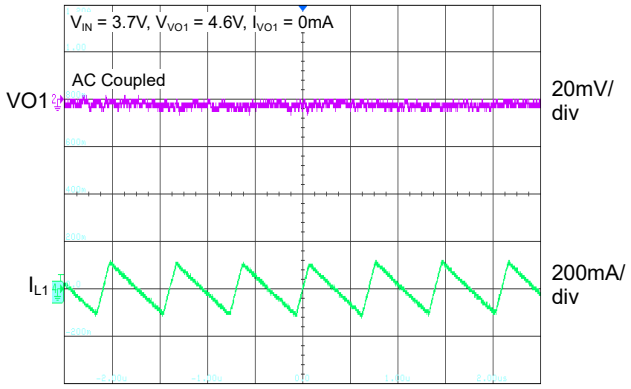


VO5_LDO Load Regulation

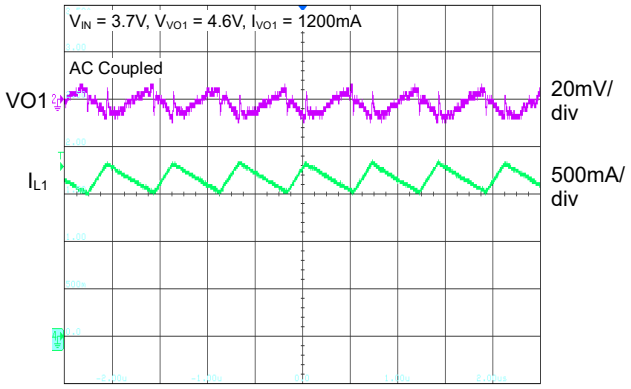


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

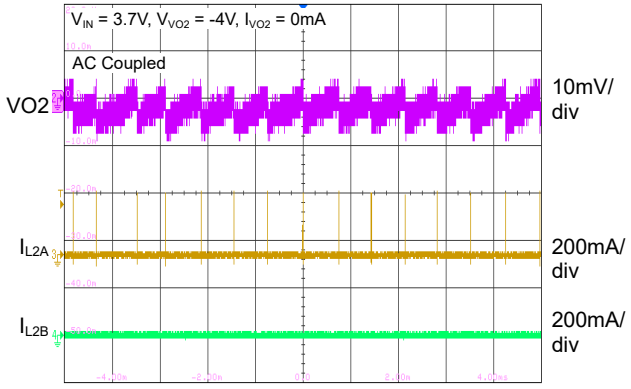
VO1 Output Voltage Ripple at No Load



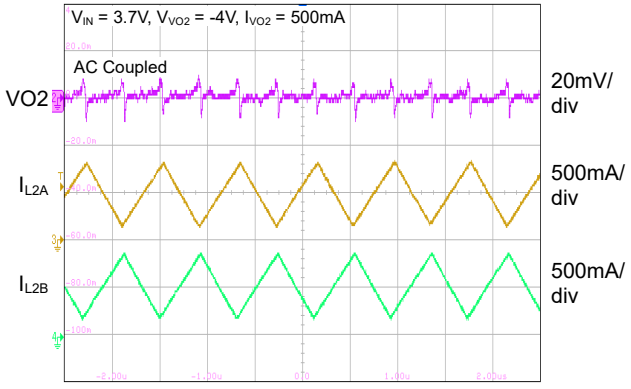
VO1 Output Voltage Ripple at Heavy Load



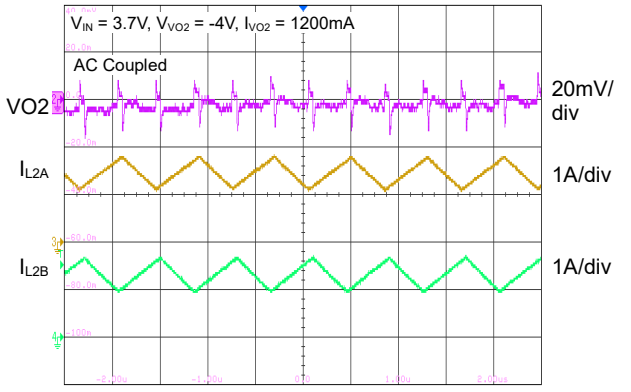
VO2 Output Voltage Ripple at No Load



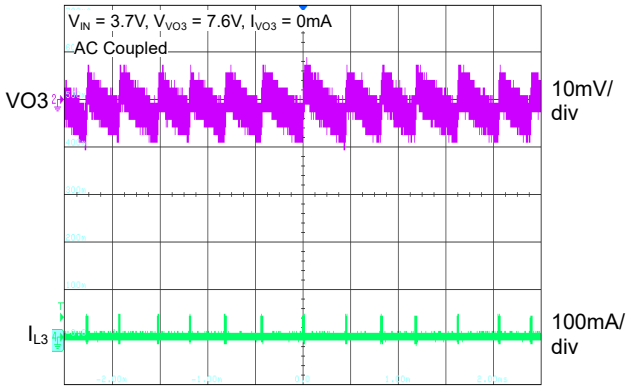
VO2 Output Voltage Ripple at Moderate Load



VO2 Output Voltage Ripple at Heavy Load

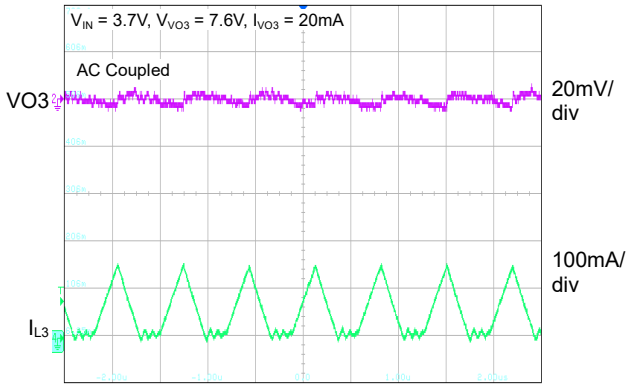


VO3 Output Voltage Ripple at No Load

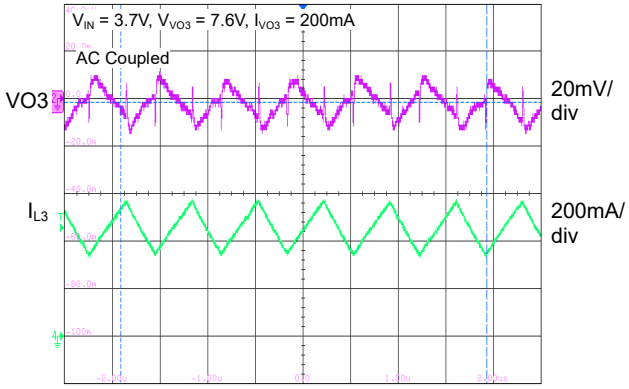


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

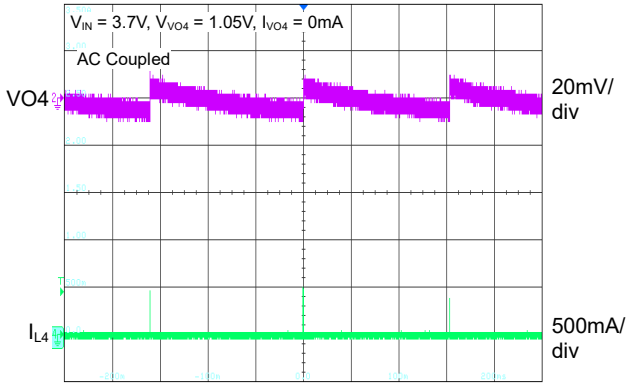
VO3 Output Voltage Ripple at Light Load



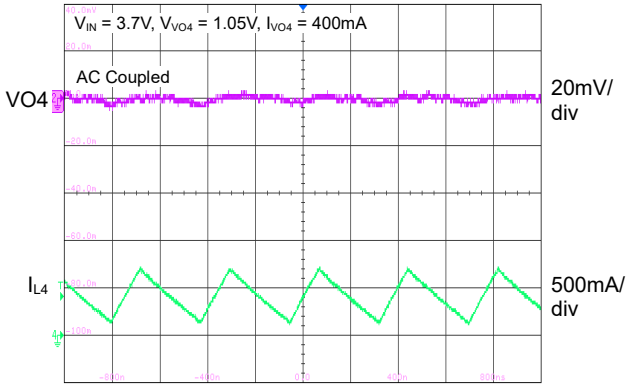
VO3 Output Voltage Ripple at Heavy Load



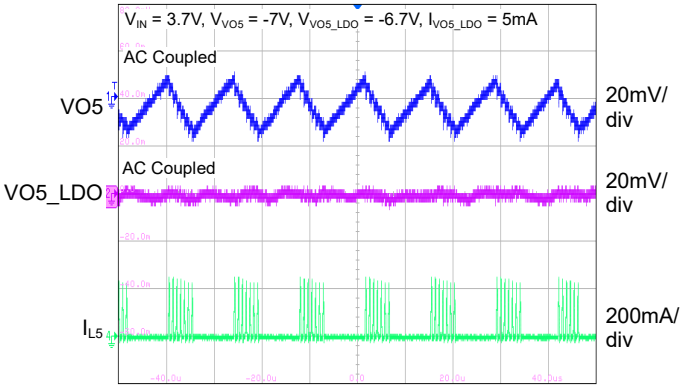
VO4 Output Voltage Ripple at No Load



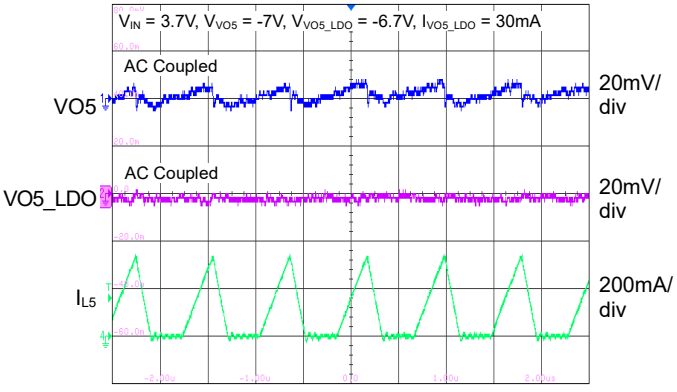
VO4 Output Voltage Ripple at Heavy Load



VO5 and VO5_LDO Output Voltage Ripple at Light Load

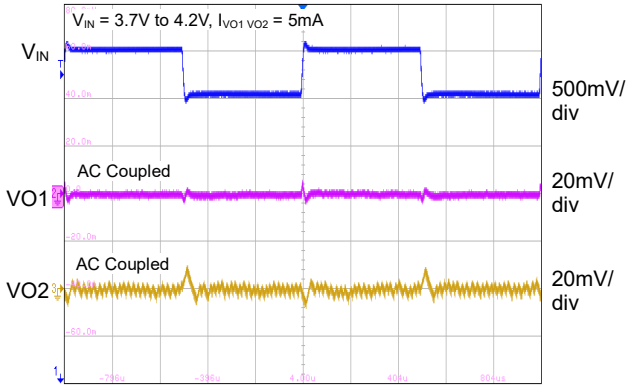


VO5 and VO5_LDO Output Voltage Ripple at Heavy Load



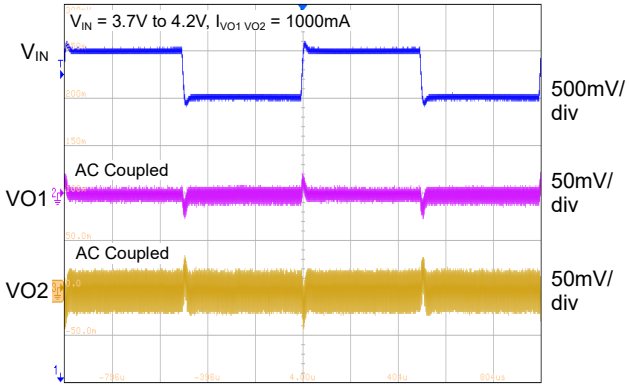
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VO1 and VO2 Line Transient at Light Load



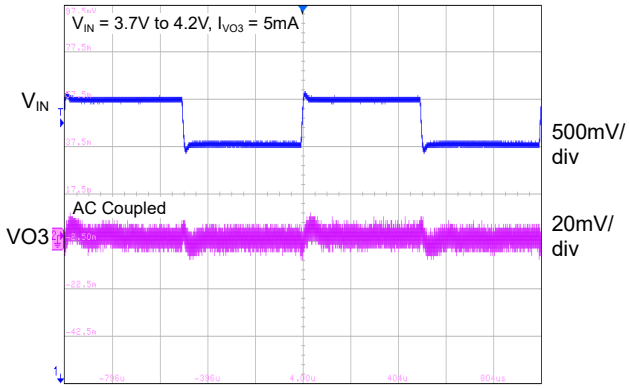
Time (200μs/div)

VO1 and VO2 Line Transient at Heavy Load



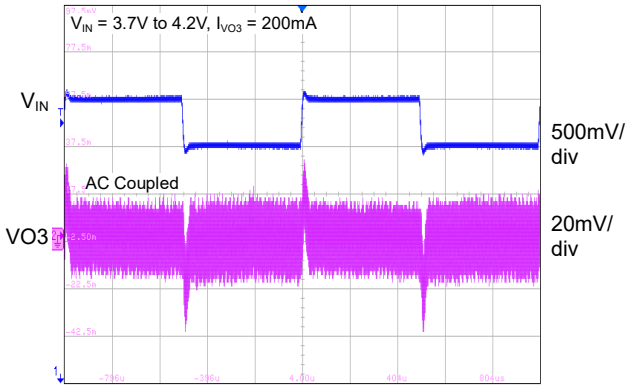
Time (200μs/div)

VO3 Line Transient at Light Load



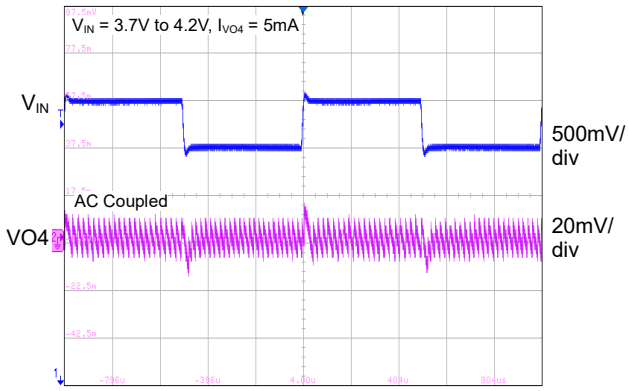
Time (200μs/div)

VO3 Line Transient at Heavy Load



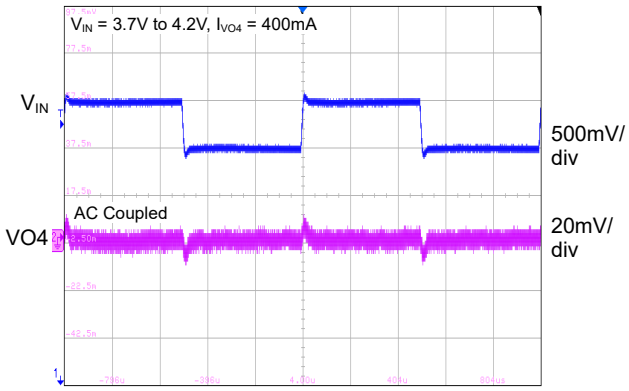
Time (200μs/div)

VO4 Line Transient at Light Load



Time (200μs/div)

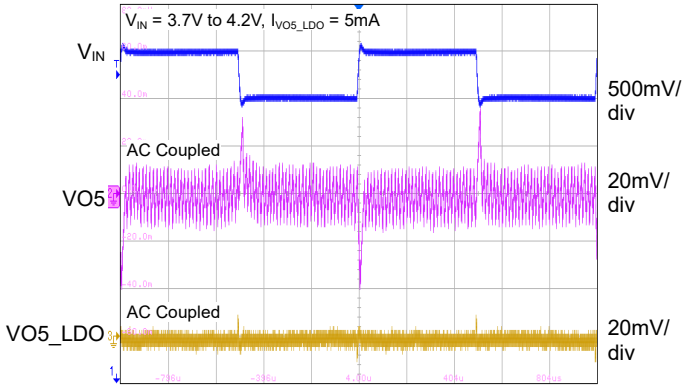
VO4 Line Transient at Heavy Load



Time (200μs/div)

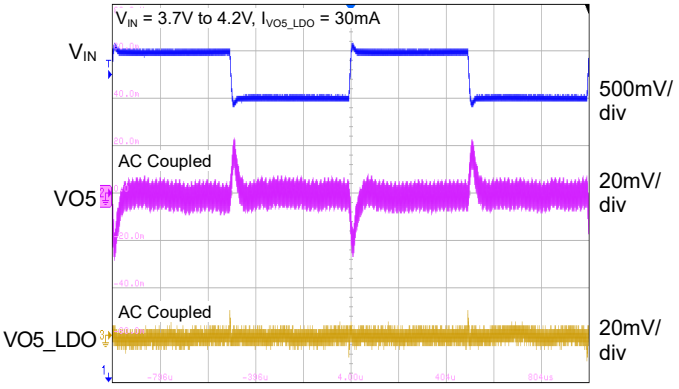
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VO5 and VO5_LDO Line Transient at Light Load



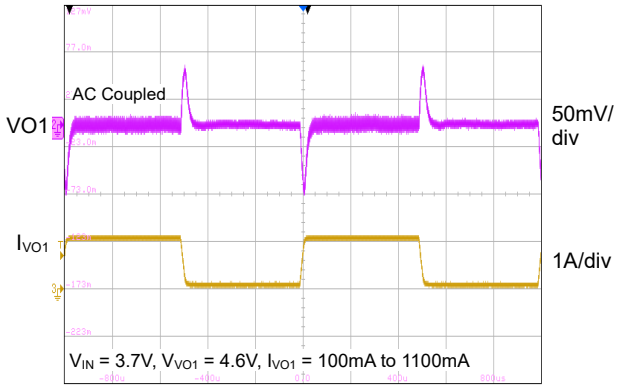
Time (200μs/div)

VO5 and VO5_LDO Line Transient at Heavy Load



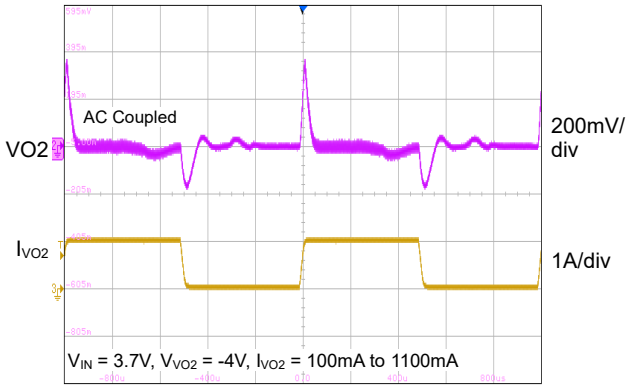
Time (200μs/div)

VO1 Load Transient



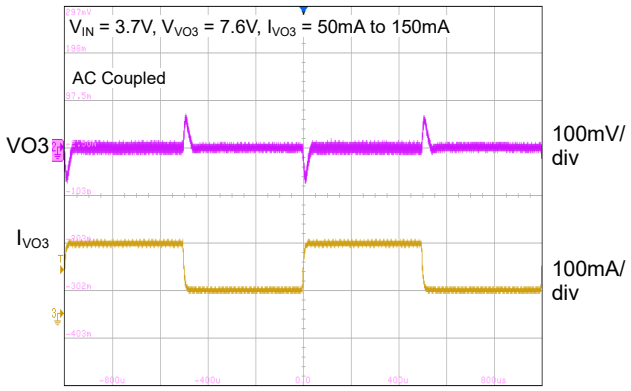
Time (200μs/div)

VO2 Load Transient



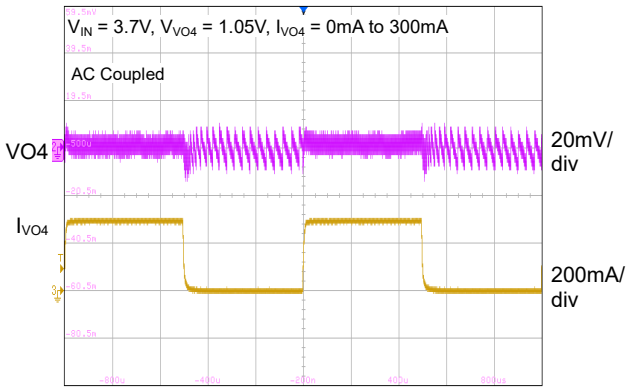
Time (200μs/div)

VO3 Load Transient



Time (200μs/div)

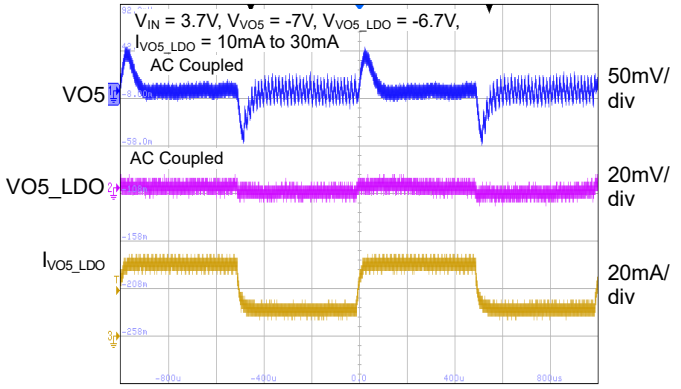
VO4 Load Transient



Time (200μs/div)

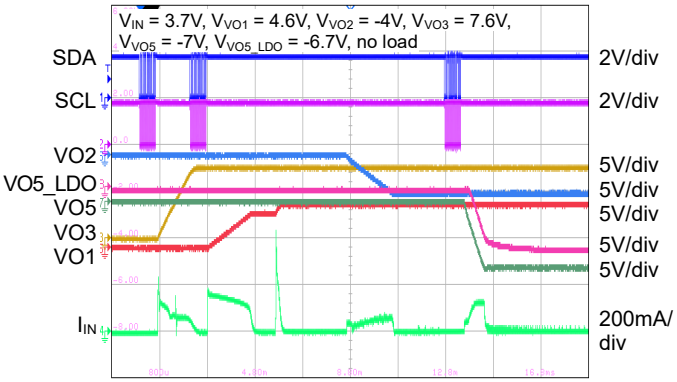
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VO5 and VO5_LDO Load Transient



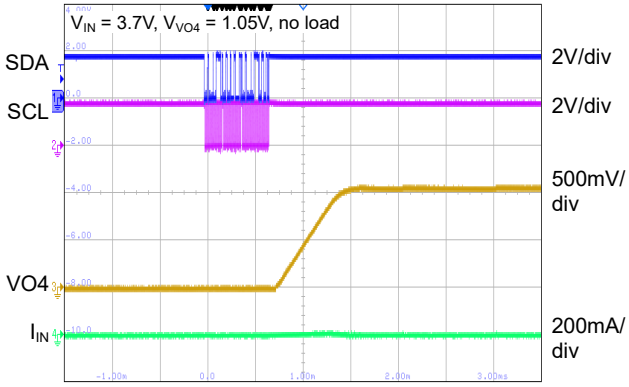
Time (200μs/div)

Start-Up Sequence



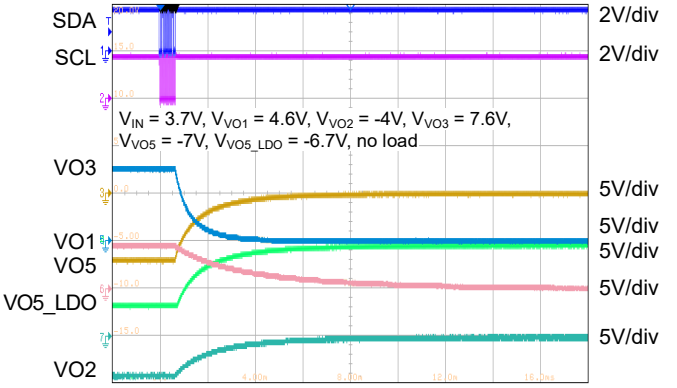
Time (2ms/div)

Start-Up Sequence



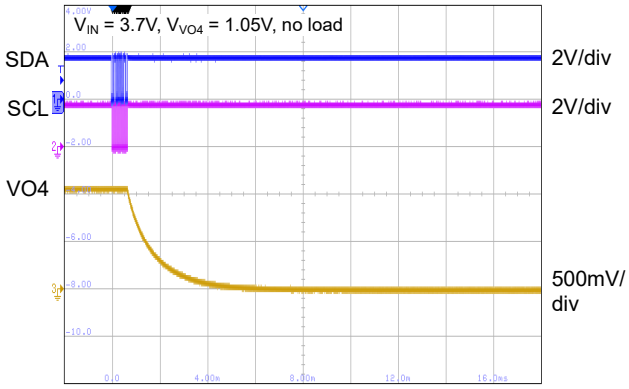
Time (500μs/div)

Shutdown Sequence Discharge = ON



Time (2ms/div)

Shutdown Sequence Discharge = ON



Time (2ms/div)

FUNCTIONAL BLOCK DIAGRAM

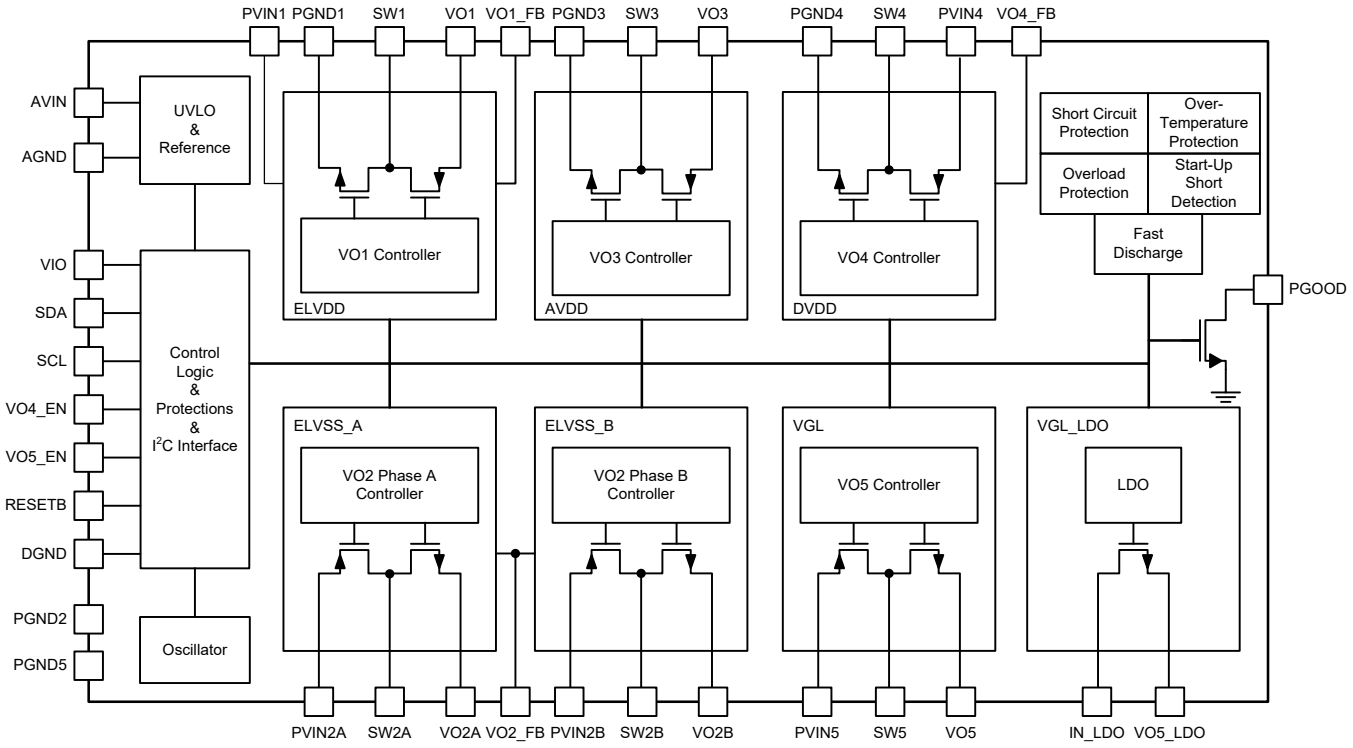


Figure 3. Functional Block Diagram

TIMING DIAGRAMS

Power-Up Sequence

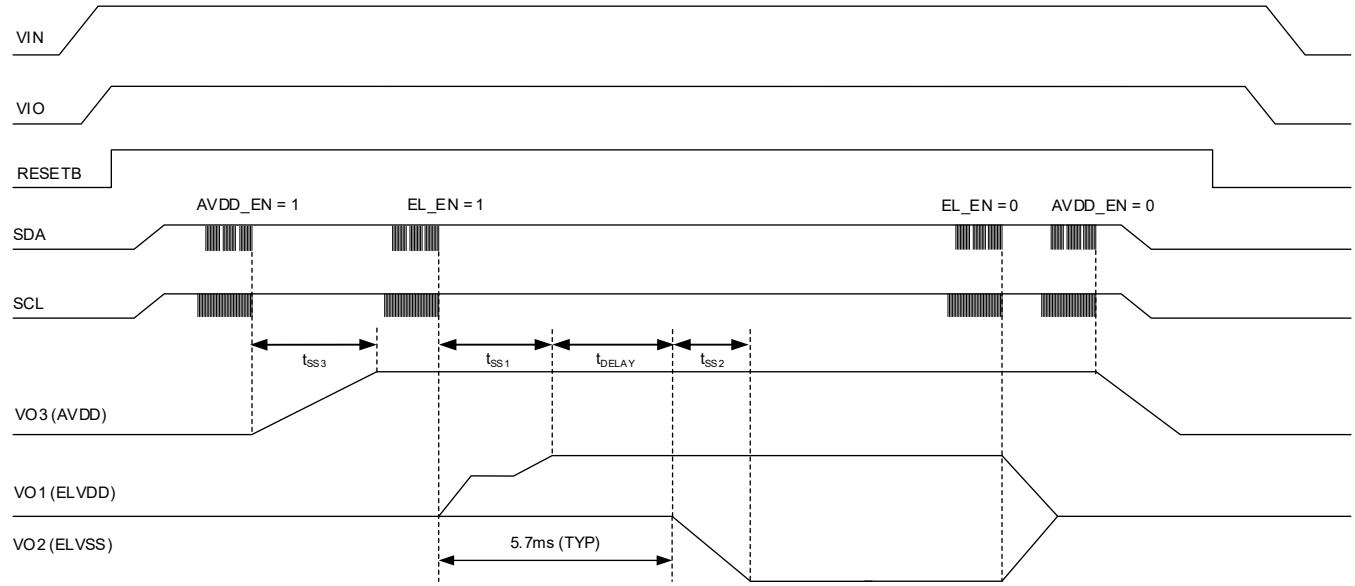


Figure 4. Power-Up Sequence with I²C

TIMING DIAGRAMS (continued)

DVDD Power-Up Timing Sequence

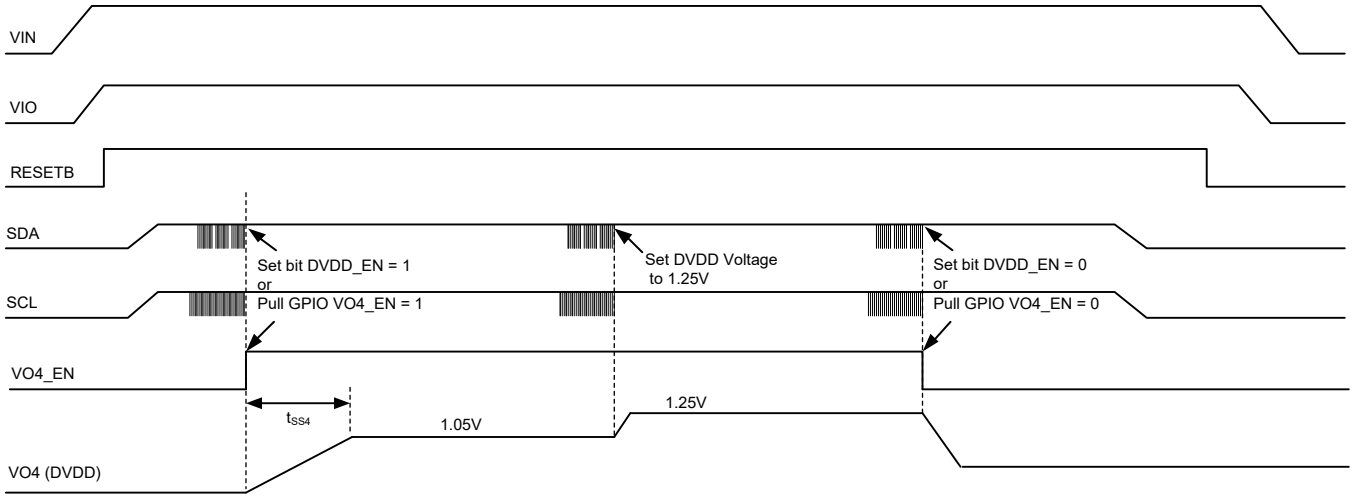


Figure 5. DVDD Timing Sequence

VGL Power-Up Timing Sequence

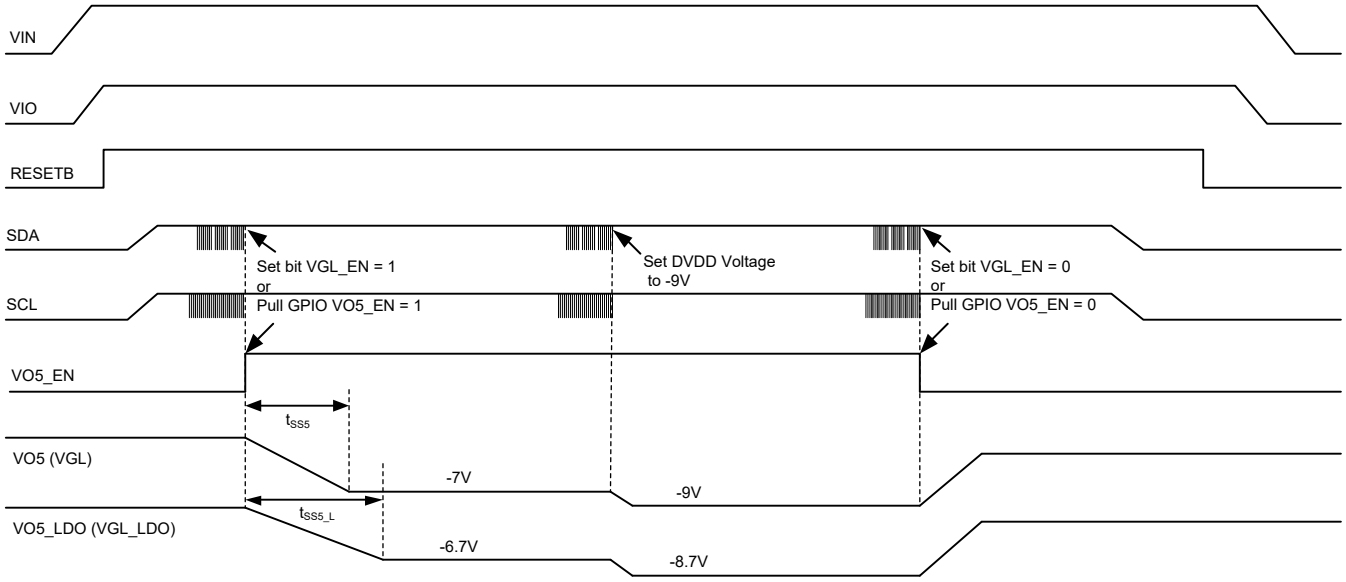


Figure 6. VGL Timing Sequence

DETAILED DESCRIPTION

Under-Voltage Lockout (UVLO)

The built-in under-voltage lockout function (UVLO) monitors the input voltage and disables the device when the input voltage is too low to operate.

Thermal Shutdown (TSD)

The device has a function of thermal shutdown, which prevents the device from damage due to overheating and excessive power dissipation. The device stops switching and shuts down all the outputs when the junction temperature exceeds +150℃ (TYP), and restarts with the same programmed voltages and sequences when the temperature decreases to +135℃ (TYP).

Boost Converter VO1 (ELVDD)

The Boost converter VO1 operates with a valley-current-mode topology and fixed 1.45MHz (TYP) frequency. The VO1 output voltage can be programmed between 4.6V and 5.0V (default 4.6V) with 100mV steps (see ELVDD_SET register).

The output sense pin (VO1_FB) is always connected to the positive pin of output capacitor for the highest output voltage accuracy.

The output of VO1 is fully isolated in shutdown mode.

Inverting Buck-Boost Converter VO2 (ELVSS)

The inverting Buck-Boost converter VO2 operates with a peak-current-mode topology and dual-phase fixed 1.25MHz (TYP) frequency. The VO2 output voltage can be programmed between -1.0V and -8.0V (default -4V) with 50mV steps (see ELVSS_SET register).

When the load current exceeds 200mA, both phase A and phase B of the inverting Buck-Boost converter work. And only phase A works when the load current decreases to 130mA for reducing the switching loss.

The output of VO2 is fully isolated in shutdown mode.

Boost Converter VO3 (AVDD)

The Boost converter VO3 operates with a peak-current-mode topology and fixed 1.45MHz (TYP) frequency. The VO3 output voltage can be programmed between 5.7V and 8.0V (default 7.6V) with 50mV steps (see AVDD_SET register).

The output of VO3 is fully isolated in shutdown mode.

Buck Converter VO4 (DVDD)

The Buck converter VO4 operates with an adaptive COT (constant-on-time) mode topology. The VO4 output voltage can be programmed between 0.7V and 2.1V (default 1.05V) with 25mV steps (see DVDD_SET register).

The output of VO4 is fully isolated in shutdown mode.

Inverting Buck-Boost Converter VO5 (VGL)

The inverting Buck-Boost converter VO5 operates with a peak-current-mode topology and fixed 1.25MHz (TYP) frequency. The VO5 output voltage can be programmed between -4V and -12.5V (default -7V) with 100mV steps (see VGL_SET register).

The output of VO5 is fully isolated in shutdown mode.

VO5_LDO (VGL_LDO)

The device contains a negative voltage LDO. The absolute output voltage is always 300mV lower than the input voltage.

The output of VO5_LDO is fully isolated in shutdown mode.

Output Current Capacity

The device operates with an input voltage range of 2.9V to 5.0V. However, due to different input voltage and different output voltage, the output current capacity is quite different. A lower input voltage (above UVLO) or a higher output voltage leads to a lower output current capacity.

Input Power Supply

The input power supply voltage is recommended between 2.9V and 5.0V. To achieve full performance, a stable and noise-free input source is needed. Once the distance between input source and SGM3843 is a bit long, additional capacitors are suggested to place as close to the device as possible. Please refer to the typical application circuit for the suggested input capacitance.

DETAILED DESCRIPTION (continued)

Soft-Start, Start-Up, Discharge and Shutdown

The built-in soft-start function is adopted to limit the inrush current.

Writing EL_EN bit enables the VO1 Boost converter. VO1 starts with a 0.4A soft-start current limit until it rises to the programmed voltage. Then the full current limit is active (2.9A, TYP).

5.7ms after writing 1 to EL_EN bit, the VO2 converter starts switching phase A (VO2A) with a 0.8A current limit until the VO2 rises to the default voltage (-4V). Then the full current limit is active (3.6A per phase, TYP).

Writing AVDD_EN bit enables the VO3 Boost converter. Before VO3 rises to the default value (7.6V), it rises linearly for 1.9ms with a 0.35A current limit. Then the full current limit is active (1.23A, TYP).

Toggling VO4_EN high starts the VO4 Buck converter. Before VO4 rises to the default value (1.05V), it rises linearly for 1ms with a 0.65A current limit. Then the full current limit is active (1.2A, TYP).

Toggling VO5_EN high starts the VO5 Buck-Boost inverting converter and the VO5_LDO. Before VO5 rises to the default value (-7V), it rises linearly for 1ms with a 0.65A current limit. Then the full current limit is active (1.05A, TYP).

The output discharge function can be controlled by the fast discharge control bits (*_FD) in ENABLE1 and ENABLE2 registers.

Short Circuit and Overload Protection

The device is protected from damage of all the converters shorting to ground. The device is also protected when V_{ELVDD} and V_{ELVSS} are shorted together.

A short at anyone of V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} can shut down all the four converters, then the shutdown state is latched, and the input is fully disconnected with these outputs.

The device detects a short or an overload when one of the below conditions is fulfilled:

- V_{ELVDD} is not in regulation 2.5ms after V_{ELVDD} is enabled then V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} converters shut down.
- V_{ELVSS} is not in regulation 6.7ms after V_{ELVSS} is enabled then V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} converters shut down.
- V_{AVDD} protection is enabled when the soft-start is completed.
- V_{VGL} protection is enabled when the soft-start is completed.
- V_{ELVDD} falls below 87% of the programmed output voltage longer than 1ms then all converters shut down.
- V_{ELVSS} rises above 83% of the programmed output voltage longer than 1ms then all converters shut down.
- V_{AVDD} falls below 86% of the programmed output voltage longer than 1ms then all converters shut down.
- V_{VGL} rises above 76% of the programmed output voltage longer than 1ms then all converters shut down.

Device Reset

In order to reset the whole device, V_{IN} has to cycle below UVLO.

- Pulling RESETB low or a power cycle resets all settings to default values.
- Short circuit at one of the V_{ELVDD}, V_{ELVSS}, V_{AVDD} and V_{VGL} resets all enable bit settings of the four converters.
- Writing EL_EN = 0 resets the output voltage of ELVDD and ELVSS.
- Writing AVDD_EN = 0 resets the output voltage of AVDD.
- Writing DVDD_EN = 0 or toggling VO4_EN low resets the output voltage of DVDD.
- Writing VGL_EN = 0 or toggling VO5_EN low resets the output voltage of VGL and VGL_LDO.
- Pulling RESETB high resets the VGL_EN_SELECT[1:0] bits.
- Fast discharge control bits (*_FD) can only be reset by power cycle.
- All voltage settings can only be reset by power cycle.

DETAILED DESCRIPTION (continued)

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM3843 parameters and get status reports. I²C is well-known 2 wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master and generates the SCL clock as long as it is master. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM3843 operates as a slave device with address 0x08 (08H). It has twelve 8-bit registers.

Physical Layer

Bus lines are pulled high by pull-up resistors and in logic high state with no clocking when the bus is free. The pull-up resistors that are tied to SDA and SCL lines should be greater than 1.2kΩ at 3.3V or 1.8kΩ at 5V supply respectively. The SGM3843 does not support the general call. The SDA and SCL pins are open-drain.

I²C Data Communication

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The transaction is terminated by releasing the bus when the data transfer job is done as shown in Figure 7. All transactions begin by the master who applies a START condition on the bus lines to take over the bus and exchange data. At the end, the master terminates the transaction by applying one (or more) STOP condition. START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP the bus is considered busy.

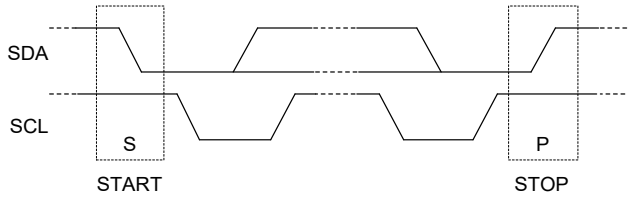


Figure 7. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable on the SDA line during the HIGH period of the clock. The state of the SDA can only change when the clock (SCL) is LOW. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 8.

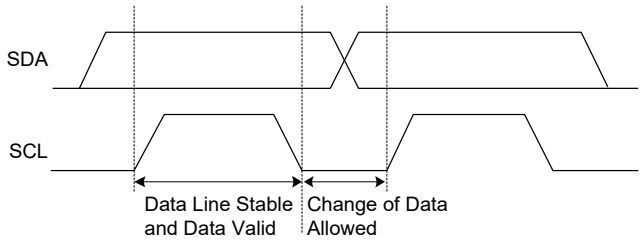


Figure 8. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 9 shows the byte transfer process with I²C interface.

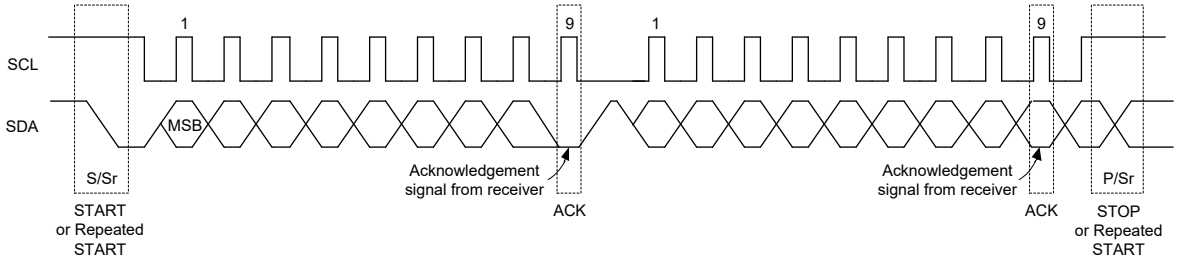


Figure 9. Byte Transfer Process

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte was received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by the master, including for the acknowledge clock pulse. SDA line is released for receiver control during the acknowledge clock pulse and the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that the master can either STOP (P) to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then without a stop condition another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/W). R/W bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 10.

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 11 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 12), it sends a new START condition along with device address with R/W bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

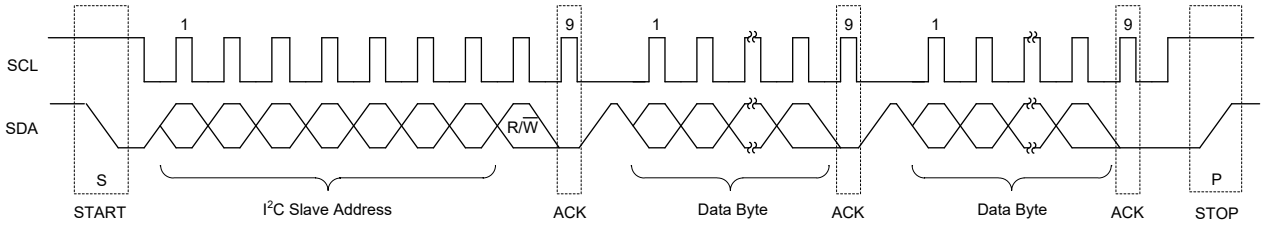


Figure 10. Data Transfer Transaction

DETAILED DESCRIPTION (continued)

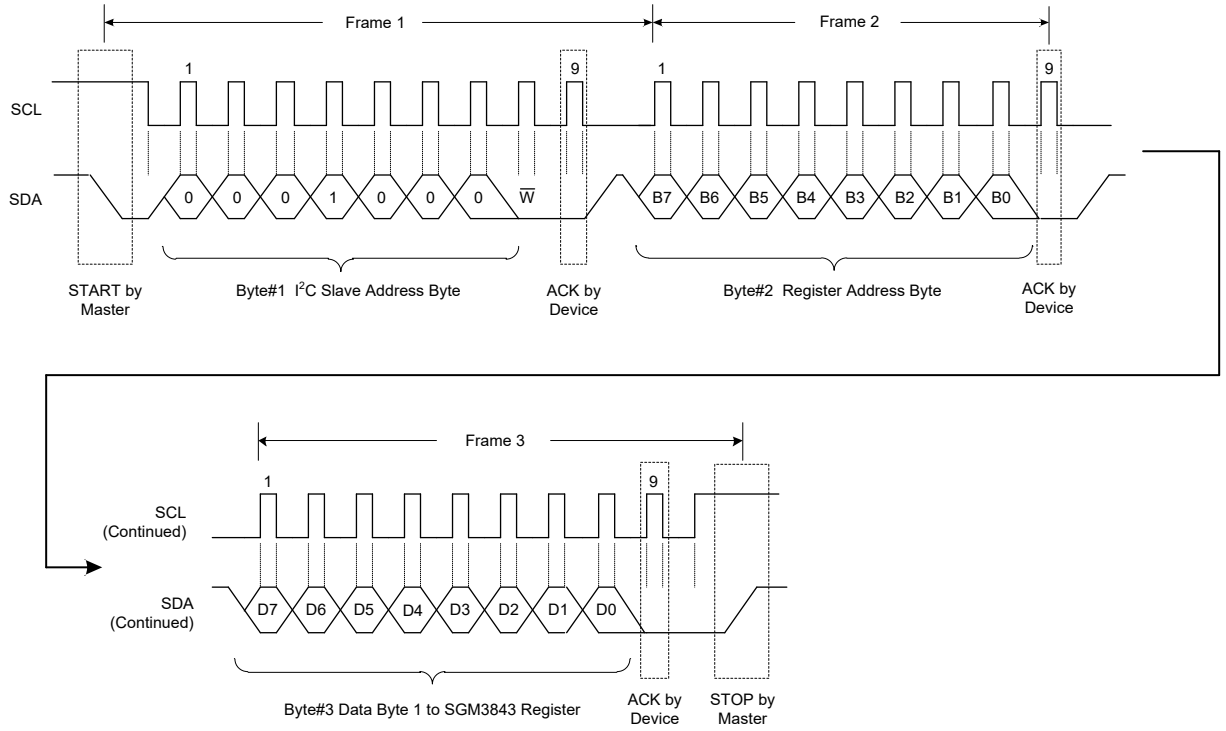


Figure 11. A Single Write Transaction

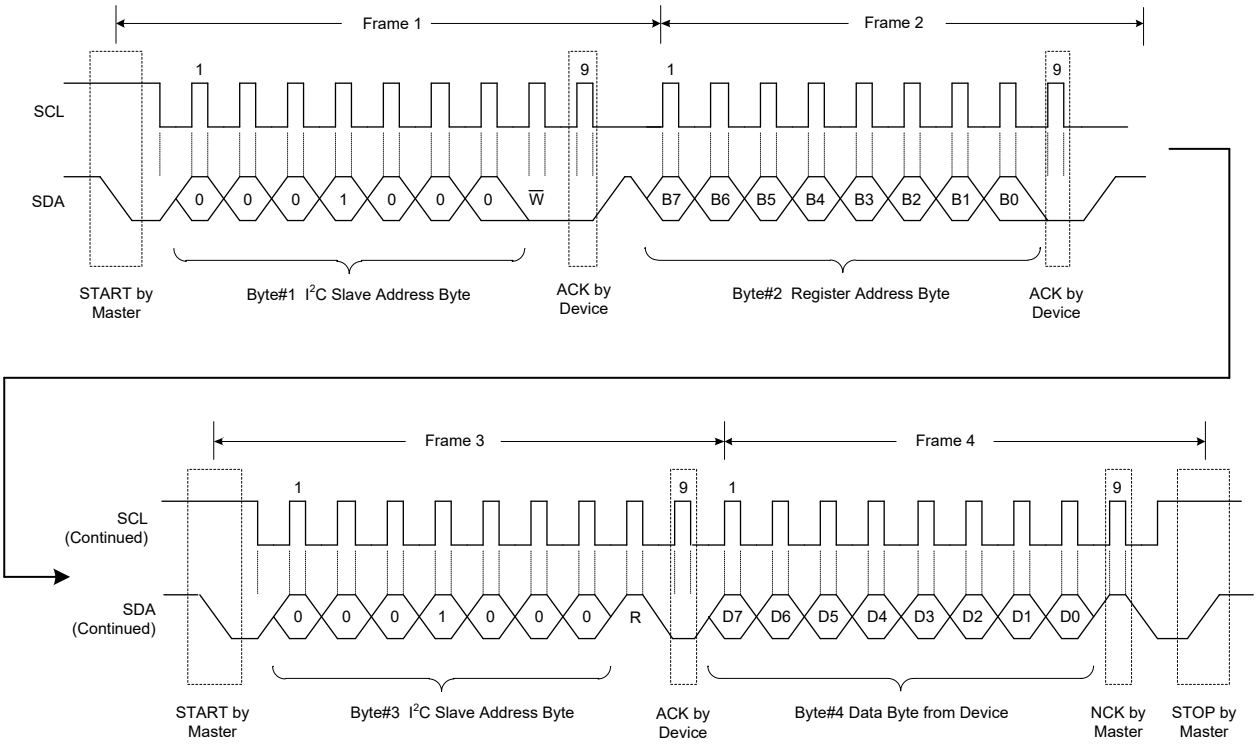


Figure 12. A Single Read Transaction

DETAILED DESCRIPTION (continued)

Data Transactions with Multi-Read or Multi-Write

Multi-read and multi-write are supported by SGM3843 as explained in Figure 13 and Figure 14. In a multi-write transaction, every new data byte sent by master is written to the next register of the device. A STOP is sent whenever master is done with writing into device registers.

In a multi-read transaction, after receiving the first register data (whose address is already written to the slave), the master replies with an ACK to ask the slave for sending the next register data. This can continue as much as it is needed by master. Master sends back an NCK after the last received byte and issues a STOP condition.

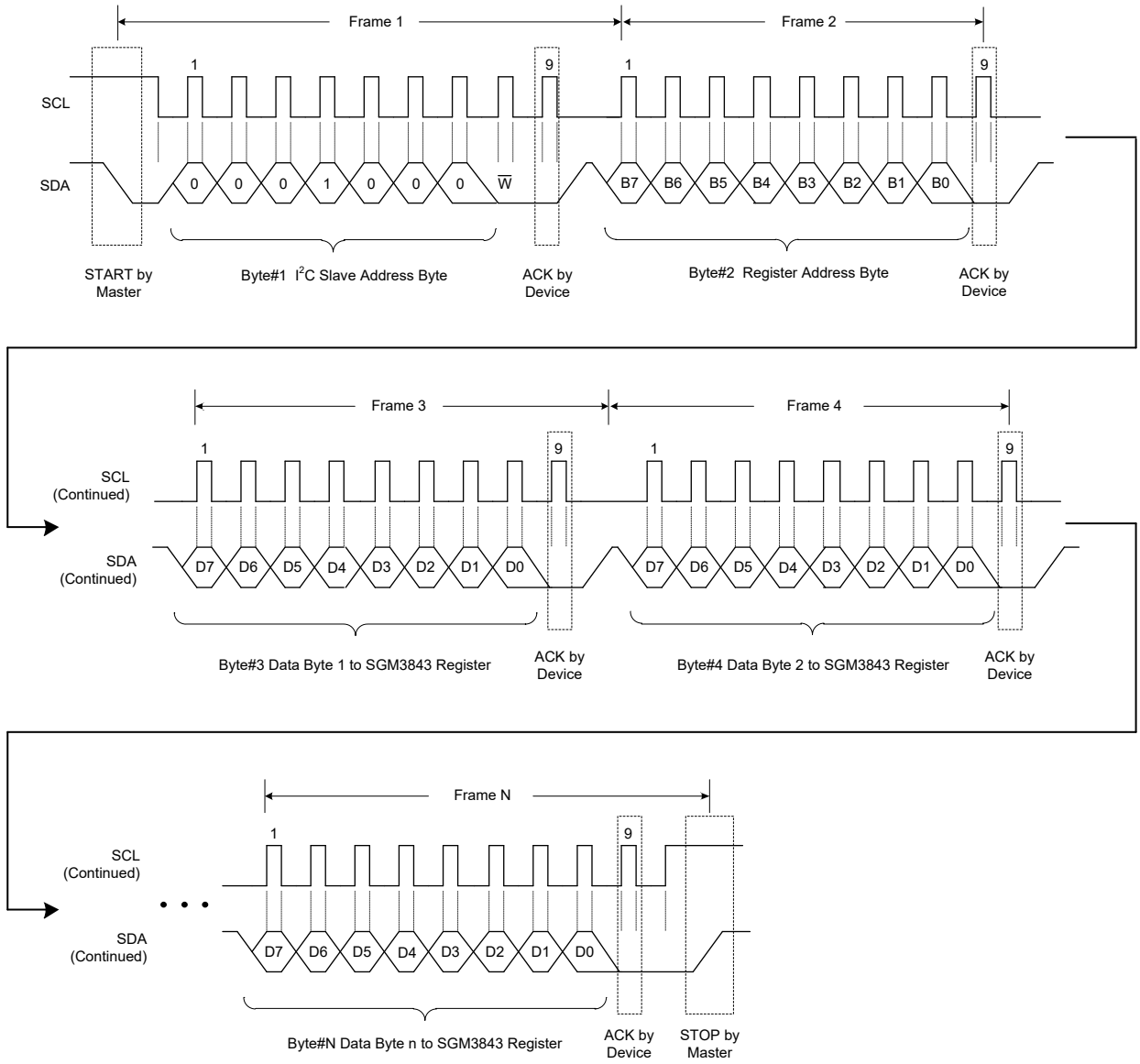


Figure 13. A Multi-Write Transaction

DETAILED DESCRIPTION (continued)

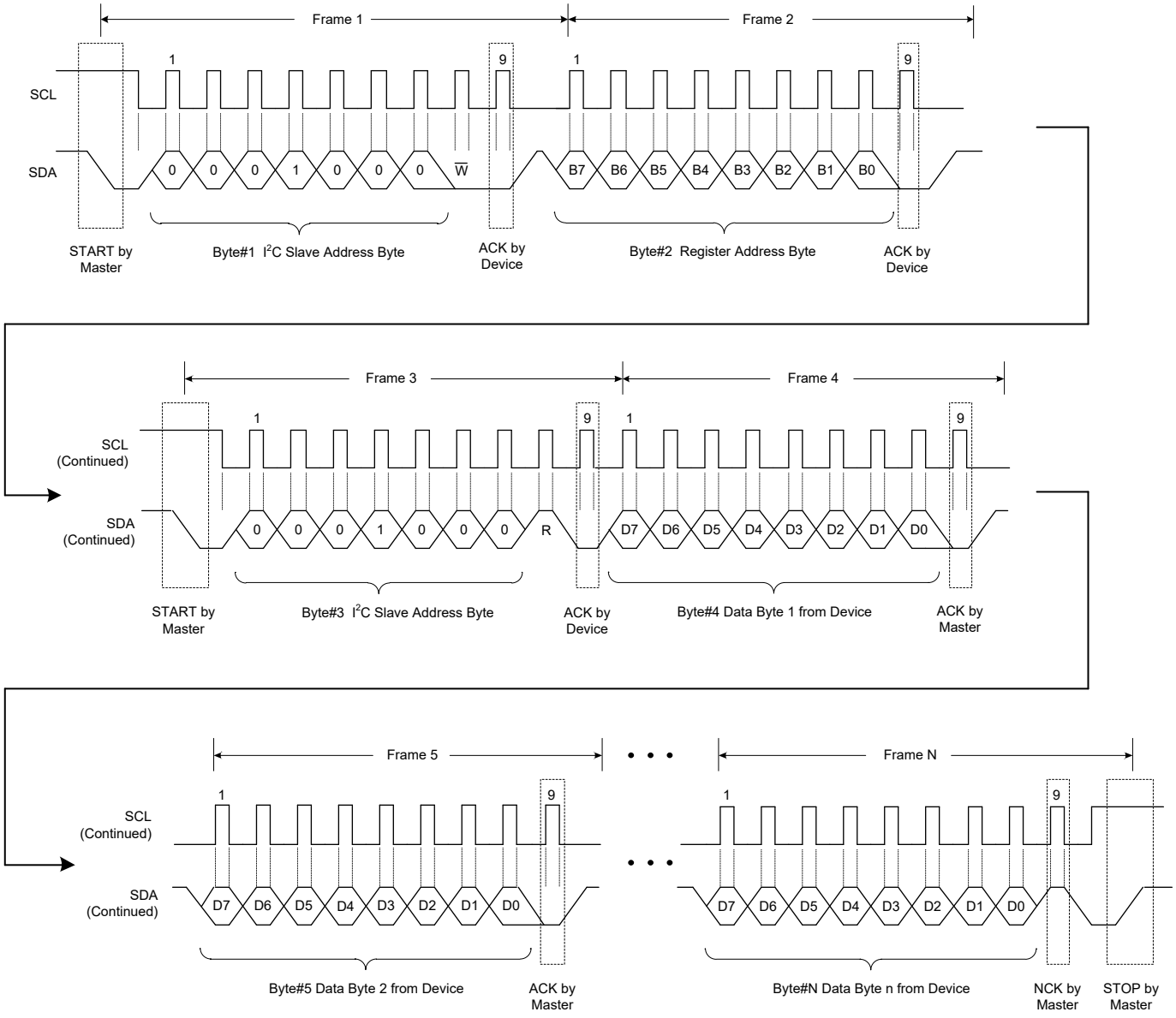


Figure 14. A Multi-Read Transaction

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address of SGM3843 is: 0x08(0001000 + W/R)

Bit Types:
R: Read only
R/W: Read/Write

Table 2. Register Map

REGISTER NAME	ADDRESS	BIT NAME AND DEFAULT VALUE							
		D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
REG_STATUS	0x02	POWER_GOOD	ELVDD_POK	ELVSS_POK	AVDD_POK	VDD_POK	VGL_POK	Reserved	
		0	0	0	0	0	0	0	0
VGL_SET	0x1C	Reserved	REG_VGL[6:0]						
		0	0	0	1	1	1	1	0
SPARE1	0x1D	Reserved							
		0	0	0	1	1	1	0	0
DVDD_SET	0x1E	Reserved		REG_VDD[5:0]					
		0	0	0	0	1	1	1	0
ENABLE1	0x1F	SSD_EN	Reserved	VGL_FD	DVDD_FD	VGL_EN_SELECT[1:0]		VGL_EN	VDD_EN
		0	0	1	1	0	0	0	0
ENABLE2	0x20	HLPM_EN	LPD_EN[2:0]			AVDD_FD	EL_FD	AVDD_EN	EL_EN
		0	0	0	0	1	1	0	0
ELVSS_SET	0x21	REG_VO2[7:0]							
		0	1	0	1	0	0	0	0
ELVDD_SET	0x22	Reserved					REG_VO1[2:0]		
		0	0	0	0	0	0	0	0
AVDD_SET	0x23	Reserved		REG_VO3[5:0]					
		0	0	0	0	1	0	0	0
SPARE3	0x24	Reserved							
		0	0	0	0	0	0	0	0
Device ID	0x25	DEVICE_ID[3:0]				DEVICE_REV[3:0]			
		1	1	0	0	0	0	0	0
I²C Slave Address	0x26	SLAVE_ADDRESS[7:0]							
		0	0	0	1	0	0	0	0

REGISTER MAPS (continued)

REG0x02: REG_STATUS Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	POWER_GOOD	0	R	Power-Good Signal 0 = PMIC Protection or Shutdown 1 = PMIC Operation
D[6]	ELVDD_POK	0	R	Power_OK Signal of ELVDD 0 = ELVDD OFF 1 = ELVDD ON
D[5]	ELVSS_POK	0	R	Power-OK Signal ELVSS 0 = ELVSS OFF 1 = ELVSS ON
D[4]	AVDD_POK	0	R	Power-OK Signal of AVDD 0 = AVDD OFF 1 = AVDD ON
D[3]	VDD_POK	0	R	Power-OK Signal of VDD 0 = VDD OFF 1 = VDD ON
D[2]	VGL_POK	0	R	Power-OK Signal of VGL 0 = VGL OFF 1 = VGL ON
D[1:0]	Reserved	00	R	Reserved

REG0x1C: VGL_SET Register Address [reset = 0x1E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0	R/W	Reserved
D[6:0]	REG_VGL[6:0]	0011110	R/W	VGL Output Control V_{GL} = REG_VGL[6:0] × (-100mV) - 4.0V Offset: -4.0V Range: -4.0V (0000000) ~ -12.5V (1010101) Default: -7V (0011110)

Table 3. REG_VGL[6:0] Description

Data (Hex)	VO5 (VGL)	Data (Hex)	VO5 (VGL)	Data (Hex)	VO5 (VGL)	Data (Hex)	VO5 (VGL)	Data (Hex)	VO5 (VGL)
0x00	-4.0V	0x12	-5.8V	0x24	-7.6V	0x36	-9.4V	0x48	-11.2V
0x01	-4.1V	0x13	-5.9V	0x25	-7.7V	0x37	-9.5V	0x49	-11.3V
0x02	-4.2V	0x14	-6.0V	0x26	-7.8V	0x38	-9.6V	0x4A	-11.4V
0x03	-4.3V	0x15	-6.1V	0x27	-7.9V	0x39	-9.7V	0x4B	-11.5V
0x04	-4.4V	0x16	-6.2V	0x28	-8.0V	0x3A	-9.8V	0x4C	-11.6V
0x05	-4.5V	0x17	-6.3V	0x29	-8.1V	0x3B	-9.9V	0x4D	-11.7V
0x06	-4.6V	0x18	-6.4V	0x2A	-8.2V	0x3C	-10.0V	0x4E	-11.8V
0x07	-4.7V	0x19	-6.5V	0x2B	-8.3V	0x3D	-10.1V	0x4F	-11.9V
0x08	-4.8V	0x1A	-6.6V	0x2C	-8.4V	0x3E	-10.2V	0x50	-12.0V
0x09	-4.9V	0x1B	-6.7V	0x2D	-8.5V	0x3F	-10.3V	0x51	-12.1V
0x0A	-5.0V	0x1C	-6.8V	0x2E	-8.6V	0x40	-10.4V	0x52	-12.2V
0x0B	-5.1V	0x1D	-6.9V	0x2F	-8.7V	0x41	-10.5V	0x53	-12.3V
0x0C	-5.2V	0x1E	-7.0V	0x30	-8.8V	0x42	-10.6V	0x54	-12.4V
0x0D	-5.3V	0x1F	-7.1V	0x31	-8.9V	0x43	-10.7V	0x55	-12.5V
0x0E	-5.4V	0x20	-7.2V	0x32	-9.0V	0x44	-10.8V		
0x0F	-5.5V	0x21	-7.3V	0x33	-9.1V	0x45	-10.9V		
0x10	-5.6V	0x22	-7.4V	0x34	-9.2V	0x46	-11.0V		
0x11	-5.7V	0x23	-7.5V	0x35	-9.3V	0x47	-11.1V		

REGISTER MAPS (continued)

REG0x1E: DVDD_SET Register Address [reset = 0x0E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:0]	REG_VDD[5:0]	001110	R/W	VDD Output Control V_{DD} = REG_VDD[5:0] × 25mV + 0.7V Offset: 0.7V Range: 0.7V (000000) ~ 2.1V (111000) Default: 1.05V (001110)

Table 4. REG_VDD[5:0] Description

Data (Hex)	VO4 (VDD)	Data (Hex)	VO4 (VDD)	Data (Hex)	VO4 (VDD)	Data (Hex)	VO4 (VDD)	Data (Hex)	VO4 (VDD)
0x00	0.700V	0x0C	1.000V	0x18	1.300V	0x24	1.600V	0x30	1.900V
0x01	0.725V	0x0D	1.025V	0x19	1.325V	0x25	1.625V	0x31	1.925V
0x02	0.750V	0x0E	1.050V	0x1A	1.350V	0x26	1.650V	0x32	1.950V
0x03	0.775V	0x0F	1.075V	0x1B	1.375V	0x27	1.675V	0x33	1.975V
0x04	0.800V	0x10	1.100V	0x1C	1.400V	0x28	1.700V	0x34	2.000V
0x05	0.825V	0x11	1.125V	0x1D	1.425V	0x29	1.725V	0x35	2.025V
0x06	0.850V	0x12	1.150V	0x1E	1.450V	0x2A	1.750V	0x36	2.050V
0x07	0.875V	0x13	1.175V	0x1F	1.475V	0x2B	1.775V	0x37	2.075V
0x08	0.900V	0x14	1.200V	0x20	1.500V	0x2C	1.800V	0x38	2.100V
0x09	0.925V	0x15	1.225V	0x21	1.525V	0x2D	1.825V		
0x0A	0.950V	0x16	1.250V	0x22	1.550V	0x2E	1.850V		
0x0B	0.975V	0x17	1.275V	0x23	1.575V	0x2F	1.875V		

REG0x1F: ENABLE1 Register Address [reset = 0x30]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	SSD_EN	0	R/W	SSD Control 0 = SSD function enabled (default) 1 = SSD function disabled
D[6]	Reserved	0	R/W	Reserved
D[5]	VGL_FD	1	R/W	VGL FD Control 0 = VGL discharge function disabled 1 = VGL discharge function enabled (default)
D[4]	DVDD_FD	1	R/W	DVDD FD Control 0 = DVDD discharge function disabled 1 = DVDD discharge function enabled (default)
D[3:2]	VGL_EN_SELECT[1:0]	00	R/W	VGL_EN Select 00 = VGL_EN or VGL Enable Pin (default) 01 = AVDD Enable + 2ms 10 = AVDD Enable + 4ms 11 = AVDD Enable + 6ms
D[1]	VGL_EN	0	R/W	VGL Control 0 = VGL disabled (default) 1 = VGL enabled
D[0]	DVDD_EN	0	R/W	DVDD Control 0 = DVDD disabled (default) 1 = DVDD enabled

REGISTER MAPS (continued)

REG0x20: ENABLE2 Register Address [reset = 0x0C]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	HLPM_EN	0	R/W	HLPM Control 0 = HLPM disabled 1 = HLPM enabled
D[6:4]	LPD_EN[2:0]	000	R/W	LPD Control 000 = Low power drive disabled (default) 111 = Low power drive enabled
D[3]	AVDD_FD	1	R/W	AVDD FD Control 0 = AVDD discharge function disabled 1 = AVDD discharge function enabled (default)
D[2]	EL_FD	1	R/W	EL FD Control 0 = EL discharge function disabled 1 = EL discharge function enabled (default)
D[1]	AVDD_EN	0	R/W	AVDD Control 0 = AVDD disabled 1 = AVDD enabled
D[0]	EL_EN	0	R/W	EL Control 0 = EL disabled. 1 = EL enabled

REG0x21: ELVSS_SET Register Address [reset = 0x50]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	REG_VO2[7:0]	01010000	R/W	VO2 Output Control V_{ELVSS} = REG_VO2[7:0] × 50mV - 8.0V Range: -8.0V (00000000) ~ -1.0V (10001100) Default: -4.0V (01010000)

REGISTER MAPS (continued)

Table 5. REG_VO2[7:0] Description

Data (Hex)	VO2 (ELVSS)	Data (Hex)	VO2 (ELVSS)	Data (Hex)	VO2 (ELVSS)	Data (Hex)	VO2 (ELVSS)	Data (Hex)	VO2 (ELVSS)
0x00	-8.00V	0x1D	-6.55V	0x3A	-5.10V	0x57	-3.65V	0x74	-2.20V
0x01	-7.95V	0x1E	-6.50V	0x3B	-5.05V	0x58	-3.60V	0x75	-2.15V
0x02	-7.90V	0x1F	-6.45V	0x3C	-5.00V	0x59	-3.55V	0x76	-2.10V
0x03	-7.85V	0x20	-6.40V	0x3D	-4.95V	0x5A	-3.50V	0x77	-2.05V
0x04	-7.80V	0x21	-6.35V	0x3E	-4.90V	0x5B	-3.45V	0x78	-2.00V
0x05	-7.75V	0x22	-6.30V	0x3F	-4.85V	0x5C	-3.40V	0x79	-1.95V
0x06	-7.70V	0x23	-6.25V	0x40	-4.80V	0x5D	-3.35V	0x7A	-1.90V
0x07	-7.65V	0x24	-6.20V	0x41	-4.75V	0x5E	-3.30V	0x7B	-1.85V
0x08	-7.60V	0x25	-6.15V	0x42	-4.70V	0x5F	-3.25V	0x7C	-1.80V
0x09	-7.55V	0x26	-6.10V	0x43	-4.65V	0x60	-3.20V	0x7D	-1.75V
0x0A	-7.50V	0x27	-6.05V	0x44	-4.60V	0x61	-3.15V	0x7E	-1.70V
0x0B	-7.45V	0x28	-6.00V	0x45	-4.55V	0x62	-3.10V	0x7F	-1.65V
0x0C	-7.40V	0x29	-5.95V	0x46	-4.50V	0x63	-3.05V	0x80	-1.60V
0x0D	-7.35V	0x2A	-5.90V	0x47	-4.45V	0x64	-3.00V	0x81	-1.55V
0x0E	-7.30V	0x2B	-5.85V	0x48	-4.40V	0x65	-2.95V	0x82	-1.50V
0x0F	-7.25V	0x2C	-5.80V	0x49	-4.35V	0x66	-2.90V	0x83	-1.45V
0x10	-7.20V	0x2D	-5.75V	0x4A	-4.30V	0x67	-2.85V	0x84	-1.40V
0x11	-7.15V	0x2E	-5.70V	0x4B	-4.25V	0x68	-2.80V	0x85	-1.35V
0x12	-7.10V	0x2F	-5.65V	0x4C	-4.20V	0x69	-2.75V	0x86	-1.30V
0x13	-7.05V	0x30	-5.60V	0x4D	-4.15V	0x6A	-2.70V	0x87	-1.25V
0x14	-7.00V	0x31	-5.55V	0x4E	-4.10V	0x6B	-2.65V	0x88	-1.20V
0x15	-6.95V	0x32	-5.50V	0x4F	-4.05V	0x6C	-2.60V	0x89	-1.15V
0x16	-6.90V	0x33	-5.45V	0x50	-4.00V	0x6D	-2.55V	0x8A	-1.10V
0x17	-6.85V	0x34	-5.40V	0x51	-3.95V	0x6E	-2.50V	0x8B	-1.05V
0x18	-6.80V	0x35	-5.35V	0x52	-3.90V	0x6F	-2.45V	0x8C	-1.00V
0x19	-6.75V	0x36	-5.30V	0x53	-3.85V	0x70	-2.40V		
0x1A	-6.70V	0x37	-5.25V	0x54	-3.80V	0x71	-2.35V		
0x1B	-6.65V	0x38	-5.20V	0x55	-3.75V	0x72	-2.30V		
0x1C	-6.60V	0x39	-5.15V	0x56	-3.70V	0x73	-2.25V		

REG0x22: ELVDD_SET Register Address [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000	R/W	Reserved
D[2:0]	REG_VO1[2:0]	000	R/W	VO1 Output Control V_{ELVDD} = REG_VO1[2:0] × 100mV + 4.6V Offset: 4.6V Range: 4.6V (000) ~ 5.0V (100) Default: 4.6V (000)

REGISTER MAPS (continued)

Table 6. REG_VO1[2:0] Description

Data (Hex)	VO1 (ELVDD)
0x00	4.6V
0x01	4.7V
0x02	4.8V
0x03	4.9V
0x04	5.0V

REG0x23: AVDD_SET Register Address [reset = 0x08]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/W	Reserved
D[5:0]	REG_VO3[5:0]	001000	R/W	VO3 Output Control V_{AVDD} = REG_VO3[5:0] × (-50mV) + 8.0V Offset: 8.0V Range: 8.0V (000000) ~ 5.7V (101110) Default: 7.6V (001000)

Table 7. REG_VO3[5:0] Description

Data (Hex)	VO3 (AVDD)	Data (Hex)	VO3 (AVDD)	Data (Hex)	VO3 (AVDD)	Data (Hex)	VO3 (AVDD)	Data (Hex)	VO3 (AVDD)
0x00	8.00V	0x0A	7.50V	0x14	7.00V	0x1E	6.50V	0x28	6.00V
0x01	7.95V	0x0B	7.45V	0x15	6.95V	0x1F	6.45V	0x29	5.95V
0x02	7.90V	0x0C	7.40V	0x16	6.90V	0x20	6.40V	0x2A	5.90V
0x03	7.85V	0x0D	7.35V	0x17	6.85V	0x21	6.35V	0x2B	5.85V
0x04	7.80V	0x0E	7.30V	0x18	6.80V	0x22	6.30V	0x2C	5.80V
0x05	7.75V	0x0F	7.25V	0x19	6.75V	0x23	6.25V	0x2D	5.75V
0x06	7.70V	0x10	7.20V	0x1A	6.70V	0x24	6.20V	0x2E	5.70V
0x07	7.65V	0x11	7.15V	0x1B	6.65V	0x25	6.15V		
0x08	7.60V	0x12	7.10V	0x1C	6.60V	0x26	6.10V		
0x09	7.55V	0x13	7.05V	0x1D	6.55V	0x27	6.05V		

REG0x25: Device ID Register Address [reset = 0xC0]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	DEVICE_ID[3:0]	1100	R	Device ID 1100 = SGM3843
D[3:0]	DEVICE_REV[3:0]	0000	R	Device Revision 0000 = Rev 0.0

REG0x26: I^{2}C Slave Address Register Address [reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	SLAVE_ADDR[7:0]	00010000	R	The Slave 1^{2}C address is defined in Register 0x26. 00010000 = Write 00010001 = Read

APPLICATION INFORMATION

Layout Considerations

The PCB layout is quite important in the power supply design. An incorrect layout could cause many problems such as instability, load and line transient regulation problems, output voltage noise, and EMI issues. Good grounding becomes important, especially in the case of heavy load current.

The following PCB layout guide should be applied:

• In order to avoid any inductive or capacitive coupling of the switching power supply noise to the sensitive analog control circuits, there are 7 separated grounds (AGND, DGND, PGND1, PGND2, PGND3, PGND4 and PGND5) in the SGM3843. The signal ground (AGND/DGND) and noisy power ground (PGND1, PGND2, PGND3, PGND4, PGND5) should be well separated on the PCB, and connected only at one point.

• Traces of switching nodes (SW1, SW2A, SW2B, SW3, SW4 and SW5) should be short and wide.

• Place input capacitors on PVIN (PVIN1, PVIN2A, PVIN2B, PVIN4 and PVIN5) as close as possible to the device.

• Place output capacitors on VO1, VO2A, VO2B, VO3 and VO5 as close as possible to the device.

• Use short and wide traces to connect the input capacitors on PVIN and the output capacitors.

• Place input capacitors on VIO as close as possible to the device.

REVISION HISTORY

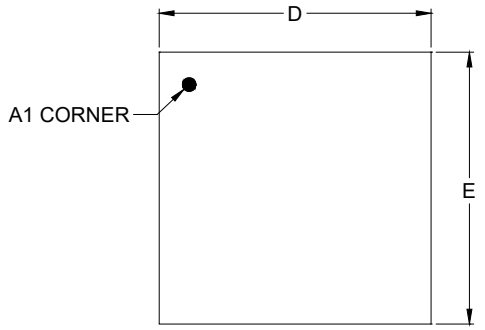
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

NOVEMBER 2023 – REV.A to REV.A.1	Page
Updated Typical Performance Characteristics section	12

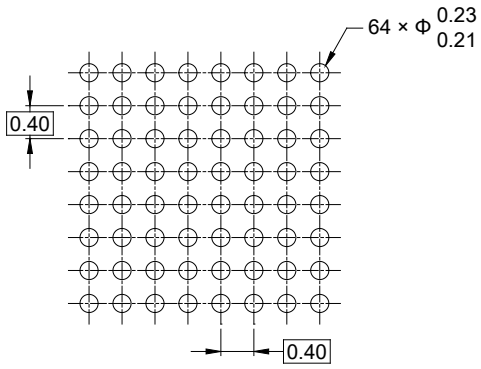
Changes from Original (OCTOBER 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

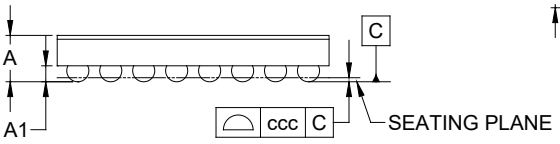
WLCSP-3.3×3.3-64B



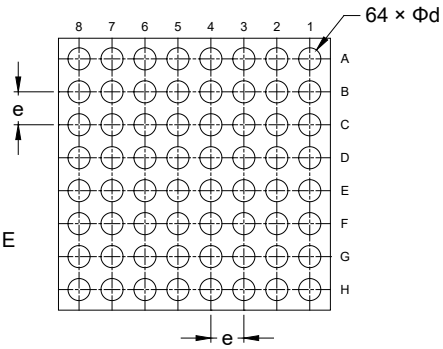
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



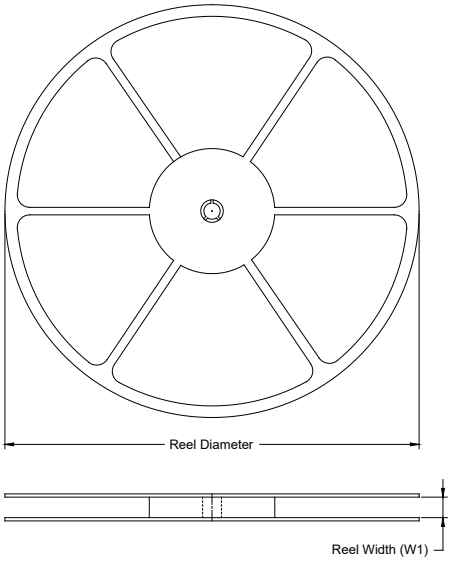
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.601
A1	0.174	-	0.214
D	3.270	-	3.330
E	3.270	-	3.330
d	0.238	-	0.298
e	0.400 BSC		
ccc	0.050		

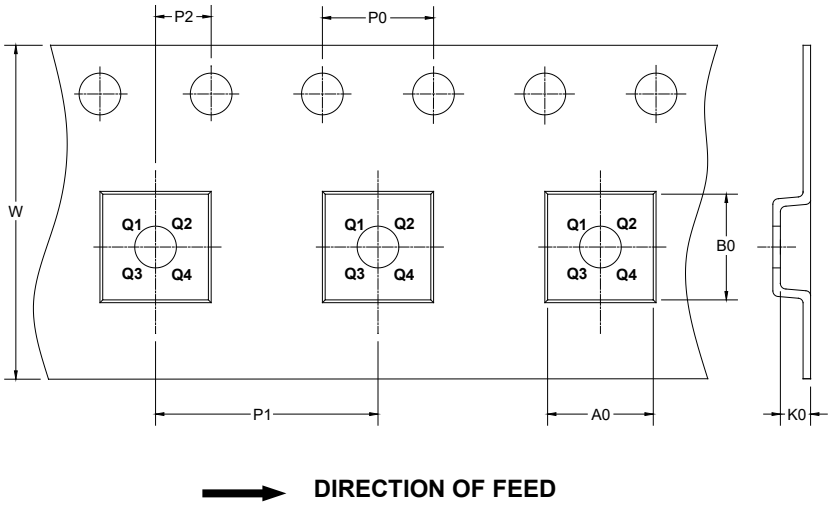
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

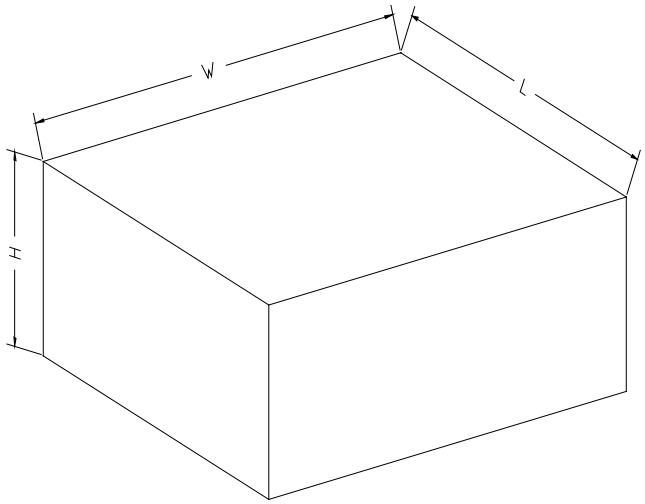
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-3.3×3.3-64B	13"	12.4	3.52	3.52	0.81	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002