SGM40642
5V eFuse with Precision Adjustable Current Limit and Over-Voltage Clamp

GENERAL DESCRIPTION

The SGM40642 is a smart low voltage load switch with a full suite of protective features that can protect the source, device, and the load against a variety of fault conditions. This eFuse device is suitable for 2.5V to 5V loads and provides accurate and adjustable current limiting (700mA to 2.9A) and over-voltage clamping (5.4V TYP). It can deliver 2.5A continuous current to the load and its input tolerates up to 20V over-voltage. In over-voltage conditions, the internal switch is turned off to keep the load disconnected with the SGM40642.

If the source voltage is higher than 5.4V but lower than 7.6V, the output will be clamped to 5.4V to protect the load. If the V_{IN} voltage exceeds 7.6V, the load will be disconnected to prevent damage.

The SGM40642 has an internal 54mΩ (TYP) power switch with current limit capability. This limit is programmable with a single external resistor (R_{ILIM}). A persistent overload condition usually results in thermal shutdown and may cause cyclic ON and OFF periods to protect the device.

The SGM40642 is available in a Green TDFN-2×2-6AL package and can operate over the -40℃ to +125℃ ambient temperature range.

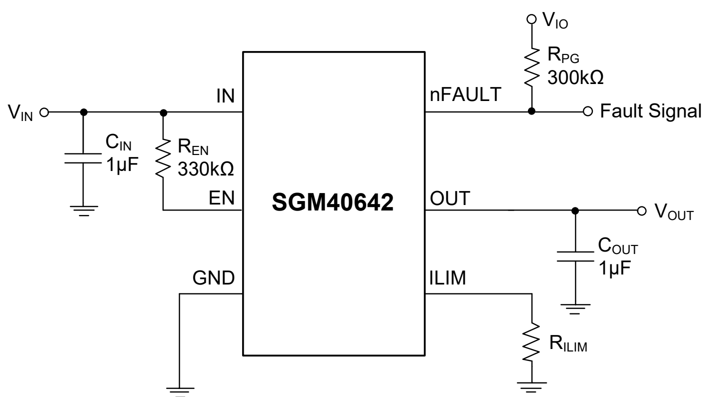
FEATURES

- **2.5V to 6.5V Operation**
- **54mΩ (TYP) Internal Switch (High-side MOSFET)**
- **Up to 2.5A Continuous Load Current**
- **Up to 20V Input Over-Voltage Tolerance**
- **Output Shutoff at 7.6V (TYP) Input Over-Voltage**
- **100ns Over-Voltage Lockout (OVLO) Response**
- **3.5μs Short-Circuit Response**
- **Reverse Current Blocking while Disabled**
- **Built-In Soft-Start**
- **Pin-to-Pin Compatible with SGM2553**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TDFN-2×2-6AL Package**

APPLICATIONS

USB Power Switches
USB Slave Devices
Smart Phones/Cell Phones
3G, 4G Wireless Data-Cards
Solid State Drives (SSD)
3V or 5V Adapter Powered Devices

TYPICAL APPLICATION



NOTE: To select the R_{ILIM} value, use either the Electrical Characteristics table (I_{OS} row).

Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM40642	TDFN-2×2-6AL	-40℃ to +125℃	SGM40642XTDI6G/TR	R87 XXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXX = Date Code and Trace Code.

YYY — Serial Number
X XXX
Trace Code
Date Code - Year

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)
- IN .... -0.3V to 20V
- OUT, EN .... -0.3V to 7V
- ILIM, nFAULT..................... -0.3V to 6V
- IN to OUT..................... -7V to 20V

Continuous Output Current, I_O .... Thermally Limited

Package Thermal Resistance
- TDFN-2×2-6AL, θ_{JA}..................... 97℃/W
- TDFN-2×2-6AL, θ_{JC}..................... 74℃/W

Junction Temperature, T_J.....................+150℃

Storage Temperature Range ....-65℃ to +150℃

Lead Temperature (Soldering, 10s).....................+260℃

ESD Susceptibility

HBM.....................2000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} ....2.5V to 6.5V

Enable Terminal Voltage Range, V_{EN} ....0V to 6.5V

Continuous nFAULT Sink Current Range, I_{nFAULT} ....0mA to 10mA

Continuous Output Current of OUT, I_{OUT} ....2.5A (MAX)

Current Limit Set Resistor Range, R_{ILIM} .... 33kΩ to 150kΩ

Operating Temperature Range ....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

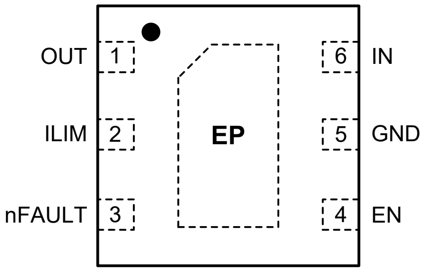
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-2×2-6AL

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	OUT	O	Power Switch Output Pin. Connect this pin to the load.
2	ILIM	O	Current Limit Programming Pin. Connect a resistor (R_{ILIM}) between this pin and GND to set the current limit threshold. Recommended range for this resistor is: 33kΩ ≤ R_{ILIM} ≤ 150kΩ.
3	nFAULT	O	Active-Low Open-Drain Fault Output Flag Pin. nFAULT is asserted during over-current, over-voltage or over-temperature faults. Connect this pin with a pull-up resistor to a logic high voltage.
4	EN	I	Enable Logic Input. Pull the EN high to enable the power switch and drive it low to turn it off. Do not leave this pin floating. EN voltage must be limited to remain in its recommended maximum rating if it is tied to V_{IN} (< 6.5V).
5	GND	—	Ground Connection. Connect this pin to the exposed pad (EP) externally.
6	IN	I	Device Supply Voltage and Power Switch Input Pin. Decouple the IN pin to GND with a 0.1μF or larger ceramic capacitor and place it as close as possible to the device.
Exposed Pad	EP	—	Exposed Pad. EP is internally connected to the GND. Use EP as a heat sinking pad to the PCB ground plane and the GND pin.

NOTE: 1. O = Output, I = Input.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, 2.5V ≤ V_{IN} ≤ 6.5V, V_{EN} = V_{IN}, R_{ILIM} = 33kΩ. Typical values are at T_A = +25℃, unless otherwise noted. Current flow into a terminal is considered positive.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current	I_Q	V_{EN} = 5V, V_{IN} = 5V, no load on OUT	R_{ILIM} = 33kΩ		190	290	μA
			R_{ILIM} = 150kΩ		190	290	
Shutdown Supply Current	I_{SD}	V_{EN} = 0V, V_{IN} = 5V			1	5	μA
		V_{EN} = 0V, V_{IN} = 20V			50	75	
		V_{EN} = 5V, V_{IN} = 20V			120	195	
Reverse Leakage Current	I_{REV}	V_{OUT} = 6.5V, V_{IN} = V_{EN} = 0V, measure I_{OUT}, T_A = +25℃			3	5	μA
EN Terminal Input Voltage Threshold	V_{IH}	V_{EN} rising		1.4			V
	V_{IL}	V_{EN} falling				0.4	
EN Terminal Leakage Current	I_{EN}	V_{EN} = 0V or 5.5V		-2		2	μA
Switch Resistance (1)	R_{DSON}	2.5V ≤ V_{IN} ≤ 5V, I_{OUT} = 100mA	T_A = +25℃		54	75	mΩ
			T_A = -40℃ to +85℃		54	95	
			T_A = -40℃ to +125℃		54	105	
OUT Discharge Resistance	R_{DIS}	V_{OUT} = 5V, V_{EN} = 0V			557	780	Ω
Current Limit Threshold	I_{OS}	R_{ILIM} = 33kΩ	See Figure 5	2382	2959	3437	mA
		R_{ILIM} = 40.2kΩ		1947	2456	2867	
		R_{ILIM} = 56kΩ		1381	1784	2105	
		R_{ILIM} = 80.6kΩ		960	1259	1524	
		R_{ILIM} = 150kΩ		517	709	891	
Over-Voltage Lockout (IN Pin)							
OVLO Voltage Threshold	V_{OVLO}	IN rising		6.7	7.6	8.5	V
Hysteresis (2)					220		mV
Voltage Clamp (OUT Pin)							
OUT Clamp Voltage Threshold	V_{OVC}	C_L = 1μF, R_L = 100Ω, V_{IN} = 6.5V		5.00	5.4	5.80	V
Under-Voltage Lockout (IN Pin)							
UVLO Voltage Threshold	V_{UVLO}	V_{IN} rising			2.32	2.47	V
UVLO Hysteresis (2)					40		mV
Thermal Shutdown							
Thermal Shutdown Threshold, OTSD2		T_J increasing			155		℃
Thermal Shutdown Threshold, OTSD1 (Only in Current Limit Mode)					115		℃
Hysteresis (2)					20		℃
nFAULT Flag							
nFAULT Output Resistance	R_{nFAULT}	nFAULT is low and I_{SINK} = 1mA	V_{IN} = 2.5V		60	80	Ω
			V_{IN} = 5V		50	70	
nFAULT Leakage Current	I_{nFAULT}	nFAULT is high				4	μA

NOTES:
1. The junction temperature is kept near the ambient temperature using pulse-test techniques for measuring these parameters, so the thermal effects should be considered separately depending on the application.
2. Provided for reference only. Not guaranteed.

TIMING REQUIREMENTS

(T_A = -40℃ to +125℃, 2.5V ≤ V_{IN} ≤ 6.5V, V_{EN} = V_{IN}, R_{ILIM} = 33kΩ. Typical values are at T_A = +25℃, unless otherwise noted. Current flow into a terminal is considered positive.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Switch							
V_{OUT} Rise Time	t_r	V_{IN} = 5V, C_L = 1μF, R_L = 100Ω, see Figure 3			2.66	8	ms
V_{OUT} Fall Time	t_f				0.2	0.5	ms
Enable Input EN							
V_{OUT} Turn-On Time	t_{ON}	V_{IN} = 5V, C_L = 1μF, R_L = 100Ω, see Figure 4			7.9	11	ms
V_{OUT} Turn-Off Time	t_{OFF}				0.23	0.6	ms
Current Limit							
V_{OUT} Short-Circuit Response Time (3)	t_{IOS}	V_{IN} = 5V, see Figure 5			3.5		μs
Over-Voltage Lockout (IN Pin)							
V_{IN} OVLO Turn-Off Delay (3)	$t_{OVLO\_off\_delay}$	V_{IN} ramp up from 5V to 10V at a rate of 1V/μs with 100Ω load on V_{OUT}			0.6		μs
nFAULT Flag							
nFAULT Deglitch Time		nFAULT is asserted due to an over-current event or de-asserted after clearing this event	V_{IN} = 2.5V		7		ms
			V_{IN} = 5V		7		

NOTE: 3. These parameters are provided for reference only.

PARAMETER MEASUREMENT INFORMATION

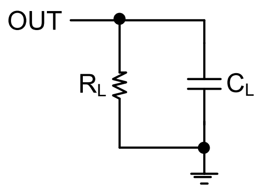


Figure 2. Test Load for V_{OUT} Rise and Fall

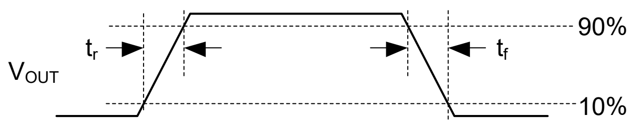


Figure 3. V_{OUT} Power-On and Power-Off Timing

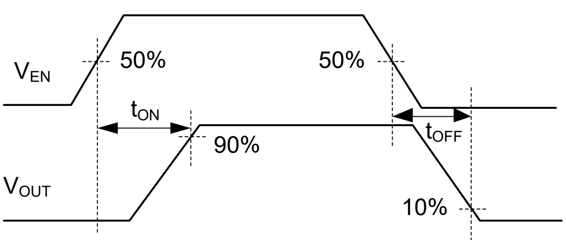


Figure 4. Enable Timing for V_{OUT}

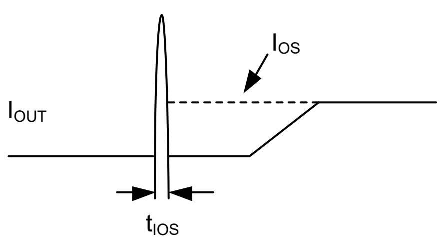
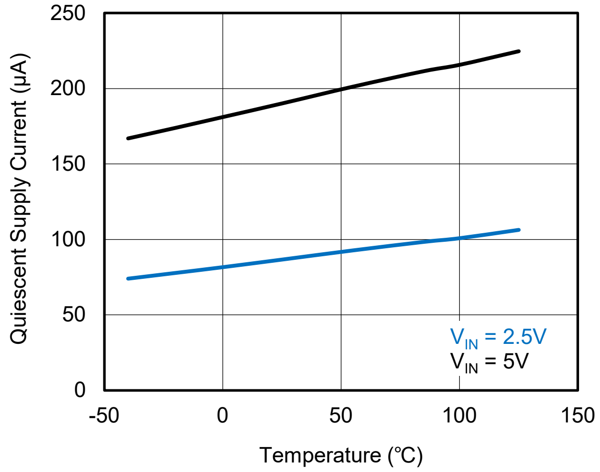


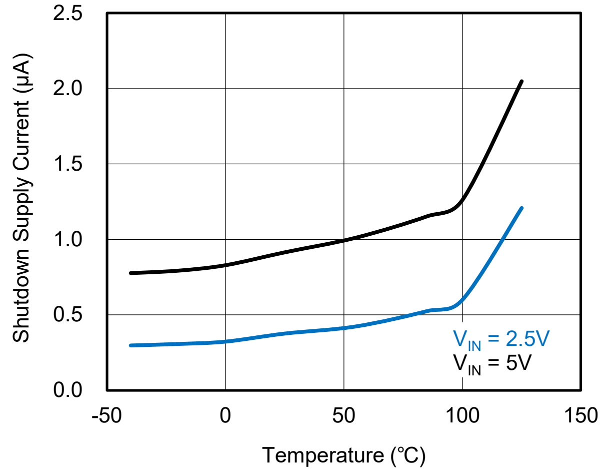
Figure 5. Output Short Timing and Current Limit (I_{OS}) Parameters

TYPICAL PERFORMANCE CHARACTERISTICS

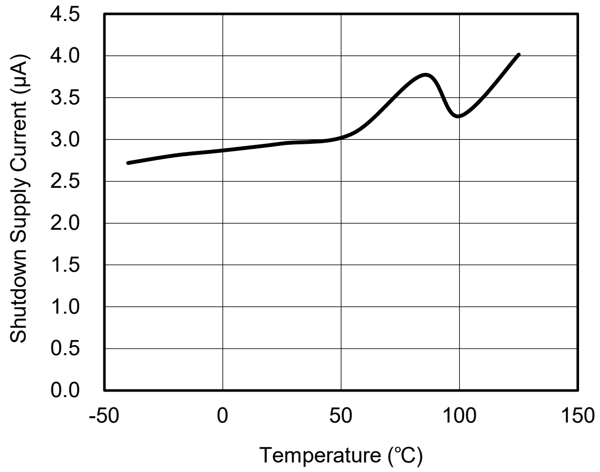
Quiescent Supply Current vs. Temperature



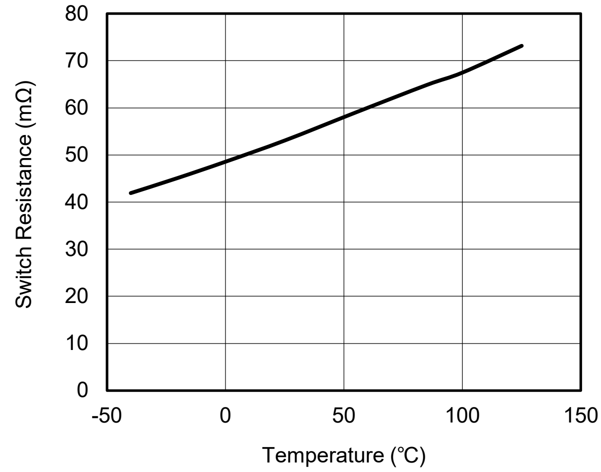
Shutdown Supply Current vs. Temperature



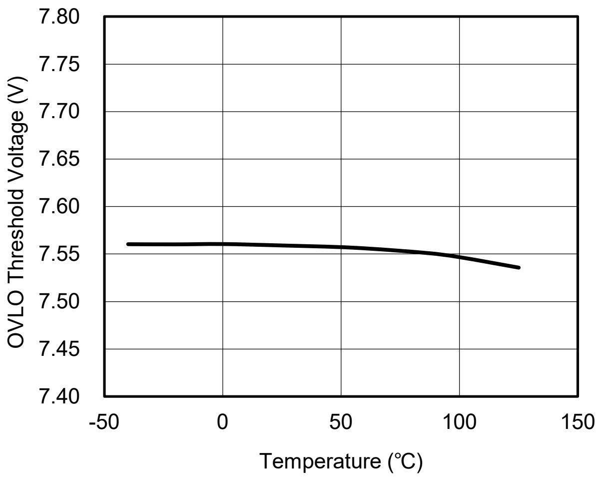
Reverse Leakage Current vs. Temperature



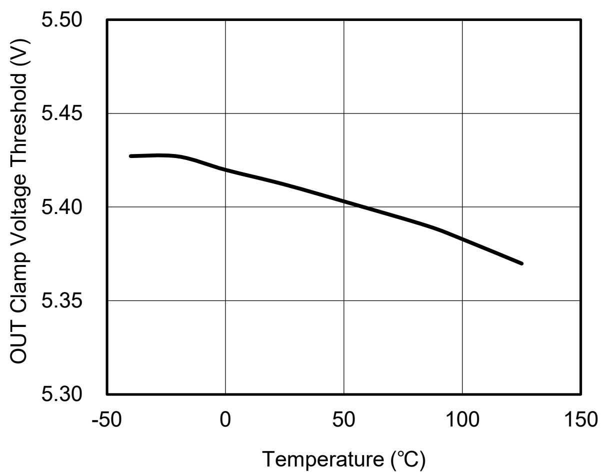
Switch Resistance vs. Temperature



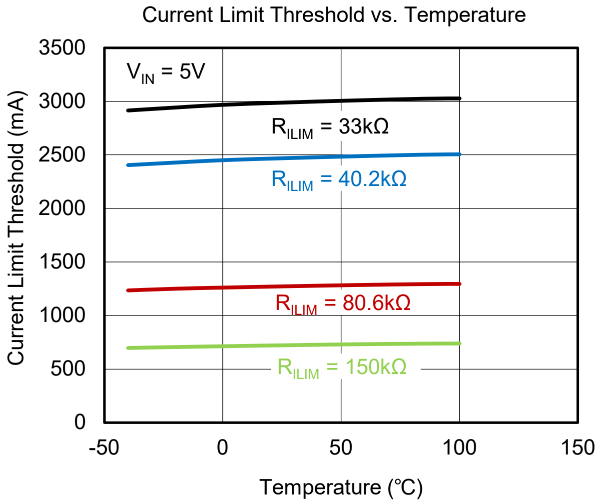
OVLO Voltage Threshold vs. Temperature

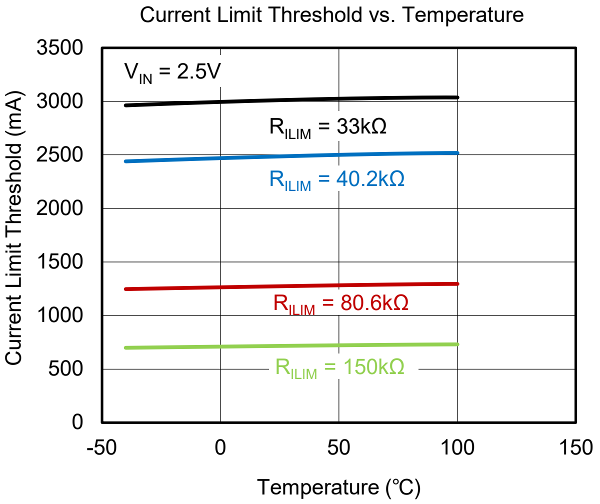


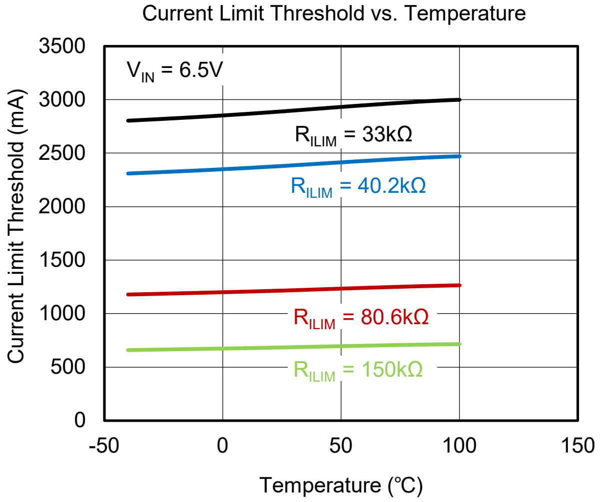
OUT Clamp Voltage Threshold vs. Temperature

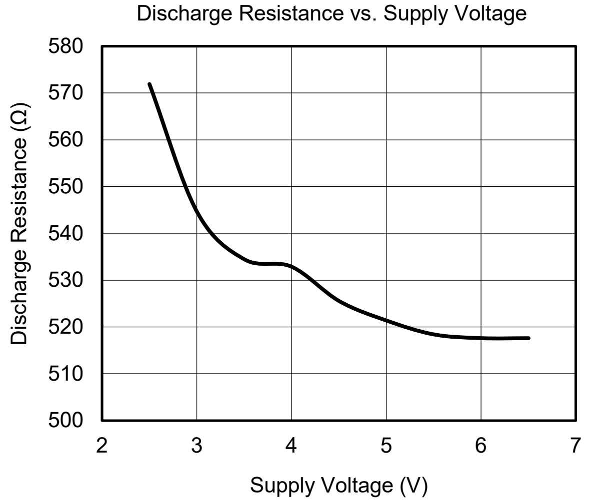


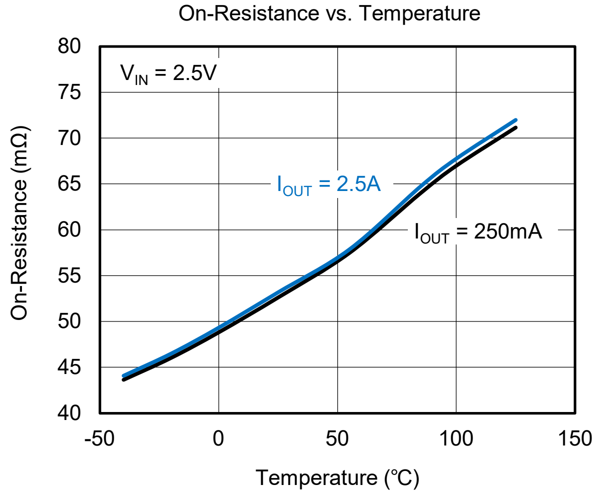
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

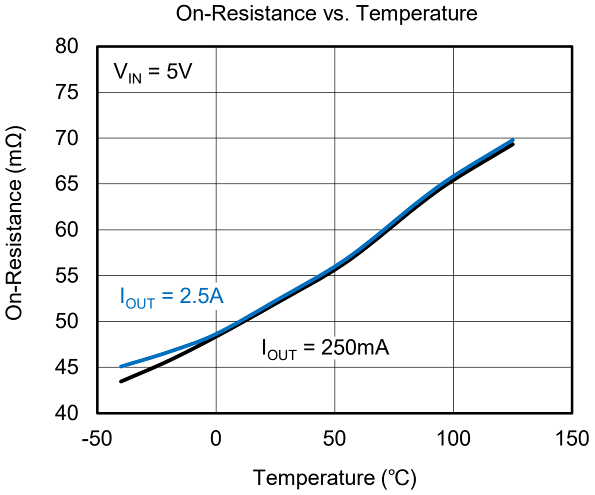






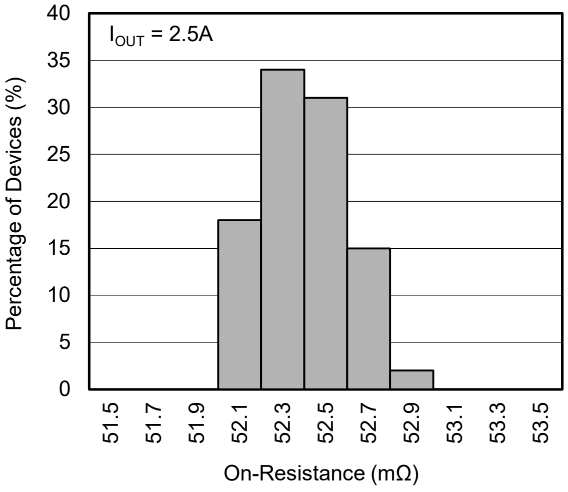




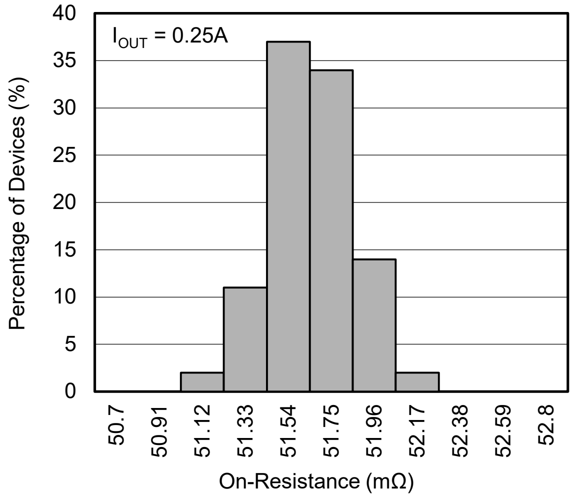


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

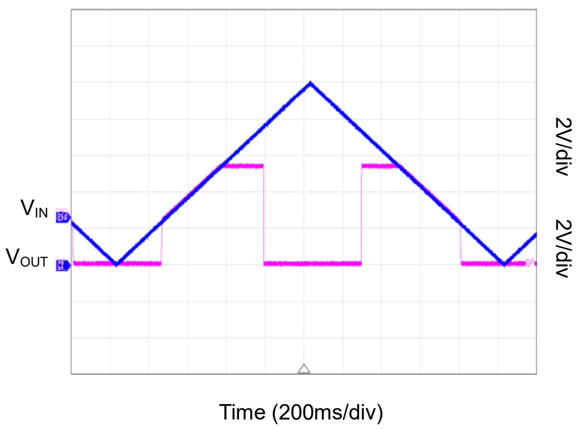
On-Resistance Distribution



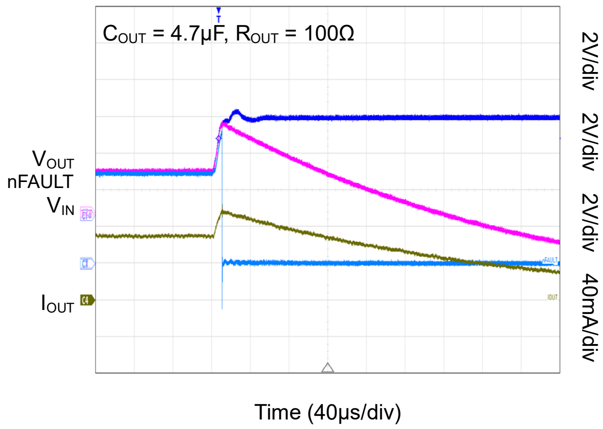
On-Resistance Distribution



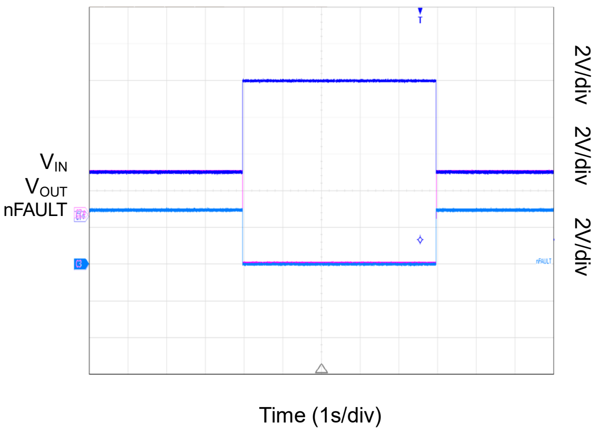
Output Voltage vs. Input Voltage (0V to 10V)



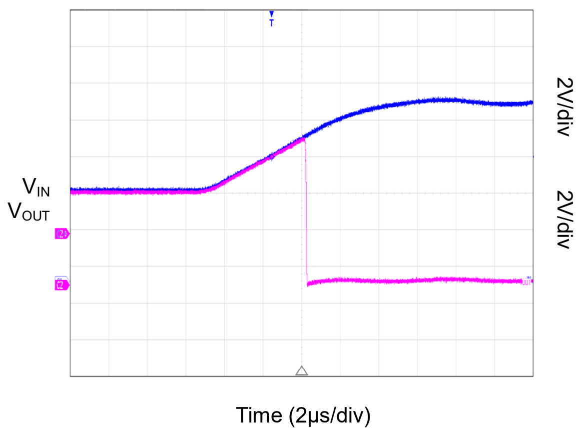
V_{IN} Step 5V to 8V



Pulse Over-Voltage with 100Ω

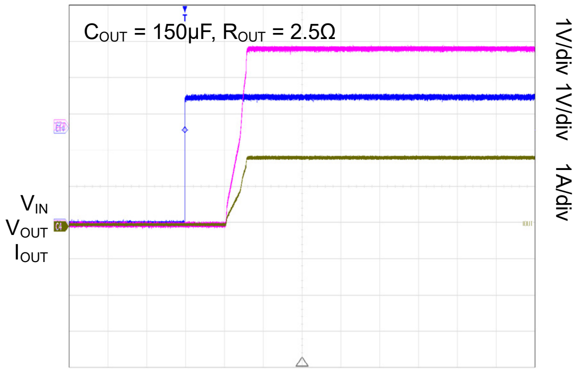


5V to 10V OVLO Response Time



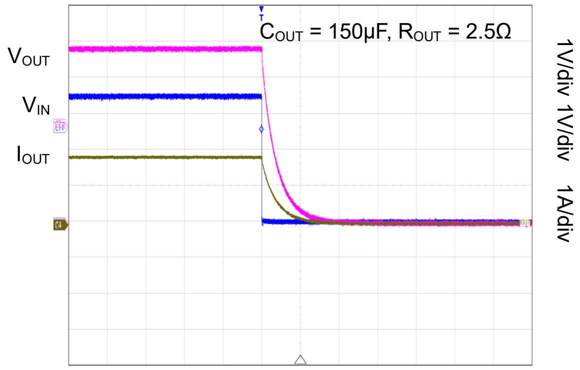
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Turn-On Delay and Rise Time



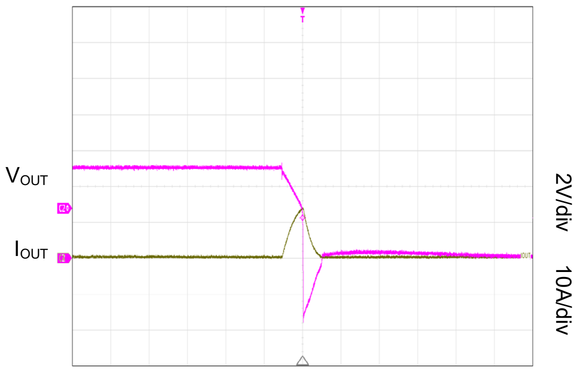
Time (5ms/div)

Turn-Off Delay and Fall Time



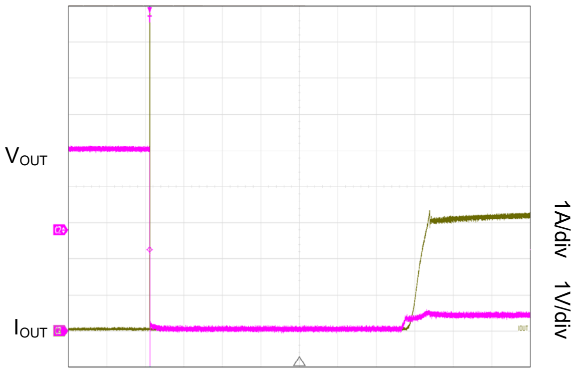
Time (1ms/div)

50mΩ Hot-Short Response Time



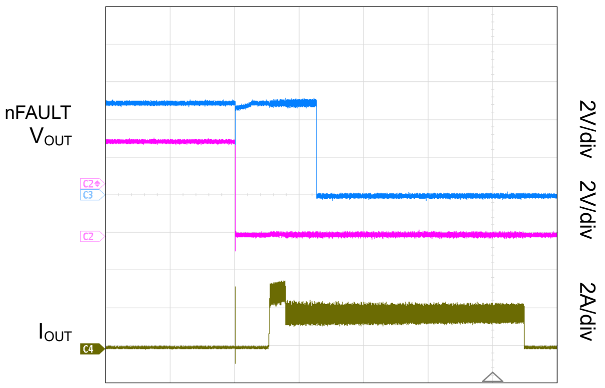
Time (2μs/div)

SGM40642 Hot-Short with 50mΩ



Time (800μs/div)

No Load to Output Short Transient Response



Time (10ms/div)

FUNCTIONAL BLOCK DIAGRAM

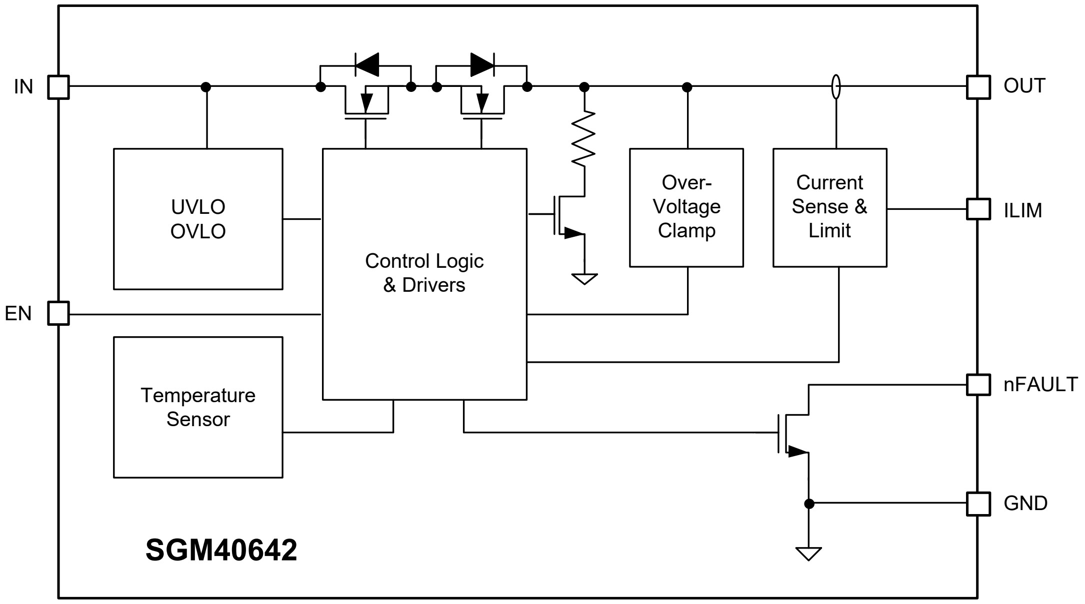


Figure 6. SGM40642 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM40642 is a smart low voltage load switch with reliable over-current and over-voltage protections. It can be used as an eFuse for a wide range of applications including slave USB devices.

N-channel MOSFETs are used to build a current limit power switch in the device that can carry up to 2.5A load current continuously. The current limit is adjustable between 700mA and 2.9A with an external resistor. If the load tends to exceed the current limit, the switch enters constant-current mode. Having a precision over-current limit allows for lower input supply over design margins.

The input tolerates over-voltage levels as high as 20V. The output (V_{OUT}) is clamped to a precisely regulated 5.4V (TYP) voltage if the over-voltage is small (V_{IN} < 7.6V). The V_{OUT} will shut down if V_{IN} exceeds 7.6V.

Other features are summarized below:

• An active high enable input that can be used to put the load in sleep mode (especially useful for portable applications).
• Over-temperature safety protection that shuts down the device if a persistent over-current or small over-voltage (V_{OUT} clamp) event lasts for a relatively long time and causes high die temperature.
• An active low deglitched fault reporting output (nFAULT) is also provided to filter the nFAULT signal from rapid state changes to avoid false fault alerts.
• Output discharge capability (pull-down). This feature helps for making sure that the load is turned off and not in an undefined operational state.
• Reverse blocking feature (when the device is disabled) prevents any reverse power flow to avoid unwanted behavior when an active load is controlled by the switch.

Enable Input

The enable is a TTL and CMOS compatible logic input that controls the device internal circuits and the power switch. A logic high enables the driver, control circuits, and power switch and a logic low will turn off the switch and reduces the supply current to very low levels.

This logic input has an internal protective Zener diode and can be pulled up to V_{IN} with a sufficiently large pull-up resistor (330kΩ) to make sure the EN voltage does not exceed the absolute maximum rating when the IN is in over-voltage condition.

Internal Temperature Sensing

The SGM40642 uses two independent temperature monitoring units to protect the switch and the device against overheating. The loss is mainly due to the current passing through the switch and the voltage drop across it. This switch voltage drop is high when the device is clamping the input voltage to keep the output at 5.4V. Also, when the switch operates in the constant-current mode during an over-current event, the voltage drop across the power switch is increased. The package power dissipation is proportional to the voltage drop across the switch. This loss will increase the junction temperature during an over-current event. The first temperature sensor (OTSD1) detects if the die temperature exceeds 115℃ (TYP) and the device is in current limit mode. If this condition is detected, the switch will be turned off. There is an almost 20℃ hysteresis in the OTSD1 detection, and the switch turns on again after the device has cooled for almost 20℃.

The SGM40642 has a second die temperature sensor (OTSD2) as well. If the die temperature exceeds 155℃ (TYP), the switch is turned off by OTSD2, regardless of the switch current level. The OSTD2 protection also has a hysteresis of 20℃ and the switch recovers its on-state automatically if the junction cools down by approximately 20℃ below the turn-off threshold.

Both types of thermal protections can cause cyclic ON and OFF periods for the switch until the fault condition is cleared.

Overload Protection

In case of an overload, the output current is limited to the I_{OS} level as shown in Figure 5. The output voltage is reduced to maintain the constant output current at the limited level.

If a persistent overload condition occurs, the current will be limited to half of the I_{OS} level or I_{OS} according to whether the difference between IN and OUT exceeds 1.7V (TYP @ V_{IN} = 5V) or not. This event can lead to an OTSD1 switch shutdown at 115℃ that initiates the thermal protection cycling to protect the device against the overload.

DETAILED DESCRIPTION (continued)

An overload or output short event may occur in two possible situations.

In the first case, a short or partial short occurs when the device is powering-up or being enabled. In this case, the current will ramp up to the I_{OS} level and remain at the I_{OS} level for 2.4ms (TYP @ V_{IN} = 5V). Then the current will be decreased to half of the I_{OS} level after 2.4ms mentioned above if the voltage drop between IN and OUT exceeds 1.7V (TYP @ V_{IN} = 5V), otherwise continue remaining at the I_{OS} level. The internal power device will be shut down if the junction temperature exceeds the thermal shutdown threshold at any time in the process mentioned above.

In the second case, the short, partial short, or a transient overload occurs when the device is already powered. If this happens, the device will react to the over-current, but the current peak can momentarily go above I_{OS} for a short t_{IOS} time (Figure 5). The high current peak overdrives the current sense circuit that leads to a brief switch disable period. After a short time, the current sense circuit recovers, and the output current will behave like the first case.

nFAULT Output Flag

The nFAULT is an active-low open-drain output that should be pulled up to a low voltage logic rail. It will be asserted when a fault occurs (over-current, over-temperature or over-voltage) and remains low until the fault is cleared and the device enters normal operation. The nFAULT is not asserted when the device operates in output clamp mode.

False over-current reporting is avoided by considering a 7ms (TYP) @ V_{IN} = 2.5V internal deglitch delay only for over-current to assure that nFAULT is not mistakenly asserted due to a non-fault situation such as powering a large capacitive load. The deglitch delay applies for both entering in and existing out of an over-current fault event. Particularly, the nFAULT is not deglitched due to an over-temperature fault caused by over-current, but it is deglitched after the device has cooled and the switch is turned on. By such asymmetric deglitch strategy, nFAULT oscillation during an over-temperature event is avoided. The nFAULT is not deglitched when the switch is disabled due to an OVLO or recovery from OVLO.

Output Discharging

When the device is disabled or is in UVLO or OVLO condition, the output is discharged with an internal 557Ω (TYP) resistive path to remove any remaining charge or leakage current on the output. The path resistance increases at lower V_{IN} values.

Functional Modes

The SGM40642 can tolerate up to 20V input voltage. The 0V to 20V input range can be split into four segments in such a way that in each segment the device operates in a different mode as shown in Figure 7.

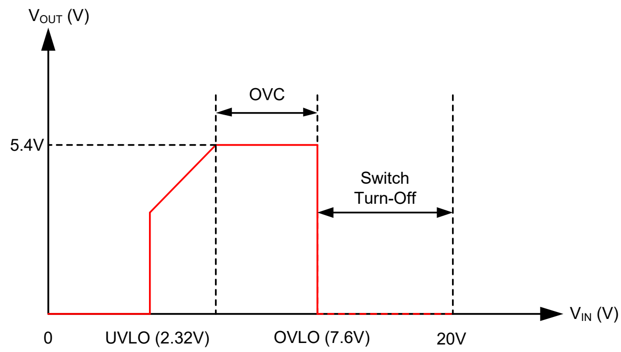


Figure 7. Four Functional Modes of the SGM40642 over the Input Voltage Range (V_{OUT} vs. V_{IN})

Mode 1: Input Under-Voltage Lockout (UVLO)

If the input voltage is below the 2.32V (TYP) under-voltage lockout level (UVLO), the power switch will be disabled. The switch cannot turn on until the input voltage exceeds the UVLO turn-on threshold. A 40mV hysteresis is considered for the UVLO comparator to avoid unwanted cycling for minor input voltage droops such as the droops caused by load connection during switch turn-on.

Mode 2: Over-Current Protection (OCP)

If a persistent overload condition occurs, the current will be limited to the over-current threshold that can be programmed by an external resistor (R_{ILIM}).

Mode 3: Over-Voltage Clamp (OVC)

When V_{IN} is in the 2.32V to 5.4V range, the switch acts as a conventional power switch with a small series resistance with over-current protection. In the 5.4V to 7.6V input range, the output voltage is clamped to 5.4V. The over-current protection is also active in the OVC mode.

The recommended capacitor on OUT pin is 1μF in the OVC mode.

Mode 4: Over-Voltage Lockout (OVLO)

If V_{IN} exceeds 7.6V, the switch will be turned off to isolate the load from the input (OVLO mode).

APPLICATION INFORMATION

The SGM40642 is a smart 5V load switch (also known as eFuse) with over-voltage clamping and accurate current limit capabilities. As shown in Figure 9, when a peripheral USB device (slave) is hot plugged or unplugged, the voltage transient caused by the rapid current change in the parasitic inductance of the cable can damage the slave device. Using the SGM40642 at the USB port of the slave device can protect it against such transients. Such transients may also occur when the cable is already connected and the SGM40642 is turned off in response to a fault. Using the SGM40642, there is no need for bulk bypass capacitors, TVS diodes or other external over-voltage protection components in the input port of the slave device. As a controlled switch, the SGM40642 can also be used in a USB master device (host). It is pin-to-pin compatible with the SGM2553.

Current Limit Programming

An external resistor (R_{ILIM}) placed between the ILIM pin and GND sets the switch over-current limit threshold (I_{OS}). The ILIM pin voltage is regulated by an internal control loop. The current limit threshold is proportional to the current pulled from the ILIM pin by the resistor. An R_{ILIM} resistor in the 33kΩ to 150kΩ range is recommended for stable internal loop operation. Use short trace routes for the R_{ILIM} on the PCB to minimize the impact of parasitics and noise on the accuracy of the current limit setting.

In many applications, the tolerance of the current limit threshold is important, so the minimum current limit level and the maximum current limit level are specified as design parameters. The R_{ILIM} value should be selected carefully such that in the worst tolerance cases, the current limit is guaranteed to fall between those two limits. Setting the current limit above a minimum is important to assure a smooth startup with no hiccup at full load or for highly capacitive loads. Similarly, setting the current limit below a maximum is important to avoid input voltage droops due to source overloading or source current limit activation.

The R_{ILIM} values for some specific current limit thresholds are provided in the Electrical Characteristics table. The current limit threshold (I_{OS}) in Equation 1 approximates the resulting over-current threshold for a given external resistor value R_{ILIM}. Current limit resistor can also be designed using the I_{OS} vs. R_{ILIM} graph in Figure 8.

$$I_{OS(MIN)}(mA) = \frac{93550V}{R_{ILIM}}$$
$$I_{OS(NOM)}(mA) = \frac{98996V}{R_{ILIM}} \quad (1)$$
$$I_{OS(MAX)}(mA) = \frac{105925V}{R_{ILIM}}$$

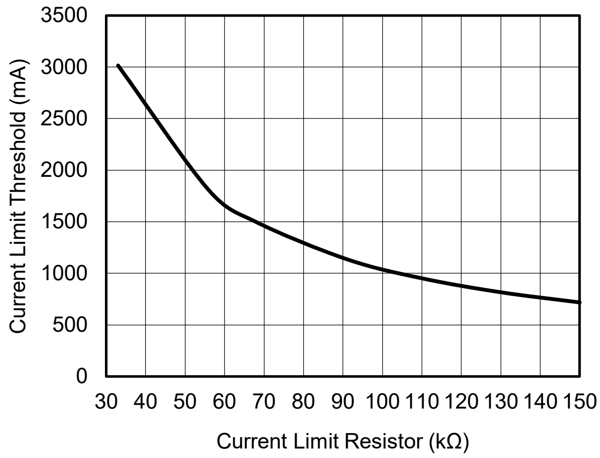


Figure 8. SGM40642 Current Limit Threshold (I_{OS}) vs. Current Limit Programming Resistor (R_{ILIM}) for Higher Current Range (33kΩ < R_{ILIM} < 150kΩ)

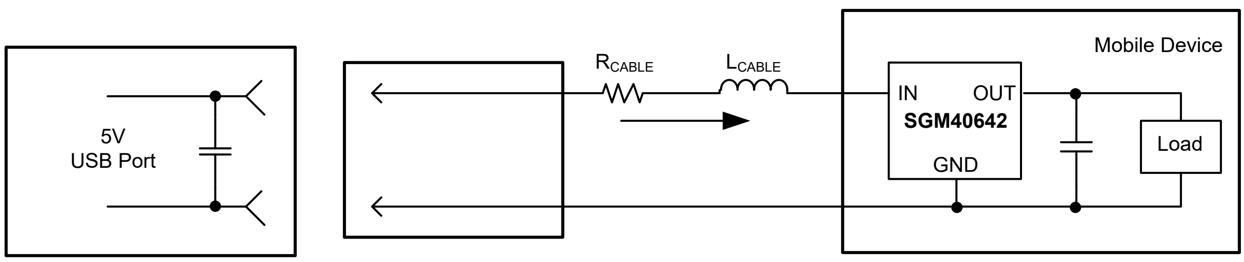


Figure 9. SGM40642 is Used to Protect a 5V USB Salve Device (Mobile) against Hot Plug or Turn-Off Transients Caused by the Cable Parasitic Impedance

APPLICATION INFORMATION (continued)

Loss Analysis and Die Temperature

Estimating the power loss and junction temperature rise is a good design practice to make sure the system using the device will have a reliable performance. In this section, a simplified thermal analysis method is provided for the SGM40642. Note that other operating or environmental factors of the system such as ventilation, PCB copper thickness and connected area and the nearby components losses have a strong impact on the thermal performance and must be considered in every specific application. The loss analysis is done in both component level and system level to assure a good design.

The small on-resistance (R_{DSON}) of the internal switch allows high current and high power-density in a small package. For thermal analysis, R_{DSON} variations against V_{IN} and T_A (ambient temperature) should be considered. For initial estimate, consider the highest expected operating ambient temperature (T_e) and evaluate the R_{DSON} from the typical characteristics graph. For the SGM40642, if $V_{IN} < V_{OVC}$, the maximum loss can be estimated by:

$$P_D = R_{DSON} \times I_{OUT}^{\ 2} \quad (2)$$

If $V_{OVC} < V_{IN} < V_{OVLO}$, the output clamps to the V_{OVC} and the loss is given by:

$$P_D = (V_{IN} - V_{OVC}) \times I_{OUT} \quad (3)$$

where

• P_D = Maximum device power loss (W)
• R_{DSON} = Switch on-resistance (Ω)
• V_{OVC} = Over-voltage clamp voltage (V)
• I_{OUT} = Maximum current limit threshold (A)

The junction temperature can be calculated from:

$$T_J = P_D \times \theta_{JA} + T_A \quad (4)$$

where

• T_A = Ambient temperature (℃)
• θ_{JA} = Device thermal resistance (℃/W)
• T_J = Junction temperature (℃)

Based on the highest current limit setting and the device thermal resistance on the PCB to calculate T_J and compare it with the initial temperature considered for evaluating R_{DSON} (T_e). If the difference is negligible, the estimate is no problem, otherwise repeat the calculation by considering the new R_{ON} value based on the calculated T_J. Usually after two or three iterations the desired result is achieved. If there is no convergence, make a more reasonable T_e assumption. Note that the thermal resistance θ_{JA} is highly dependent on the PCB and its value is critical in determination of the junction temperature.

Source Supply Voltage Range

The SGM40642 is designed to operate with 2.7V to 5V rails. The V_{OUT} clamping at 5.4V is a protection feature and is not intended to be used as a regulator.

Layout Considerations

• Use a 0.1μF or larger ceramic capacitor to bypass V_{IN} to GND and place it as close as possible to the device.
• Use a low ESR ceramic capacitor on output selected based on design guidelines.
• Use short traces to connect the R_{ILIM} resistor and the device.
• Connect the device EP pad directly to the PCB ground or through a wide and short copper trace.

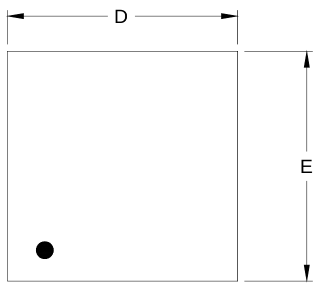
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

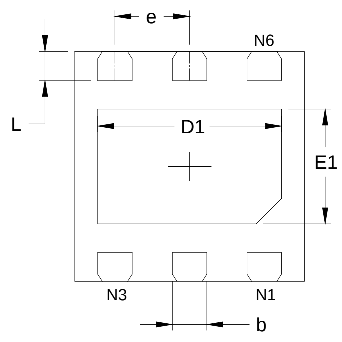
Changes from Original (SEPTEMBER 2021) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

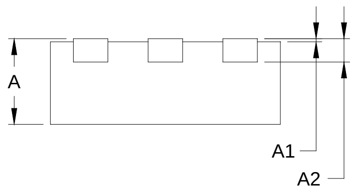
TDFN-2×2-6AL



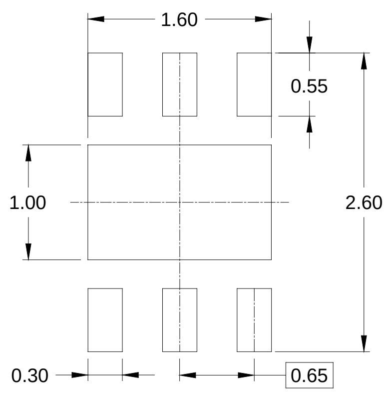
TOP VIEW



BOTTOM VIEW



SIDE VIEW



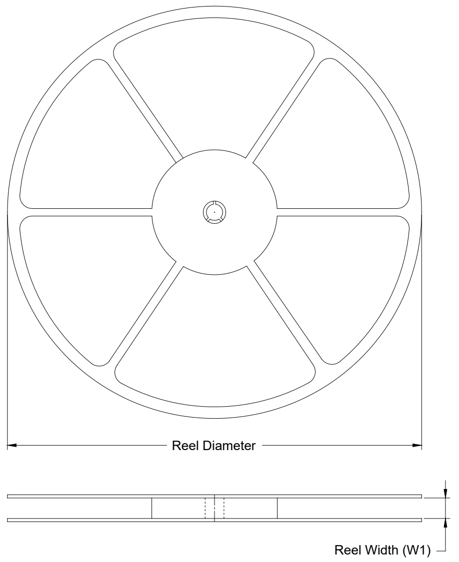
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.500	1.700	0.059	0.067
E	1.900	2.100	0.075	0.083
E1	0.900	1.100	0.035	0.043
b	0.250	0.350	0.010	0.014
e	0.650 BSC		0.026 BSC	
L	0.174	0.326	0.007	0.013

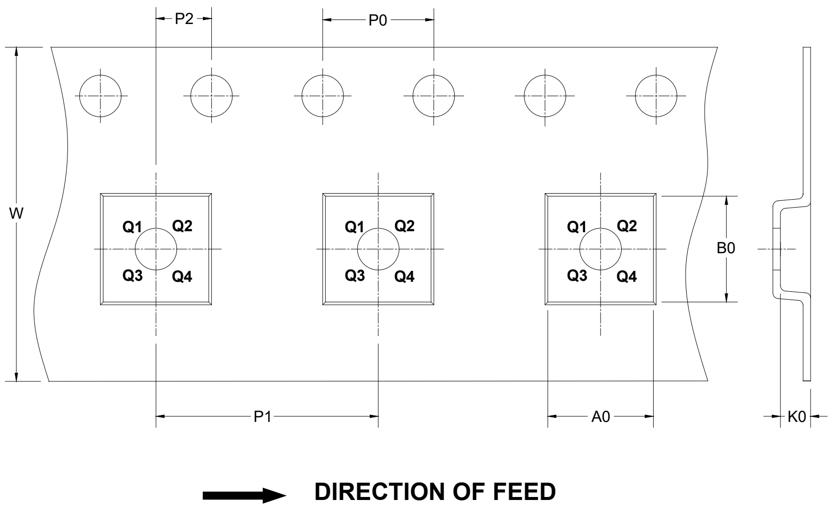
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



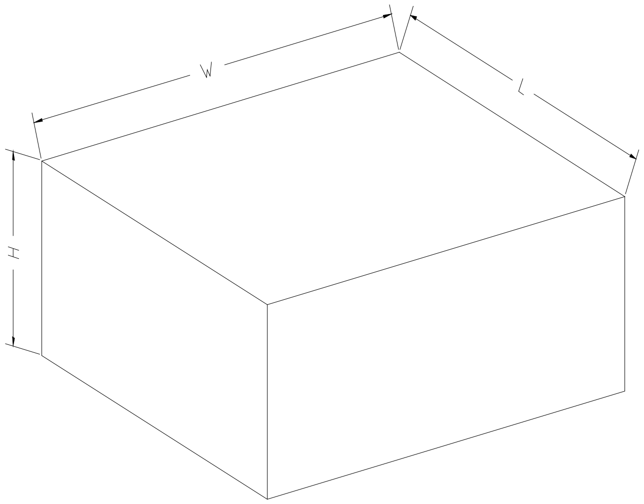
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-2×2-6AL	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002