74LV1T126
Single-Supply Translating Buffer/Line Driver with 3-State Output

GENERAL DESCRIPTION

The 74LV1T126 is a single translating buffer/line driver with 3-state output. It operates with a wide voltage range from 1.6V to 5.5V, making it suitable for industrial, portable and telecom applications. Due to the wide power supply voltage range, this device can generate the required output levels for connection to the controllers or processors.

The input features a low threshold circuit. When the supply voltage is at 3.3V, the input can match 1.8V input logic, allowing a level-up translation from 1.8V to 3.3V. Furthermore, the input pin can tolerate up to 5.5V and support level-down translation. For instance, when the supply voltage is at 2.5V, the output voltage can translate from 3.3V to 2.5V. With a reference to the supply voltage, the CMOS levels of output can be at 1.8V, 2.5V, 3.3V and 5.0V. The 3-state output is controlled by the output enable input (OE). When OE is low, the output is in the high-impedance state.

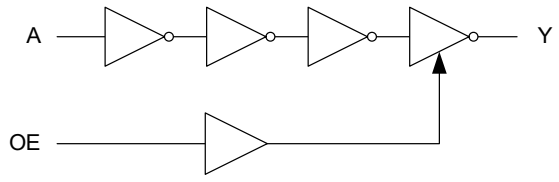
This device has output driving capability of 8mA that can be used to reduce line reflection, overshoot and undershoot resulted from high driving output.

The 74LV1T126 is available in Green SC70-5 and SOT-23-5 packages. It operates over an operating temperature range of -40℃ to +125℃.

APPLICATIONS

Telecom Equipment
Battery Powered Equipment
Industrial Equipment
Medical Equipment
Computing Equipment

LOGIC DIAGRAM



FEATURES

- **Wide Supply Voltage Range: 1.6V to 5.5V**
- **Single-Supply Voltage Translator at 1.8V, 2.5V, 3.3V and 5.0V**
- **Input Accepts Voltages up to 5.5V**
- **Level-Up Translation:**
  - **1.2V to 1.8V at V_{CC} = 1.8V**
  - **1.5V to 2.5V at V_{CC} = 2.5V**
  - **1.8V to 3.3V at V_{CC} = 3.3V**
  - **3.3V to 5.0V at V_{CC} = 5.0V**
- **Level-Down Translation:**
  - **3.3V to 1.8V at V_{CC} = 1.8V**
  - **3.3V to 2.5V at V_{CC} = 2.5V**
  - **5.0V to 3.3V at V_{CC} = 3.3V**
- **Logic Output Refers to Supply Voltage**
- **Latch-Up Performance (> 250mA) Meets JESD 78**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SC70-5 and SOT-23-5 Packages**

FUNCTION TABLE

INPUT (1) (LOWER LEVEL INPUT)		OUTPUT (2) (V_{CC} CMOS)
OE (3)	A	Y
H	H	H
H	L	L
L	*X*	Z

NOTES:

1. H = High Voltage Level, L = Low Voltage Level, Z = High -Impedance State, *X* = Don't Care.

2. H = Driving High, L = Driving Low, Z = High-Impedance State.

3. Avoid floating the OE pin to prevent signal oscillation.

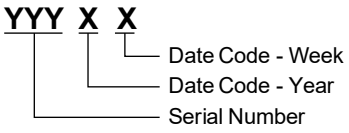
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LV1T126	SC70-5	-40℃ to +125℃	74LV1T126XC5G/TR	1FQXX	Tape and Reel, 3000
	SOT-23-5	-40℃ to +125℃	74LV1T126XN5G/TR	1FO XXXXX	Tape and Reel, 3000

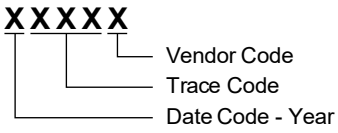
MARKING INFORMATION

NOTE: XX = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

SC70-5



SOT-23-5



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} ..... -0.5V to 7.0V
Input Voltage Range, V_I (1) ..... -0.5V to 7.0V
Output Voltage Range, V_O (1) -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Input Clamp Current, I_{IK} (V_I < 0V) .....-20mA
Output Clamp Current, I_{OK} (V_O > V_{CC} or V_O < 0V)..... ±20mA
Continuous Output Current, I_O ..... ±25mA
Continuous Current through V_{CC} or GND..... ±50mA
Junction Temperature (2) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility (3) (4)
HBM.....±6000V
CDM .....±1000V

NOTES:

1. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

3. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

4. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} ..... 1.6V to 5.5V
Input Voltage Range, V_I..... 0V to 5.5V
Output Voltage Range, V_O .....0V to V_{CC}
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 1.8V ..... 20ns/V (MAX)
V_{CC} = 2.5V or 3.3V..... 20ns/V (MAX)
V_{CC} = 5.0V ..... 20ns/V (MAX)
Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

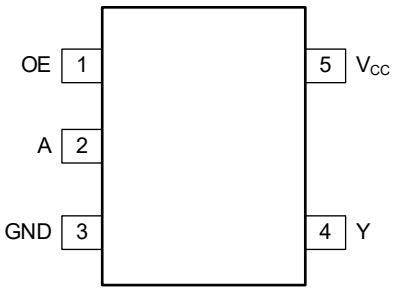
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



SC70-5/SOT-23-5

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	OE	Output Enable Input (Active-High).
2	A	Data Input.
3	GND	Ground.
4	Y	Data Output.
5	V_{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.65V to 1.8V		Full	1.00			V
		V_{CC} = 2.0V		Full	1.03			
		V_{CC} = 2.25V to 2.5V		Full	1.18			
		V_{CC} = 2.75V		Full	1.25			
		V_{CC} = 3.0V to 3.3V		Full	1.39			
		V_{CC} = 3.6V		Full	1.48			
		V_{CC} = 4.5V to 5.0V		Full	2.03			
		V_{CC} = 5.5V		Full	2.11			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.65V to 2.0V		Full			0.55	V
		V_{CC} = 2.25V to 2.75V		Full			0.71	
		V_{CC} = 3.0V to 3.6V		Full			0.65	
		V_{CC} = 4.5V to 5.5V		Full			0.80	
High-Level Output Voltage	V_{OH}	V_{CC} = 1.65V to 5.5V, I_{OH} = -20μA		Full	V_{CC} - 0.1	V_{CC} - 0.005		V
		V_{CC} = 1.65V, I_{OH} = -2mA		Full	1.210	1.540		
		V_{CC} = 1.8V, I_{OH} = -2mA		Full	1.450	1.700		
		V_{CC} = 2.3V, I_{OH} = -3mA		Full	1.930	2.200		
		V_{CC} = 2.5V, I_{OH} = -3mA		Full	2.150	2.410		
		V_{CC} = 3.0V, I_{OH} = -3mA		Full	2.700	2.925		
		V_{CC} = 3.0V, I_{OH} = -5.5mA		Full	2.490	2.860		
		V_{CC} = 3.3V, I_{OH} = -5.5mA		Full	2.800	3.170		
		V_{CC} = 4.5V, I_{OH} = -4mA		Full	4.100	4.430		
		V_{CC} = 4.5V, I_{OH} = -8mA		Full	3.950	4.350		
		V_{CC} = 5.0V, I_{OH} = -8mA		Full	4.500	4.860		
Low-Level Output Voltage	V_{OL}	V_{CC} = 1.65V to 5.5V, I_{OL} = 20μA		Full		0.005	0.100	V
		V_{CC} = 1.65V, I_{OL} = 2mA		Full		0.065	0.250	
		V_{CC} = 2.3V, I_{OL} = 3mA		Full		0.070	0.200	
		V_{CC} = 3.0V, I_{OL} = 3mA		Full		0.060	0.150	
		V_{CC} = 3.0V, I_{OL} = 5.5mA		Full		0.110	0.250	
		V_{CC} = 4.5V, I_{OL} = 4mA		Full		0.070	0.200	
		V_{CC} = 4.5V, I_{OL} = 8mA		Full		0.130	0.350	
Input Leakage Current	I_I	A input, V_{CC} = 0V, 1.8V, 2.5V, 3.3V, 5.5V, V_I = 0V or V_{CC}		Full		±0.01	±1	μA
Supply Current	I_{CC}	V_I = 0V or V_{CC}, open on loading, I_O = 0A	V_{CC} = 1.8V	Full		0.01	10	μA
			V_{CC} = 2.5V	Full		0.01	10	
			V_{CC} = 3.3V	Full		0.01	10	
			V_{CC} = 5.0V	Full		0.01	10	
Additional Supply Current	ΔI_{CC}	V_{CC} = 1.8V, one input at 0.3V or 1.1V, other inputs at 0V or V_{CC}, I_O = 0A		Full		0.1	10	μA
		V_{CC} = 5.5V, one input at 0.3V or 3.4V, other inputs at 0V or V_{CC}, I_O = 0A		Full		0.35	1.5	mA
Input Capacitance	C_I	V_{CC} = 3.3V, V_I = V_{CC} or GND		Full		4.0	10	pF
Output Capacitance	C_O	V_{CC} = 3.3V, V_O = V_{CC} or GND		+25℃		6.5		pF

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃ and V_{CC} = 1.8V, 2.5V, 3.3V and 5.0V respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Propagation Delay (2)	t_{PD}	A to Y, see Figure 2	V_{CC} = 1.8V, C_L = 15pF	Full	0.5	8.5	16.0	ns
			V_{CC} = 1.8V, C_L = 30pF	Full	0.5	9.0	18.1	
			V_{CC} = 2.5V, C_L = 15pF	Full	0.5	6.0	9.6	
			V_{CC} = 2.5V, C_L = 30pF	Full	0.5	6.5	10.1	
			V_{CC} = 3.3V, C_L = 15pF	Full	0.5	5.0	7.6	
			V_{CC} = 3.3V, C_L = 30pF	Full	0.5	5.5	8.1	
			V_{CC} = 5.0V, C_L = 15pF	Full	0.5	4.0	5.7	
			V_{CC} = 5.0V, C_L = 30pF	Full	0.5	4.5	6.1	
Off-to-High/Off-to-Low Propagation Delay	t_{PZH}, t_{PZL}	OE to Y, R_L = 1kΩ, see Figure 3	V_{CC} = 1.8V, C_L = 15pF	Full	0.5	6.0	13.8	ns
			V_{CC} = 1.8V, C_L = 30pF	Full	0.5	6.5	17.7	
			V_{CC} = 2.5V, C_L = 15pF	Full	0.5	4.0	7.8	
			V_{CC} = 2.5V, C_L = 30pF	Full	0.5	4.5	10.0	
			V_{CC} = 3.3V, C_L = 15pF	Full	0.5	3.5	6.0	
			V_{CC} = 3.3V, C_L = 30pF	Full	0.5	4.0	7.6	
			V_{CC} = 5.0V, C_L = 15pF	Full	0.5	3.5	5.2	
			V_{CC} = 5.0V, C_L = 30pF	Full	0.5	4.0	5.7	
High-to-Off/Low-to-Off Propagation Delay	t_{PHZ}, t_{PLZ}	OE to Y, R_L = 1kΩ, see Figure 3	V_{CC} = 1.8V, C_L = 15pF	Full	1.0	12.0	19.0	ns
			V_{CC} = 1.8V, C_L = 30pF	Full	1.0	13.0	22.5	
			V_{CC} = 2.5V, C_L = 15pF	Full	1.0	9.0	12.3	
			V_{CC} = 2.5V, C_L = 30pF	Full	1.0	9.5	13.3	
			V_{CC} = 3.3V, C_L = 15pF	Full	1.0	6.0	9.3	
			V_{CC} = 3.3V, C_L = 30pF	Full	1.0	6.5	9.6	
			V_{CC} = 5.0V, C_L = 15pF	Full	0.5	4.5	6.3	
			V_{CC} = 5.0V, C_L = 30pF	Full	1.0	5.0	7.1	
Power Dissipation Capacitance (3)	C_{PD}	f = 1MHz and 10MHz	V_{CC} = 1.8V	+25℃		11.0		pF
			V_{CC} = 2.5V	+25℃		11.0		
			V_{CC} = 3.3V	+25℃		11.0		
			V_{CC} = 5.0V	+25℃		11.0		

NOTES:

1. Specified by design and characterization, not production tested.

2. t_{PD} is the same as t_{PLH} and t_{PHL}.

3. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

where:

f_i = Input frequency in MHz.

f_o = Output frequency in MHz.

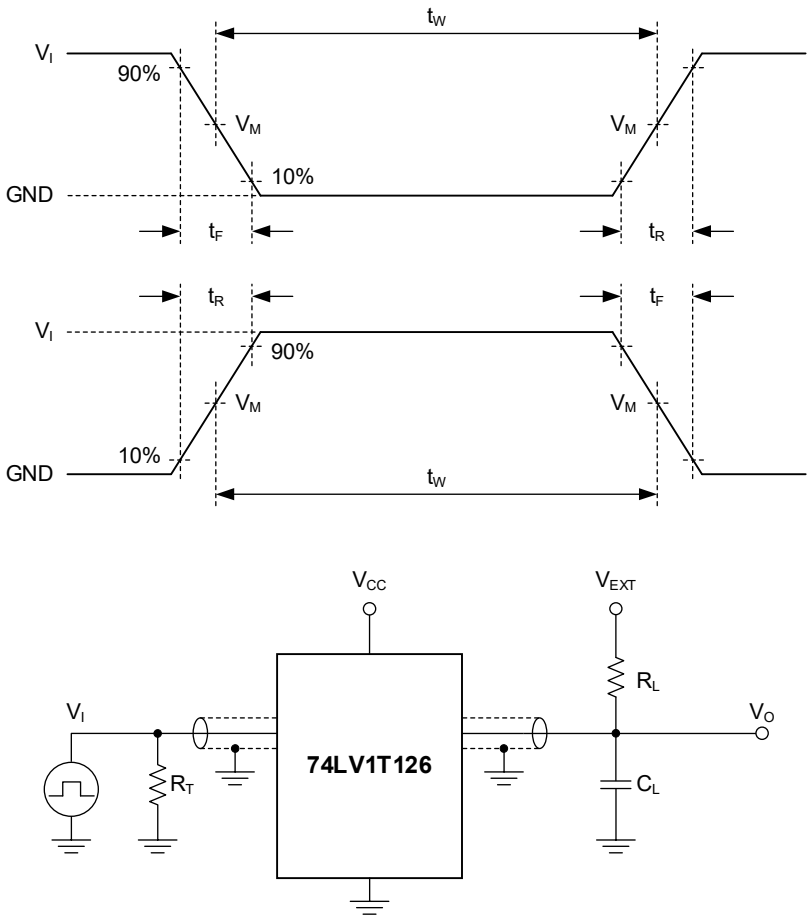
C_L = Output load capacitance in pF.

V_{CC} = Supply voltage in Volts.

N = Number of inputs switching.

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

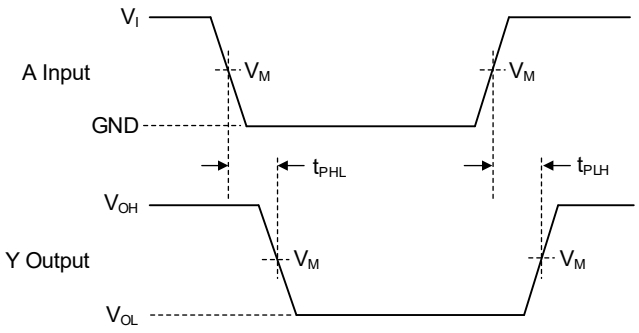
V_{EXT}: External voltage is used to measure switching time.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT			LOAD		V_{EXT}		
V_{CC}	V_I	t_R, t_F	f_{MAX}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.8V	V_{CC}	≤ 1.0ns	15MHz	15pF, 30pF	1kΩ	Open	V_{CC}	GND
2.5V	V_{CC}	≤ 1.0ns	25MHz	15pF, 30pF	1kΩ	Open	V_{CC}	GND
3.3V	3V	≤ 1.0ns	50MHz	15pF, 30pF	1kΩ	Open	V_{CC}	GND
5.0V	3V	≤ 1.0ns	50MHz	15pF, 30pF	1kΩ	Open	V_{CC}	GND

WAVEFORMS

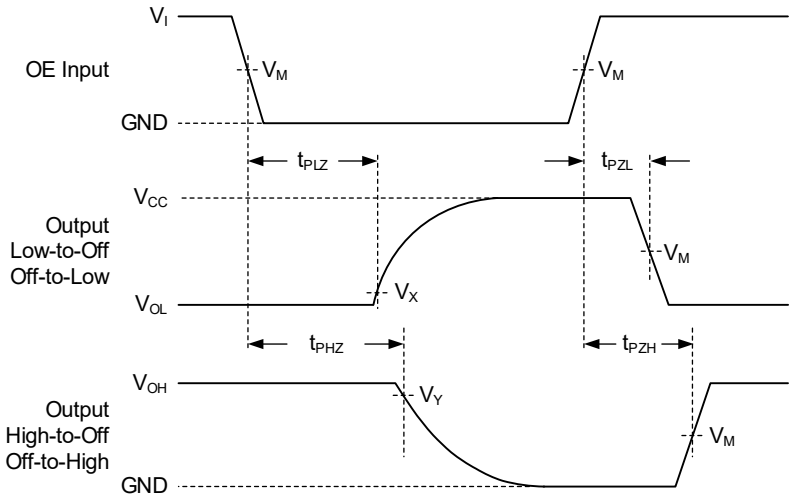


Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 2. Input (A) to Output (Y) Propagation Delay Times



Test conditions are given in Table 1.

Measurement points are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT		
V_{CC}	V_M (1)	V_M	V_X	V_Y
1.6V to 5.5V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3V	V_{OH} - 0.3V

NOTE:

1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 1.0ns.

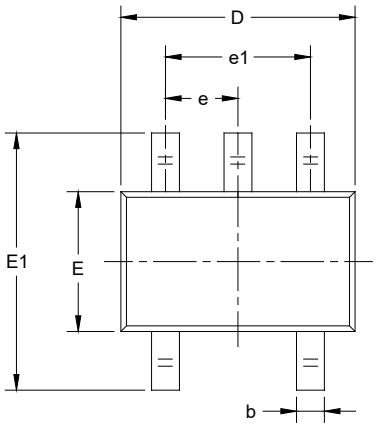
REVISION HISTORY

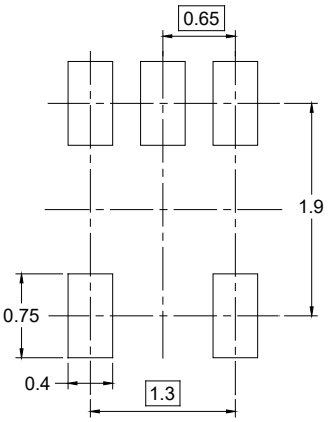
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (MARCH 2025) to REV.A	Page
Changed from product preview to production data	All

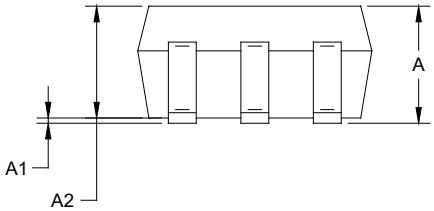
PACKAGE OUTLINE DIMENSIONS

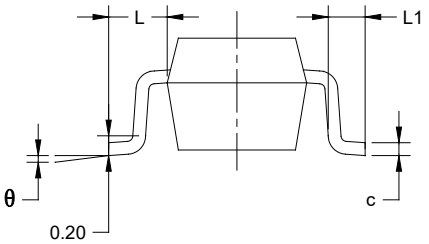
SC70-5





RECOMMENDED LAND PATTERN (Unit: mm)



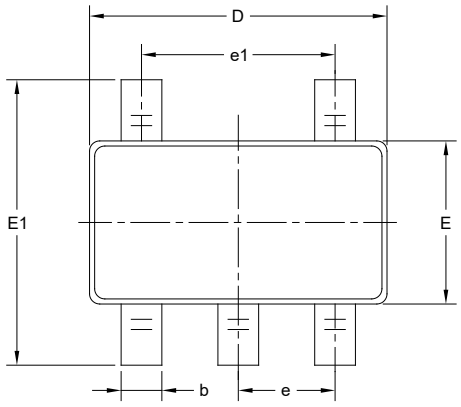


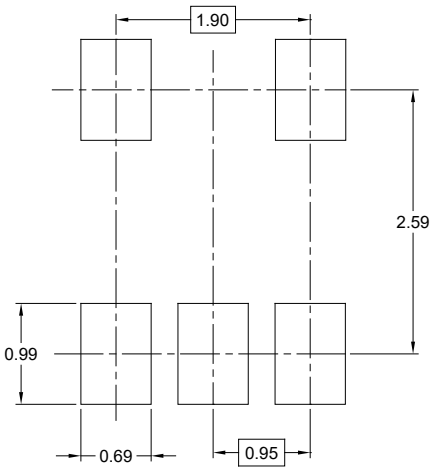
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	1.000	0.031	0.039
b	0.150	0.350	0.006	0.014
c	0.080	0.220	0.003	0.009
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.65 TYP		0.026 TYP	
e1	1.300 BSC		0.051 BSC	
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

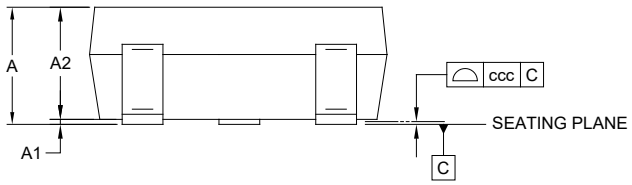
PACKAGE OUTLINE DIMENSIONS

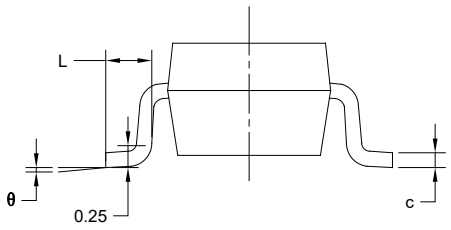
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



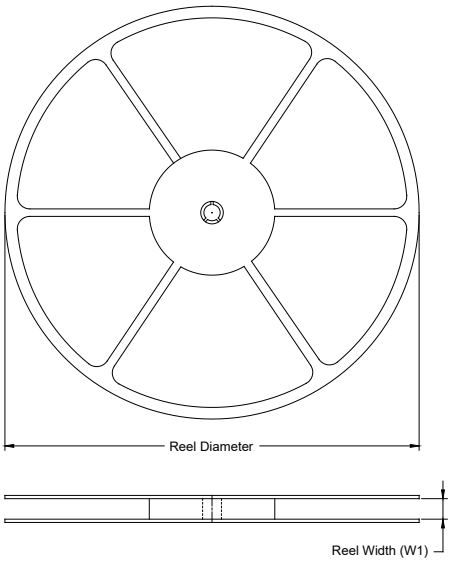


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

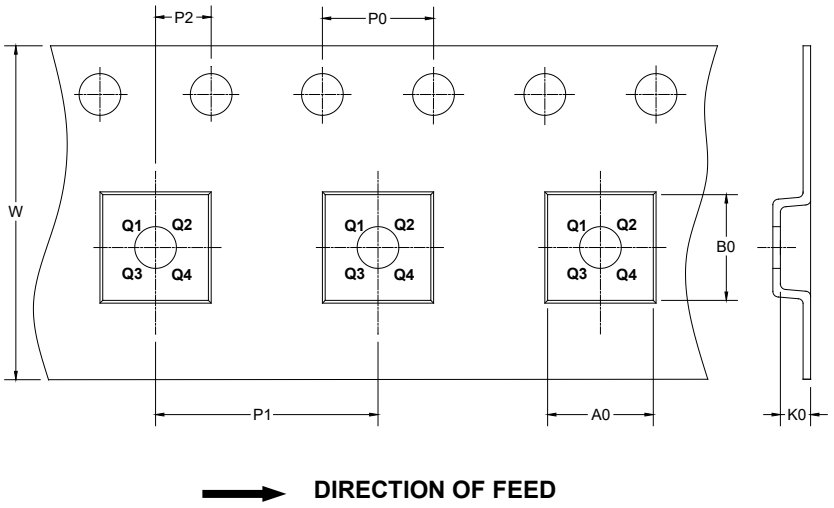
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



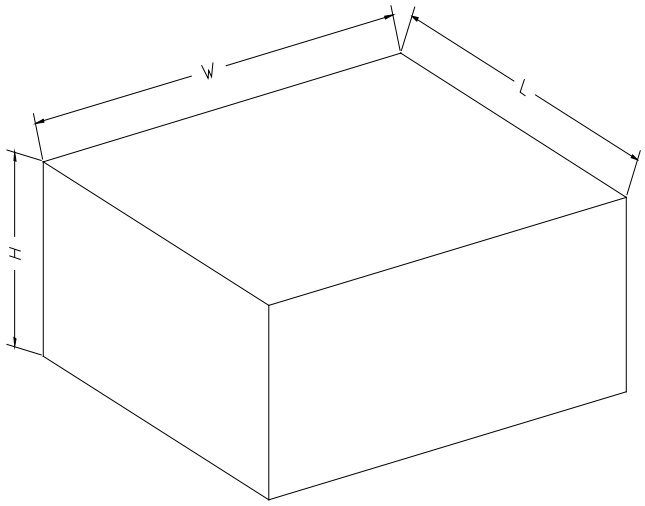
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-5	7″	9.5	2.40	2.50	1.20	4.0	4.0	2.0	8.0	Q3
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002