SGM8212-1Q/SGM8212-2Q
Low Noise, High Voltage, Automotive Operational Amplifiers

GENERAL DESCRIPTION

The single SGM8212-1Q and dual SGM8212-2Q are low noise operational amplifiers optimized for high voltage operation. These devices operate from 2.7V to 36V single supply or ±1.35V to ±18V dual power supplies, and consume low quiescent current. They provide rail-to-rail input with a wide input common mode voltage range from ($-V_S$) - 0.1V to ($+V_S$) + 0.1V, and rail-to-rail output voltage swing. However, the performance is reduced within 2V of the top rail.

The SGM8212-1Q and SGM8212-2Q also feature low offset voltage and high gain-bandwidth product.

These devices are AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and they are suitable for automotive applications.

The SGM8212-1Q is available in a Green SOT-23-5 package. The SGM8212-2Q is available in a Green SOIC-8 package. They are specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **Input Offset Voltage: ±1.8mV (MAX)**
- **Low Input Bias Current: ±10pA (TYP)**
- **High CMRR: 98dB (TYP)**
- **Unity-Gain Stable**
- **Gain-Bandwidth Product: 2.5MHz**
- **Phase Margin: 60° for G = +1 and C_L = 10pF**
- **Low Noise: 18nV/$\sqrt{\text{Hz}}$ at 1kHz**
- **Rail-to-Rail Input and Output**
- **Support Single or Dual Power Supplies:**
  2.7V to 36V or ±1.35V to ±18V
- **Low Quiescent Current: 530μA/Amplifier**
- **Small Packaging:**
  SGM8212-1Q Available in a Green SOT-23-5 Package
  SGM8212-2Q Available in a Green SOIC-8 Package

APPLICATIONS

Automotive Applications
Strain Gauge Amplifiers
Bridge Amplifiers
Transducer Amplifiers
Precision Integrators

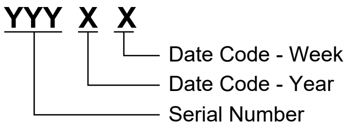
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE TOP MARKING	PACKING OPTION
SGM8212-1Q	SOT-23-5	-40℃ to +125℃	SGM8212-1QN5G/TR	0JUXX	Tape and Reel, 3000
SGM8212-2Q	SOIC-8	-40℃ to +125℃	SGM8212-2QS8G/TR	0JYS8 XXXXX	Tape and Reel, 4000

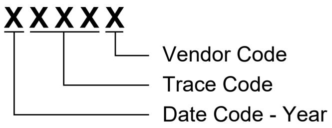
MARKING INFORMATION

NOTE: XX = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

SOT-23-5



SOIC-8



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V_S to -V_S	40V
Differential Input Voltage, |V_{ID}|	(+V_S) - (-V_S)
Input/Output Voltage Range	(-V_S) - 0.3V to (+V_S) + 0.3V
Junction Temperature	+150℃
Storage Temperature Range	-65℃ to +150℃
Lead Temperature (Soldering, 10s)	+260℃
ESD Susceptibility	
HBM (SGM8212-1Q)	2500V
HBM (SGM8212-2Q)	4000V
CDM	1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range	-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

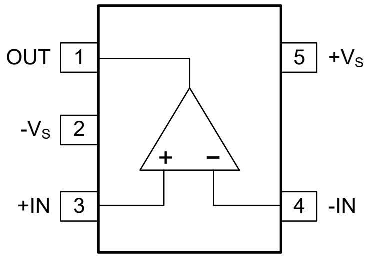
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

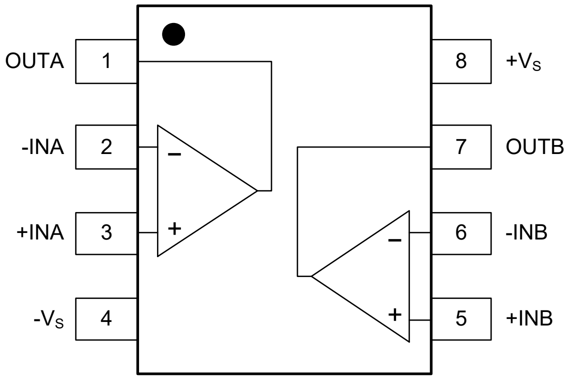
PIN CONFIGURATIONS

SGM8212-1Q (TOP VIEW)



SOT-23-5

SGM8212-2Q (TOP VIEW)



SOIC-8

ELECTRICAL CHARACTERISTICS

(V_S = ±1.35V to ±18V, R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Input Characteristics							
Input Offset Voltage	V_{OS}	V_{CM} = 0V	+25℃		±0.4	±1.8	mV
			Full			±2.0	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		Full		1.4		μV/℃
Input Bias Current	I_B	V_{CM} = 0V	+25℃		±10	±150	pA
			+85℃			±1000	pA
			Full			±14	nA
Input Offset Current	I_{OS}	V_{CM} = 0V	+25℃		±10	±150	pA
			+85℃			±1000	pA
			Full			±14	nA
Maximum Input Difference Bias Current	$\lvert I_{ID} \rvert$	V_S = ±18V, V_{ID} = ±18V	+25℃		2	3	μA
			Full			4	
Input Common Mode Voltage Range	V_{CM}		Full	$(-V_S) - 0.1$		$(+V_S) + 0.1$	V
Common Mode Rejection Ratio	CMRR	V_S = ±2V, $(-V_S) - 0.1V < V_{CM} < (+V_S) + 0.1V$	+25℃	63	80		dB
			Full	60			
		V_S = ±2V, $(-V_S) - 0.1V < V_{CM} < (+V_S) - 2V$	+25℃	76	94		
			Full	73			
		V_S = ±18V, $(-V_S) - 0.1V < V_{CM} < (+V_S) + 0.1V$	+25℃	82	98		
			Full	79			
		V_S = ±18V, $(-V_S) - 0.1V < V_{CM} < (+V_S) - 2V$	+25℃	96	114		
			Full	93			
Open-Loop Voltage Gain	A_{OL}	V_S = ±1.35V, $(-V_S) + 0.35V < V_{OUT} < (+V_S) - 0.35V$	+25℃	100	130		dB
			Full	97			
		V_S = ±18V, $(-V_S) + 0.35V < V_{OUT} < (+V_S) - 0.35V$	+25℃	120	140		
			Full	112			
Output Characteristics							
Output Voltage Swing from Rail	V_{OUT}	V_S = ±18V	+25℃		110	150	mV
			Full			240	
Output Short-Circuit Current	I_{SC}	V_S = ±18V	+25℃	±16	±30		mA
			Full	±10			
Power Supply							
Operating Voltage Range	V_S		Full	2.7		36	V
Power Supply Rejection Ratio	PSRR	V_S = 4V to 36V	+25℃	102	120		dB
			Full	96			
Quiescent Current/Amplifier	I_Q	I_{OUT} = 0A	+25℃		530	700	μA
			Full			750	

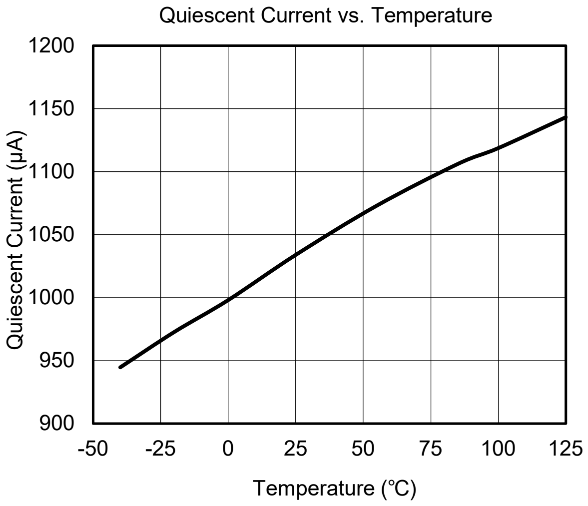
ELECTRICAL CHARACTERISTICS (continued)

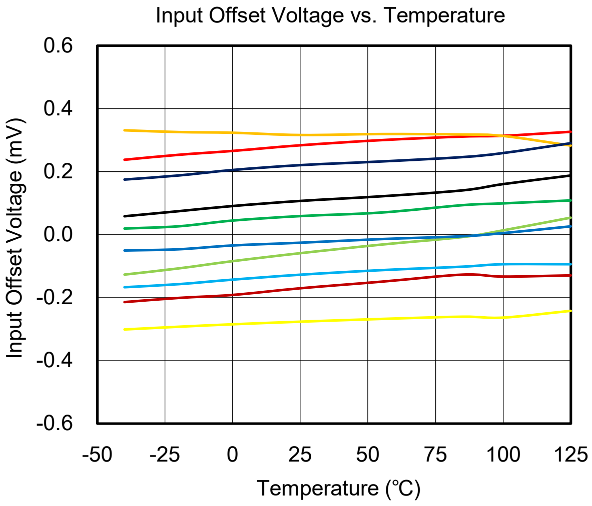
(V_S = ±1.35V to ±18V, R_L = 10kΩ connected to 0V, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

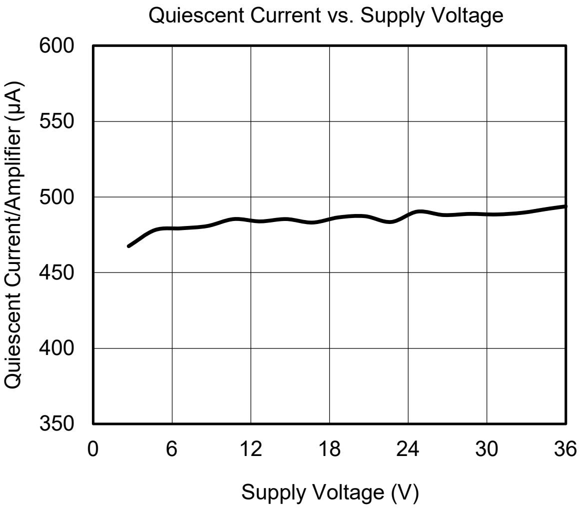
PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Dynamic Performance							
Gain-Bandwidth Product	GBP	C_L = 10pF	+25℃		2.5		MHz
Phase Margin	$φ_O$	C_L = 10pF	+25℃		60		°
Slew Rate	SR	V_S = ±2V to ±18V, G = +1	+25℃		1.4		V/μs
Settling Time to 0.1%	t_S	V_S = ±18V, G = +1, 10V step	+25℃		15		μs
Overload Recovery Time	ORT	V_{IN} × G > V_S	+25℃		2.7		μs
Total Harmonic Distortion + Noise	THD+N	V_S = 36V, V_{OUT} = $3V_{RMS}$, f = 1kHz, G = +1	+25℃		0.0002		%
Noise							
Input Voltage Noise		f = 0.1Hz to 10Hz	+25℃		3		$μV_{P-P}$
Input Voltage Noise Density	e_n	f = 1kHz	+25℃		18		$nV/\sqrt{Hz}$
		f = 100Hz	+25℃		33		
Input Current Noise Density	i_n	f = 1kHz	+25℃		420		$fA/\sqrt{Hz}$

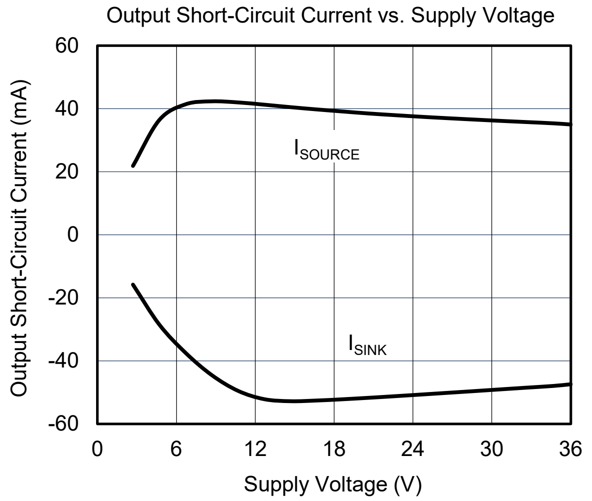
TYPICAL PERFORMANCE CHARACTERISTICS

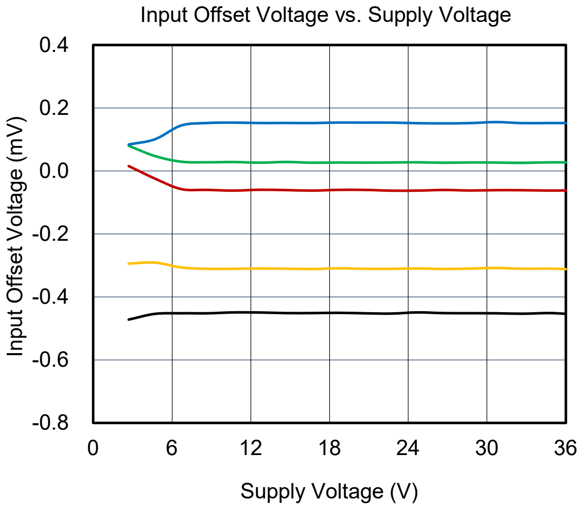
At T_A = +25℃, V_S = 36V, unless otherwise noted.

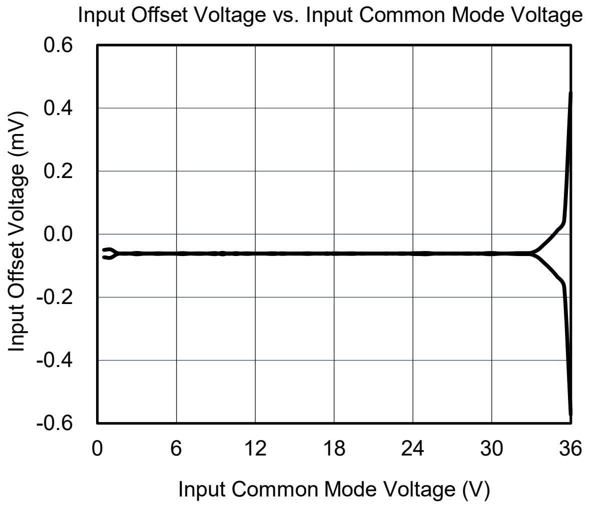






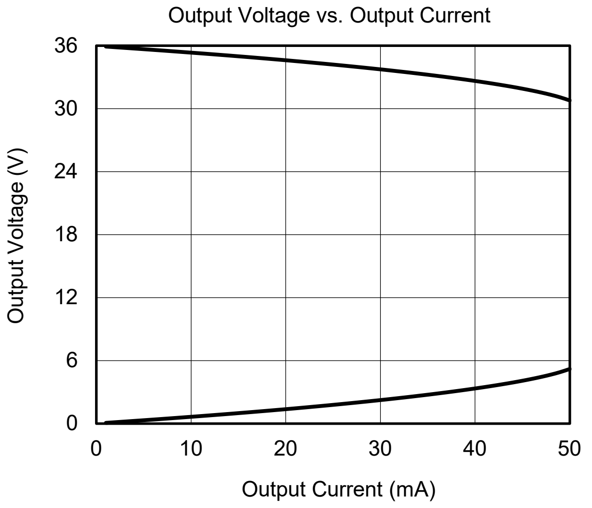


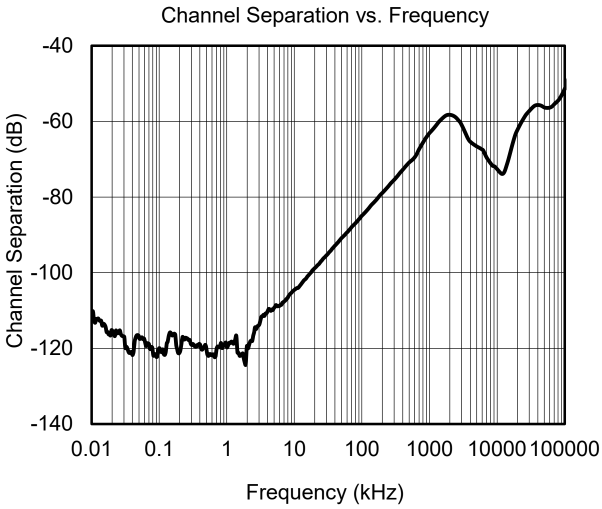


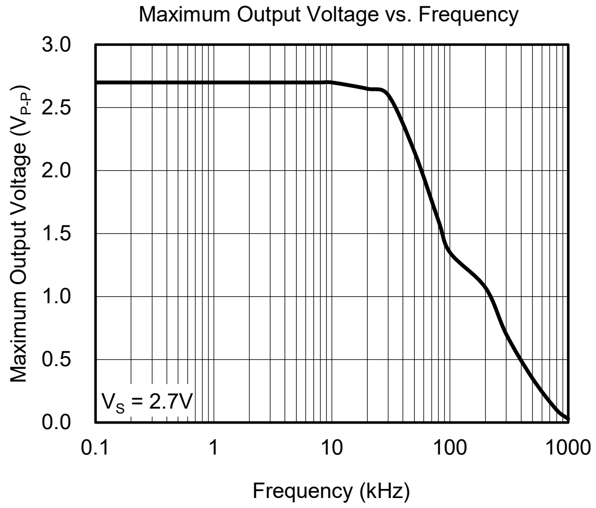


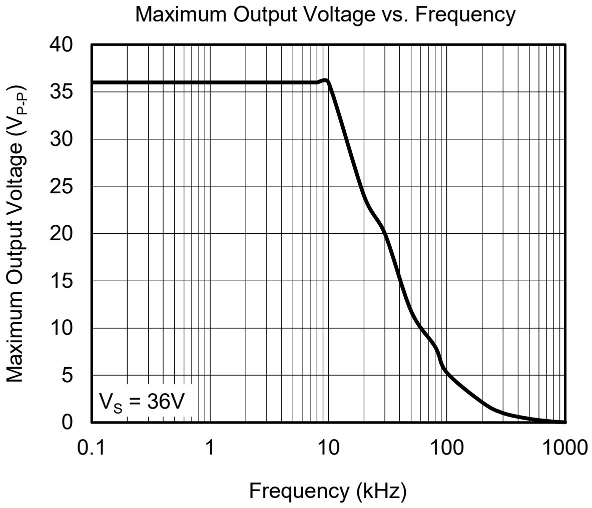
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

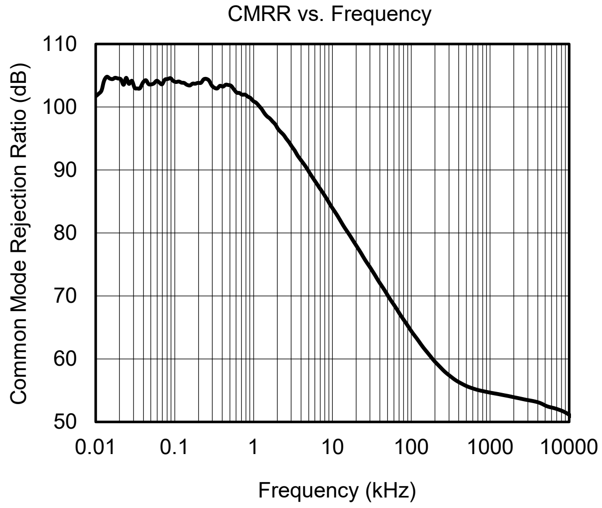
At T_A = +25℃, V_S = 36V, unless otherwise noted.

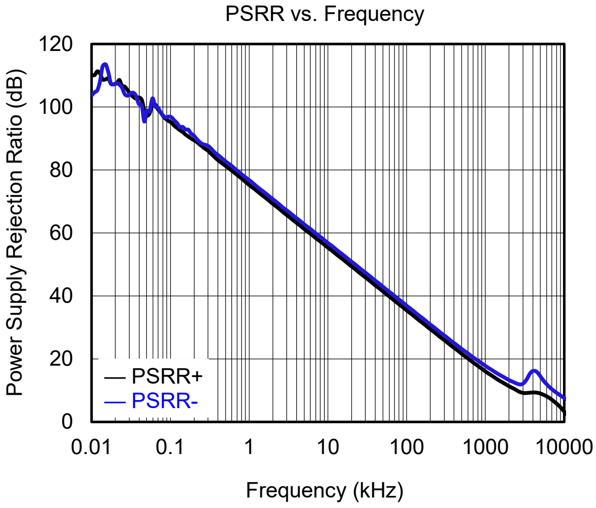








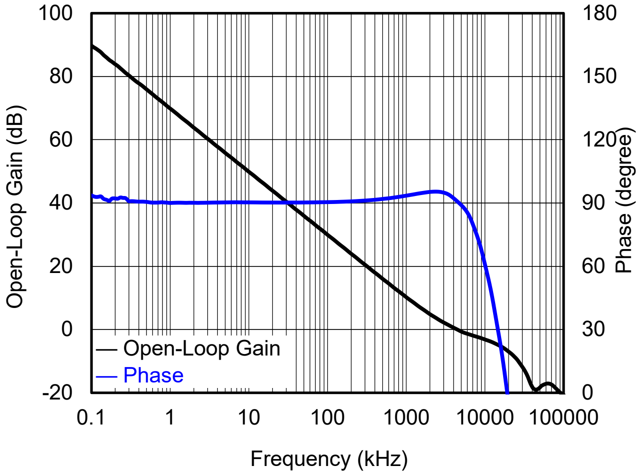




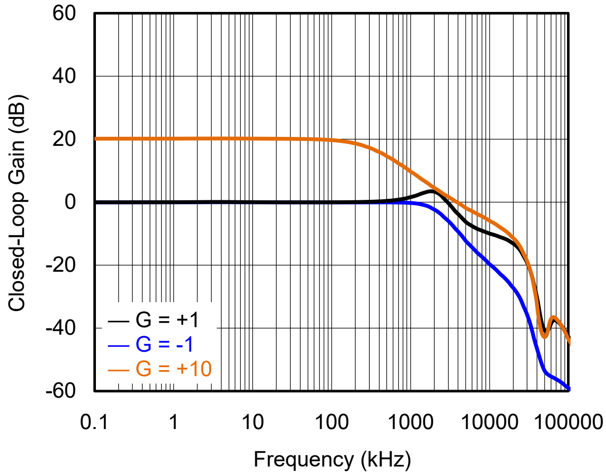
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 36V, unless otherwise noted.

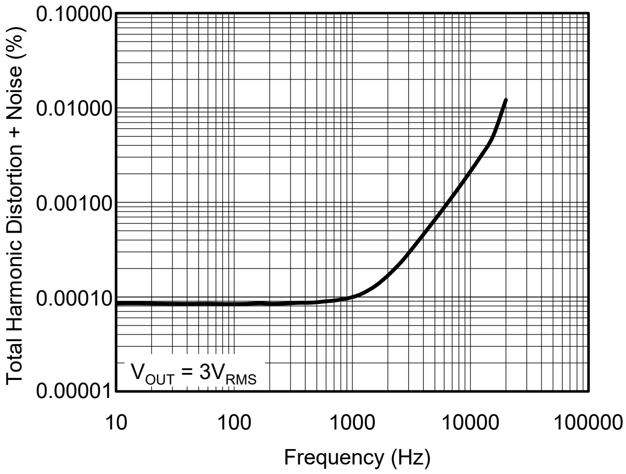
Open-Loop Gain and Phase vs. Frequency



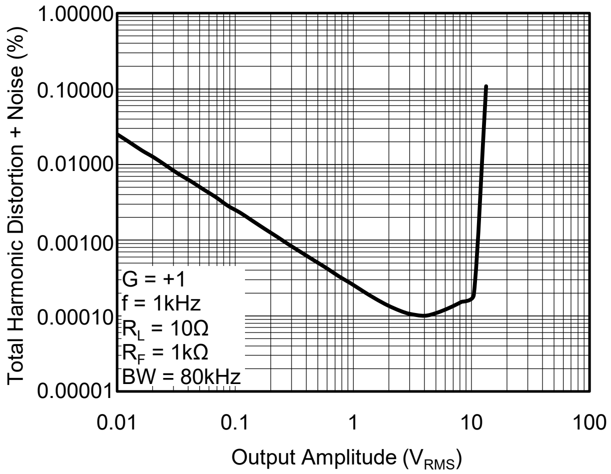
Closed-Loop Gain vs. Frequency



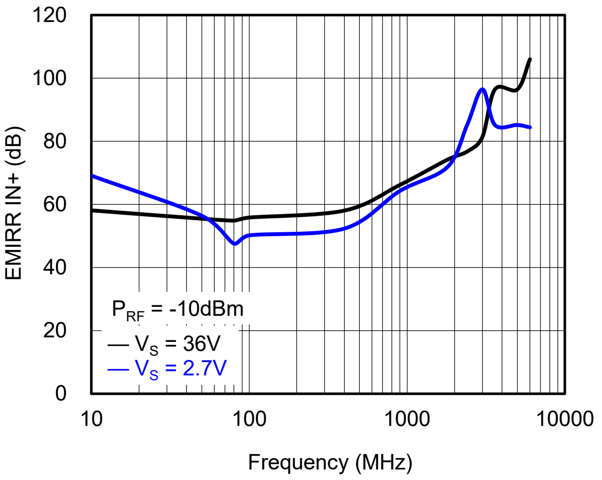
THD+N vs. Frequency



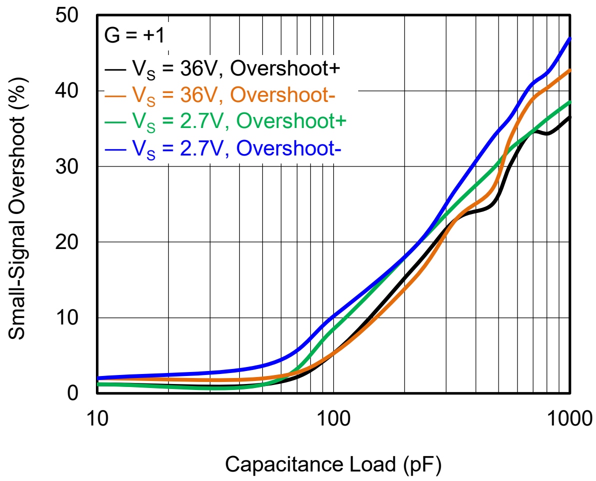
THD+N vs. Output Amplitude



EMIRR IN+ vs. Frequency



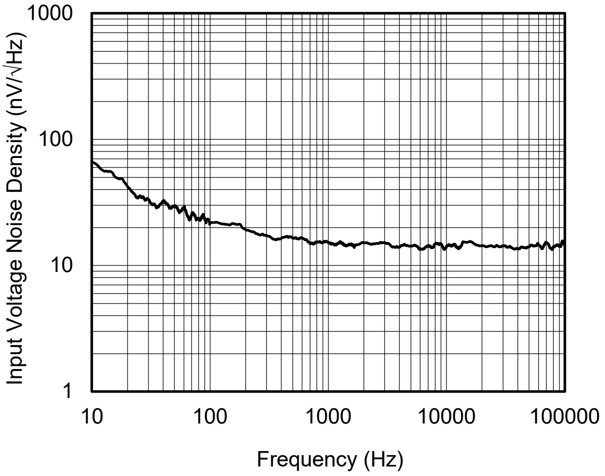
Small-Signal Overshoot vs. Capacitive Load



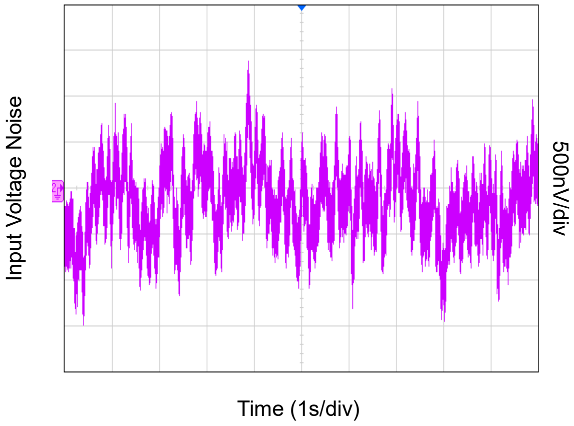
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 36V, unless otherwise noted.

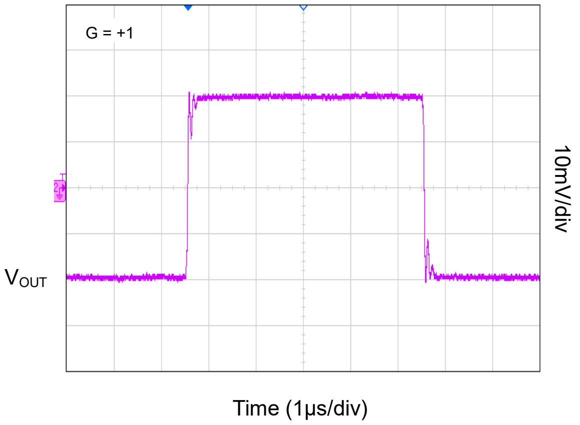
Input Voltage Noise Density vs. Frequency



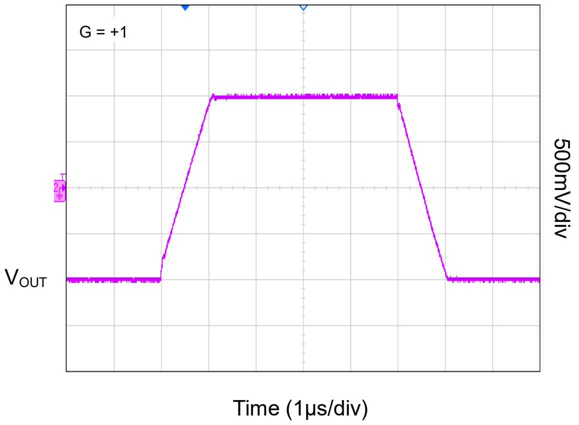
0.1Hz to 10Hz Input Voltage Noise



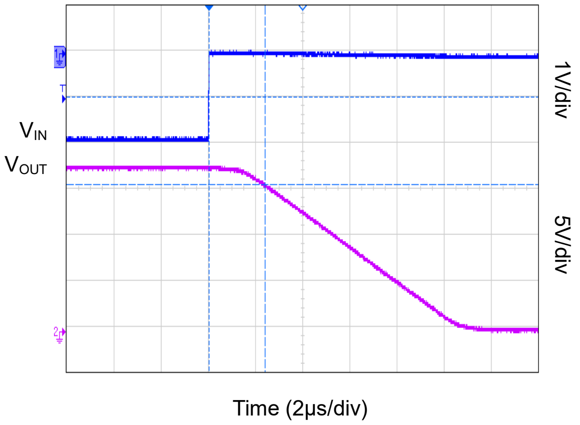
Small-Signal Step Response



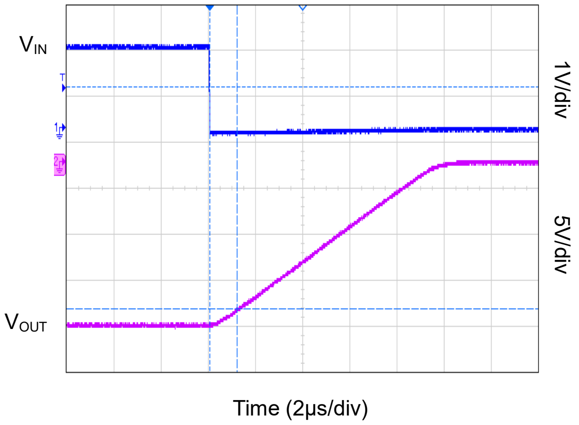
Large-Signal Step Response



Positive Overload Recovery



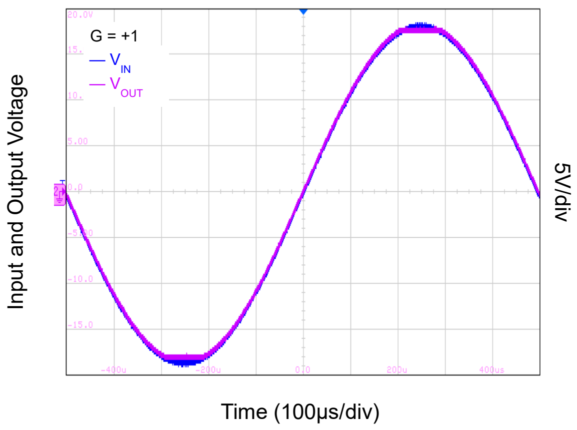
Negative Overload Recovery



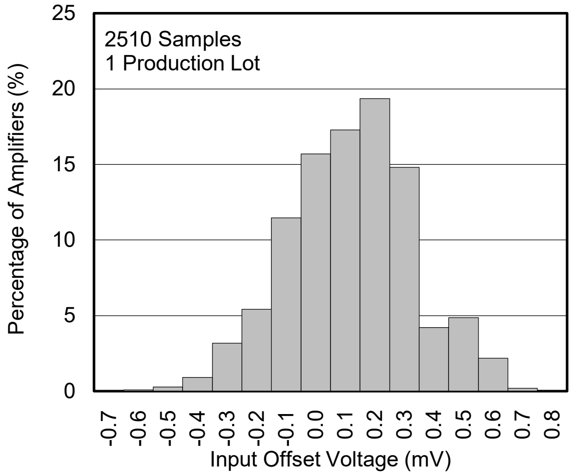
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = 36V, unless otherwise noted.

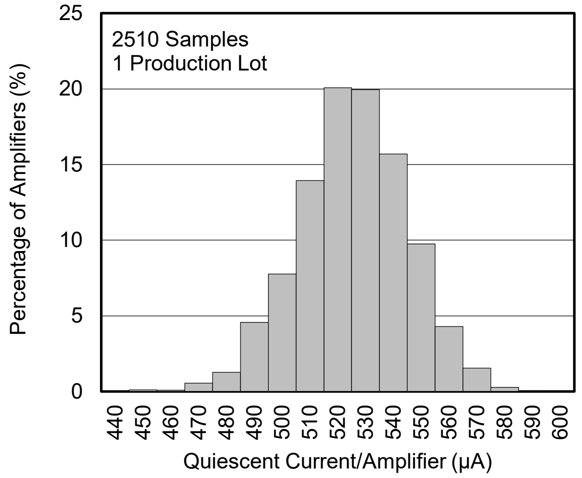
No Phase Reversal



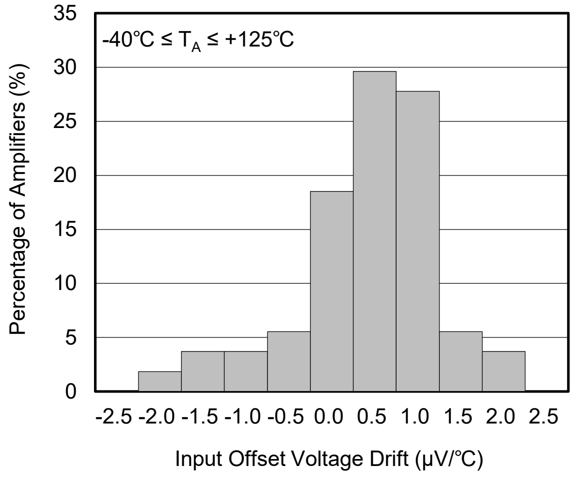
Input Offset Voltage Production Distribution



Quiescent Current Production Distribution



Input Offset Voltage Drift Distribution



APPLICATION INFORMATION

Rail-to-Rail Input

When SGM8212-1Q/2Q work at the power supply between 2.7V and 36V, the input common mode voltage range is from (-V_S) - 0.1V to (+V_S) + 0.1V. In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage so that it does not exceed the rails.

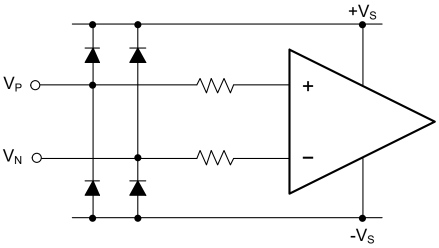


Figure 1. Input Equivalent Circuit

Input Current-Limit Protection

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 2, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is that it contributes thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

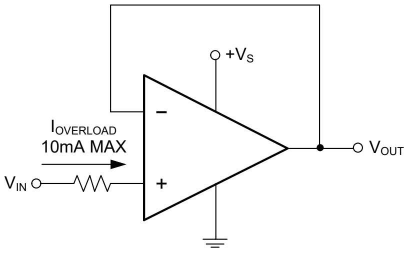


Figure 2. Input Current-Limit Protection

Rail-to-Rail Output

The SGM8212-1Q/2Q support rail-to-rail output operation. In single power supply application, for example, when +V_S = 36V, -V_S = GND, 10kΩ load resistor is tied from OUT pin to ground, the typical output swing range is from 0.11V to 35.89V.

Driving Capacitive Loads

The SGM8212-1Q/2Q are designed for driving the 300pF capacitive load with unity-gain stable. If greater capacitive load must be driven in application, the circuit in Figure 3 can be used. In this circuit, the IR drop voltage generated by R_{ISO} is compensated by feedback loop.

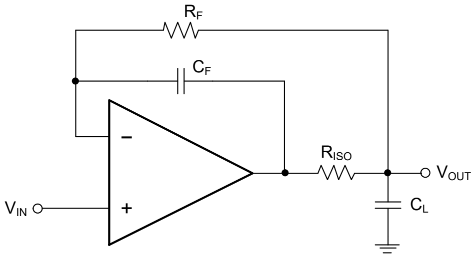


Figure 3. Circuit to Drive Heavy Capacitive Load

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design. Besides of input signal noise, the power supply is one of important source of noise to the amplifiers through +V_S and -V_S pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, 10μF ceramic capacitor paralleled with 0.1μF or 0.01μF ceramic capacitor is used in Figure 4. The ceramic capacitors should be placed as close as possible to +V_S and -V_S power supply pins.

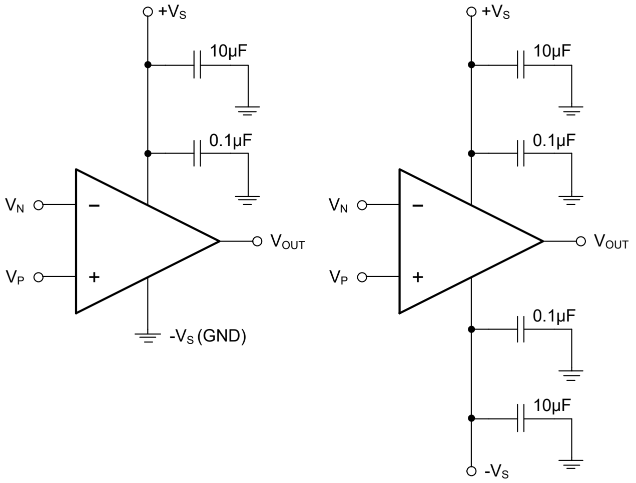


Figure 4. Amplifier Power Supply Bypassing

APPLICATION INFORMATION (continued)

Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in the same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

Typical Application Circuits

Difference Amplifier

The circuit in Figure 5 is a design example of classical difference amplifier. If $R_4/R_3 = R_2/R_1$, then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

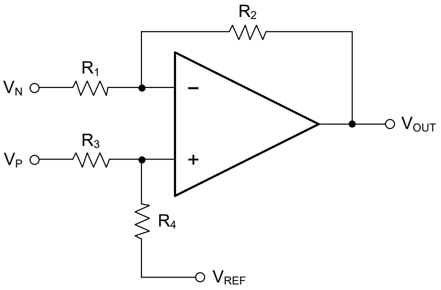


Figure 5. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 6 is a design example of high input impedance difference amplifier. The added amplifiers at the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 5.

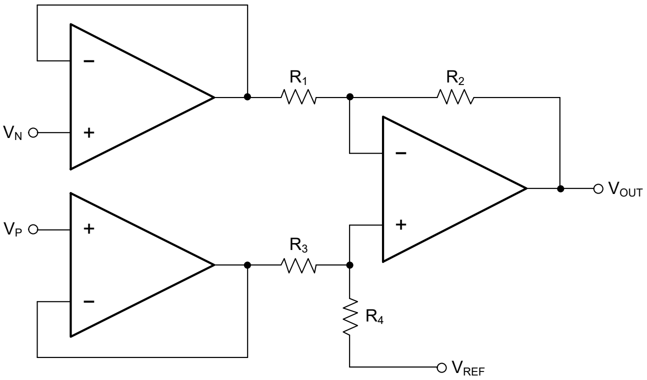


Figure 6. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The circuit in Figure 7 is a design example of active low-pass filter, the DC gain is equal to $-R_2/R_1$ and the -3dB corner frequency is equal to $1/(2\pi R_2C)$. In this design, the filter bandwidth must be less than the bandwidth of the amplifier, and the resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

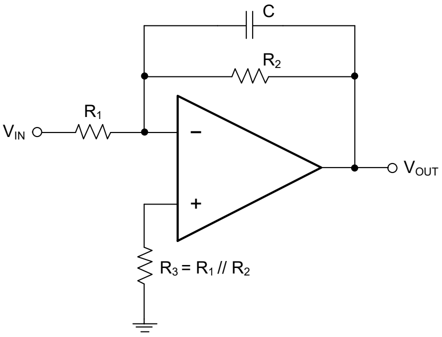


Figure 7. Active Low-Pass Filter

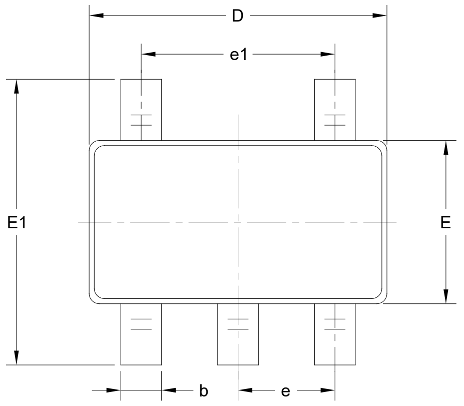
REVISION HISTORY

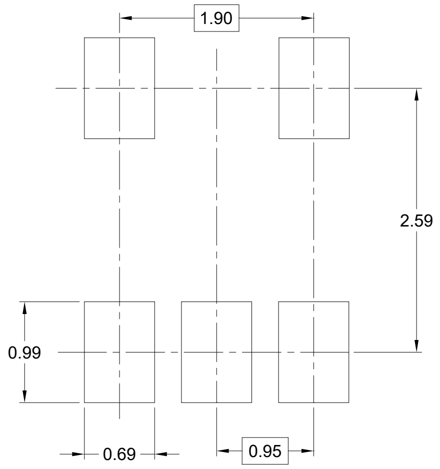
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (AUGUST 2024) to REV.A	**Page**
Changed from product preview to production data	All

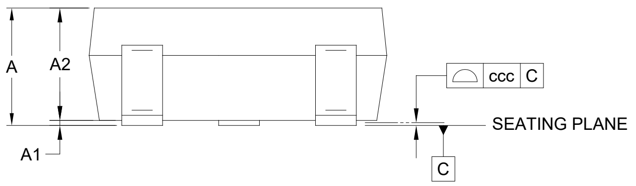
PACKAGE OUTLINE DIMENSIONS

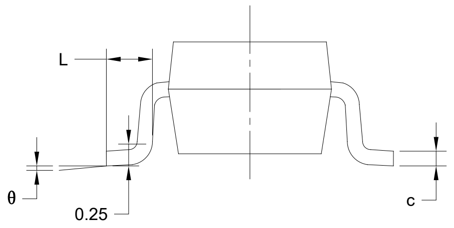
SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)



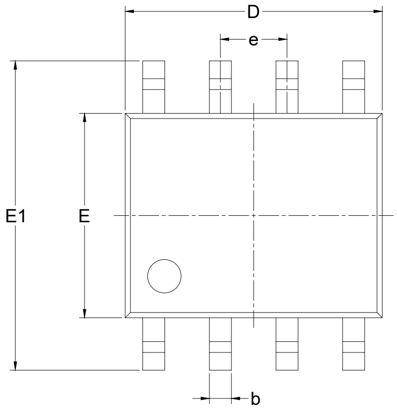


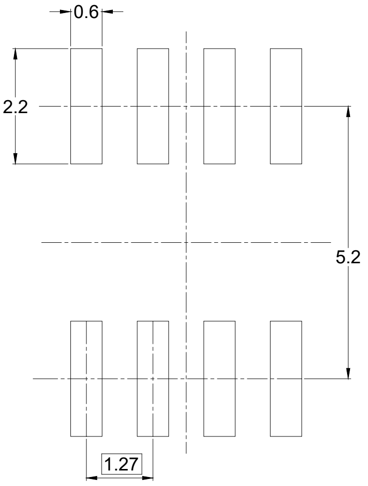
Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

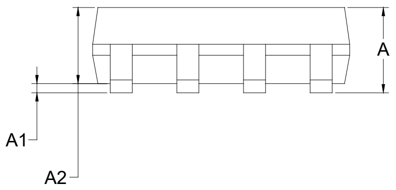
PACKAGE OUTLINE DIMENSIONS

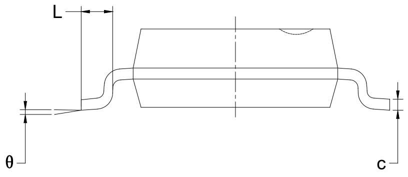
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



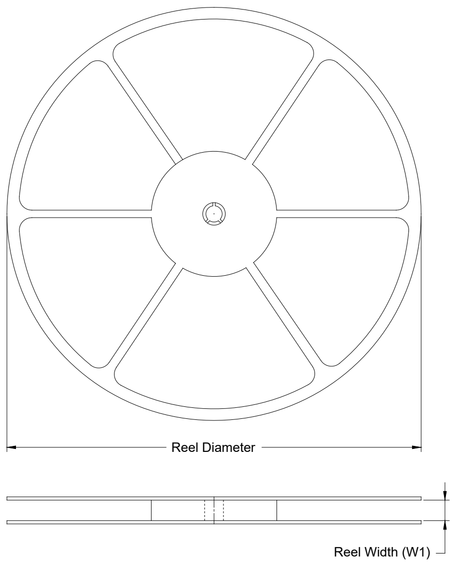


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

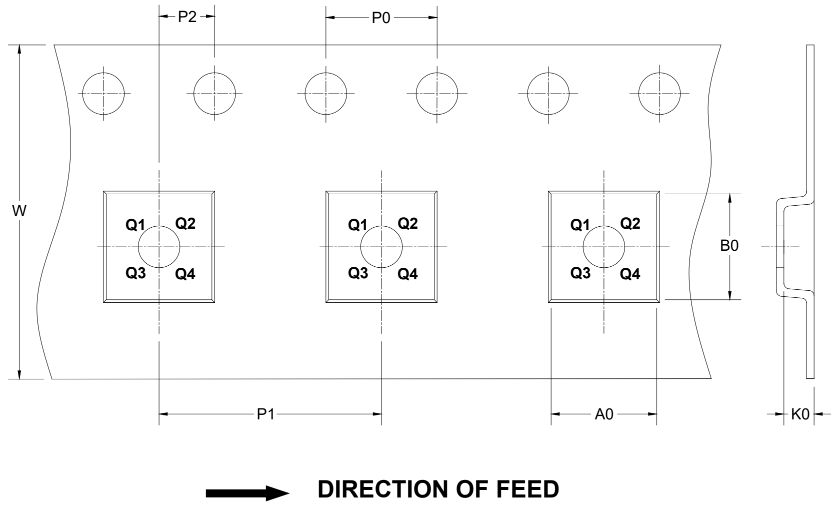
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



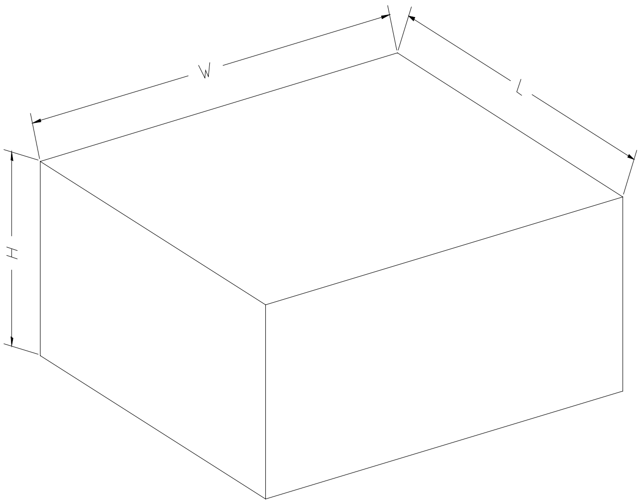
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7″	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002