SGM5100/SGM5101
14-Bit, 10MSPS/40MSPS Low Power 3V ADCs

GENERAL DESCRIPTION

The SGM5100/SGM5101 are 14-bit 10MSPS/40MSPS, low power 3V single-channel analog-to-digital converters (ADCs) suitable for sampling high frequency and wide dynamic range signals. With 74.1dB/72.8dB SNR and 79dB/88dB SFDR for signals at the Nyquist frequency, the SGM5100/SGM5101 meet demanding requirements in imaging and communication applications.

The SGM5100/SGM5101 feature good DC performances such as ±1.7LSB (TYP) INL, ±0.65LSB (TYP) DNL and no missing codes over-temperature. Besides, the $1LSB_{RMS}$ transition noise is also a remarkable feature of the devices.

The SGM5100/SGM5101 support single-ended sampling clock input with an internal optional clock duty cycle stabilizer, which guarantees high performance for a wide range of clock duty cycles when sampling at full speed.

The SGM5100/SGM5101 are available in a Green TQFN-5×5-32DL package.

FEATURES

- **Single 3V Supply (2.7V to 3.4V)**
- **Sample Rate:**
  - **SGM5100: 10MSPS**
  - **SGM5101: 40MSPS**
- **Low Power:**
  - **SGM5100: 55.5mW (TYP)**
  - **SGM5101: 190mW (TYP)**
- **SNR:**
  - **SGM5100: 74.1dB (TYP)**
  - **SGM5101: 72.8dB (TYP)**
- **SFDR:**
  - **SGM5100: 79dB (TYP)**
  - **SGM5101: 88dB (TYP)**
- **Flexible Input: $1V_{P-P}$ to $2V_{P-P}$ Range**
- **Full Power Bandwidth S/H: 575MHz**
- **No Missing Codes**
- **Sleep and Nap Modes**
- **Support Clock Duty Cycle Stabilizer**
- **Available in a Green TQFN-5×5-32DL Package**

APPLICATIONS

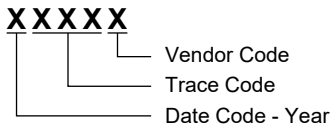
Communication Infrastructures
Medical Imaging Systems
Instrumentations

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5100	TQFN-5×5-32DL	-40℃ to +125℃	SGM5100XTVJ32G/TR	SGM5100 XTVJ32 XXXXX	Tape and Reel, 3000
			SGM5100XTVJ32SG/TR	SGM5100 XTVJ32 XXXXX	Tape and Reel, 250
SGM5101	TQFN-5×5-32DL	-40℃ to +125℃	SGM5101XTVJ32G/TR	SGM5101 XTVJ32 XXXXX	Tape and Reel, 3000
			SGM5101XTVJ32SG/TR	SGM5101 XTVJ32 XXXXX	Tape and Reel, 250

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

OV_{DD} = V_{DD} (1)

Supply Voltage (V_{DD}) 4V

Analog Input Voltage Range (2) ..... -0.3V to (V_{DD} + 0.3V)

Digital Input Voltage Range ..... -0.3V to (V_{DD} + 0.3V)

Digital Output Voltage Range ..... -0.3V to (OV_{DD} + 0.3V)

Power Dissipation 4600mW

Package Thermal Resistance

TQFN-5×5-32DL, θ_{JA} ..... 26.9℃/W

TQFN-5×5-32DL, θ_{JB} ..... 8.6℃/W

TQFN-5×5-32DL, $\theta_{JC\ (TOP)}$ ..... 18.5℃/W

TQFN-5×5-32DL, $\theta_{JC\ (BOT)}$ ..... 1.9℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 4000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

NOTES:

1. All voltage values are referred to ground. If no special comments, GND and OGND are connected together.

2. When these pin voltages are lower than GND or higher than V_{DD}, they will be clamped by the internal protection circuits. The device can deal with the input currents of greater than 100mA below GND or above V_{DD} without latch-up.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

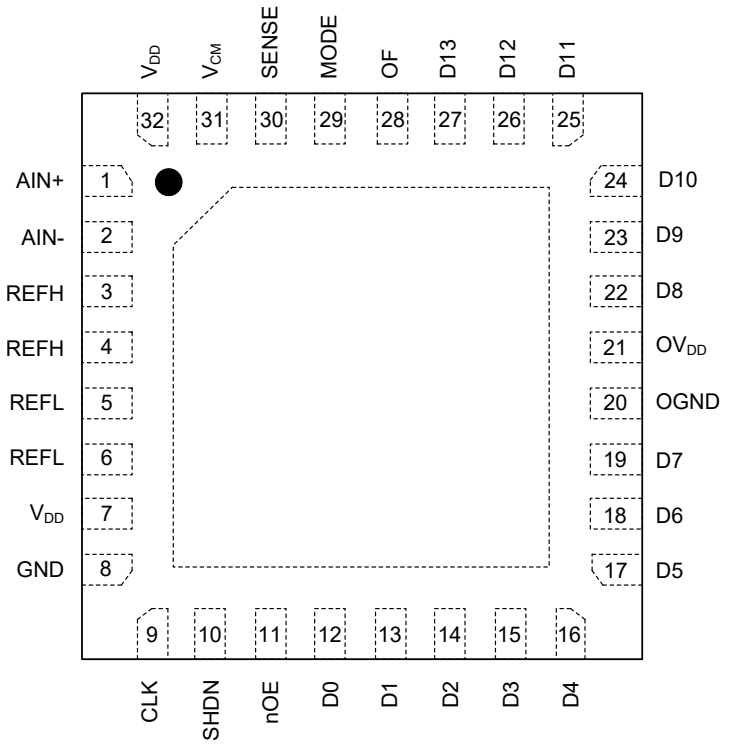
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM5100/SGM5101 (TOP VIEW)



TQFN-5×5-32DL

PIN DESCRIPTION

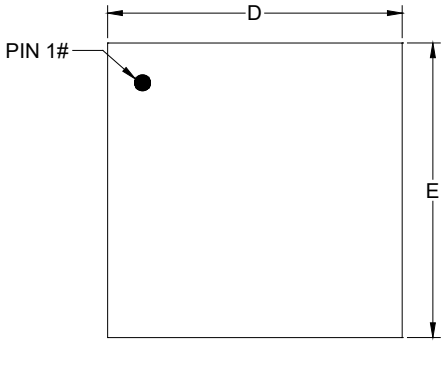
PIN	NAME	FUNCTION
1	AIN+	Positive Differential Analog Input Pin.
2	AIN-	Negative Differential Analog Input Pin.
3, 4	REFH	ADC Reference Input High. Connect them together and place a 0.1μF between the pins and pin 5/pin 6. Also a 2.2μF along with another 1μF ceramic chip capacitor is suggested to connect between the pin and ground.
5, 6	REFL	ADC Reference Input Low. Connect them together and place a 0.1μF between the pins and pin 3/pin 4. Also a 2.2μF along with another 1μF ceramic chip capacitor is suggested to connect between the pin and ground.
7, 32	V_{DD}	3V Power Supply. A 0.1μF bypass ceramic capacitors is suggested between this pin and ground.
8	GND	ADC Power Ground.
9	CLK	Clock Input Pin. Conversion starts on the rising edge.
10	SHDN	Shutdown Pin. Co-work with nOE pin. (0 means connecting the pin to GND and 1 means connecting the pin to V_{DD}) SHDN = 0 and nOE = 0: normal operation with the outputs enabled. SHDN = 0 and nOE = 1: normal operation with the outputs at high impedance. SHDN = 1 and nOE = 0: nap mode with the outputs at high impedance. SHDN = 1 and nOE = 1: sleep mode with the outputs at high impedance.
11	nOE	Output Enable Pin. Refer to SHDN pin function.

PIN DESCRIPTION (continued)

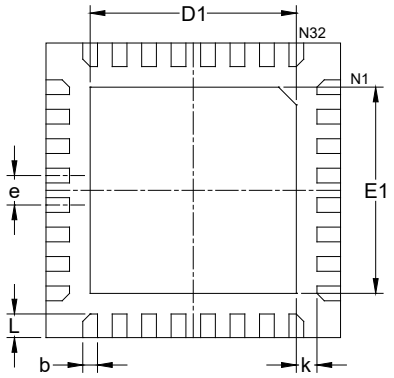
PIN	NAME	FUNCTION
12	D0	Digital Output Pin 0. This is the LSB.
13	D1	Digital Output Pin 1.
14	D2	Digital Output Pin 2.
15	D3	Digital Output Pin 3.
16	D4	Digital Output Pin 4.
17	D5	Digital Output Pin 5.
18	D6	Digital Output Pin 6.
19	D7	Digital Output Pin 7.
20	OGND	Output Ground.
21	OV_{DD}	Power Supply for Digital Output. It should be bypassed to ground with 0.1μF ceramic chip capacitor.
22	D8	Digital Output Pin 8.
23	D9	Digital Output Pin 9.
24	D10	Digital Output Pin 10.
25	D11	Digital Output Pin 11.
26	D12	Digital Output Pin 12.
27	D13	Digital Output Pin 13. This is the MSB.
28	OF	Over/Under Flow Indicator. High if an over or under flow occurs.
29	MODE	Output Format and Clock Duty Cycle Stabilizer Selection Pin. MODE = GND: offset binary output format and disables the clock duty cycle stabilizer. MODE = 1/3 V_{DD}: offset binary output format and enables the clock duty cycle stabilizer. MODE = 2/3 V_{DD}: two's complement output format and enables the clock duty cycle stabilizer MODE = V_{DD}: two's complement output format and disables the clock duty cycle stabilizer.
30	SENSE	Internal reference and a ±1V input range are selected if SENSE is connected to V_{DD}. Similarly, Internal reference and a ±0.5V input range are selected if SENSE is connected to V_{CM}. External reference and an input range of $\pm V_{SENSE}$ are selected if SENSE is connected to a voltage from 0.5V to 1V. Note that ±1V is the largest valid input range.
31	V_{CM}	1.5V Output and Input Common Mode Bias Pin. It is recommended to connect a 2.2μF bypass capacitor between the pin and ground.
Exposed Pad	—	ADC Power Ground. The exposed pad should be connected to ground.

PACKAGE OUTLINE DIMENSIONS

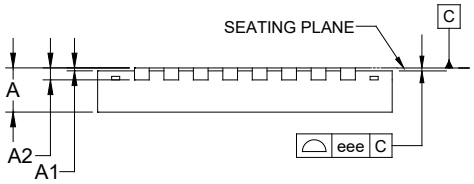
TQFN-5×5-32DL



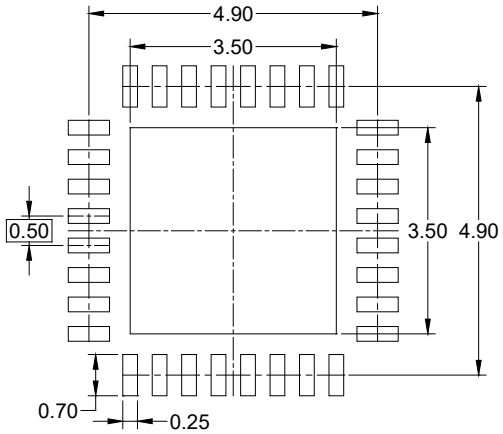
TOP VIEW



BOTTOM VIEW



SIDE VIEW



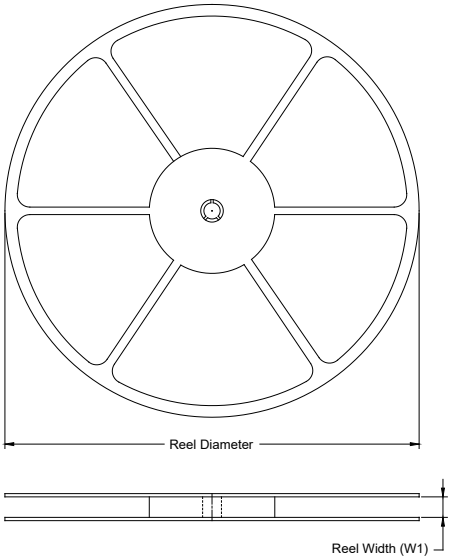
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.100
A2		0.203 REF	
b	0.180	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.400	3.500	3.600
E1	3.400	3.500	3.600
e		0.500 BSC	
k		0.350 REF	
L	0.300	-	0.500
eee		0.080	

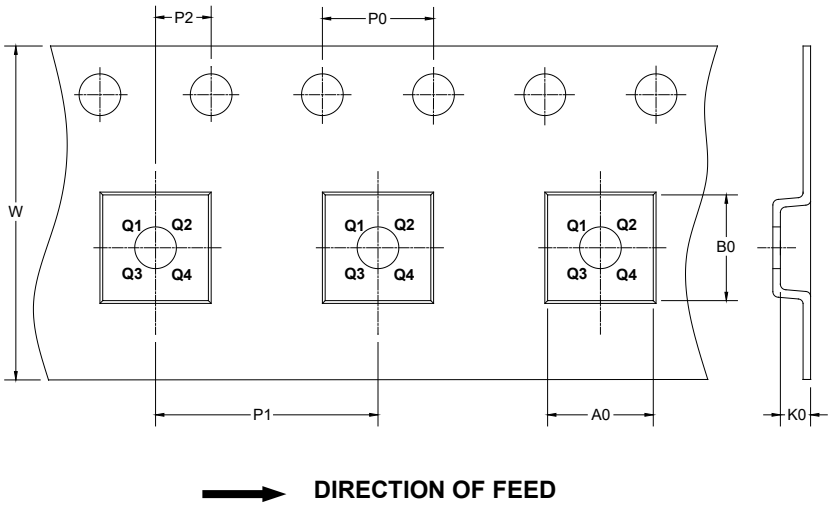
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



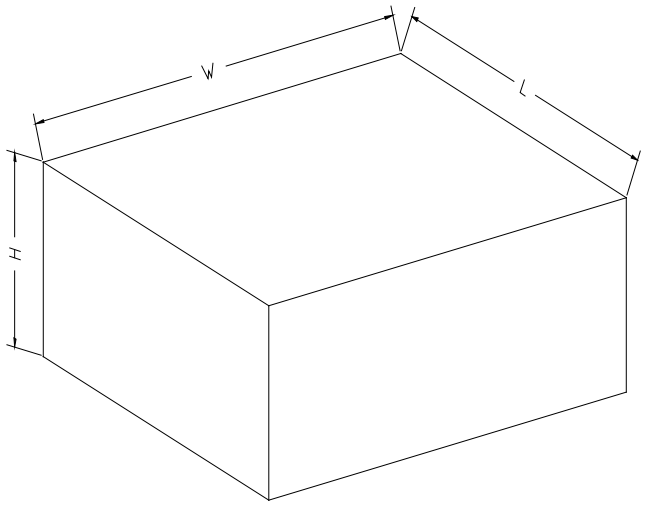
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-32DL	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002