SGM64104
4.5V to 18V Input, Voltage-Mode, Synchronous Buck Controller with Power Good

GENERAL DESCRIPTION

The SGM64104 is a voltage-mode controlled Buck controller with an operating voltage range of 4.5V to 18V. The operating frequency of SGM64104A is fixed at 600kHz and the SGM64104B is fixed at 300kHz. Smaller inductors and output capacitors can be used for higher frequency, making the layout more compact and cost-optimized.

The device senses the voltage difference between SW and GND and compares it with the selected current limit threshold to perform low-side valley current limit protection. Users can select three different current limit threshold voltages of 100mV, 200mV and 280mV by connecting an external resistor (R_{COMP}) between COMP and GND. This current limit threshold is latched during startup. And the high-side over-current protection is achieved by comparing the sensed voltage difference between VDD and SW with an internal 550mV threshold voltage, and the high-side MOSFET will be shut off immediately. When the device determines an output short-circuit, both high-side and low-side MOSFETs are turned off, and the device attempts to restart after hiccup timeout.

The SGM64104 is available in a Green TQFN-3×3-10L package and can operate in the -40℃ to +125℃ temperature range.

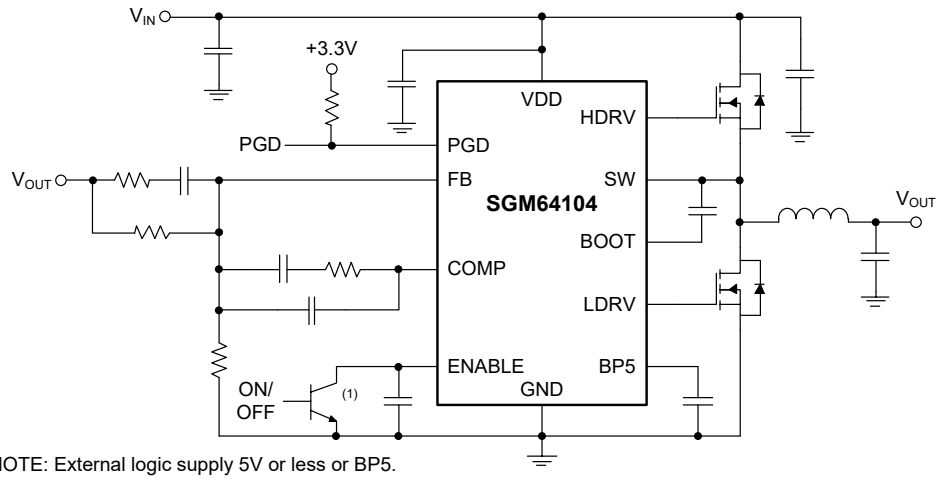
FEATURES

- **Wide Input Supply from 4.5V to 18V**
- **Up to 20A Output Currents**
- **Support Pre-Biased Outputs**
- **Precise Reference: 591mV, ± 0.5% (TYP) at +25℃**
- **Switching Frequency**
  - **SGM64104A: 600kHz**
  - **SGM64104B: 300kHz**
- **Three Editable Thermally-Compensated Short-Circuit Protection Thresholds**
- **Hiccup Restart from Faults**
- **Internal 5V Regulator**
- **Both High-side MOSFETs and Low-side MOSFETs $R_{DS(ON)}$ Current Sensing**
- **3ms Soft-Start Time**
- **Thermal Shutdown**
- **Available in a Green TDFN-3×3-10L Package**

APPLICATIONS

Digital Set Top Box
Cable Modem CPE
Entry Level and Mid-Range Servers
Graphics/Audio Cards

TYPICAL APPLICATION



NOTE: External logic supply 5V or less or BP5.

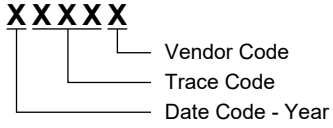
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM64104A	TDFN-3×3-10L	-40℃ to +125℃	SGM64104AXTD10G/TR	SGM 0BFD XXXXX	Tape and Reel, 4000
SGM64104B	TDFN-3×3-10L	-40℃ to +125℃	SGM64104BXTD10G/TR	SGM 0BGD XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VDD, ENABLE Voltage ..... -0.3V to 20V
SW Voltage ..... -0.3V to 25V
SW Voltage (< 10ns pulse width) ..... -5V to 25V
BOOT, HDRV Voltage ..... -0.3V to 30V
BOOT-SW, HDRV-SW Voltage (Differential from BOOT or HDRV to SW) ..... -0.3V to 6V
FB, BP5, LDRV, PGD Voltage ..... -0.3V to 6V
COMP Voltage ..... -0.3V to 5.5V
Package Thermal Resistance
TDFN-3×3-10L, θ_{JA} ..... 43.0℃/W
TDFN-3×3-10L, θ_{JB} ..... 16.7℃/W
TDFN-3×3-10L, $\theta_{JC\ (TOP)}$ ..... 42.6℃/W
TDFN-3×3-10L, $\theta_{JC\ (BOT)}$ ..... 6.2℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±1500V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 4.5V to 18V
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

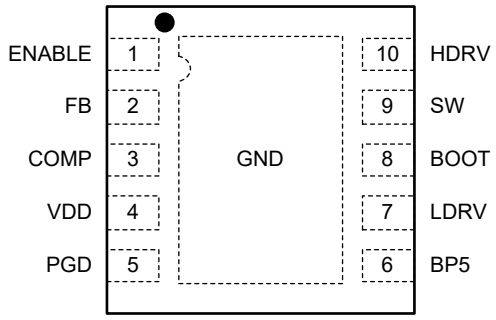
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TDFN-3×3-10L

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	ENABLE	I	Logic Enable Level Pin. A high level turns on the device, and the pin is internally pulled up weakly, so it can be left floating without using this function.
2	FB	I	Inverting Input of the Error Amplifier. This pin should be at 591mV (TYP) when the output voltage is in regulation.
3	COMP	O	Error Amplifier Output Pin.
4	VDD	P	Power Supply Voltage Pin.
5	PGD	O	Open-Drain Power Good Output.
6	BP5	O	Output Bypassed Pin of Internal Regulator. Connecting a capacitor (up to of 4.7μF) to this pin can improve the noise performance when using a low-side MOSFET with gate charge greater than 25nC. The device is allowed to connect with low power loads, and the sum of the current required for additional loads and gate drive is prohibited from exceeding 50mA. This regulator is controlled by ENABLE pin.
7	LDRV	O	Rectifier MOSFET Gate Output.
8	BOOT	I	Drive Pin for High-side MOSFET. Connect a capacitor (100nF, TYP) between SW and this pin.
9	SW	I	It is the return for high-side gate driver. It is also used for current sense.
10	HDRV	O	A bootstrap output which is used to drive a high-side MOSFET.
Exposed Pad	GND	G	Thermal Exposed Pad. It is the main thermal relief path of the die connected to the ground plane on the PCB.

NOTE: I = input, O = output, I/O = input/output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(V_{VDD} = 12V, T_J = -40℃ to +85℃, all parameters at zero power dissipation, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference						
Feedback Voltage Range	V_{FB}	T_J = 0℃ to +85℃	587	591	595	mV
		T_J = -40℃ to +85℃	585	591	595	
Input Supply						
Input Voltage Range	V_{VDD}		4.5		18	V
Operating Current	I_{VDD}	V_{ENABLE} = 3V		2	4	mA
		V_{ENABLE} = 0.6V		39	70	μA
On-Board Regulator						
Output Voltage	V_{5VBP}	V_{VDD} > 6V, I_{5VBP} ≤ 10mA	4.75	5	5.25	V
Regulator Dropout Voltage	V_{DO}	V_{VDD} - V_{BP5} , V_{VDD} = 5V, I_{BP5} ≤ 25mA		160	550	mV
Regulator Current Limit Threshold	I_{SC}		50			mA
Average Current	I_{BP5}				50	mA
Oscillator						
Switching Frequency	f_{SW}	SGM64104A	500	600	700	kHz
		SGM64104B	240	300	360	
Ramp Amplitude	V_{RMP}	Input feedforward		V_{VDD}/12		V
PWM						
Maximum Duty Cycle	D_{MAX}	SGM64104A	77	85		%
		SGM64104B	89	93		
Minimum Controlled Pulse	t_{ON_MIN}				110	ns
Output Driver Dead Time	t_{DEAD}	HDRV off to LDRV on		41		ns
		LDRV off to HDRV on		22		
Soft-Start						
Soft-Start Time	t_{SS}		2	3	6	ms
Soft-Start Delay Time	t_{SSDLY}			2		ms
Time to Regulation	t_{REG}			6		ms
Error Amplifier						
Gain Bandwidth Product (1)	G_{BWP}			16		MHz
DC Gain (1)	A_{OL}			95		dB
Input Bias Current (Current out of FB Pin)	I_{IB}				100	nA
Output Source Current	I_{EAOP}	V_{FB} = 0V	1			mA
Output Sink Current	I_{EAOM}	V_{FB} = 2V	1			mA

NOTE:

1. Guaranteed by design, not tested in production.

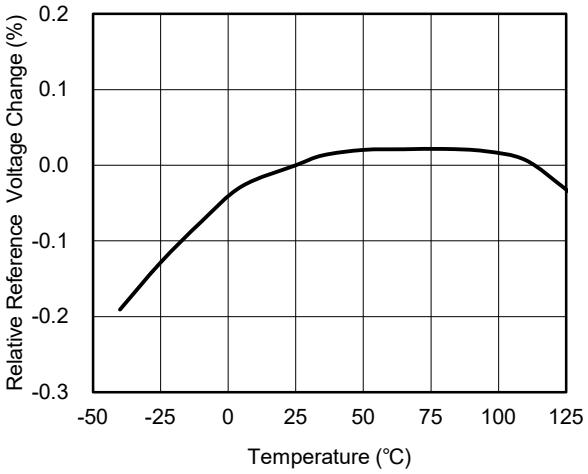
ELECTRICAL CHARACTERISTICS (continued)

(V_{VDD} = 12V, T_J = -40℃ to +85℃, all parameters at zero power dissipation, typical values are measured at T_J = +25℃, unless otherwise noted.)

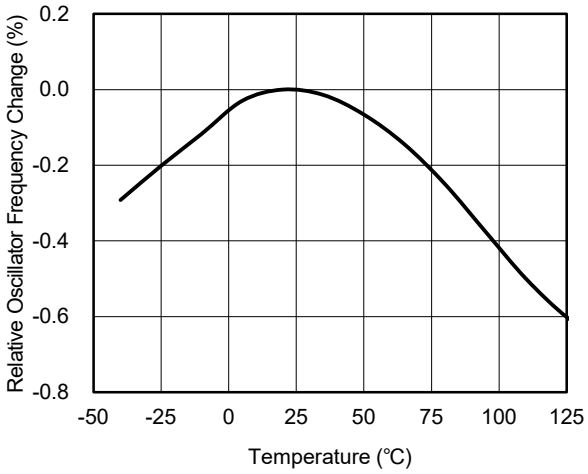
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Short-Circuit Protection						
Minimum Pulse during Short-Circuit	t_{PSS_MIN}			130		ns
Blanking Time	t_{BLNK}		60	105	140	ns
Off-Time between Restart Attempts	t_{OFF}		30	55		ms
Short-Circuit Comparator Threshold Voltage	V_{ILIM}	R_{COMP_GND} = open, T_J = +25℃	160	200	240	mV
		R_{COMP_GND} = 4kΩ, T_J = +25℃	80	100	120	
		R_{COMP_GND} = 12kΩ, T_J = +25℃	228	280	342	
Short-Circuit Threshold Voltage on High-side MOSFET	V_{ILIMH}	T_J = +25℃	400	550	650	mV
Output Drivers						
High-side Driver Pull-up Resistance	R_{HDHI}	V_{BOOT} - V_{SW} = 4.5V, I_{HDRV} = -100mA		3	6	Ω
High-side Driver Pull-down Resistance	R_{HDLO}	V_{BOOT} - V_{SW} = 4.5V, I_{HDRV} = 100mA		1.3	3	Ω
Low-side Driver Pull-up Resistance	R_{LDHI}	I_{LDRV} = -100mA		2.4	5	Ω
Low-side Driver Pull-down Resistance	R_{LDLO}	I_{LDRV} = 100mA		0.9	1.5	Ω
High-side Driver Rise Time	t_{HRISE}	C_{LOAD} = 1nF		10	35	ns
High-side Driver Fall Time	t_{HFALL}	C_{LOAD} = 1nF		9	25	ns
Low-side Driver Rise Time	t_{LRISE}	C_{LOAD} = 1nF		10	35	ns
Low-side Driver Fall Time	t_{LFALL}	C_{LOAD} = 1nF		8	25	ns
UVLO						
Turn-On Voltage	V_{UVLO}		3.9	4.3	4.4	V
Hysteresis	$U_{VLOHYST}$		700	800	900	mV
Shutdown						
High-Level Input Voltage, ENABLE	V_{IH}		2.4			V
Low-Level Input Voltage, ENABLE	V_{IL}				0.5	V
Power Good						
Feedback Voltage Limit for Power Good	V_{OV}			650		mV
Feedback Voltage Limit for Power Good	V_{UV}			523		mV
Power Good Hysteresis Voltage at FB Pin	V_{PG_HYST}			25		mV
Pull-Down Resistance of PGD Pin	R_{PGD}	V_{FB} = 0V		22	50	Ω
Leakage Current	I_{PDGLK}	V_{FB} = 0V		7	12	μA
BOOT Switch						
Bootstrap Switch Voltage Drop	V_{DFWD}	I_{BOOT} = 5mA		0.03		V
Thermal Shutdown						
Junction Shutdown Temperature	T_{JSD}			145		℃
Hysteresis	T_{JSDH}			20		℃

TYPICAL PERFORMANCE CHARACTERISTICS

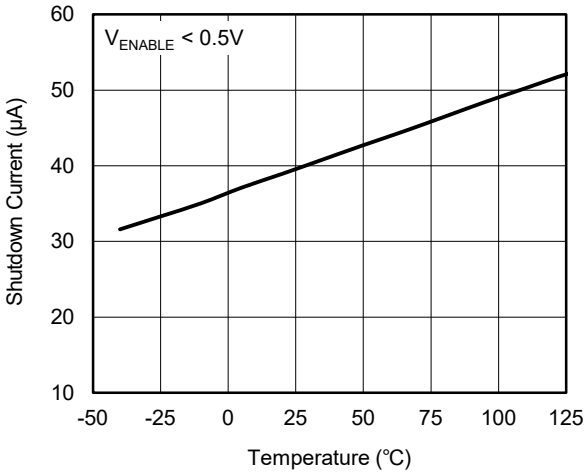
Relative Reference Voltage Change vs. Temperature



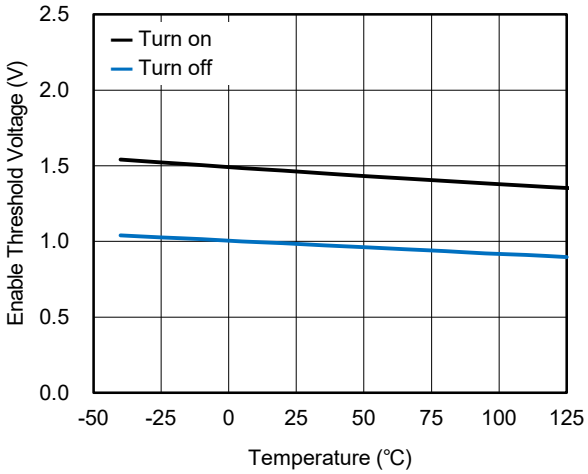
Relative Oscillator Frequency Change vs. Temperature



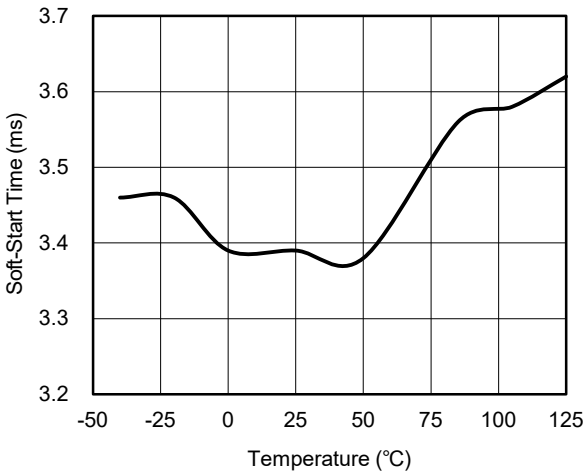
Shutdown Current vs. Temperature



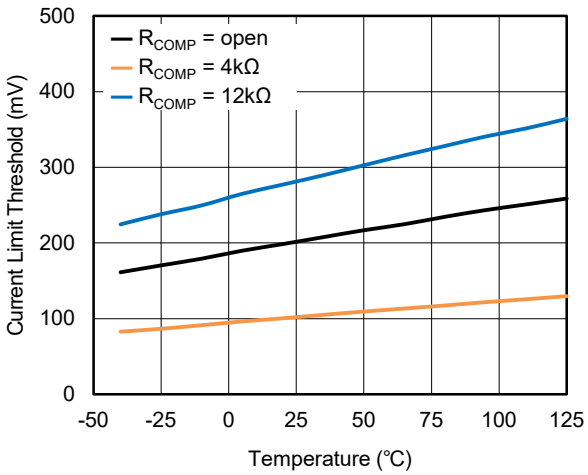
Enable Threshold Voltage vs. Temperature



Soft-Start Time vs. Temperature

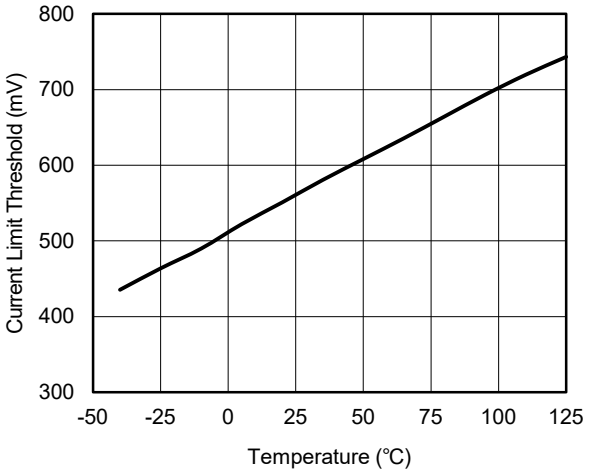


Low-side MOSFET Current Limit Threshold vs. Temperature

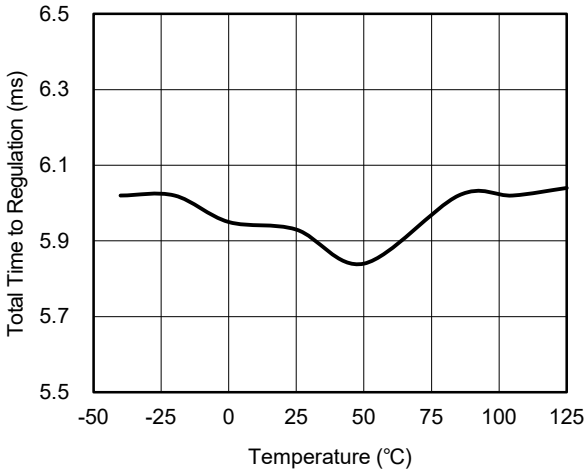


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

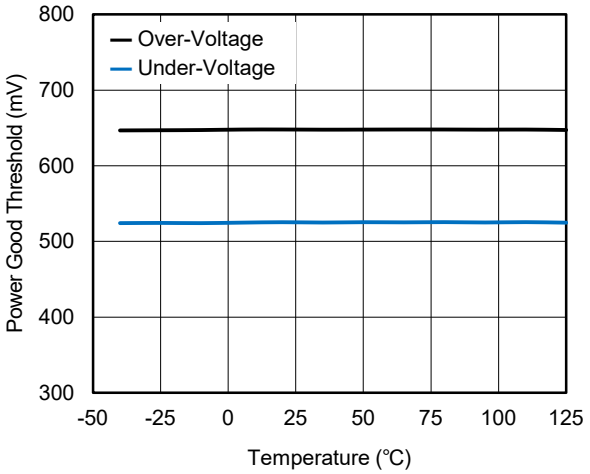
High-side MOSFET Current Limit Threshold vs. Temperature



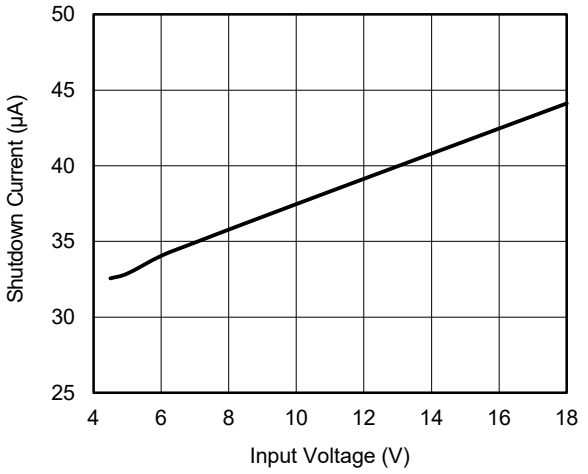
Total Time to Regulation vs. Temperature



Power Good Threshold Voltage vs. Temperature



Shutdown Current vs. Input Voltage



FUNCTIONAL BLOCK DIAGRAM

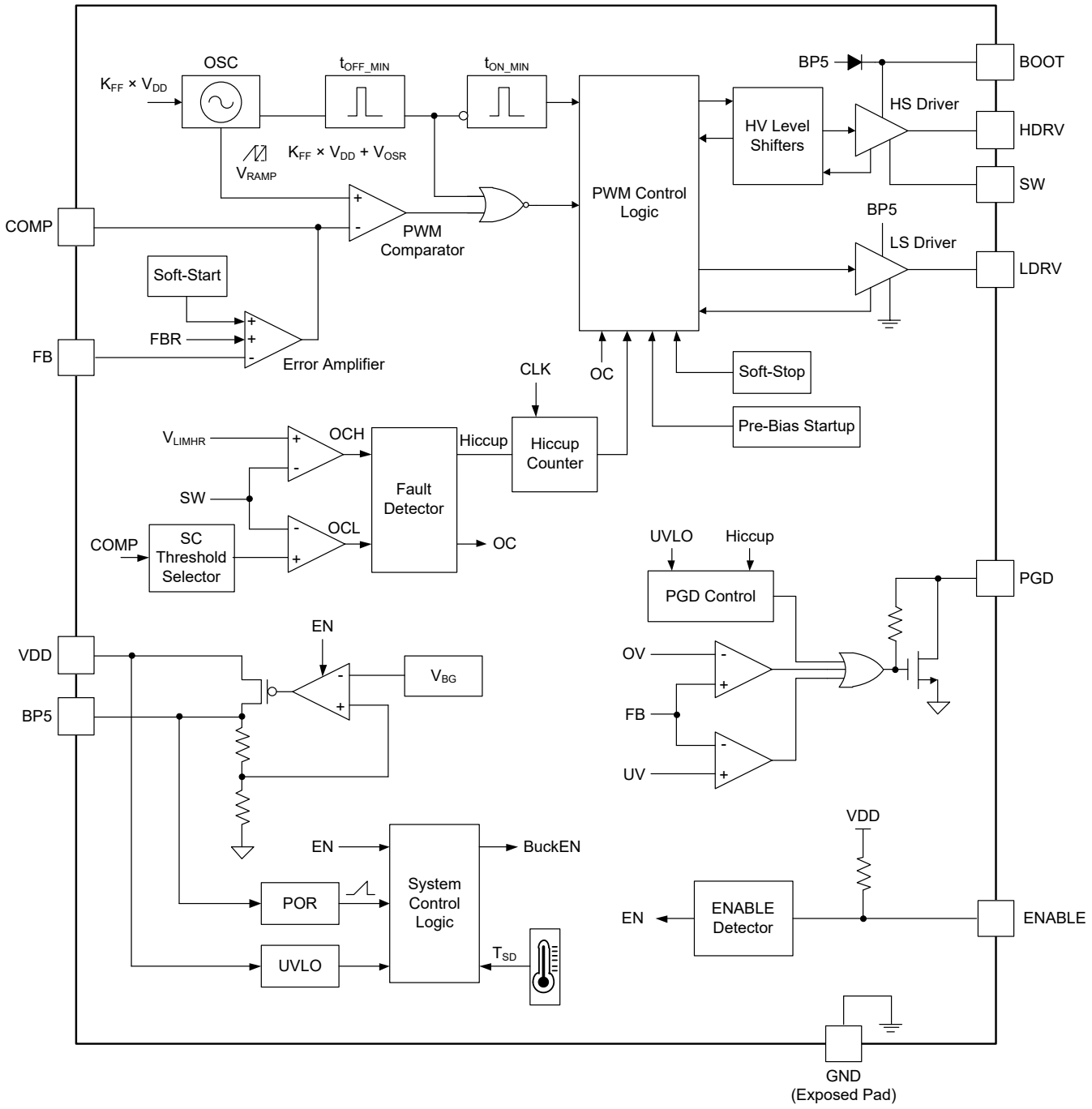


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM64104 is a cost-saving and complete feature choice for controlling a high-performance DC/DC converter. The feature of pre-bias startup can provide effective protection for the load sensitive to the input voltage. Powerful driving capacity can reduce the switching loss of high-side and low-side NMOS to increase efficiency. An anti-cross-conduction circuit has an internal minimum dead time. Also, the device will sense HDRV voltage to determine when HDRV driver is OFF and then it will turn on LDRV driver to prevent anti-cross-conduction. Similarly, device will sense LDRV voltage to determine when LDRV driver is OFF and then it will turn on HDRV driver.

Selectable low-side short-circuit protection threshold can increase design flexibility and reduce the power loss in prolonged short-circuit or overload faults. ENABLE pin can ensure that the device can be placed in a low quiescent current during shutdown mode. Internal fixed clock, switching frequency and fixed soft-start time can reduce the number of external components, simplify design and layout. And the 3mm × 3mm package reduces the overall converter footprint.

Voltage Reference

The 591mV trimmed reference is connected to the positive input end of the amplifier. The reference voltage with a tolerance of 0.5% (TYP) allows the customer to design a very precise power supply.

Control Strategy

Voltage-Mode Control

The SGM64104 is a synchronous controller implementing voltage-mode control architecture with the switching frequency fixed at either 600kHz (SGM64104A) or 300kHz (SGM64104B). The COMP pin is convenient for compensation loop design. The design flexibility allows DC/DC converter to satisfy various applications.

Input Voltage Feed-forward

By adding voltage feed-forward, The SGM64104 keeps the power stage gain constant when the input voltage changes, and has a fast response to line transition. At the same time, the simple power stage also simplifies the compensation network design. In order to accurately modeling, the front-end gain from COMP to the average voltage of SW, that is, the average input voltage of the L-C filter, is 12V/V.

Input Under-Voltage Lockout (UVLO)

When the VDD pin voltage is below the UVLO threshold, all the driver signals are pulled down to OFF state. Conversely, when the VDD pin voltage rises above the UVLO threshold and the chip is enabled, the internal oscillator works and enable the startup sequence. The internal UVLO threshold is fixed at 4.3V.

Enable Functionality

ENABLE pin simplifies the front-end interface design and also ensures the device can be placed in a low quiescent current during shutdown mode. When the ENABLE pin voltage is below the threshold voltage (0.6V), the device shuts off all unnecessary circuits including internal BP5 regulator to reduce the VDD quiescent current to 39μA (TYP).

The chip can start automatically even ENABLE pin is floating due to the internal pull-up resistor. Note that the impedance of ENABLE pin is relatively high. Special care should be taken to avoid nearby noisy circuits to cause ENABLE pin to swing below 600mV and falsely shut down the device. The following is the two suggestions to solve this problem:

1. Place a decoupling capacitance between ENABLE and GND to remove high-frequency noise. Note that the decoupling capacitance may cause a time-delay of the externally enable and disable signal.

2. Place a resistor between VDD and ENABLE. Although this causes more operating current in the shutdown mode, but avoids the time-delay.

Startup and Shutdown

Startup Sequence

When V_{DD} falls below UVLO threshold or ENABLE is low, the converter is turned off, and when V_{DD} rises above UVLO threshold as well as ENABLE is floating or pulled up, the BP5 regulator comes up. Once the BP5 regulator voltage is stable, the chip can determine the low-side short-circuit threshold by sampling the impedance of the COMP pin within 1ms. During this 1ms, the COMP voltage is maintained at 400mV, and the chip determines the corresponding threshold by measuring the current sourcing from the COMP pin. After this, the COMP pin is pulled low for another 1ms to make the compensation network zeroed, which avoids the sudden rise of the output voltage when the converter is allowed to start up.

DETAILED DESCRIPTION (continued)

After these initial 2ms, the device is allowed to soft-start. ENABLE, VDD UVLO, Fault and Thermal Shutdown will trigger the soft-start sequence.

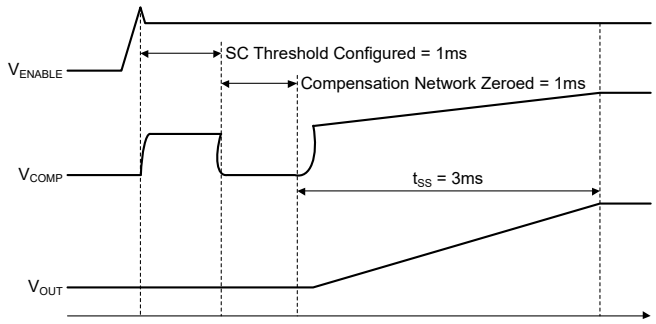


Figure 3. Startup Sequence and SC Threshold Calibration

Pre-Bias Startup

The SGM64104 supports pre-biased startup. During soft-start, it does not generate any PWM pulse until internal soft-start exceeds the FB voltage. Once internal soft-start exceeds the FB voltage, PWM pulses are initiated with very short on-time of synchronous rectifier. The on-time is then gradually increased cycle after cycle to meet the duration determined by (1-D)/f_{SW} within 32 clock cycles where D is the duty cycle. This scheme can prevent sinking of current from the pre-biased output, and support a smooth and controllable ramping of output voltage.

During a soft-start sequence, pulse skipping may occur when the PWM pulse width is shorter than the minimum controllable on-time.

Soft-Stop

When the controller is commanded to turn the converter off or enter hiccup restart, HDRV will be turned off and LDRV will stay on for an extra 3.5μs soft-stop time.

Short-Circuit and Over-Current Protection

The chip determines the short-circuit protection by detecting the voltage drop across the high-side and low-side MOSFETs. If any voltage drops exceed their corresponding short-circuit threshold voltages during a cycle, counter increments by one count. If the voltage drop on the high-side MOSFET exceeds the high-side short-circuit threshold, the MOSFET will be turned off immediately. If the voltage drop on the low-side MOSFET exceeds the low-side short-circuit threshold, the MOSFET will stay on until the voltage drop is below the threshold. For every switching cycle, if the voltage drop across both MOSFETs are lower than the corresponding short-circuit threshold voltages, the counter decreases by one count. If the counter reaches its maximum value of 7, fault signal will be triggered, prompting the gate drivers to disable the MOSFETs.

When a 55ms timeout expires, the chip attempts to restart. If the short-circuit condition still exists, the current will rise quickly to the short-circuit threshold and a fault declaration will occur again, and the controller will be off and wait for 55ms timeout to restart.

Low-side Short-Circuit Protection

The SGM64104 provides three selectable short-circuit thresholds for the low-side MOSFET. The specific method of selecting the threshold is to place a resistor between the COMP and GND. The relationship between the different resistance and the corresponding threshold is shown in Table 1. It needs 1ms to determine the SC threshold as shown in Figure 4, so a high impedance compensation network with short network time constant is preferred.

Specifically, the time constant and impedance of the compensation network between COMP and FB need to meet the Equation 1, so that the short-circuit threshold setting is not affected by the compensation network.

$$\frac{0.4V}{R_1} \times e^{\left(\frac{-t}{R_1 \times C_1}\right)} < 10\mu A \quad (1)$$

Where t = 1ms, SC threshold configuration time, R_1 and C_1 are the values of the components in Figure 4.

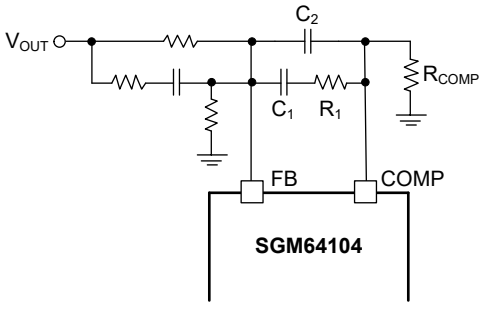


Figure 4. Short-Circuit Threshold Feedback Network

DETAILED DESCRIPTION (continued)

Table 1. Short-Circuit Threshold Voltage Selection

R_{COMP} (kΩ)	V_{ILIM} (V)
12 ± 10%	280
Open	200
4 ± 10%	100

The short-circuit current thresholds can be calculated as

$$I_{SCP} = \frac{V_{ILIM}}{R_{DS(ON)}} \quad (2)$$

Where
I_{SCP} = Short-circuit current threshold
V_{ILIM} = Selected low-side short-circuit threshold
$R_{DS(ON)}$ = On-resistance of low-side MOSFET

When over-current is detected in the low-side MOSFET, the low-side MOSFET will continue to conduct until the flowing current is below the threshold. Specifically, when the next clock arrives but the current flowing through the low-side MOSFET is still above the threshold, the high-side MOSFET will not conduct and the low-side MOSFET will continue to conduct.

Considering the Blanking time, the accuracy of the short-circuit current threshold may fall off when the duty cycle is relatively large. Specifically, the over-current comparator has only a short time to sample the voltage of the SW pin. Therefore, the comparator may have no time to respond to the situation where the current is close to the SC threshold.

High-side Short-Circuit Protection

The high-side short-circuit threshold is fixed at 550mV typical, 400mV minimum. This threshold determines the limitation of the peak current cycle by cycle. When the voltage drop on the high-side MOSFET exceeds the threshold, the high-side MOSFET is immediately turned off. The minimum value of the high-side short-circuit current threshold can be obtained by

$$I_{OUT\_MAX} = \frac{V_{ILIM\_MIN}}{R_{DS(ON)\_MAX}} \quad (3)$$

where
I_{OUT_MAX} = Maximum sourcing current of the converter
V_{ILIM_MIN} = Minimum short-circuit threshold of high-side MOSFET (400mV)
$R_{DS(ON)\_MAX}$ = Maximum on-resistance of high-side MOSFET

When over-current is detected in the high-side MOSFET, the high-side MOSFET will turn off immediately. In other words, the peak current of the inductor will not exceed the over-current threshold of the high-side MOSFET.

If the required current is greater than the calculated I_{OUT_MAX}, a high-side MOSFET with a lower on-resistance is required. Both high-side and low-side short-circuit thresholds have temperature compensation characteristics to approximate the rising of the external power MOSFET on-resistance when temperature increases. In order to effectively use the feature, the power MOSFET and the device should be well coupled thermally.

Integrated 5V Voltage Regulator

An on board 5V regulator is provided from the single input power supply to simplify the auxiliary supply circuit. A ceramic capacitor larger than 1μF is required to ensure the stability of the regulator. It should be noted that although the BP5 regulator can be used for the external load, the regulator is also the power supply of the internal circuit of the chip. The noise on the regulator may adversely affect the internal circuitry, which may lead to increased pulse jitter, or skewed reference voltage. In addition, when the device is shut down with the EN pulled low, the regulator is also turned off.

The limitation of the regulator output current is 50mA. The chip consumes up to 4mA, and the remaining part needs to be applied to the driver and external load. So that the amount of current applied on the external load varies with the size of the power MOSFETs which are driven by the drivers. MOSFETs with bigger size require more power, which lead to the reduced power for other loads. The total gate drive current can be calculated as:

$$I_G = f_{SW} \times (Q_{G\_HS} + Q_{G\_LS}) \quad (4)$$

where
I_G = Total gate drive current
f_{sw} = Switching frequency
Q_{G_HS} = High-side MOSFET gate charge
Q_{G_LS} = Low-side MOSFET gate charge

As mentioned above, at least a 1μF capacitor place between BP5 and GND can ensure the stable output. A larger capacitor can suppress the noise caused by the higher gate charge. If the total gate charge of both the high and low-side MOSFETs is greater than 20nC, it is suggested to place a 2.2μF or larger capacitor.

DETAILED DESCRIPTION (continued)

HDRV and LDRV Drivers

Both the HDRV and LDRV drivers are able to drive a 5V gate-to-source voltage powered by BP5 regulator. An anti-cross-conduction circuit has an internal minimum dead time. Also, the device will sense HDRV voltage to determine when HDRV driver is OFF and then it will turn on LDRV driver to prevent anti-cross-conduction. Similarly, device will sense LDRV voltage to determine when LDRV driver is OFF and then it will turn on HDRV driver.

Power Good Indicator

The SGM64104 implements a PGD indicator. This pin is an open-drain output, and the PGD pin is pulled low under the abnormal conditions where the output is out of regulation. These conditions include:

- ENABLE is low.
- V_{FB} is not within ±10% from nominal.
- Soft-start is active.
- Under-voltage condition exists for the device.
- Short-circuit condition has been declared.
- Die temperature is over +145℃.

Note that when no power supply connected to the device and an auxiliary supply applied on the PGD, PGD is not able to pull the indication signal down. In this case, a built-in resistor placed between drain and gate of the pull-down MOSFET makes the PGD pin look approximately like a diode to GND.

Thermal Shutdown

When the junction temperature of the device reaches the thermal shutdown threshold of +145℃, PWM and oscillator shut off, and high-side and low-side drivers also shut off. The device recovers to a hysteresis value of approximately 20℃, that is, PWM begins soft-start when the device cools down to +125℃.

Device Functional Modes

Continuous Conduction Mode

The SGM64104A and SGM64104B devices are in continuous conduction mode operation, which means the conduction time of the high-side MOSFET is completely complementary to the low-side MOSFET. An exception is that during the pre-bias startup, the on-time of low-side MOSFET is gradually increased cycle after cycle to meet the duration determined by $(1-D)/f_{SW}$ within 32 clock cycles.

Low-Quiescent Shutdown

When the ENABLE pin voltage is below the threshold voltage (0.6V), the device shuts off all unnecessary circuits including internal BP5 regulator to reduce the device operating current to 39μA.

APPLICATION INFORMATION

In this application, SGM64104A is the controller of a 12V to 1.8V synchronous step-down converter. The design procedure and configuration process are shown in this section.

Typical Application

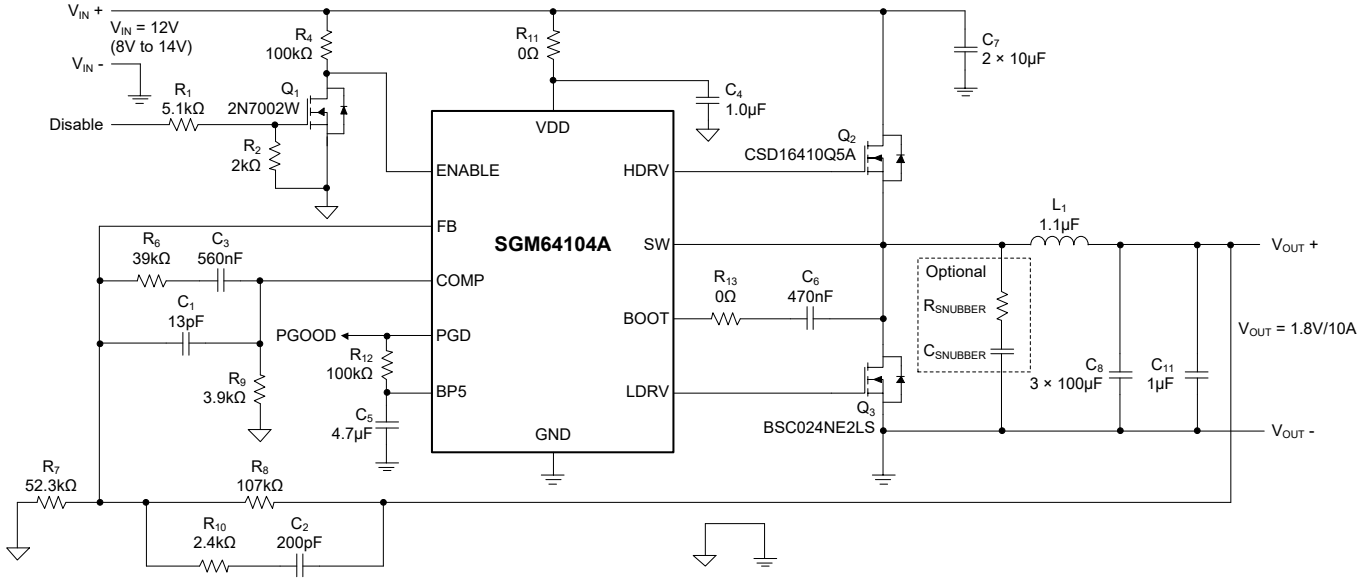


Figure 5. SGM64104A Typical Application Design Example

Table 2 below shows the detailed design requirements of this application.

Table 2. Design Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics						
Input Voltage	V_{IN}		8	12	14	V
Input Current	I_{IN}	V_{IN} = 8V, I_{OUT} = 10A		2.7	2.85	A
No Load Input Current		V_{IN} = 8V, I_{OUT} = 0A		48	60	mA
Input UVLO	V_{IN_UVLO}	I_{OUT} = 0A to 10A	3.9	4.3	4.4	V
Output Characteristics						
Output Voltage	V_{OUT}	V_{IN} = 12V, I_{OUT} = 6A		1.8		V
Line Regulation		V_{IN} = 8V to 14V, I_{OUT} = 6A			0.5	%
Load Regulation		V_{IN} = 12V, I_{OUT} = 0A to 10A			0.5	%
Output Voltage Ripple	V_{OUT_RIPPLE}	V_{IN} = 12V, I_{OUT} = 10A			40	mVpp
Output Current	I_{OUT}	V_{IN} = 8V to 14V	0	6	10	A
Output Over-Current Inception Point	I_{OCP}	V_{IN} = 12V, V_{OUT} = V_{OUT} - 5%		19		A
Transient Response						
Load Step	ΔI	0.75 × I_{OUT_MAX} to 0.25 × I_{OUT_MAX}		5		A
Load Slew Rate				5		A/μs
Overshoot					50	mV
Systems Characteristics						
Switching Frequency	f_{SW}		480	600	720	kHz
Peak Efficiency	η_{PK}	V_{IN} = 8V, I_{OUT} = 0A to 10A		89		%
Full-Load Efficiency	η	V_{IN} = 8V, I_{OUT} ≤ 10A		86		%
Operating Temperature Range	T_J	V_{IN} = 8V to 14V, I_{OUT} = 0A to 10A	-40	+25	+60	℃

APPLICATION INFORMATION (continued)

Switching Frequency Selection

SGM64104A with 600kHz switching frequency is chosen as the trade off between efficiency and size of passive components.

Inductor Selection

The selection of synchronous Buck inductor is usually based on the design criteria of 20% to 40% of the inductance current ripple. At the maximum load current, the inductance can be obtained by Equation 5.

$$L_1 \approx \frac{V_{IN\_MAX} - V_{OUT}}{0.3 \times I_{OUT\_MAX}} \times \frac{V_{OUT1}}{V_{IN\_MAX}} \times \frac{1}{f_{SW}} = \frac{14V - 1.8V}{0.3 \times 10A} \times \frac{1.8V}{14V} \times \frac{1}{600kHz} = 0.871\mu H \quad (5)$$

Select a standard 1.1μH inductance, and the ripple current I_{RIPPLE} = 2.38A.

The RMS current through the inductor is calculated by Equation 6.

$$L_{1\_RMS} = \sqrt{(I_{OUT\_MAX})^2 + \frac{(I_{RIPPLE})^2}{12}} = \sqrt{(10A)^2 + \frac{(2.38A)^2}{12}} \approx 10.02A \quad (6)$$

Using Equation 6, the maximum RMS current in the inductor is approximately 10.02A.

Input Capacitor Selection (C_7)

The input current provided by the input capacitor is discontinuous, therefore the input capacitor need to supply the AC current and keep the DC input voltage stable. It is highly recommended to use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. A enough ripple current rating is required to make the input capacitor be able to absorb the discontinuous input current. The RMS current of the input capacitor can be calculated as:

$$I_{C1\_RMS} = L_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (7)$$

The worst case is that V_{IN} = 2 × V_{OUT}, where

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (8)$$

So it is simple and safe to choose an input capacitor with the RMS current greater than half of the maximum load current.

Another factor of choosing the input capacitor is to avoid the excessive input voltage ripple caused by the switching current. The capacitance can be obtained as

$$C_{IN} \geq \frac{I_{LOAD}}{f_{SW} \times V_{IN\_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

Two ceramic capacitors of type 1210, rated at 10μF, 25V, with X5R dielectric, approximately 2mΩ ESR, and a 2A RMS current rating are chosen. Using capacitors with a higher voltage rating helps reduce capacitance reduction under DC bias, ensuring adequate capacitance at the operating voltage.

Output Capacitor Selection (C_8)

The selection of output capacitance needs to consider the transient response. Equations 10 and 11 leave a margin when estimating the voltage deviation, so as to consider the response delay in the loop, and thus determine the output capacitance:

$$V_{OVER} < \frac{\Delta I_{OUT}}{C_{OUT}} \times \Delta t = \frac{\Delta I_{OUT}}{C_{OUT}} \times \frac{\Delta I_{OUT} \times L}{V_{OUT}} = \frac{(\Delta I_{OUT})^2 \times L}{V_{OUT} \times C_{OUT}} \quad (10)$$

$$V_{UNDER} < \frac{\Delta I_{OUT}}{C_{OUT}} \times \Delta t = \frac{\Delta I_{OUT}}{C_{OUT}} \times \frac{\Delta I_{OUT} \times L1}{V_{IN} - V_{OUT}} = \frac{(\Delta I_{OUT})^2 \times L}{(V_{IN} - V_{OUT}) \times C_{OUT}} \quad (11)$$

When V_{IN_MIN} > 2 × V_{OUT1}, use Equation 10 to calculate the minimum output capacitance. When V_{IN_MIN} < 2 × V_{OUT1}, calculate the value using Equation 11. In this design example, the V_{IN_MIN} is much larger than 2 × V_{OUT1}, so Equation 12 is used for calculation.

$$C_{OUT\_MIN} = \frac{(\Delta I_{OUT})^2 \times L}{V_{OUT} \times V_{OVER}} = \frac{5^2 \times 1.1\mu H}{1.8 \times 50mV} = 305.8\mu F \quad (12)$$

When the capacitance is minimum value, the maximum ESR is determined by the maximum ripple, as shown in Equation 13.

APPLICATION INFORMATION (continued)

$$C_{ESR\_MAX} = \frac{V_{RIPPLE} - V_{RIPPLE\_CAP}}{I_{RIPPLE}} = \frac{V_{RIPPLE} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT1} \times f_{SW}}\right)}{I_{RIPPLE}} = \frac{40mV - \left(\frac{2.38A}{8 \times 305.8\mu F \times 600kHz}\right)}{2.38A} = 16.8m\Omega \quad (13)$$

Three 1206 100μF, 6.3V X5R ceramic capacitors are selected according to the requirements of ripple and output response. In addition, two 0805 10μF and one 0603 1μF ceramic capacitors are selected to filter high-frequency noise.

Peak Current Rating of the Inductor

Equations 14 and 15 are used to calculate the charging current at startup and the current peak value of the inductor, respectively, to determine the minimum saturation current of the inductor.

$$I_{CHARGE} = \frac{V_{OUT} \times C_{OUT}}{t_{ss}} = \frac{1.8V \times 320\mu F}{3ms} = 192mA \quad (14)$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{I_{RIPPLE}}{2} + I_{CHARGE} = 10A + \frac{2.38A}{2} + 192mA = 11.382A \quad (15)$$

Table 3. Inductor Parameters

PARAMETER	SYMBOL	VALUE	UNITS
Inductance	L	1	μH
RMS Current (Thermal Rating)	I_{L_RMS}	10.02	A
Peak Current (Saturation Rating)	I_{L_PEAK}	11.382	A

Wurth744314110 inductance is selected, and the inductance is 1.1μH. Under 10A load current, the inductance value drops to about 0.88μH. The DCR is 3.15mΩ and the size is 7mm × 7mm.

Short-Circuit Threshold Selection (R_9)

Since the output over-current inception point (I_{OCP}) is set to 19A, the high and low-side short-circuit current threshold can be obtained by Equations 16 and 17.

$$I_{PEAK\_TH} \geq I_{OCP} + \frac{I_{RIPPLE}}{2} = 19A + \frac{2.38A}{2} = 20.19A \quad (16)$$

$$I_{VALLEY\_TH} \geq I_{OCP} - \frac{I_{RIPPLE}}{2} = 19A - \frac{2.38A}{2} = 17.81A \quad (17)$$

For this design, the high-side short-circuit current threshold is set to 40A, and the low-side short-circuit current threshold is set to 25A.

For the efficiency matters in this design and V_{IN} is much larger than V_{OUT}, a low on-resistance low-side MOSFET and a low gate charge high-side MOSFET are required. Therefore, a lower short-circuit voltage threshold (100mV) should be selected by selecting R_9 = 3.9kΩ.

MOSFET Switch Selection (Q_1, Q_2)

High-side short-circuit current threshold determines the choice of on-resistance of low-side MOSFET, and low-side short-circuit voltage and current thresholds determine the choice of on-resistance of low-side MOSFET. Considering the requirement of high efficiency, it is more effective to reduce the conduction losses rather than the switching losses for the low-side MOSFET due to the conduction of the body diode. Therefore, the on-resistance of Q_1 and Q_2 can be calculated by Equations 18 and 19.

$$R_{DS(ON)\_Q1} = \frac{V_{PEAK\_TH}}{I_{PEAK\_TH}} = \frac{550mV}{40A} = 13.75m\Omega \quad (18)$$

$$R_{DS(ON)\_Q2} = \frac{V_{VALLEY\_TH}}{I_{VALLEY\_TH}} = \frac{100mV}{25A} = 4m\Omega \quad (19)$$

Table 4. Power MOSFET Parameters

PARAMETER	SYMBOL	VALUE	UNITS
High-side MOSFET on-resistance	$R_{DS(ON)\_Q1}$	13.75	mΩ
Low-side MOSFET on-resistance	$R_{DS(ON)\_Q2}$	4	mΩ

The CSD16410Q5A has an $R_{DS(ON)\_MAX}$ of 12mΩ at 4.5V gate drive and only 5nC of total gate charge with a 4.5V gate drive, and is chosen as a high-side MOSFET. The BSC024NE2LS has an $R_{DS(ON)\_MAX}$ of 3.4mΩ at 4.5V gate drive and 11nC of total gate charge. These two FETs have maximum total gate charges of 5nC and 11nC respectively, which draws 40.2mA from the 5V regulator, less than its 50mA minimum rating.

Boot Strap Capacitor

In order to drive high-side FET normally, the ripple of BST capacitor is limited to less than 25mV.

$$C_{BOOST} = \frac{Q_{G1}}{V_{BST\_RIPPLE}} = \frac{11nC}{25mV} = 440nF \approx 470nF \quad (20)$$

Use the standard value of 470nF or higher value for the bootstrap capacitor.

VDD Bypass Capacitor (C_6)

As shown in the Pin Configuration section, use a 1μF/0.1μF capacitor for VDD bypass.

APPLICATION INFORMATION (continued)

BP5 Bypass Capacitor (C_5)

To maintain stability of the 5V regulator, a minimum ceramic capacitance of 1μF is advised. Equation 21 is used to determine the appropriate bypass capacitor to keep the regulator noise below 10mV.

$$C_{BP5} = 100 \times MAX(Q_{G1}, Q_{G2}) = 100 \times MAX(5nC, 11nC) \cong 1.1\mu F \quad (21)$$

Since Q_2 has a greater gate charge than Q_1, with a total gate charge of 11nC, a BP5 capacitor value of 1.1μF is calculated. To further reduce noise on the BP5 regulator, the next standard capacitor value of 4.7μF is selected.

Input Voltage Filter Resistor (R_{11})

When the minimum input voltage V_{IN_MIN} is greater than 6V, select R_{11} = 0Ω. When V_{IN_MIN} < 6V, it is suggested to place an optional series VDD resistor with a value between 1Ω and 2Ω to filter switching noise from the device. Note that the voltage drop on this filter resistor should be less than 50mV.

$$R_{VDD} = \frac{V_{RVDD\_MAX}}{I_{DD}} = \frac{50mV}{3mA + (Q_{G1} + Q_{G2}) \times f_{sw}} = \frac{50mV}{3mA + (5nC + 11nC) \times 600kHz} = \frac{50mV}{12.6mA} \cong 4\Omega \quad (22)$$

Driving the two FETs with 5nC and 11nC respectively, the maximum I_{VDD} current calculation of 12.6mA yields a resistor value of approximately 2Ω.

Feedback Divider (R_7, R_8)

The SGM64104 uses an operational amplifier with an internal reference voltage of 591mV. The value of voltage divider is about 10kΩ to 100kΩ, which is a compromise between static current and noise resistance. The calculation formula is as follows.

$$R_7 = \frac{V_{FB} \times R_8}{V_{OUT1} - V_{FB}} \quad (23)$$

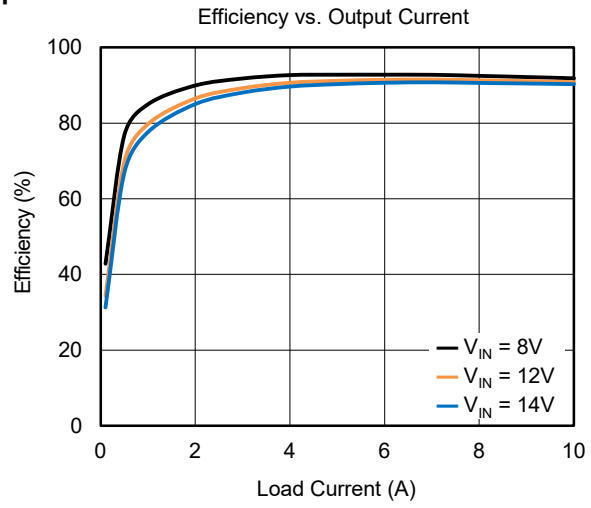
It is highly recommended to use to the SGM64104 calculation tool, which can select a most appropriate feedback divider in E96 Series to achieve a most accurate output voltage. As calculated by the calculation tool, R_7 = 52.3kΩ and R_8 = 107kΩ.

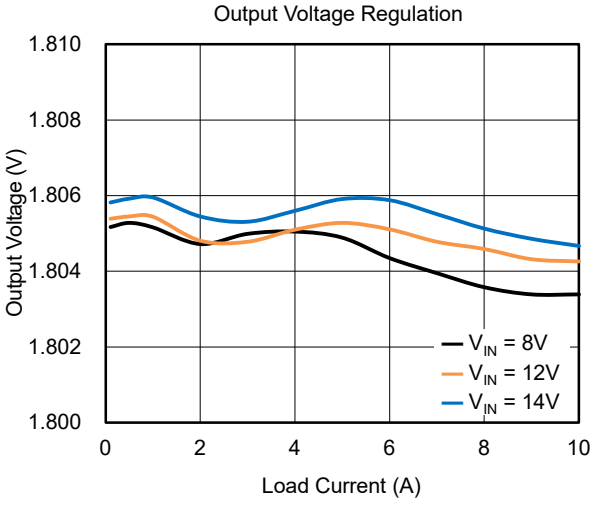
Error Amplifier Compensation (R_6, R_{10}, C_1, C_2, C_3)

The common method of designing the voltage-mode compensation network is to first model the power stage of the converter, and then use the Type-III compensator to compensate. It is effective to use the K-factor method or Zero-Pole placement method.

Using the SGM64104 loop calculation tool which uses the K-factor method, set the 50kHz bandwidth and 65° phase margin, measured the calculated results in the experimental values and modified the parameters to obtain the following values: C_1 = 13pF, C_2 = 200pF, C_3 = 560pF, R_6 = 39kΩ, R_{10} = 2.4kΩ.

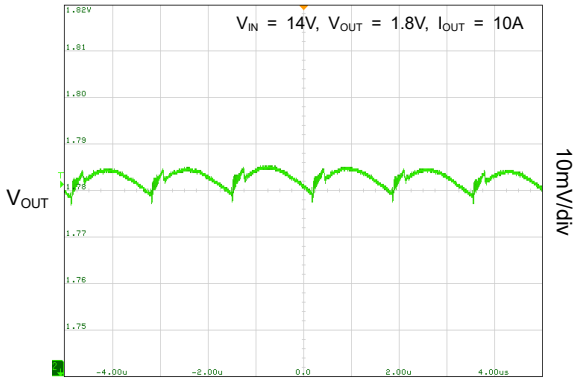
Application Curves





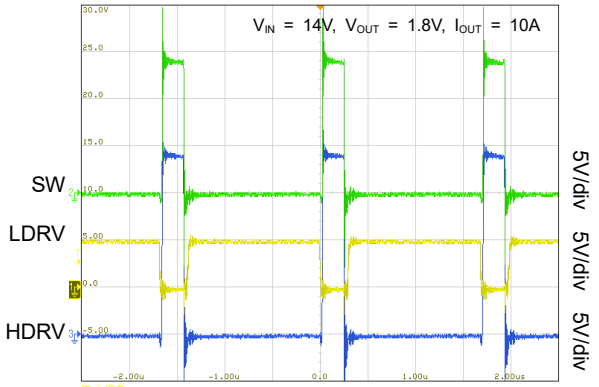
APPLICATION INFORMATION (continued)

Output Voltage Ripple



Time (1μs/div)

Switching Waveforms



Time (500ns/div)

Power Supply Recommendations

The SGM64104 requires a power source connected to the VDD pin, operating within a voltage range of 4.5V to 18V. To maintain reliable performance, the power supply should be stable and well-filtered. For accurate high-side current detection, the VDD pin must share the same power source as the input voltage of the power stage converter. The BP5 pin, which outputs from an internal low-dropout regulator supplying gate drive voltages, also needs effective local bypassing to support proper device functionality.

Layout Guidelines

Power Stage

The Buck power stage has two current loops. One of them is the input loop with high-frequency AC discontinuous current, and the other is the output loop with high-frequency continuous current. In order to make the input loop as small as possible, the input ceramic capacitor should be as close to the high and low-side MOSFETs as possible. Like the input loop, the output capacitor in the output loop also needs to be closer to the inductor and PGND to reduce the area of the output loop. The SW node needs to be very small to reduce the radiation area.

Device Peripheral

SGM64104 needs to distinguish signal ground (AGND) from power ground (PGND). It is necessary to correctly distinguish the grounding in the circuit. All the pins related to the power stage are connected to PGND, and other pins related to the signal stage (such as VDD, ENABLE, FB and COMP) are connected to AGND. Connect the signal ground island to the thermal pad using a single 10-mil-wide trace. Installing R_{11} as a VDD filter resistor is optional. Create an isolated and continuous analog ground island beneath the compensation network components, including C_1, C_2, C_3, R_6, R_7, R_8, R_9 and R_{10}, in order to suppress noise and interference. It is effective to locate several vias in thermal pad land for heat dissipation from the device.

APPLICATION INFORMATION (continued)

Layout Examples

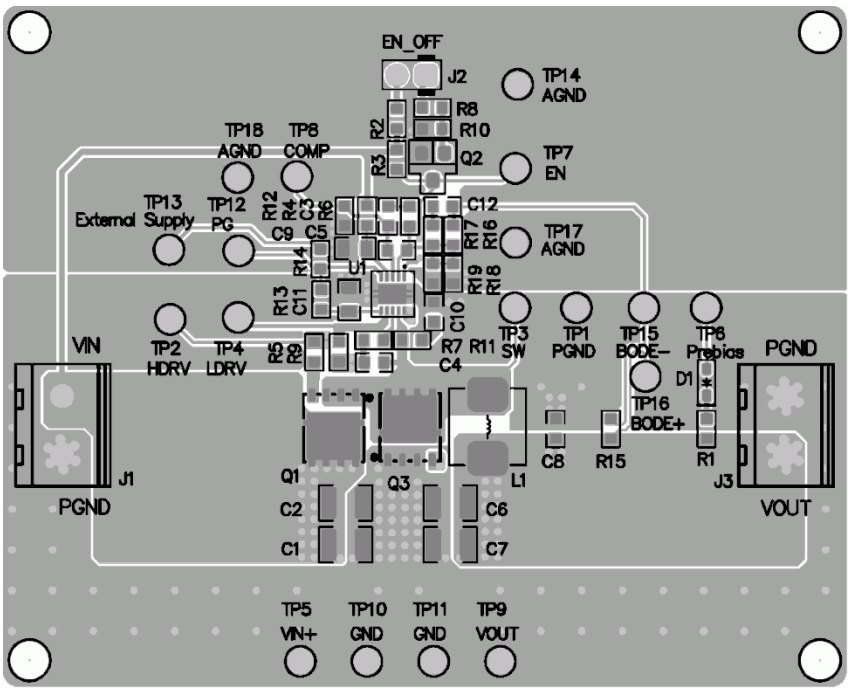


Figure 6. PCB Layout (Top Layer)

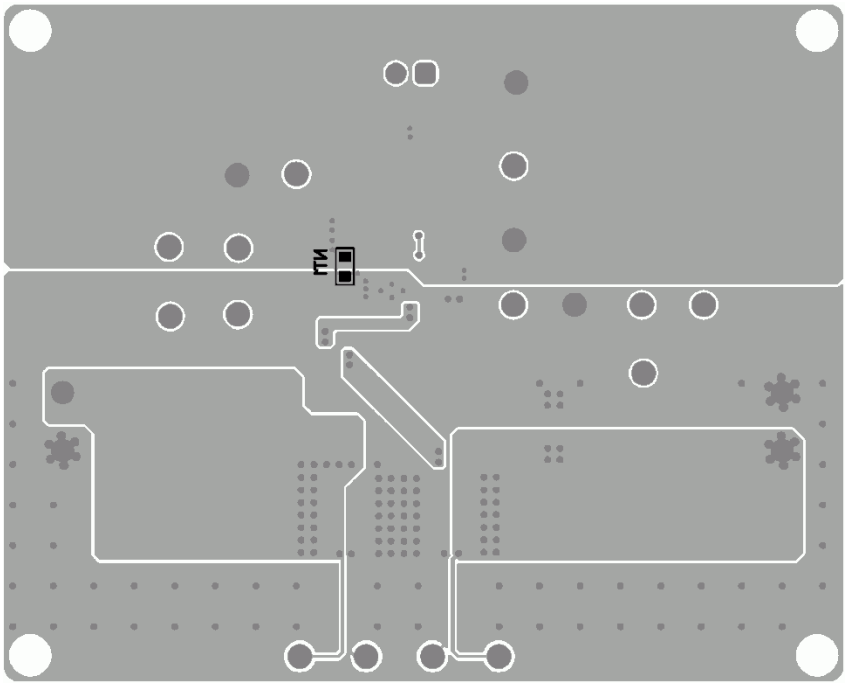


Figure 7. PCB Layout (Bottom Layer)

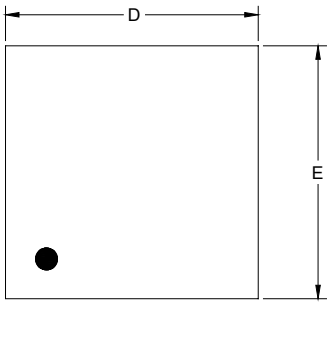
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

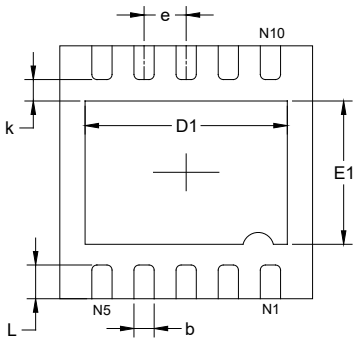
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

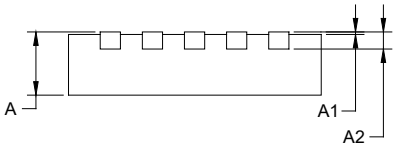
TDFN-3×3-10L



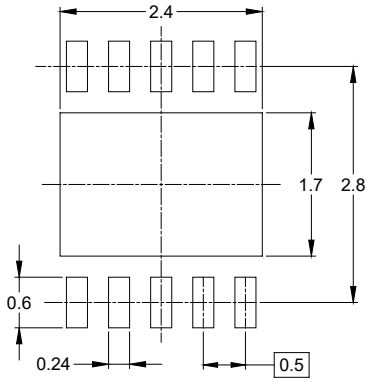
TOP VIEW



BOTTOM VIEW



SIDE VIEW



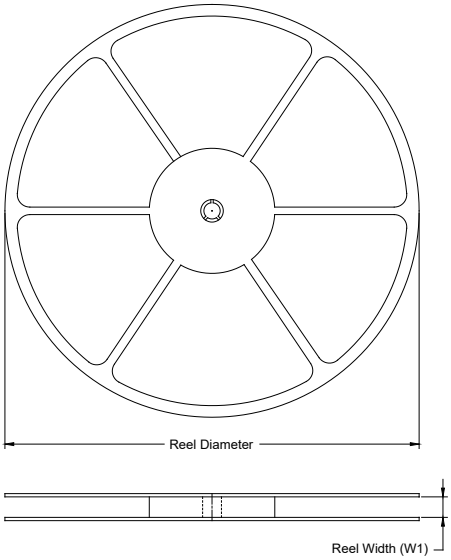
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

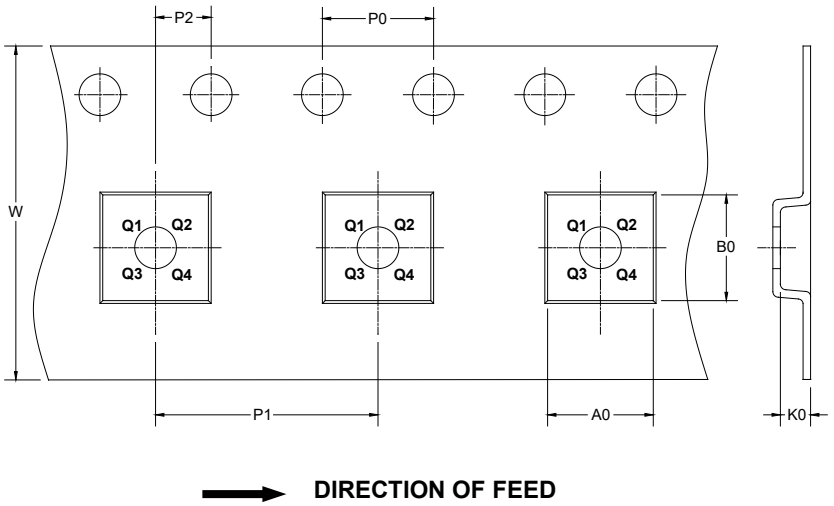
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



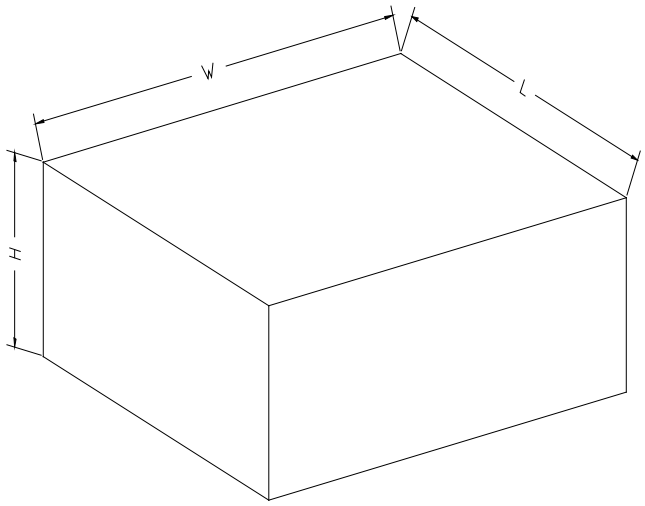
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-10L	13"	12.4	3.30	3.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002