SGM5102
14-Bit, 25MSPS, Low Power Dual Analog-to-Digital Converter Cores

GENERAL DESCRIPTION

The SGM5102 is a 14-bit, 2 channels simultaneous sampling pipeline analog-to-digital converter (ADC). Its good DC and AC performances are designed for low power high-speed control application.

It supports both oversampling and undersampling of IF frequencies.

The SGM5102 offers series LVDS interface. Each ADC channel output can be shifted out by 2-lane mode (2 bits at a time) or 1-lane mode (1 bit at a time). The LVDS drivers have internal optional termination resistors and they are turned off by default.

The SGM5102 supports either differential or single ended clock signal. Clock signals with PECL, TTL, CMOS or LVDS format can be provided to ENC+ and ENC- pins. The device has internal clock duty cycle stabilizer, which allows a wide range clock duty cycles and keeps high ADC performance at the same time.

The SGM5102 is available in a Green TQFN-6×6-40AL package. It operates over an ambient temperature range -40℃ to +125℃.

FEATURES

- **2-Channel Simultaneous Sampling**
- **INL: ±1.5LSB (TYP), DNL: ±0.6LSB (TYP)**
- **Typical SNR: 71dB (TYP)**
- **Typical SFDR: 93dB (TYP)**
- **Low Power:**
  - **128mW (TYP) Total**
  - **64mW per Channel**
- **Single Supply: 1.8V**
- **Digital Outputs: Serial LVDS with 1 or 2 Bits per Channel**
- **Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$**
- **Full Power Bandwidth S/H: 800MHz**
- **Sleep and Nap Modes**
- **Serial SPI Port for Configuration**
- **Available in a Green TQFN-6×6-40AL Package**

APPLICATIONS

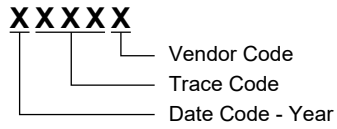
Security Monitoring Equipment
Communication Systems
Medical Imaging Systems
Testing and Measurement Instruments

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM5102	TQFN-6×6-40AL	-40℃ to +125℃	SGM5102XTSQ40G/TR	SGM5102 XTSQ40 XXXXX	Tape and Reel, 3000
			SGM5102XTSQ40SG/TR	SGM5102 XTSQ40 XXXXX	Tape and Reel, 250

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range
V_{DD}, OV_{DD} ..... -0.3V to 2V
Analog Input Voltage Range (2)
AIN+, AIN-, PAR/nSER, SENSE ..... -0.3V to (V_{DD} + 0.2V)
Digital Input Voltage Range (3)
ENC+, ENC-, CS, SDI, SCLK ..... -0.3V to 3.9V
SDO (3) ..... -0.3V to 3.9V
Digital Output Voltage Range..... -0.3V to (OV_{DD} + 0.3V)
Package Thermal Resistance
TQFN-6×6-40AL, θ_{JA}..... 26.8℃/W
TQFN-6×6-40AL, θ_{JB}..... 8.6℃/W
TQFN-6×6-40AL, $\theta_{JC\ (TOP)}$ ..... 15.6℃/W
TQFN-6×6-40AL, $\theta_{JC\ (BOT)}$ ..... 2.8℃/W
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....3000V
CDM 1000V

NOTES:

1. All voltage values are referenced to GND and assume that GND and OGND are shorted, unless otherwise stated.

2. Internal protection circuits help clamp these pin voltages when they are driven below GND or beyond V_{DD}. The device is designed to handle more than 100mA input currents below GND or beyond V_{DD} without the risk of latch-up.

3. Internal protection circuits help clamp these pin voltages when they are driven below GND. These pin voltages won't be clamped when these pin voltages are beyond V_{DD}. The device is designed to handle more than 100mA input currents below GND without the risk of latch-up.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

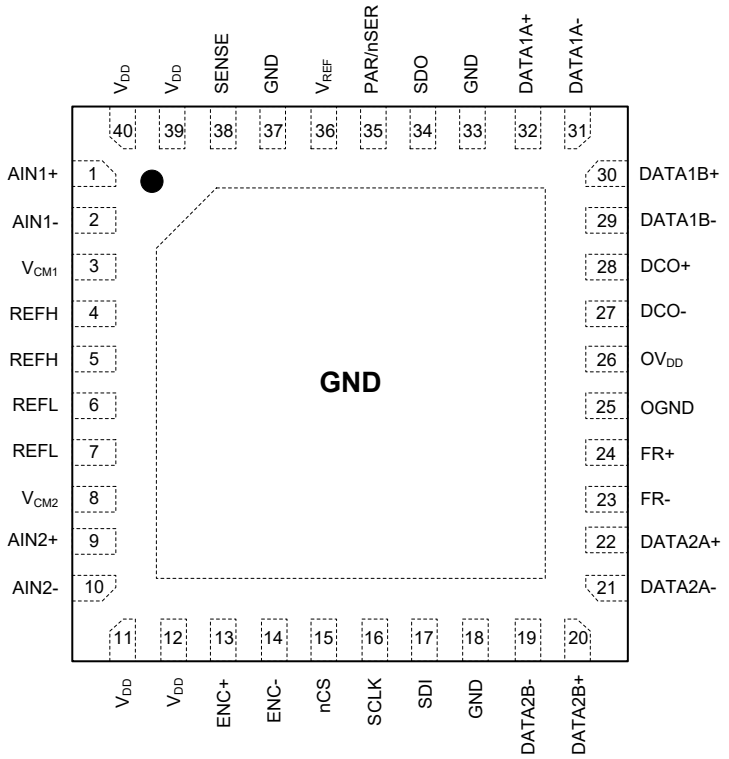
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-6×6-40AL

PIN DESCRIPTION

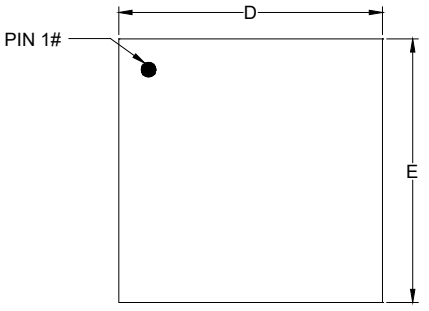
PIN	NAME	FUNCTION
1	AIN1+	Channel 1 Positive Differential Analog Input.
2	AIN1-	Channel 1 Negative Differential Analog Input.
3	V_{CM1}	Common Mode Bias Voltage Output, nominally equal to 0.85V. V_{CM1} is suggested to be used as the bias voltage of input channel 1. A 0.1μF bypass capacitor is suggested to connect between this pin and ground.
4, 5	REFH	ADC High Reference. At least a 2.2μF capacitor coupled with a 0.1μF capacitor is suggested to connect between REFH and REFL.
6, 7	REFL	ADC Low Reference. At least a 2.2μF capacitor coupled with a 0.1μF capacitor is suggested to connect between REFH and REFL.
8	V_{CM2}	Common Mode Bias Voltage Output, nominally equal to 0.85V. V_{CM2} is suggested to be used as the bias voltage of input channel 2. A 0.1μF bypass capacitor is suggested to connect between this pin and ground.
9	AIN2+	Channel 2 Positive Differential Analog Input.
10	AIN2-	Channel 2 Negative Differential Analog Input.
11, 12, 39, 40	V_{DD}	1.8V Analog Power Supply. A 0.1μF bypass ceramic capacitors is suggested to connect between this pin and Ground.
13	ENC+	Encode Positive Input. The input sample starts on the positive edge.
14	ENC-	Encode Negative Input. The input sample starts on the negative edge.
15	nCS	When PAR/nSER = 0V (The device works in serial programming mode.), nCS goes to logic low which means the data on SDI is being shifted into the mode control registers. When PAR/nSER = V_{DD} (The device works in parallel programming mode.), nCS is used to select 2-lane output mode or 1-lane output mode. nCS supports the driven voltage from 1.8V to 3.3V.

PIN DESCRIPTION (continued)

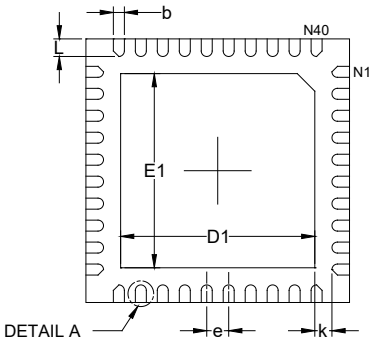
PIN	NAME	FUNCTION
16	SCLK	When PAR/nSER = 0V (The device works in serial programming mode.), SCLK is the serial interface clock input. When PAR/nSER = V_{DD} (The device works in parallel programming mode.), SCLK is used to select 3.5mA or 1.75mA LVDS output current. SCLK supports the driven voltage from 1.8V to 3.3V.
17	SDI	When PAR/nSER = 0V (The device works in serial programming mode.), SDI is the serial interface data input. Data is locked in at the rising edge of SCLK. When PAR/nSER = V_{DD} (The device works in parallel programming mode.), SDI is used to power down the part. SDI supports the driven voltage from 1.8V to 3.3V.
18, 33, 37	GND	ADC Power Ground.
19	DATA2B-	Serial LVDS Outputs for Channel 2. Only OUT2A-/OUT2A+ are used in 1-lane output mode. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
20	DATA2B+	
21	DATA2A-	
22	DATA2A+	
23	FR-	Frame Start Output. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
24	FR+	
25	OGND	Output Driver Ground. Connect directly to the ground plane. Multiple vias close to the pin in the layout is strongly recommended.
26	OV_{DD}	Output Driver Supply. A 0.1μF bypass ceramic capacitors is suggested to connect between this pin and Ground.
27	DCO-	Data Clock Output. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
28	DCO+	
29	DATA1B-	Serial LVDS Outputs for Channel 1. Only OUT1A-/OUT1A+ are used in 1-lane output mode. Note: These are differential LVDS output pins with programmable output current level. Also, an optional internal 100Ω termination resistor is provided between the pins of each LVDS output pair.
30	DATA1B+	
31	DATA1A-	
32	DATA1A+	
34	SDO	In serial programming mode (PAR/nSER = 0V), if SDO is used as data output pin, as SDO pin is an open-drain output, it must be pulled up to OV_{DD} by an external resistor (suggest 2kΩ). If data output is not needed, it can be left floated. In parallel programming mode (PAR/nSER = V_{DD}), SDO is an input which enables an internal 100Ω termination resistor on the pin connection, SDO can be driven through a 1kΩ series resistor from the interface logic.
35	PAR/nSER	Programming Mode Selection Pin. This pin must be connected to GND or V_{DD} directly. If this pin is connected to GND, nCS, SCLK, SDI and SDO are packaged to serial interface to configure ADC working mode. If this pin is connected to V_{DD}, nCS, SCLK, SDI and SDO are packaged as logic inputs to setting the ADC working mode.
36	V_{REF}	Reference Voltage Output. Voltage nominally 1.25V. A 1μF bypass ceramic capacitors is suggested to connect between this pin and ground.
38	SENSE	Internal reference and a ±1V input range is selected if SENSE is connected to V_{DD}. Similarly, Internal reference and a ±0.5V input range is selected if SENSE is connected to ground. External reference and an input range of ±0.8 • V_{SENSE} is selected if SENSE is connected to a voltage from 0.625V to 1.3V.
Exposed Pad	GND	Must be connected to the PCB ground.

PACKAGE OUTLINE DIMENSIONS

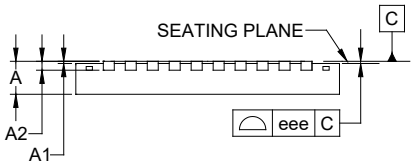
TQFN-6×6-40AL



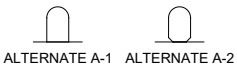
TOP VIEW



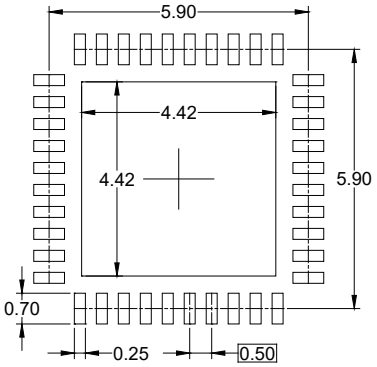
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



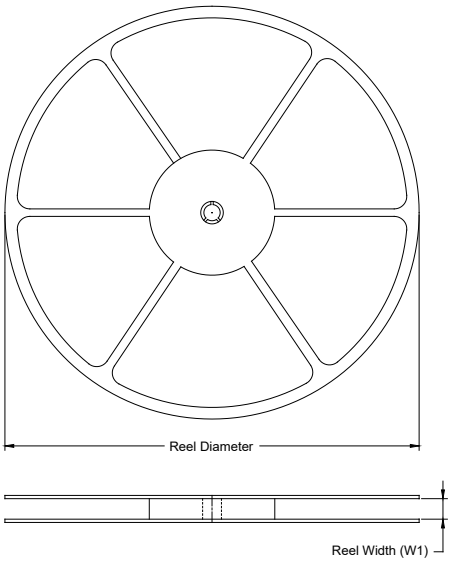
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	5.900	-	6.100
E	5.900	-	6.100
D1	4.320	-	4.520
E1	4.320	-	4.520
e	0.500 BSC		
k	0.390 REF		
L	0.300	-	0.500
eee	0.080		

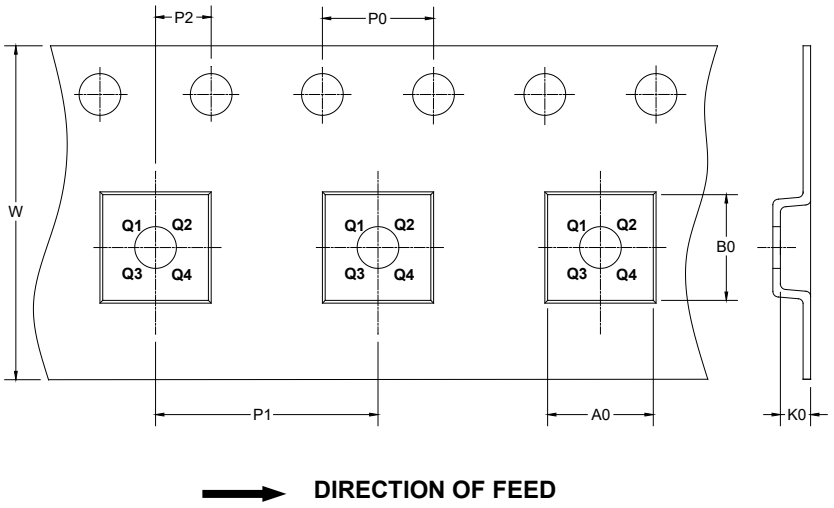
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



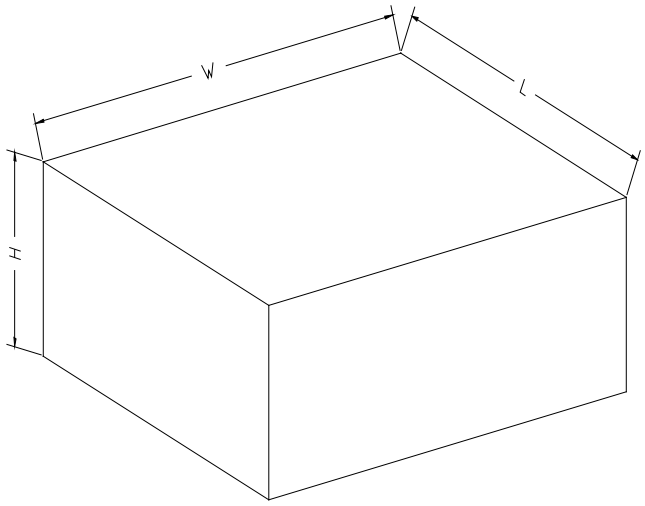
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-6×6-40AL	13″	16.4	6.40	6.40	1.40	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002