74AHCT595
8-Bit Serial-In/Serial-Out or Parallel-Out Shift Register with Output Latches

GENERAL DESCRIPTION

The 74AHCT595 is an 8-bit serial-in/serial-out or parallel-out shift register with output latches designed for 4.5V to 5.5V V_{CC} operation.

The device integrates an 8-bit shift register and an 8-bit D-type storage register. The storage register features parallel 3-state outputs. The shift register provides a clear input ($\overline{SRCLR}$) with direct overriding function, serial input (SER) and serial outputs to implement cascading. When output enable input ($\overline{OE}$) is held low, the data in storage register will appear at the output. When $\overline{OE}$ is held high, all outputs are in high-impedance state.

Both the shift register and storage register have separate clocks. The shift register clock (SRCLK) and storage register clock (RCLK) are positive-edge triggered.

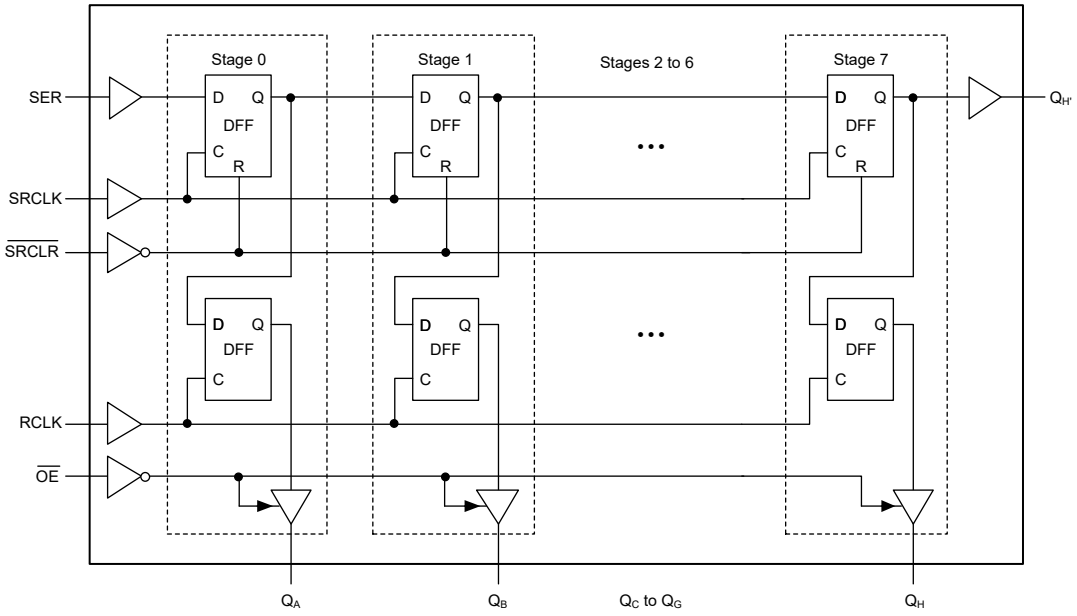
FEATURES

- **Supply Voltage Range: 4.5V to 5.5V**
- **+8mA/-8mA Output Current**
- **Direct Clear Input of Shift Register**
- **Inputs are Compatible with TTL-Voltage**
- **Latch-up Performance (> 100mA) Meets JESD 78, Class II Standard**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TSSOP-16 and SOIC-16 Packages**

APPLICATIONS

Computing: Server, PC, Notebook, Network Switch
Telecom Equipment
Medical Equipment
Industrial Equipment

LOGIC DIAGRAM

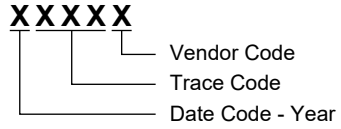


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHCT595	TSSOP-16	-40℃ to +125℃	74AHCT595XTS16G/TR	0LA XTS16 XXXXX	Tape and Reel, 4000
	SOIC-16	-40℃ to +125℃	74AHCT595XS16G/TR	74AHCT595XS16 XXXXX	Tape and Reel, 2500

MARKING INFORMATION

NOTE: XXXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage Range, V_{CC} ..... -0.5V to 7.0V
Input Voltage Range, V_I (2)..... -0.5V to 7.0V
Output Voltage Range, V_O (2) -0.5V to MIN(7.0V, V_{CC} + 0.5V)
Input Clamp Current, I_{IK} (V_I < 0V) .....-20mA
Output Clamp Current, I_{OK} (V_O < 0V or V_O > V_{CC}).....±20mA
Continuous Output Current, I_O (V_O = 0V to V_{CC}).....±25mA
Continuous Current through V_{CC} or GND .....±50mA
Junction Temperature (3).....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} .....4.5V to 5.5V
Input Voltage Range, V_I (4).....0V to 5.5V
Output Voltage Range, V_O ..... 0V to V_{CC}
Output Current, I_O .....±8mA (MAX)
Input Transition Rise or Fall Rate, Δt/ΔV
V_{CC} = 4.5V to 5.5V.....20ns/V (MAX)
Operating Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

4. Unused input pins must be held at V_{CC} or GND to guarantee the device in normal operation.

ESD SENSITIVITY CAUTION

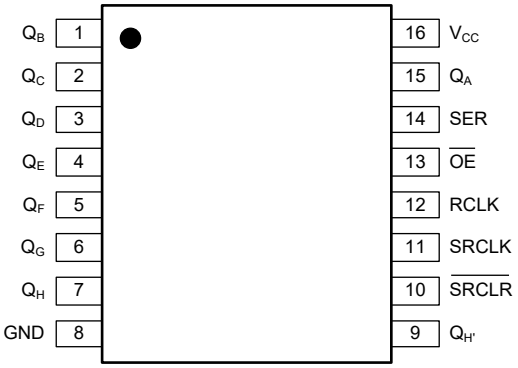
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-16/SOIC-16

PIN DESCRIPTION

PIN	NAME	FUNCTION
15, 1, 2, 3, 4, 5, 6, 7	Q_A, Q_B, Q_C, Q_D, Q_E, Q_F, Q_G, Q_H	Parallel Data Outputs.
8	GND	Ground.
9	$Q_{H'}$	Serial Data Output.
10	$\overline{SRCLR}$	Shift Register Clear Input (Active Low).
11	SRCLK	Shift Register Clock Input (Rising Edge Triggered).
12	RCLK	Storage Register Clock Input (Rising Edge Triggered).
13	$\overline{OE}$	Output Enable Input (Active Low).
14	SER	Serial Data Input.
16	V_{CC}	Power Supply.

FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	*X*	*X*	*X*	H	Outputs (Q_A-Q_H) are disabled.
X	*X*	*X*	*X*	L	Outputs (Q_A-Q_H) are enabled.
X	X	L	*X*	*X*	Data of the shift register is cleared.
L	↑	H	*X*	*X*	Logic low-level shifted into shift register Stage 0. Other stages can transfer data from the previous stage respectively.
H	↑	H	*X*	*X*	Logic high-level shifted into shift register Stage 0. Other stages can transfer data from the previous stage respectively.
X	*X*	*X*	↑	*X*	Data of the shift register is transferred to the storage register.

H = High Voltage Level

L = Low Voltage Level

↑ = Low to High Clock Transition

X = Don't Care

TIMING DIAGRAM

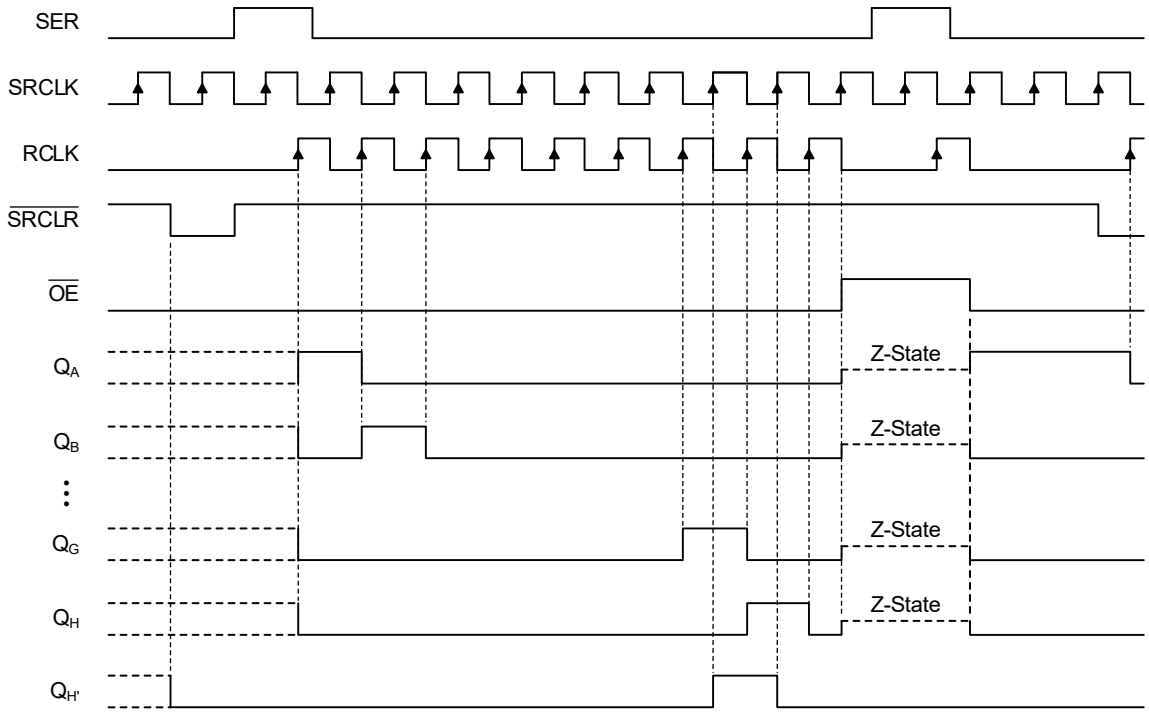


Figure 1. Timing Diagram

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}		Full	2			V
Low-Level Input Voltage	V_{IL}		Full			0.8	V
High-Level Output Voltage	V_{OH}	V_{CC} = 4.5V, I_{OH} = -50μA	Full	4.4	4.495		V
		V_{CC} = 4.5V, I_{OH} = -8mA	Full	4.0	4.28		
		V_{CC} = 5.5V, I_{OH} = -8mA	Full	5.08	5.31		
Low-Level Output Voltage	V_{OL}	V_{CC} = 4.5V, I_{OL} = 50μA	Full		0.005	0.10	V
		V_{CC} = 4.5V, I_{OL} = 8mA	Full		0.21	0.44	
		V_{CC} = 5.5V, I_{OL} = 8mA	Full		0.20	0.42	
Input Leakage Current	I_I	V_{CC} = 0 to 5.5V, V_I = V_{CC} or GND	Full			±2	μA
Off-State Output Current	I_{OZ}	Q_A-Q_H, V_{CC} = 5.5V, V_O = V_{CC} or GND	Full			±2	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, V_I = V_{CC} or GND, I_O = 0A	Full			20	μA
Additional Supply Current (1)	ΔI_{CC}	V_{CC} = 5.5V, one input at 3.4V, other inputs at V_{CC} or GND	Full			1	mA
Input Capacitance	C_I	V_{CC} = 5.0V, V_I = V_{CC} or GND	+25℃		4.5		pF
Output Capacitance	C_O	V_{CC} = 5.0V, V_O = V_{CC} or GND	+25℃		6		pF

NOTE:

1. It is the increase in supply current for per input at the specified TTL voltage levels except V_{CC} or GND.

NOISE CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 5.0V, C_L = 50pF and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
Maximum Dynamic Low-Level Output Voltage	V_{OLDMAX}	Quiet output	+25℃		1		V
Minimum Dynamic Low-Level Output Voltage	V_{OLDMIN}	Quiet output	+25℃		-0.6		V
Minimum Dynamic High-Level Output Voltage	V_{OHDMIN}	Quiet output	+25℃		3.2		V
Dynamic High-Level Input Voltage	V_{IHD}		Full	2			V
Dynamic Low-Level Input Voltage	V_{ILD}		Full			0.8	V

DYNAMIC CHARACTERISTICS

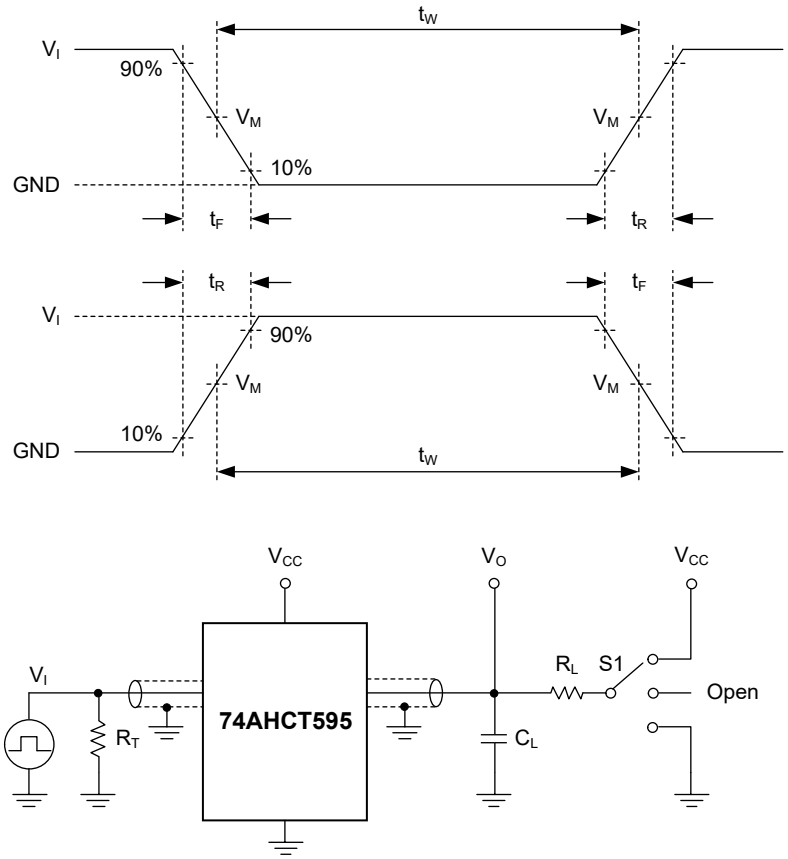
(See Figure 2 for test circuit. Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 5.0V ± 0.5V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN (1)	TYP	MAX (1)	UNITS
Low to High Propagation Delay	t_{PLH}	RCLK to Q_A-Q_H	C_L = 15pF	Full	1	4	8.5	ns
			C_L = 50pF	Full	1	5.5	11.5	
High to Low Propagation Delay	t_{PHL}		C_L = 15pF	Full	1	4	8.5	ns
			C_L = 50pF	Full	1	5.5	11.5	
Low to High Propagation Delay	t_{PLH}	SRCLK to $Q_{H'}$	C_L = 15pF	Full	1	4	8.5	ns
			C_L = 50pF	Full	1	5.5	11.4	
High to Low Propagation Delay	t_{PHL}		C_L = 15pF	Full	1	4	8.5	ns
			C_L = 50pF	Full	1	5.5	11.4	
High to Low Propagation Delay	t_{PHL}	$\overline{SRCLR}$ to $Q_{H'}$	C_L = 15pF	Full	1	8	13.5	ns
			C_L = 50pF	Full	1	10	16	
Off-State to High Propagation Delay	t_{PZH}	$\overline{OE}$ to Q_A-Q_H	C_L = 15pF	Full	1	6.5	10.5	ns
			C_L = 50pF	Full	1	8	13.5	
Off-State to Low Propagation Delay	t_{PZL}		C_L = 15pF	Full	1	6	10.5	ns
			C_L = 50pF	Full	1	8	13.5	
High to Off-State Propagation Delay	t_{PHZ}	$\overline{OE}$ to Q_A-Q_H	C_L = 15pF	Full	1	3	6.5	ns
			C_L = 50pF	Full	1	4	8.5	
Low to Off-State Propagation Delay	t_{PLZ}		C_L = 15pF	Full	1	3	6.5	ns
			C_L = 50pF	Full	1	4	8.5	
Maximum Frequency	f_{MAX}	C_L = 15pF		Full	115	165		MHz
		C_L = 50pF		Full	85	160		
Pulse Width	t_W	SRCLK high or low		Full	5.5			ns
		RCLK high or low		Full	5.5			
		$\overline{SRCLR}$ low		Full	8			
Set-up Time (2)	t_{SU}	SER before SRCLK ↑		Full	9			ns
		SRCLK ↑ before RCLK ↑		Full	5			
		$\overline{SRCLR}$ low before RCLK ↑		Full	10			
		$\overline{SRCLR}$ high (inactive) before SRCLK ↑ (3)		Full	5			
Hold Time	t_H	SER after SRCLK ↑		Full	5			ns
Power Dissipation Capacitance (4) (5)	C_{PD}	No load, V_{CC} = 5.0V, f = 10MHz		+25℃		30		pF

NOTES:

1. Specified by design and characterization, not production tested.
2. The set-up time enables the storage register to get stable data from the shift register. In this case where clocks can be tied together, the shift register is a clock pulse in front of the storage register.
3. t_{REC} is the same as $\overline{SRCLR}$ high (inactive) before SRCLK ↑.
4. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$
   where:
   f_i = Input frequency in MHz.
   f_o = Output frequency in MHz.
   C_L = Output load capacitance in pF.
   V_{CC} = Supply voltage in Volts.
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.
5. All 9 outputs switching.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions test circuit:

R_L: Load resistance.

C_L: Load capacitance (includes jig and probe).

R_T: Termination resistance (equals to output impedance Z_O of the pulse generator).

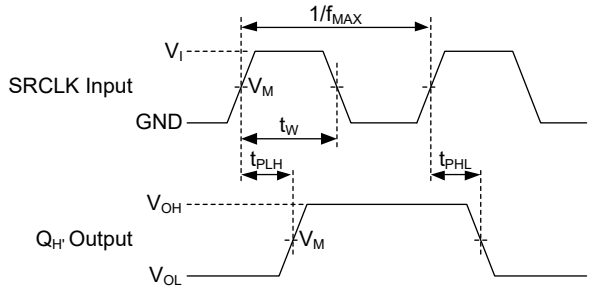
S1: Test selection switch.

Figure 2. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

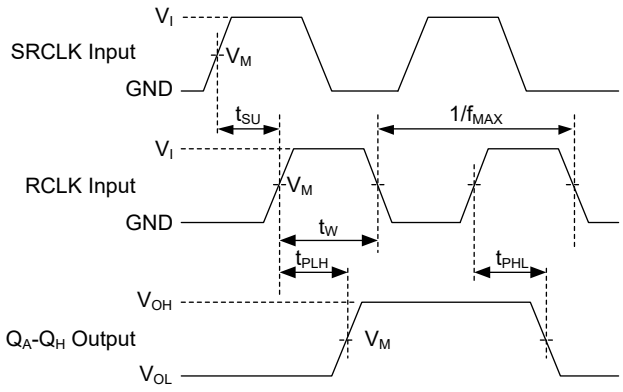
SUPPLY VOLTAGE	INPUT		LOAD		S1 POSITION		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
4.5V to 5.5V	V_{CC}	≤ 3.0ns	15pF, 50pF	1kΩ	Open	GND	V_{CC}

WAVEFORMS



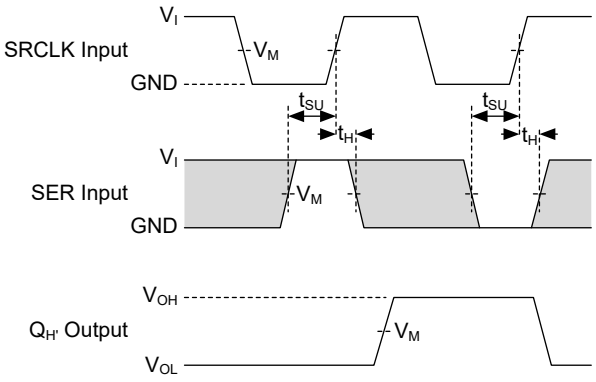
Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 3. Shift Clock Pulse, Maximum Frequency and Shift Register Clock Input to Output Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

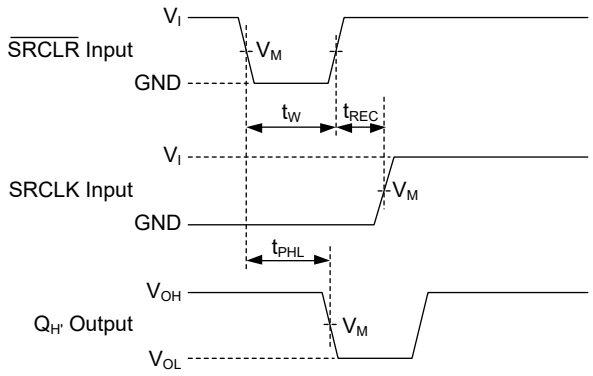
Figure 4. Storage Register Clock to Output Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

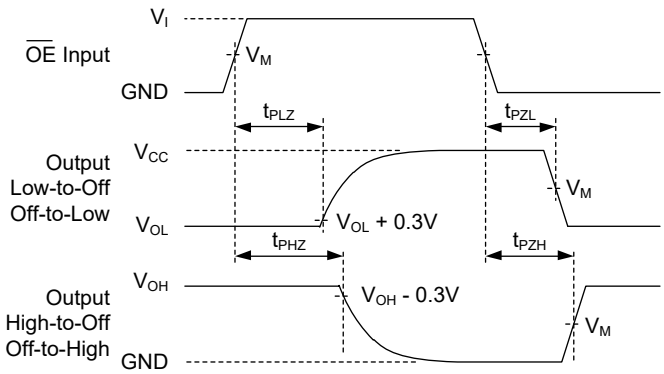
Figure 5. Data Set-up and Hold Times

WAVEFORMS (continued)



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Clear Input to Output Propagation Delays



Test conditions are given in Table 1.
Measurement points are given in Table 2.
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. Enable and Disable Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT		OUTPUT
V_{CC}	V_I	V_M (1)	V_M
4.5V to 5.5V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.

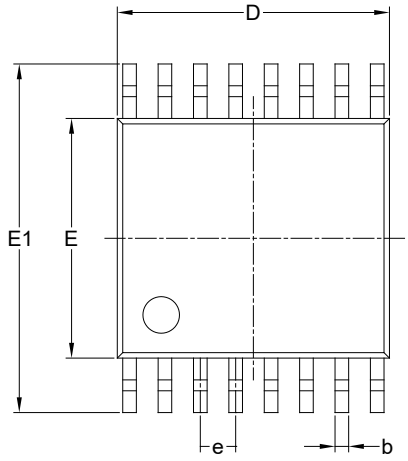
REVISION HISTORY

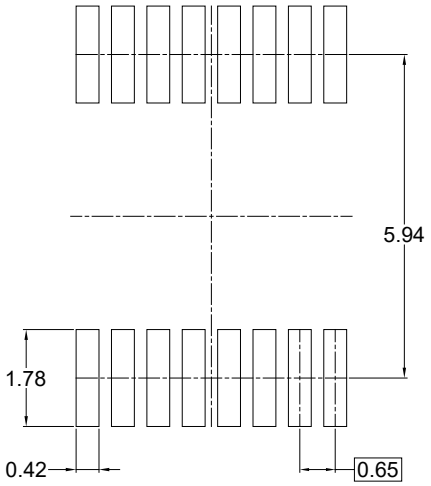
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (OCTOBER 2023) to REV.A	Page
Changed from product preview to production data	All

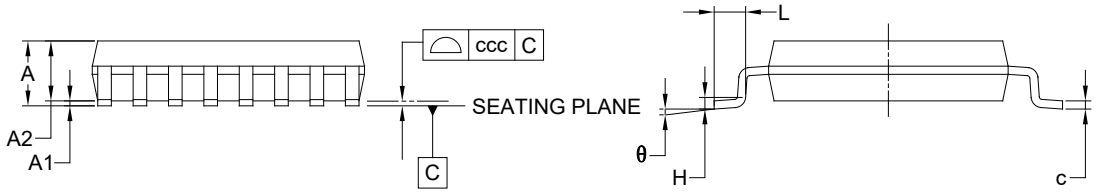
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

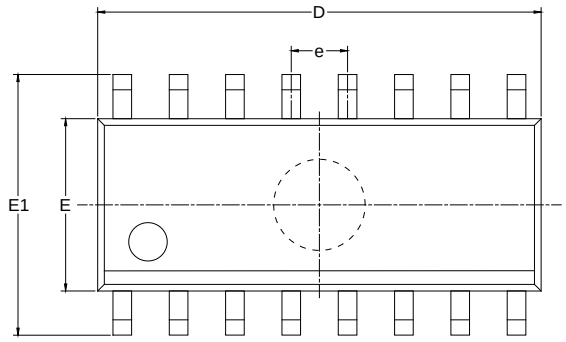


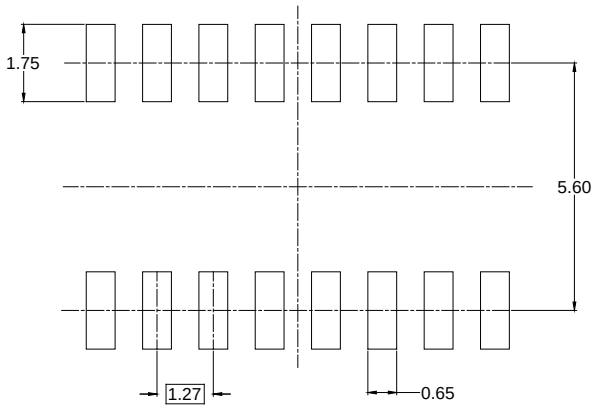
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

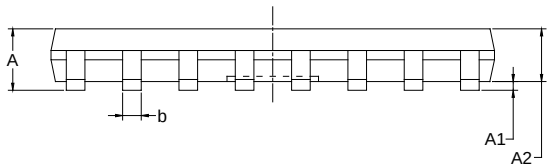
PACKAGE OUTLINE DIMENSIONS

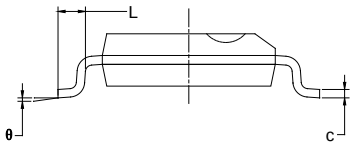
SOIC-16





RECOMMENDED LAND PATTERN (Unit: mm)



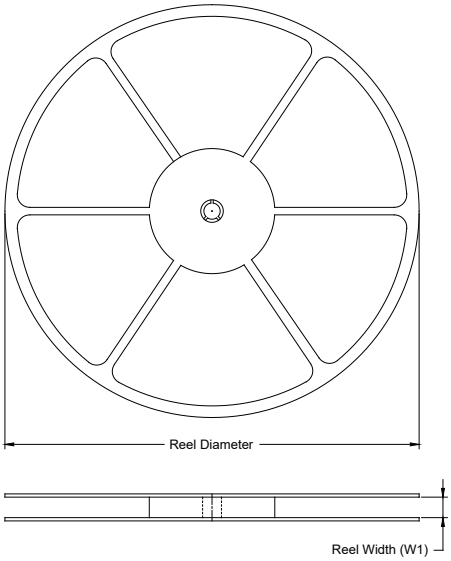


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

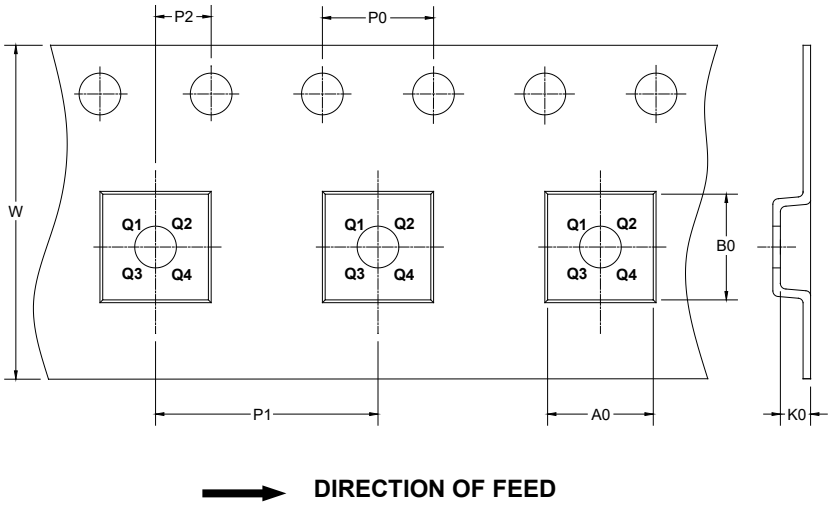
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



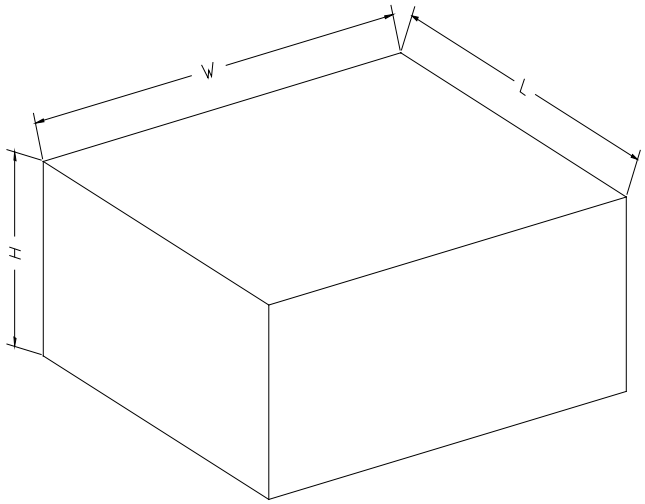
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-16	13″	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002