SGM61432
40V/3.5A, Adjustable Switching Frequency Buck Converter with 38μA I_Q

GENERAL DESCRIPTION

The SGM61432 is a current mode controlled non-synchronous Buck converter with 4V to 40V input range and 3.5A continuous output current. A low R_{DSON} N-MOSFET is integrated as high-side switch. Moreover, the low 38μA quiescent current and low shutdown current of only 1.3μA (TYP) make it a suitable choice for battery-powered applications. Also, the internal loop compensation simplifies compensation network design and saves user design time and cost. The UVLO level can be adjusted (increased) by an external resistor divider. Switching frequency can be selected over a wide range (200kHz to 2500kHz) to allow desired tradeoff among efficiency, component sizes and conversion voltage ratio. Protection against over-voltage transient is provided to limit the startup or other transient overshoots. Secure operation in overload conditions is ensured by cycle-by-cycle current limit, frequency fold-back and thermal shutdown protection.

The SGM61432 is available in a Green SOIC-8 (Exposed Pad) package.

FEATURES

- **4V to 40V Input Voltage Range**
- **0.8V to 28V Adjustable Output Voltage Range**
- **Peak Current Mode Control**
- **Integrated 93mΩ High-side MOSFET Supports up to 3.5A Continuous Output Current**
- **Adjustable Switching Frequency from 200kHz to 2500kHz**
- **Ultra-Low Quiescent Current: 38μA (TYP)**
- **Low Shutdown Current: 1.3μA (TYP)**
- **Power-Save Mode for High Light Load Efficiency**
- **External Soft-Start**
- **Frequency Synchronization to External Clock**
- **Programmable UVLO Threshold**
- **Output Over-Voltage Protection**
- **Cycle-by-Cycle Current Limit**
- **Frequency Fold-Back Protection**
- **Thermal Shutdown Protection**
- **Available in a Green SOIC-8 (Exposed Pad) Package**

APPLICATIONS

Automotive Battery Regulation
Industrial Power Supplies
Telecom and Datacom Systems
Battery Powered System

TYPICAL APPLICATION

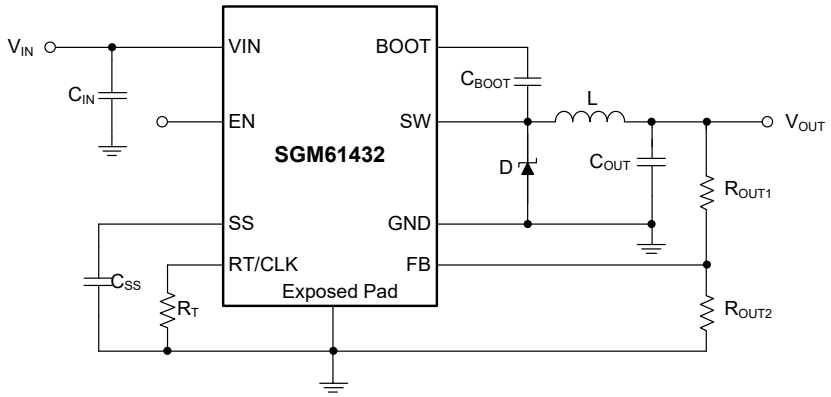


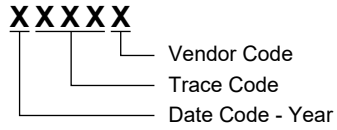
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61432	SOIC-8 (Exposed Pad)	-40℃ to +125℃	SGM61432XPS8G/TR	SGM 61432XPS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltages
- VIN, EN to GND ..... -0.3V to 44V
- BOOT to GND ..... -0.3V to 50V
- SS to GND ..... -0.3V to 5V
- FB to GND ..... -0.3V to 6V
- RT/CLK to GND ..... -0.3V to 3.6V

Output Voltages
- BOOT to SW ..... 6V (MAX)
- SW to GND ..... -0.6V to 44V
- SW to GND (10ns Transient) ..... -3.5V to 44V

Package Thermal Resistance
- SOIC-8 (Exposed Pad), θ_{JA} ..... 41℃/W

Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 4V to 40V
Output Voltage Range ..... 0.8V to 28V
Switching Frequency Range at RT Mode
..... 200kHz to 2500kHz
Switching Frequency Range at SYNC Mode
..... 250kHz to 2300kHz
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

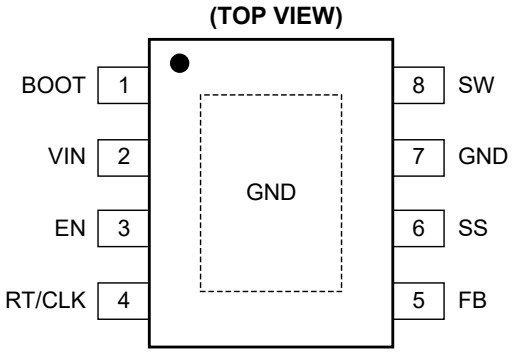
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	BOOT	O	Bootstrap Input (for N-MOSFET Gate Driver Supply Voltage). Connect this pin to SW pin with a 0.1μF ceramic capacitor. The MOSFET will turn off if the BOOT capacitor voltage drops below its BOOT-UVLO level to get the capacitor voltage refreshed.
2	VIN	P	Supply Input. Connect VIN to a power source with 4V to 40V output voltage range. Decouple VIN to GND as close as possible to the catch diode anode and the device with a high frequency, low ESR ceramic capacitor (X5R or higher grade is recommended).
3	EN	I	Active High Enable Input. Float or pull up to VIN to enable, or pull down below 1.11V to disable the device. Input UVLO level can be programmed using a resistor divider from V_{IN}.
4	RT/CLK	I	Resistor Timing and External Clock. Frequency is set by the external RT resistor or external SYNC clock, refer to Synchronization to RT/CLK Pin for more details.
5	FB	I	Feedback Pin for Setting the Output Voltage. The SGM61432 regulates the FB pin to 0.75V. Connect a feedback resistor divider tap to this pin.
6	SS	O	Soft-Start Control Pin. Connect an external capacitor (C_{SS}) between this pin and the GND to set the soft-start time.
7	GND	G	Ground Pin.
8	SW	P	Switching Node of the Converter (Source of the Internal MOSFET). Connect it to the cathode of the external power diode (catch diode), the bootstrap capacitor and the inductor.
—	Exposed Pad	G	Exposed Pad. It helps cooling the device junction and must be connected to GND pin for proper operation.

NOTE: I = input, O = output, G = ground, P = power.

ELECTRICAL CHARACTERISTICS

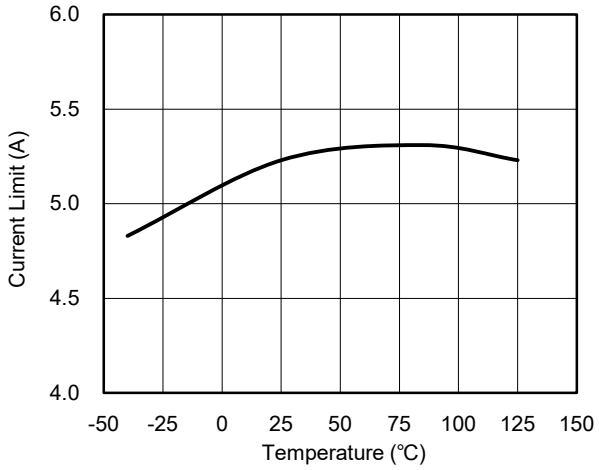
(T_J = -40℃ to +125℃, V_{IN} = 4V to 40V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Power Supply (VIN Pin)						
Operation Input Voltage	V_{IN}		4		40	V
Under-Voltage Lockout Threshold	V_{UVLO}	Rising threshold	3.68	3.85	4	V
Under-Voltage Lockout Threshold Hysteresis	V_{UVLO_HYS}			255		mV
Shutdown Supply Current	I_{SHDN}	T_J = +25℃, 4.0V ≤ V_{IN} ≤ 40V, V_{EN} = 0V		1.3	3.8	μA
Quiescent Current	I_Q	T_J = +25℃, V_{IN} = 12V, V_{FB} = 1V		38		μA
Enable (EN Pin)						
EN Threshold Voltage	V_{ENH}	V_{EN} rising		1.19	1.27	V
	V_{ENL}	V_{EN} falling	1.05	1.11		
	V_{EN_HYS}	Hysteresis		80		mV
EN Input Current	I_{EN_PIN}	Enable threshold +50mV		-4.4		μA
		Enable threshold -50mV		-1.0		
EN Hysteresis Current	I_{EN_HYS}			-3.4		μA
External Soft-Start						
SS Pin Current	I_{SS}	T_J = +25℃		3		μA
Voltage Reference (FB Pin)						
Feedback Voltage	V_{FB}	T_J = +25℃	0.745	0.75	0.765	V
		T_J = -40℃ to +125℃	0.739	0.75	0.769	
High-side MOSFET						
On-Resistance	R_{DSON}	V_{IN} = 12V, V_{BOOT} to V_{SW} = 5V		93	150	mΩ
High-side MOSFET Current Limit						
Current Limit	I_{LIMT}	T_J = +25℃, V_{IN} = 12V, close-loop	4.4	5.1	5.8	A
Thermal Performance						
Thermal Shutdown Threshold	T_{SHDN}			175		℃
Hysteresis	T_{HYS}			20		℃
Switching Characteristics						
Switching Frequency	f_{SW}	R_T = 49.9kΩ, 1% accuracy	470	500	530	kHz
SYNC Clock High Level Threshold	V_{SYNC_HI}		1.7			V
SYNC Clock Low Level Threshold	V_{SYNC_LO}				0.7	V
Minimum SYNC Input Pulse Width	T_{SYNC_MIN}	Measured at 500kHz, V_{SYNC_HI} > 3V, V_{SYNC_LO} < 0.3V		30		ns
PLL Lock in Time	t_{LOCK_IN}	Measured at 500kHz		100		μs
Minimum Controllable on Time	t_{ON_MIN}			85		ns
Maximum Duty Cycle	D_{MAX}	f_{SW} = 200kHz		97		%

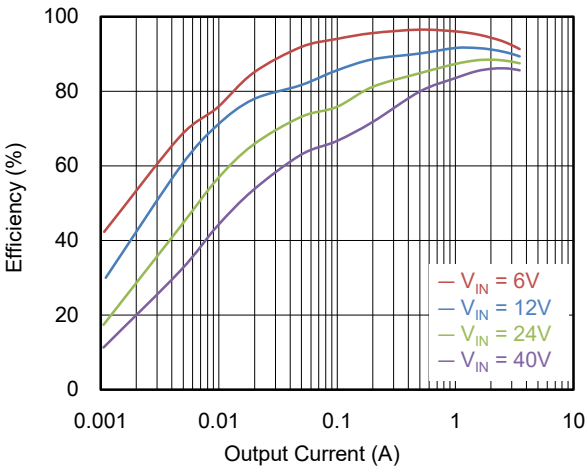
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 6.8μH and C_{OUT} = 47μF × 2, unless otherwise noted.

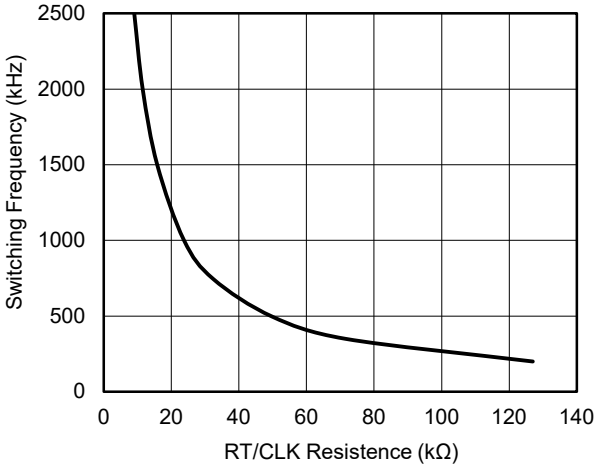
Current Limit vs. Temperature



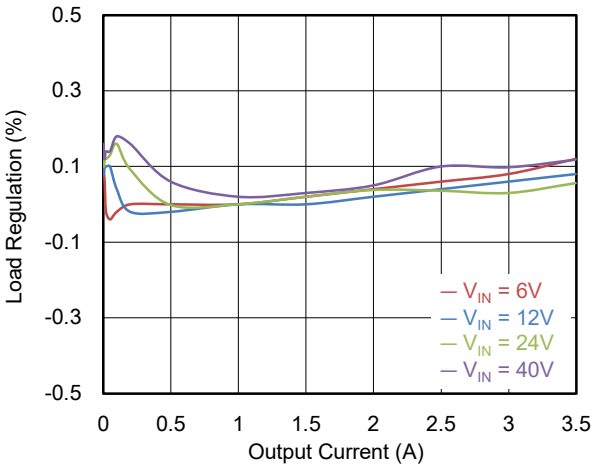
Efficiency Curve at 5V Output



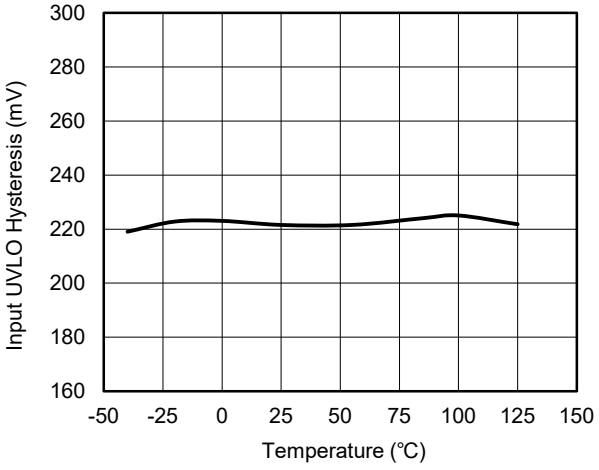
F_{SW} vs. RTCLK Resistance



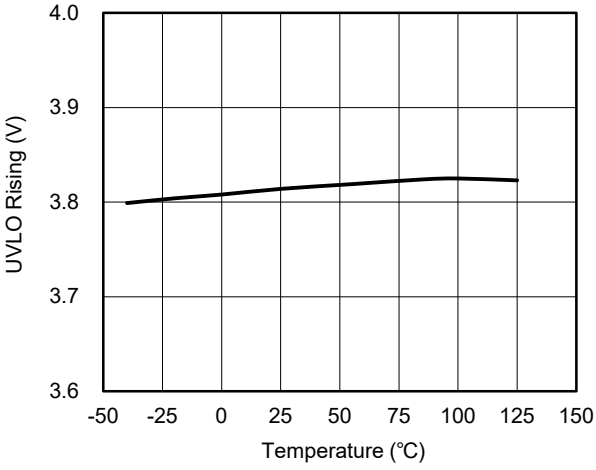
Load Regulation at 5V Output



UVLO Hysteresis vs. Junction Temperature



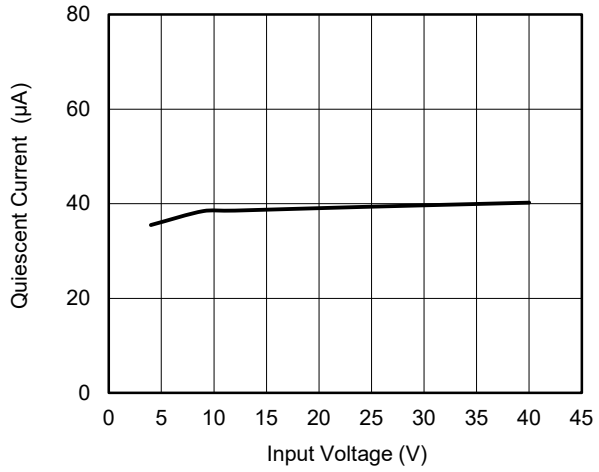
UVLO Rising vs. Junction Temperature



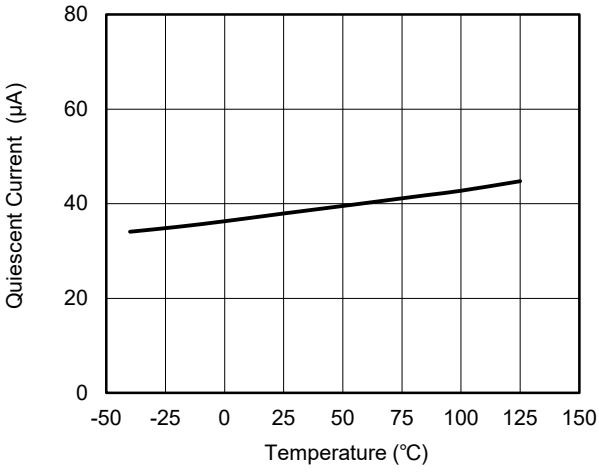
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 6.8μH and C_{OUT} = 47μF × 2, unless otherwise noted.

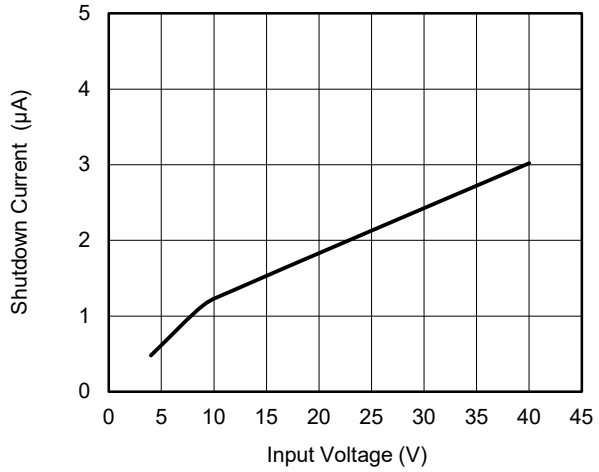
Quiescent Current vs. Input Voltage



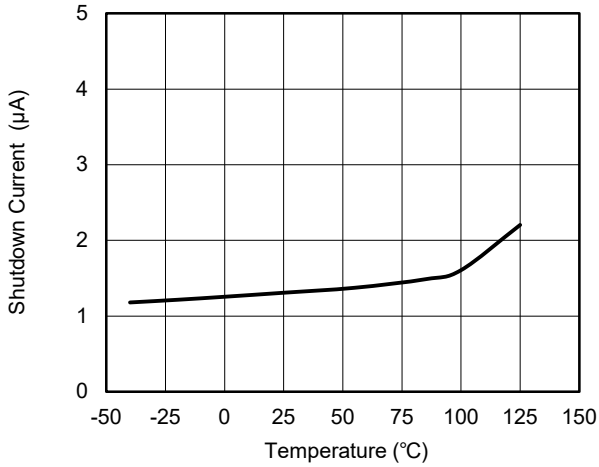
Quiescent Current vs. Junction Temperature



Shutdown Current vs. Input Voltage



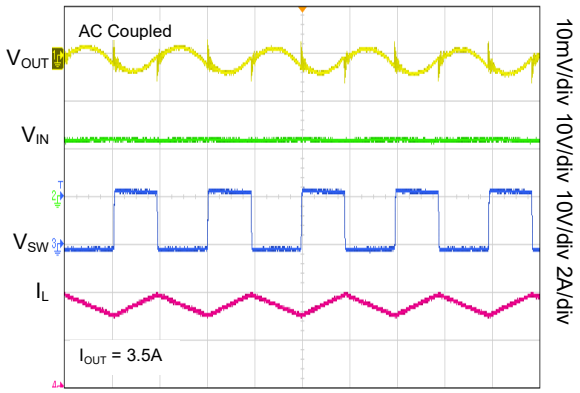
Shutdown Current vs. Junction Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

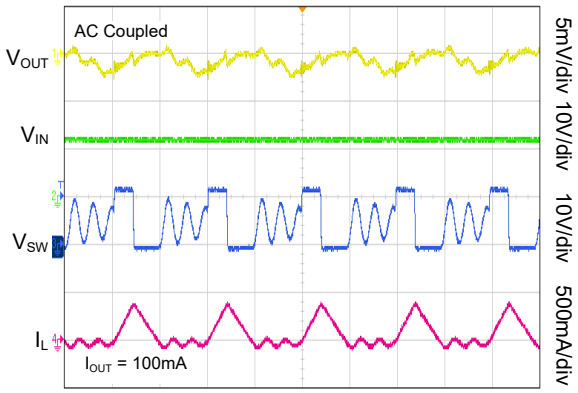
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 6.8μH and C_{OUT} = 47μF × 2, unless otherwise noted.

CCM Mode



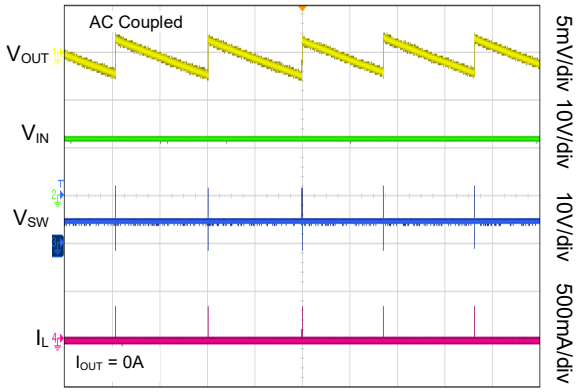
Time (1μs/div)

DCM Mode



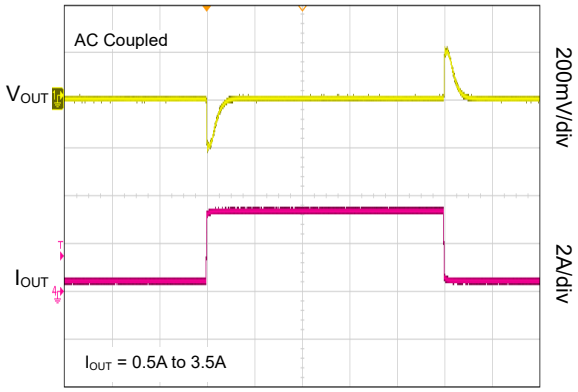
Time (1μs/div)

PSM Mode



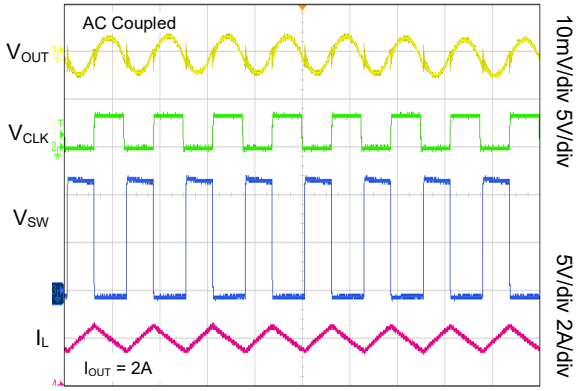
Time (1ms/div)

Load Transient



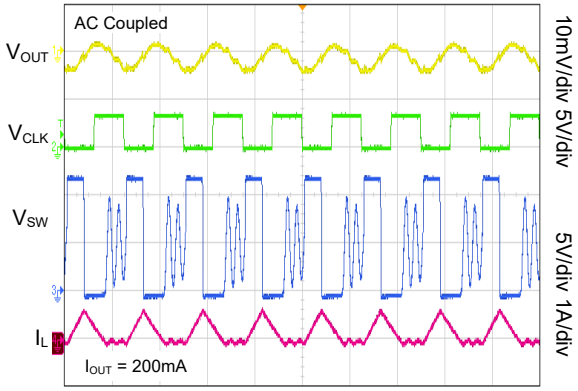
Time (200μs/div)

Synchronizing in CCM



Time (2μs/div)

Synchronizing in DCM

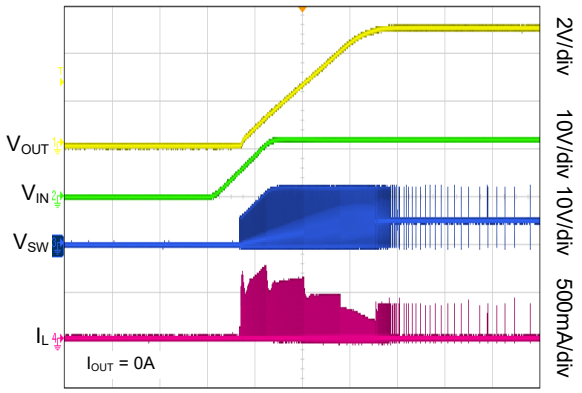


Time (2μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

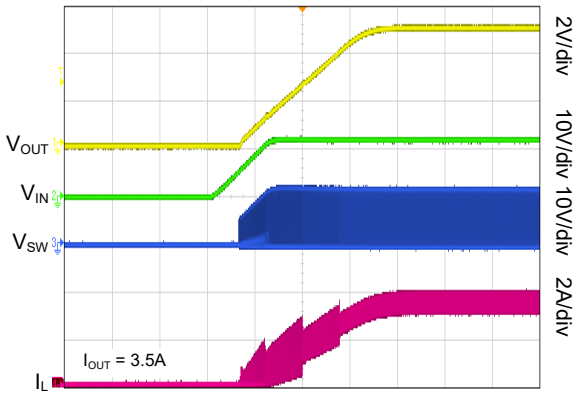
T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 6.8μH and C_{OUT} = 47μF × 2, unless otherwise noted.

Startup by VIN



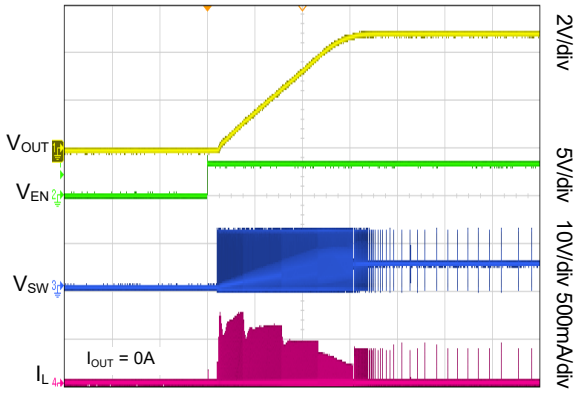
Time (2ms/div)

Startup by VIN



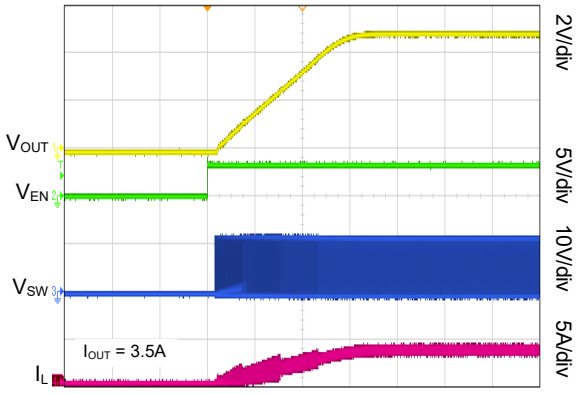
Time (2ms/div)

Startup by EN



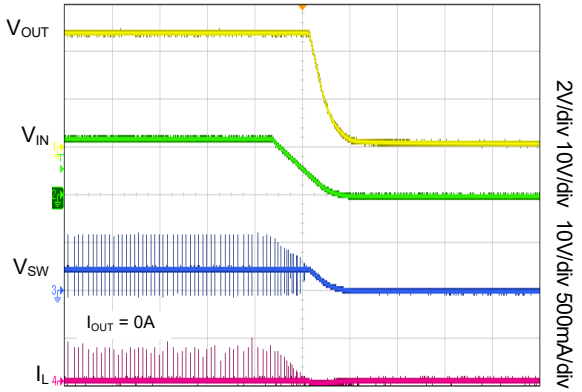
Time (2ms/div)

Startup by EN



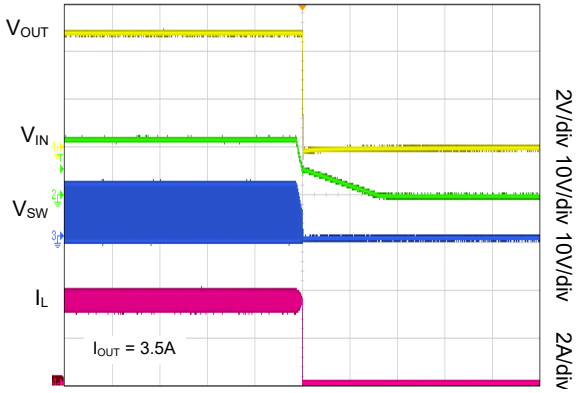
Time (2ms/div)

Shutdown by VIN



Time (20ms/div)

Shutdown by VIN

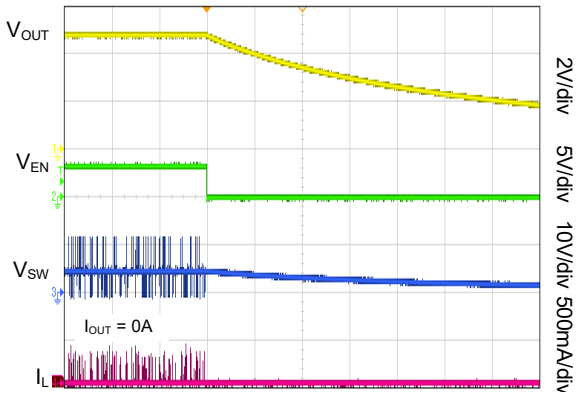


Time (20ms/div)

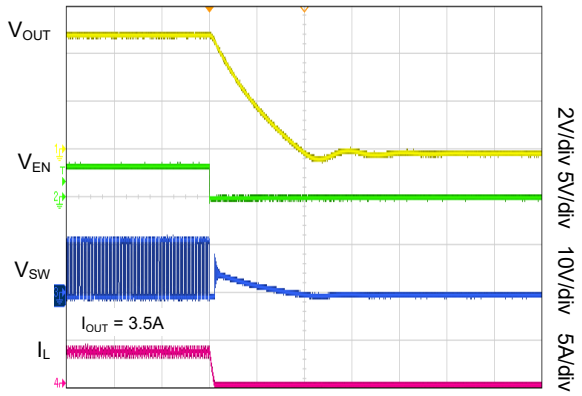
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 500kHz, L = 6.8μH and C_{OUT} = 47μF × 2, unless otherwise noted.

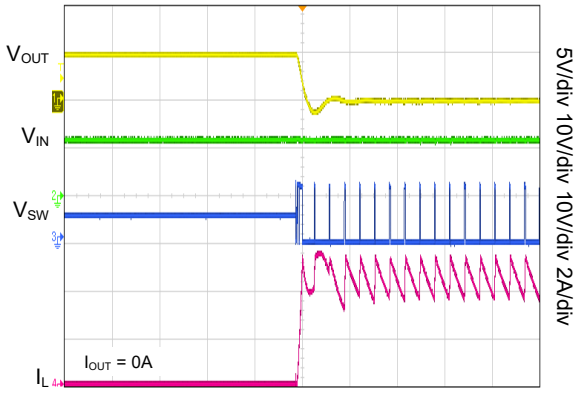
Shutdown by EN



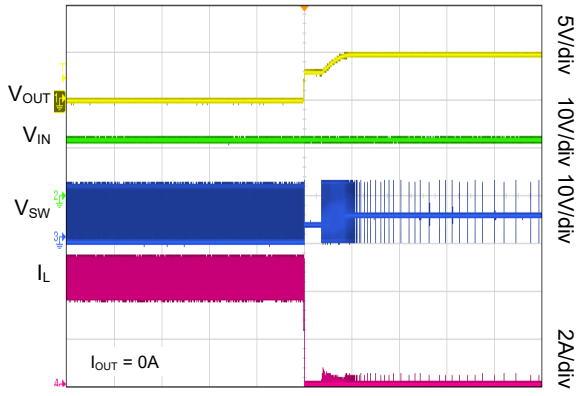
Shutdown by EN



Short-Circuit Entry



Short-Circuit Recovery



FUNCTIONAL BLOCK DIAGRAM

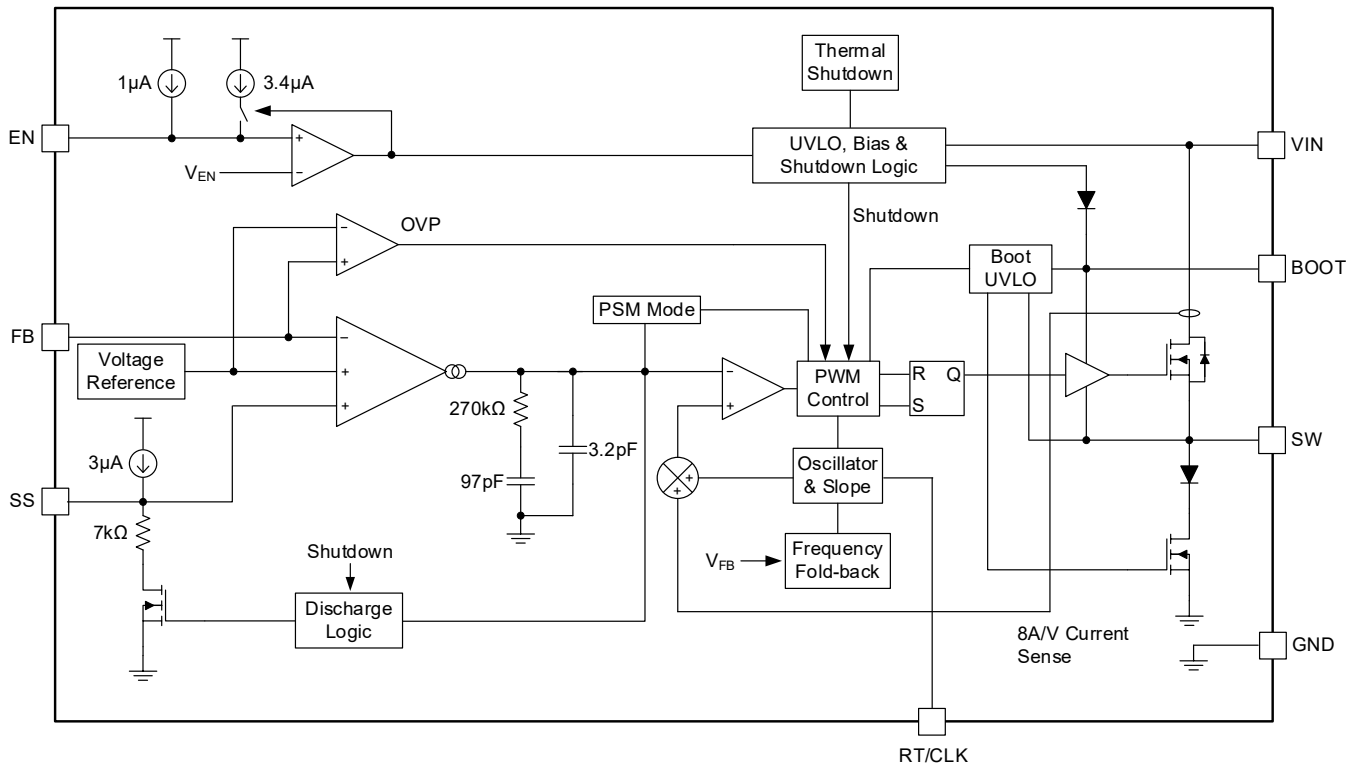


Figure 2. SGM61432 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61432 is a 40V Buck converter with an integrated N-MOSFET power switch and 3.5A continuous output current capability. Using peak current mode control, this device provides good line and load transient responses with reduced output capacitance.

The minimum operating input voltage of the device is 4V and its nominal frequency is 500kHz. The quiescent current is 38μA. It reduces to 1.3μA if the device is disabled. The low R_{DSON} high-side switch (93mΩ) allows high operating efficiency.

The EN pin is internally pulled up by a current source that can keep the device enabled if EN is floating. It can also be used to increase the input UVLO threshold using a resistor divider.

The bootstrap diode is integrated and only a small capacitor between BOOT and SW pins (C_{BOOT}) is needed for the MOSFET gate driving bias. A separate UVLO circuit monitors C_{BOOT} voltage and turns the switch off if this voltage falls below a preset threshold.

The switching frequency is adjusted by using a resistor to ground which is connected to the RT/CLK pin. It is also can be synchronized to an external clock signal.

Over-voltage protection (OVP) circuit is designed to minimize the output over-voltage transients. When this comparator detects an OVP (V_{FB} > 110% × V_{REF}), the switch is kept off until the V_{FB} falls below 106% of the V_{REF}.

The SS pin internal current source allows soft-start time adjustments with a small external capacitor. This feature provides more flexibility in output filter design.

Light load efficiency is enhanced by a special power-save mode.

During startup and over-current, the frequency is reduced (frequency fold-back) to allow easy maintenance of low inductor current. The thermal shutdown provides an additional protection in fault conditions.

DETAILED DESCRIPTION (continued)

Minimum Input Voltage (4V) and UVLO

The recommended minimum operating input voltage is 4V. It may operate with lower voltages that are above the V_{IN} rising UVLO threshold (3.85V TYP). If V_{IN} falls below its falling UVLO threshold, the device will stop switching.

Enable Input and UVLO Adjustment

An internal current source pull-up keeps the EN pin voltage at high state by default. The device will enable if the EN pin voltage exceeds the enable threshold of 1.19V and V_{IN} exceeds its UVLO threshold. The device will disable if the EN voltage is externally pulled low or the VIN pin voltage falls below its UVLO threshold.

If an application requires a higher input UVLO threshold, an external input UVLO adjustment circuit is recommended in Figure 3. Figure 3 shows how UVLO and hysteresis are increased using R_{EN1} and R_{EN2}. A 3.4μA additional current is injected to the divider when EN pin voltage exceeds V_{ENH} (1.19V) to provide hysteresis and it will be removed when EN pin voltage is below V_{ENL} (1.11V). Use Equations 1 and 2 to calculate these resistors. V_{START} is the input start (turn-on) threshold voltage and V_{STOP} is the input stop (turn-off) threshold voltage.

$$R_{EN1}=\frac{(V_{START}-V_{STOP})-V_{EN\_HYS}\times\frac{V_{START}}{V_{ENH}}}{3.4\mu A+V_{EN\_HYS}\times\frac{1\mu A}{V_{ENH}}} \quad (1)$$

$$R_{EN2}=\frac{V_{ENH}}{\frac{V_{START}-V_{ENH}}{R_{EN1}}+1\mu A} \quad (2)$$

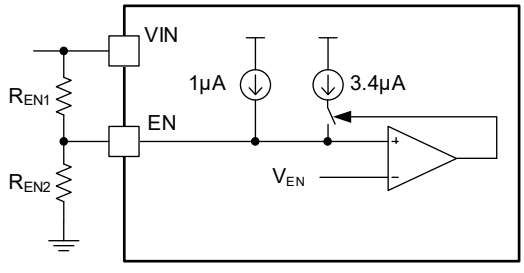


Figure 3. Input UVLO Adjustment

Synchronization to RT/CLK Pin

The internal oscillator can synchronize to an external logic clock applied to the RT/CLK pin (see Figure 4) in the 250kHz to 2300kHz range. The SW rising edge (switch turn-on) is synchronized with the CLK falling edge. The CLK low and high levels must be less than 0.7V and more than 1.7V and have a pulse width larger than 30ns. So, when the CLK source is off, the DC resistance (R_T) between RT/CLK and GND pins determines the default switching frequency.

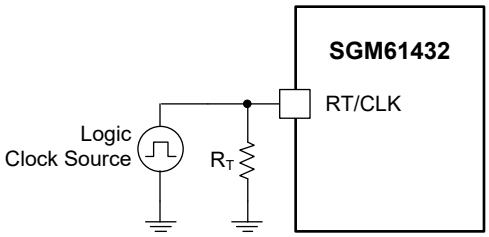


Figure 4. Synchronization to External Clock

Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency can be set from 200kHz to 2500kHz by a timing resistor (R_T) placed between the RT/CLK and GND pins. There is an internal bias voltage (0.5V TYP) on the RT/CLK pin during the RT mode and must have a resistor to ground to set the switching frequency. Use Equation 3 to find the R_T resistance for any desired switching frequency (f_{SW}).

$$R_T(k\Omega)=\frac{31928}{f_{SW}(kHz)^{1.042}} \quad (3)$$

Low Dropout Operation and Bootstrap Gate Driving (BOOT Pin)

An internal regulator provides the bias voltage for gate driver using a 0.1μF ceramic capacitor. X5R or better dielectric types are recommended. The capacitor must have a 10V or higher voltage rating.

The SGM61432 operates at maximum duty cycle when input voltage is closed to output voltage as long as the bootstrap voltage (V_{BOOT} - V_{SW}) is greater than its UVLO threshold. When the bootstrap voltage falls below its UVLO, the high-side switch is turned off, and the integrated low-side switch is turned on to recharge the BOOT capacitor. After the recharge, the high-side switch is turned on again to regulate the output.

DETAILED DESCRIPTION (continued)

SS Pin and Soft-Start Adjustment

It is recommended to add a soft-start capacitor (C_{SS}) between the SS and GND pins to set the soft-start time from 1ms to 10ms for a proper startup. The lower of the SS pin voltage V_{SS} and V_{REF} is applied to the error amplifier to regulate the output. The internal I_{SS} = 3μA current charges C_{SS} and provides a linear voltage ramp on the SS pin. Use Equation 4 to calculate the soft-start time.

$$t_{SS}\ (ms) = \frac{C_{SS}\ (nF) \times V_{REF}\ (V)}{I_{SS}\ (\mu A)} \quad (4)$$

Slope Compensation

Without implementing some slope compensation, the PWM pulse widths will be unstable and oscillatory at duty cycles above 50%. To avoid sub-harmonic oscillations in this device, an internal compensation ramp is added to the measured switch current before comparing it with the control signal by the PWM comparator.

Power-Save Mode

At light loads, the SGM61432 employs pulse-skipping power-save mode (PSM) to maintain its high efficiency by reducing the number of switching pulses. When the peak inductor current falls below the PSM current threshold, the corresponding internal COMP voltage (V_{COMP}) drops below the internal threshold. In such cases, the device will enter PSM to conserve power and improve efficiency.

After entering PSM for a delay time, some modules are shut down to minimum input current, and the device draws only 38μA (TYP) input quiescent current. The device can exit PSM if V_{COMP} rises above the internal threshold and the peak inductor current exceeds current threshold. During PSM operation, the peak inductor current is the sensed parameter for entering the PSM, and the actual load current (DC) threshold for PSM will depend on the output filter.

Over-Current Protection and Frequency Fold-back

Over-current protection (OCP) is naturally provided by current mode control. In each cycle, the high-side current sensing starts a short time (blanking time) after the high-side switch is turned on. The sensed high-side switch current is continuously compared with the current limit threshold and when the high-side current reaches to that threshold, the high-side switch is turned off. If the output is overloaded, V_{OUT} will drop and V_{COMP} will be increased by EA to compensate that, while the EA output (V_{COMP}) is clamped to a maximum value. By limiting V_{COMP} (maximum peak current), the output current can actually be limited precisely.

The natural OCP of the peak current mode control may not be able to provide a complete protection when an output short-circuit occurs and an extra protection mechanism for short-circuit is needed. During an output short, inductor current may runaway above over-current limits because of the high input voltage and the minimum controllable on-time. During an output short, the inductor current decreases slowly because a small negative diode forward voltage appears across the inductor during the off-time, which results in the inductor current cannot be reset. In these conditions, current can saturate the inductor and the current may even increase higher until the device is damaged. In the SGM61432, this problem is effectively solved through increasing the off-time during short-circuit by reducing the switching frequency (frequency fold-back). As the output voltage drops and the FB pin voltage falls from 0.75V to 0V, the frequency will be divided by 1, 2, 4 and 8.

Over-Voltage Transient Protection

When an overload or an output fault condition is removed, large overshoots may occur on the output. The SGM61432 includes over-voltage protection (OVP) circuit to reduce such over-voltage transients. If V_{FB} voltage exceeds 110% of the V_{REF} threshold, the MOSFET is turned off. When it returns below 106% of the V_{REF} threshold, the MOSFET is released again.

Thermal Shutdown (TSD)

If the junction temperature (T_J) exceeds +175℃, the TSD protection circuit will stop switching to protect the device from overheating. The device will automatically restart with a power up sequence when the junction temperature drops below +155℃.

APPLICATION INFORMATION

A typical application circuit for the SGM61432 as a Buck converter is shown in Figure 5. It is used for converting a 7V to 40V supply voltage to a lower voltage level supply voltage (5V) suitable for the system.

Typical Application

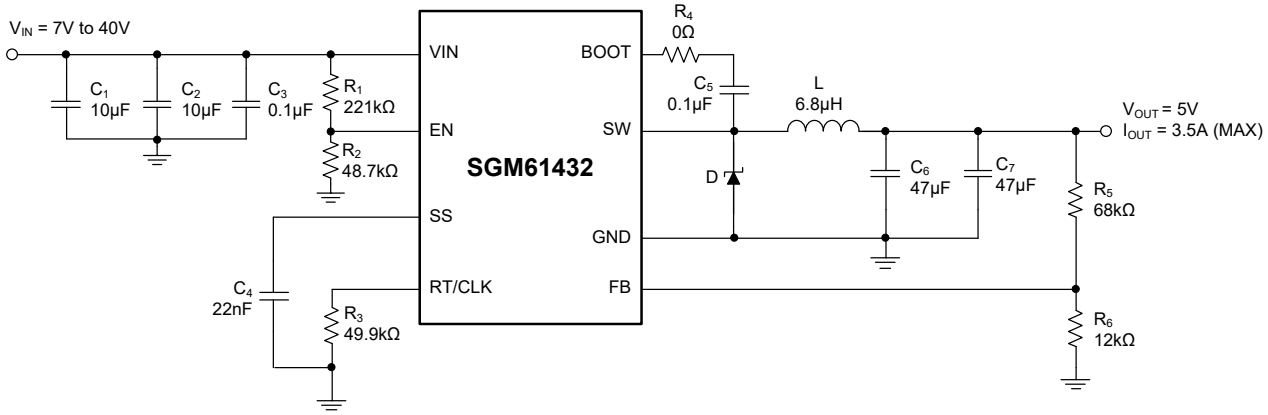


Figure 5. 5V Output SGM61432 Design Example

Design Requirements

The design parameters given in Table 1 are used for this design example.

Table 1. Design Parameters

Design Parameters	Example Values
Input Voltage	12V (TYP) 7V to 40V
Start Input Voltage (Rising V_{IN})	6.74V
Stop Input Voltage (Falling V_{IN})	5.52V
Input Ripple Voltage	360mV, 3% of V_{IN_TYP}
Output Voltage	5V
Output Voltage Ripple	50mV, 1% of V_{OUT}
Output Current Rating	3.5A
Transient Response 1.75A to 3.5A Load Step	250mV, 5% of V_{OUT}
Operation Frequency	500kHz

Switching Frequency Selection

Several parameters such as losses, inductor and capacitors sizes and response time are considered in selection of the switching frequency. Higher frequency increases the switching and gate charge losses, and lower frequency requires larger inductance and capacitances, which results in larger overall physical size and higher cost. Therefore, a tradeoff is needed between losses and component size. If the application is noise-sensitive to a frequency range, the frequency should be selected out of that range.

For this design, a lower switching frequency of 500kHz is chosen and a 49.9kΩ resistor can be chosen for R_3 according to Equation 3.

Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61432. At least 3μF of effective capacitance (after deratings) is needed on the VIN input. In some applications, additional bulk capacitance may also be required for the VIN input, for example, when the SGM61432 is more than 5cm away from the input source. The VIN capacitor ripple current rating must also be greater than the maximum input current ripple. The input current root mean square (RMS) can be calculated using Equation 5 and the maximum value occurs at 50% duty cycle. Using the design example values, I_{OUT} = 3.5A, yields an RMS input ripple current of 1.75A.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For this design, a ceramic capacitor with at least 50V voltage rating is required to support the maximum input voltage. So, 2 × 10μF/50V capacitors in parallel are selected for VIN to cover all DC bias, thermal and aging deratings. The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 6. In this example, the total effective capacitance of the 2 × 10μF/50V capacitors is around 10μF at 12V input, and the input voltage ripple is 200mV.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} + I_{OUT} \times ESR_{CIN} \quad (6)$$

APPLICATION INFORMATION (continued)

It is recommended to place an additional small size 0.1μF ceramic capacitor right beside VIN and GND pins (anode of the diode) for high frequency filtering.

Inductor Design

Equation 7 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions, especially if a hard-saturation core type inductor (such as ferrite) is chosen. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 20% to 40% ripple is selected (K_{IND} = 0.2 ~ 0.4). Choosing a higher K_{IND} value reduces the selected inductance, however, a too high K_{IND} factor may result in insufficient slope compensation.

$$L = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (7)$$

In this example, the calculated inductance will be 6.25μH with K_{IND} = 0.4, so the nearest larger inductance of 6.8μH is selected. The ripple, RMS and peak inductor current calculations are summarized in Equations 8, 9 and 10 respectively.

$$\Delta I_L = \frac{V_{IN\_MAX} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \quad (8)$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \quad (9)$$

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (10)$$

Note that during startup, load transients or the peak inductor current under fault conditions may exceed the calculated I_{L_PEAK}. Therefore, it is always safer to choose the inductor saturation current higher than the switch current limit.

External Diode

An external power diode between the SW and GND pins is needed for the SGM61432 to complete the converter. This diode must tolerate the application's absolute maximum ratings. The reverse blocking voltage must be higher than V_{IN_MAX} and its peak current must be above the maximum inductor current. Choose a diode with small forward voltage drop for higher efficiency. Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 50V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SGM61432.

Output Capacitor

Three primary criteria must be considered for design of the output capacitor (C_{OUT}):

1. The converter pole location.
2. The output voltage ripple.
3. The transient response to a large change in load current.

The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually a more stringent criterion in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step).

APPLICATION INFORMATION (continued)

Equation 11 can be used to calculate the minimum output capacitance that is needed to supply a current step (ΔI_{OUT}) for at least 2 cycles until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} \quad (11)$$

where:

ΔI_{OUT} is the change in output current.

ΔV_{OUT} is the allowable change in the output voltage.

For example, if the acceptable transient from 1.75A to 3.5A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V and ΔI_{OUT} = 1.75A, the minimum required capacitance will be 28μF. Note that the impact of output capacitor ESR on the transient is not taken into account in Equation 11. For ceramic capacitors, the ESR is generally small enough to ignore its impact on the calculation of ΔV_{OUT} transient. However, for aluminum electrolytic and tantalum capacitors, or high current power supplies, the ESR contribution to ΔV_{OUT} must be considered.

When the load steps down, the excess inductor current will charge the capacitor and the output voltage will overshoot. The catch diode current cannot discharge C_{OUT}, so C_{OUT} must be large enough as given in Equation 12 to absorb the excess inductor energy with limited over-voltage. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the desired output voltage during these transient periods. Equation 12 calculates the minimum capacitance required to keep the output-voltage overshoot to a desired value.

$$C_{OUT} > L \times \frac{I_{OUT\_H}^2 - I_{OUT\_L}^2}{(V_{OUT} + \Delta V_{OUT})^2 - V_{OUT}^2} \quad (12)$$

For example, if the acceptable transient from 3.5A to 1.75A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 5V = 0.25V, the minimum required capacitance will be 24.4μF.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (13)$$

where:

I_{OUT_H} is the high level of the current step.

I_{OUT_L} is the low level of the current step.

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 13. For a specific output capacitance value, use Equation 14 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement.

$$ESR_{COUT} < \frac{V_{OUT\_RIPPLE}}{\Delta I_L} - \frac{1}{8 \times f_{SW} \times C_{OUT}} \quad (14)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, 2 × 47μF/25V X5R ceramic capacitors with 1.5mΩ of ESR are used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 15 calculates the RMS current that the output capacitor must support. In this example, it is 371mA.

$$I_{COUT\_RMS} = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{\sqrt{12} \times V_{IN\_MAX} \times L \times f_{SW}} \quad (15)$$

Bootstrap Capacitor Selection

Use a 0.1μF high-quality ceramic capacitor (X7R or X5R) with 10V or higher voltage rating for the bootstrap capacitor (C_5). A 5Ω to 10Ω resistor (R_4) can be added in series with C_5 to slow down switch-on speed of the high-side switch and reduce EMI if needed. Too high values for R_4 may cause insufficient C_5 charging in high duty-cycle applications. Slower switch-on speed will also increase switch losses and reduce efficiency.

UVLO Setting

The Input UVLO can be programmed using an external voltage divider on the EN pin of the SGM61432. In this design R_1 is connected between VIN pin and EN pin and R_2 is connected between EN pin and GND (see Figure 5). The UVLO has two thresholds (hysteresis), one for power-up (turn-on) when the input voltage is rising and one for power-down (turn-off) when the voltage is falling. In this design, the turn-on (enable to start switching) occurs when V_{IN} rises above 6.74V (UVLO rising threshold). When the regulator is working, it will not stop switching (disabled) until the input falls below 5.52V (UVLO falling threshold). Equations 1 and 2 are provided to calculate the resistors. For this example, the nearest standard resistor values are R_1 = 221kΩ and R_2 = 48.7kΩ.

APPLICATION INFORMATION (continued)

Feedback Resistors Setting

Use an external resistor divider (R_5 and R_6) to set the output voltage using Equations 16 and 17.

$$R_5 = R_6 \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}} \right) \quad (16)$$

$$V_{OUT} = V_{REF} \times \left(\frac{R_5}{R_6} + 1 \right) \quad (17)$$

For this example, 12kΩ was selected for R_6. Using Equation 16, R_5 is calculated as 68kΩ.

Layout Considerations

PCB is an essential element of any switching power supply. The converter operation can be significantly disturbed due to the existence of the large and fast rising/falling voltages that can couple through stray capacitances to other signal paths, and also due to the large and fast changing currents that can interact through parasitic magnetic couplings, unless those interferences are minimized and properly managed in the layout design. Insufficient conductance in copper traces for the high current paths results in high resistive losses in the power paths and voltage errors. Following the guidelines provided here are necessary to design a good layout:

- Bypass VIN pin to GND pin with low-ESR ceramic capacitors (X5R or X7R or better dielectric) placed as close as possible to VIN pin and the catch diode anode pin.
- Minimize the area and path length of the loop formed by VIN pin, bypass capacitors connections, SW pin and the catch diode.
- Connect the device GND pin directly to the exposed pad (Power Pad) copper area under the IC device.
- Stitch the exposed pad to the internal ground planes and the back side of the PCB directly under the IC using multiple thermal vias.
- Use a short and wide path for routing the SW pin to the cathode of the catch diode on the same layer and to the output inductor.
- Keep the SW area minimal and away from sensitive signals like FB input and divider resistors or RT/CLK to avoid capacitive noise coupling.
- Top side GND plane that is connected to the exposed pad provides the best heat removal path for the IC. It should be large enough for designs that operate with full rated loads. Thicker copper planes can improve heat dissipation.
- Place the RT resistor (R_3) as close as possible to the RT/CLK pin with short routes.

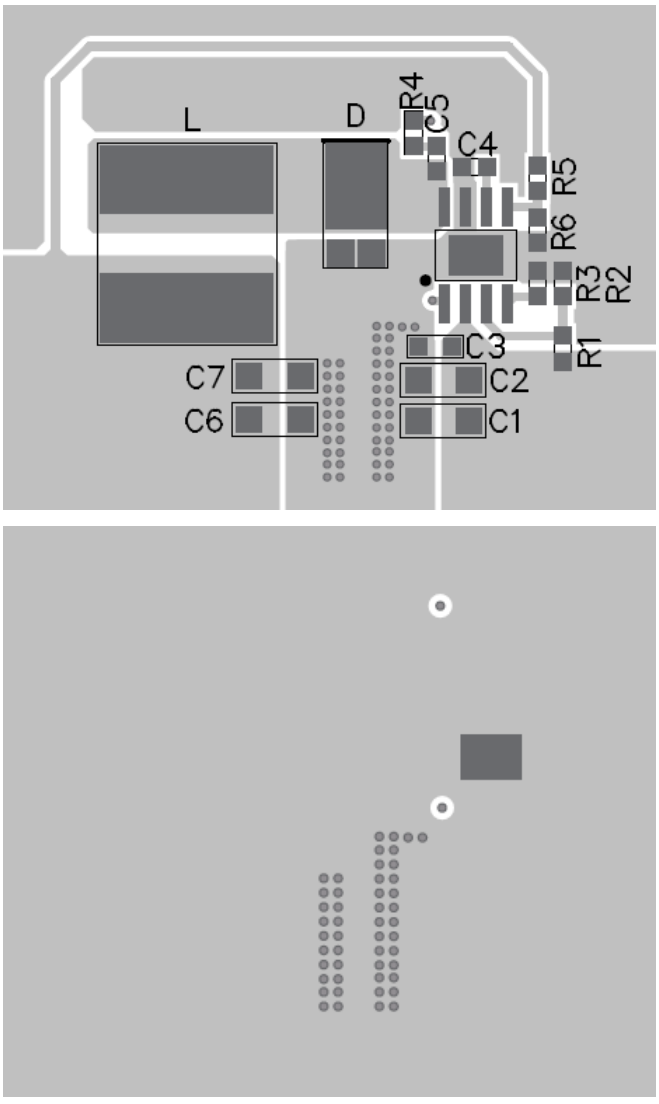


Figure 6. Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

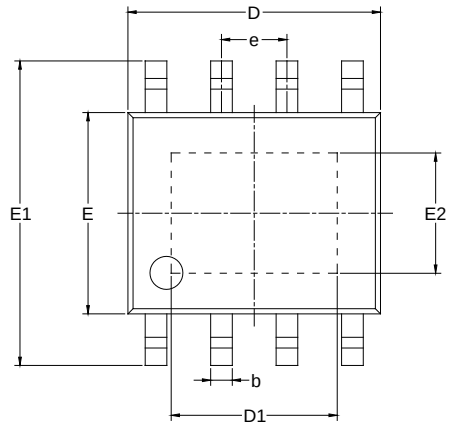
MAY 2023 – REV.A.1 to REV.A.2	Page
Updated Typical Performance Characteristics and Layout	7, 16

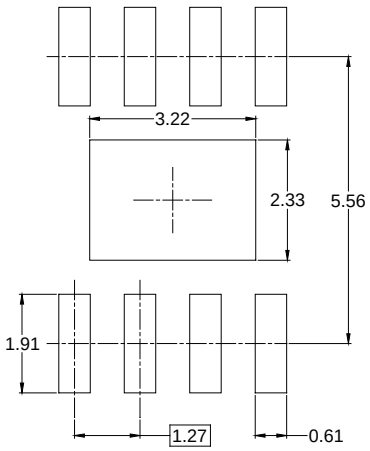
APRIL 2023 – REV.A to REV.A.1	Page
Updated Functional Block Diagram, Detailed Description and Application Information sections	10, 11, 12, 13

Changes from Original (MARCH 2022) to REV.A	Page
Changed from product preview to production data	All

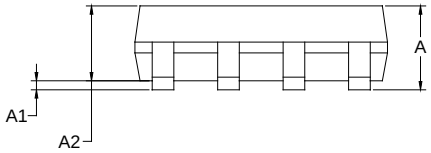
PACKAGE OUTLINE DIMENSIONS

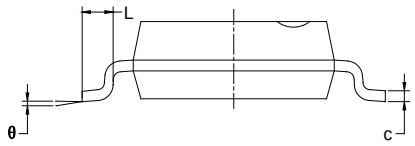
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)





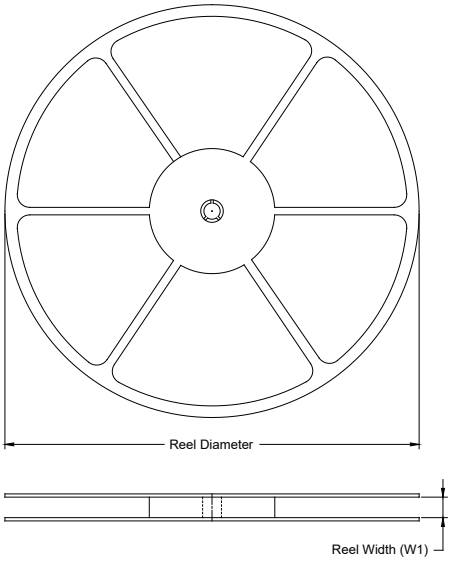
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A			1.700
A1	0.000	-	0.150
A2	1.250	-	1.650
b	0.330	-	0.510
c	0.170	-	0.250
D	4.700	-	5.100
D1	3.020	-	3.420
E	3.800	-	4.000
E1	5.800	-	6.200
E2	2.130	-	2.530
e	1.27 BSC		
L	0.400	-	1.270
θ	0°	-	8°

NOTES:

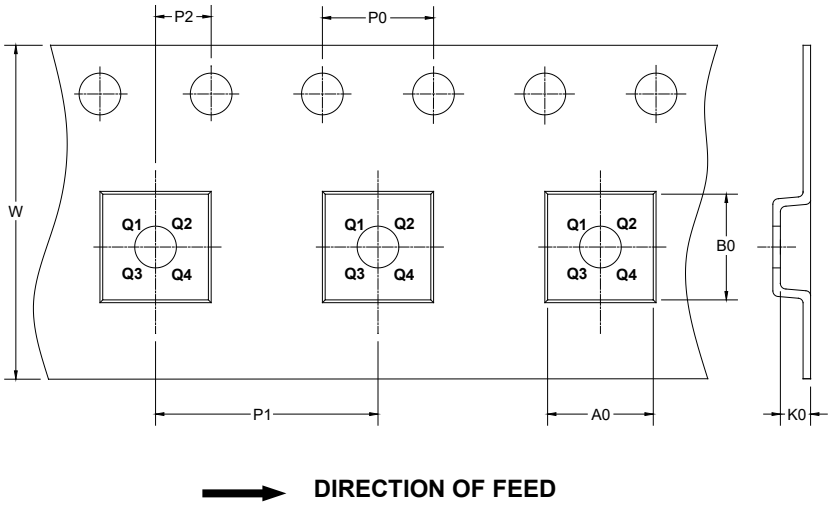
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



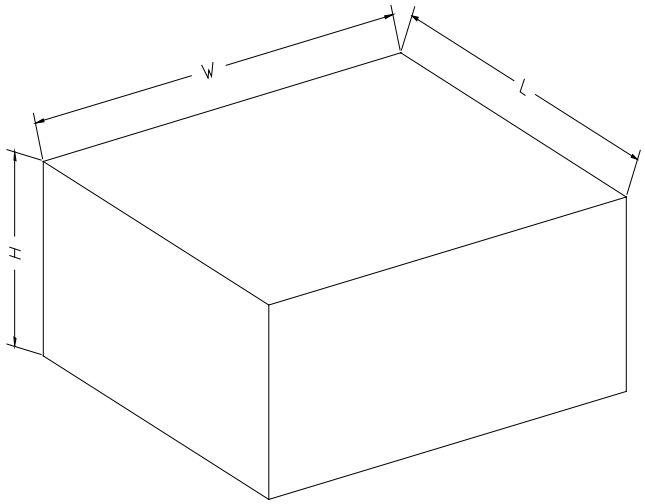
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002