SGM64200
Dual-Output or Two-Phase Synchronous Buck Controller

GENERAL DESCRIPTION

The SGM64200 integrates two synchronous Buck controllers which can be configured as two independent single-phase outputs or one dual-phase output. Two devices can also be linked up as a master-slave through an external pin to provide four single-phase outputs or two dual-phase outputs. The switching phases of linked devices are adjustable to achieve four phases interleaving. The device accepts an input range from 3V to 20V with a precise reference voltage of 0.6V.

The controllers employ fixed frequency voltage mode PWM regulation scheme. Separated enable, current-sense and PGOOD pins are incorporated to allow soft-start times and current limits to be programmable individually. The device offers individual over-current, output over-voltage and output under-voltage protections.

APPLICATIONS

Servers
Telecom Base Station
Switcher and Router Networking
Multiple Rail or Storage System
xDSL Broadband Access

FEATURES

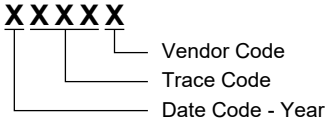
- **Two Single-Phase or One Dual-Phase Outputs**
- **SYNC Pin with One Cycle Clock Recovery**
- **PHASE Pin with 0°/180° or 90°/270° Operation**
- **Two Devices in Master-Slave Mode**
- **Wide Input Supply from 3V to 20V**
- **Precise Reference of 600mV: ±0.75%**
- **Adjustable Output from 0.6V to 5.4V**
- **Adjustable Frequency from 100kHz to 1MHz**
- **Voltage Mode PWM with Input Feedforward**
- **Dual N-MOSFET Drivers with Integrated Bootstrap Switch**
- **Accurate Inductor DCR or Resistor Current Sense**
- **Individual Power Good Open-Drain Pin**
- **Individual Enable Pin & Programmable Soft-Start Time Capable of Pre-Bias Startup**
- **Accurate Current Sharing in Dual-Phase**
- **Remote Output Sense Amplifier in Dual-Phase**
- **Individual Over-Current Limit Set**
- **Cycle-by-Cycle Over-Current Limit with Hiccup**
- **Input Supply Under-Voltage Lock-Out Pin**
- **Individual Output Over-Voltage/Under-Voltage Protection**
- **Thermal Shutdown Protection**
- **Available in a Green TQFN-5×5-32AL Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM64200	TQFN-5×5-32AL	-40℃ to +125℃	SGM64200XTRX32G/TR	SGM64200 XTRX32 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... -0.3V to 22V
SW1, SW2 Voltage ..... -3V to 27V
SW1, SW2 Voltage (< 100ns Pulse Width) .....-5V
SW1, SW2 Voltage (< 10ns Pulse Width) ..... -7.5V to 30V
BST1, BST2 Voltage ..... -0.3V to 30V
BST1, BST2 Voltage (< 10ns Pulse Width) ..... -0.5V to 33V
VDD6V Voltage ..... -0.3V to 7V
HS1, HS2 Voltage ..... -2V to 30V
BST1-SW1, BST2-SW2, HS1-SW1, HS2-SW2 Voltage (Differential from BST or HS to SW) ..... -0.3V to 7V
All Other Pins Voltage ..... -0.3V to 7V
Package Thermal Resistance
TQFN-5×5-32AL, θ_{JA} ..... 35℃/W
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range .....3V to 20V
Operating Junction Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

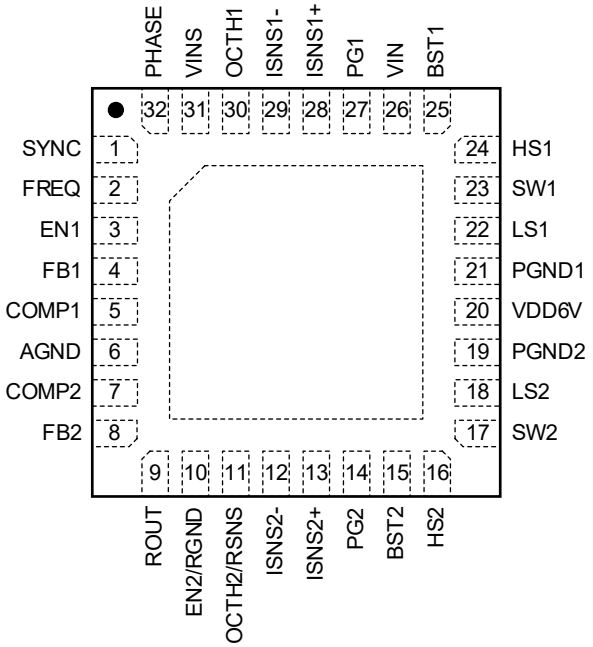
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-5×5-32AL

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	SYNC	In master mode, the internal 2x free running clock, set by FREQ pin, is driven out at SYNC pin. The 2x free running clock is at 50% duty cycle. In slave mode, the device can be synchronized to an external clock which is ±20% of the 2x free running clock. This pin must be left floating while not being used.
2	FREQ	Connect a resistor from this pin to AGND to set the internal free running clock. This pin is normally regulated at 0.8V.
3	EN1	Input pin to start and stop CH1. Pulling this pin low disables CH1 while connecting this pin to AGND through a capacitor enables CH1. The capacitor is charged with an internal current source of 10μA to control the soft-start time. The ramp voltage of this pin is shifted down by 0.85V before applying to the second non-inverting input to the error amplifier of CH1.
4	FB1	Inverting input of the error amplifier of CH1. This pin should be at 0.6V when the output voltage is in regulation.
5	COMP1	Output of the error amplifier of CH1.
6	AGND	Analog Ground.
7	COMP2	Output of the error amplifier of CH2. Connect this pin to COMP1 for dual-phase operation.
8	FB2	Inverting input of the error amplifier of CH2. This pin should be at 0.6V when the output voltage is in regulation. Connecting FB2 pin to the VDD6V pin enables dual-phase operation.
9	ROUT	Output of the remote sense differential amplifier. Connect this pin to the sense resistor of CH1 in dual-phase operation. This pin must be left floating while not being used.
10	EN2/RGND	Input pin to start and stop CH2. Pulling this pin low disables CH2 while connecting this pin to AGND through a capacitor enables CH2. The capacitor is charged by an internal current source of 10μA to control the soft-start time. The ramp voltage of this pin is shifted down by 0.85V before applying to the second non-inverting input to the error amplifier of CH2. In dual-phase operation, this pin serves as the negative input (RGND) of the remote sense differential amplifier.

PIN DESCRIPTION (continued)

PIN	NAME	DESCRIPTION
11	OCTH2/RSNS	Connect a resistor from this pin to AGND. A precise 10μA current source flowing out from this pin through the resistor to AGND adjusts the over-current limit of CH2. In two-phase mode, this pin serves as the positive input (RSNS) of the remote sense differential amplifier.
12	ISNS2-	Negative input of current sense amplifier of CH2.
13	ISNS2+	Positive input of current sense amplifier of CH2.
14	PG2	Open-drain power good output of CH2. Connect a pull-up resistor to this pin.
15	BST2	Bootstrapped supply of the high-side driver of CH2. Connect a 0.1μF ceramic capacitor from this pin to SW2 pin.
16	HS2	High-side driver output of CH2.
17	SW2	Return path of the high-side driver of CH2.
18	LS2	Low-side driver output of CH2.
19	PGND2	Power ground of CH2 and return path of the low-side driver of CH2. Connect this pin to AGND at a single point.
20	VDD6V	Output of the internal 6V regulator. Connect a low ESR ceramic capacitor of at least 3.3μF from this pin to AGND.
21	PGND1	Power ground of CH1 and return path of the low-side driver of CH1. Connect this pin to AGND at a single point.
22	LS1	Low-side driver output of CH1.
23	SW1	Return path of the high-side driver of CH1.
24	HS1	High-side driver output of CH1.
25	BST1	Bootstrapped supply of the high-side driver of CH1. Connect a 0.1μF ceramic capacitor from this pin to SW1 pin.
26	VIN	Supply input of the device. Connect a low ESR ceramic capacitor of at least 1μF from this pin to AGND.
27	PG1	Open-drain power good output of CH1. Connect a pull-up resistor to this pin.
28	ISNS1+	Positive input of current sense amplifier of CH1.
29	ISNS1-	Negative input of current sense amplifier of CH1.
30	OCTH1	Connect a resistor from this pin to AGND. A precise 10μA current source flowing out from this pin through the resistor to AGND adjusts the over-current limit of CH1. In two-phase mode, this pin also adjusts the over-current limit.
31	VINS	Connect this pin to the supply voltage through a resistive divider to AGND to control the minimum operating voltage of the device.
32	PHASE	Set master or slave mode, and select the operating phase.
—	Exposed Pad	Thermal Exposed Pad. It is the main thermal relief path of the die connected to the ground plan on the PCB.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, V_{VIN} = 12V, R_{FREQ} = 40kΩ, f_{SW} = 500kHz, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply							
Input Voltage Range		V_{VIN}		3		20	V
Shutdown		I_{VINSD}	$V_{EN1/2}$ = 0V		170	240	μA
Quiescent, Non-Switching		I_{VINQ}	V_{FB} = 0.65V, EN1/EN2 float		5.2	7	mA
VINS UVLO							
Minimum Turn-on Voltage		UVLO		1.21	1.24	1.27	V
Hysteresis Current		$UVLO_{HYS}$		13	15	17	μA
VDD6V Regulator							
Regulator Voltage		V_{VDD6V}	V_{VIN} = 7V to 20V	5.7	6	6.3	V
Regulator Dropout Voltage		$V_{VDD6VDO}$	I_{VDD6V} = 25mA, V_{VIN} = 3V		85	150	mV
Regulator Continuous Current Limit (1)		I_{VDD6V}		110			mA
Regulator Output UVLO		$V_{VDD6V-UVLO}$		2.5	2.75	2.98	V
Regulator Output UVLO Hysteresis		$V_{VDD6V-HYS}$		160	210	270	mV
Oscillator and Ramp Generator							
Oscillator Frequency		f_{SW}		100		1000	kHz
			R_{FREQ} = 40kΩ	470	500	530	kHz
Ramp Amplitude (Peak-to-Peak)		V_{RAMP}	3V < V_{VIN} < 20V		V_{VIN}/8.5		V
Valley Voltage		V_{VAL}			0.85		V
Master Clock Frequency		f_{MASTER}		200		2000	kHz
Percent of Master Frequency for Synchronization		Δf_{SYNC}		-20		20	%
SYNC Frequency Range		f_{SYNC}		200		2000	kHz
SYNC Input Minimum Pulse Width		$t_{PW(SYNC)}$		100			ns
Rising Edge Threshold to Set Sync Pulse		$V_{H(SYNC)}$		2			V
Falling Edge Threshold to Reset Sync Pulse		$V_{L(SYNC)}$				0.8	V
PHASE Set Voltage	Master	V_{PHASE}	0°/180° phase shift			0.5	V
	Slave		0°/180° phase shift		Float		V
	Slave		90°/270° phase shift	2.3			V
PWM							
Minimum PWM Off-Time		$PWM_{(OFF)}$			110	155	ns
Minimum Controllable Pulse Width (1)		$t_{ON(MIN)}$			110		ns
Output Driver Dead Time		$t_{DEAD-HL}$	HS off to LS on	10	30	50	ns
		$t_{DEAD-LH}$	LS off to HS on	10	30	50	ns
Error Amplifier and Voltage Reference							
FB Input Voltage		V_{FB}	0℃ < T_J < +70℃	594.5	600	604.5	mV
			-40℃ < T_J < +125℃	593	600	607	
FB Input Bias Current		I_{FB}			10	130	nA
Unity Gain Bandwidth (1)		G_{BW}			24		MHz
Open Loop Gain (1)		A_{EA}		80			dB
High-Level Output Current		I_{EAH}			3		mA
Low-Level Output Current		I_{EAL}			9		mA
Enable and Soft-Start							
High-Level Input Voltage		V_{IH}		0.55	0.77	1	V
Low-Level Input Voltage		V_{IL}		0.2	0.26	0.32	V

ELECTRICAL CHARACTERISTICS (continued)

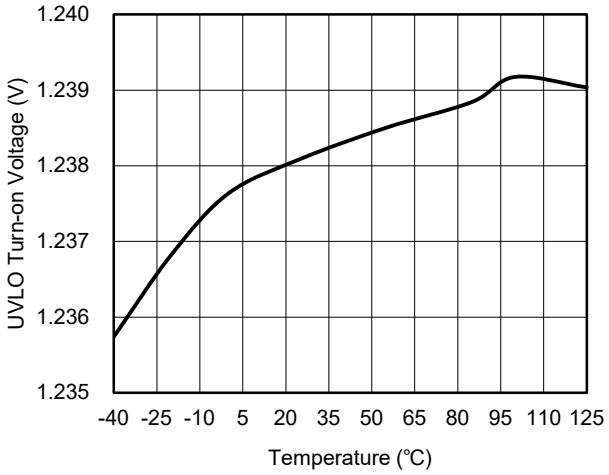
(T_J = -40℃ to +125℃, V_{VIN} = 12V, R_{FREQ} = 40kΩ, f_{SW} = 500kHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Source Current	I_{SS}		8	10	12	μA
Soft-Start Voltage Level	V_{SS}			0.8		V
Soft-Start Discharge Current	I_{DISCHG}			130		μA
Over-Current Protection						
OCTH Program Current	I_{OCTH}	T_J = +25℃	9.2	10	10.8	μA
Hiccup Cycles to Recover	t_{HICCUP}			6		Cycles
Current Sense Amplifier						
Differential Input Voltage Range	$V_{CS-DIFF}$		-60		60	mV
Input Common Mode Range	V_{CS-CM}		0		5.6	V
Current Sensing Gain	A_{CS}			15		V/V
Current Sense Amplifier Output	V_{CSOUT}	V_{CSIN} = 20mV, T_J = +25℃	290	300	310	mV
Closed Loop Bandwidth (1)	f_{CS0}		3			MHz
Current Sense Amplifier Output Difference Between CH1 and CH2		V_{CSIN} = 20mV to both ISNS1 and ISNS2	-10		10	mV
Over-Voltage and Under-Voltage Protection						
Feedback Voltage Limit for OVP	V_{OVP}		670	700	730	mV
Feedback Voltage Limit for UVP	V_{UVP}		480	505	530	mV
Gate Drivers						
High-side Driver Pull-Up Resistance	R_{HSHI}	V_{BST} - V_{SW} = 6.0V, I_{HS} = -40mA	0.6	1.05	1.5	Ω
High-side Driver Pull-Down Resistance	R_{HSLO}	V_{BST} - V_{SW} = 6.0V, I_{HS} = 40mA	0.2	0.65	1.1	Ω
Low-side Driver Pull-Up Resistance	R_{LSHI}	I_{LS} = -40mA	0.6	1.05	1.5	Ω
Low-side Driver Pull-Down Resistance	R_{LSLO}	I_{LS} = 40mA	0.2	0.55	0.9	Ω
High-side Driver Rise Time (1)	t_{HRISE}	C_{LOAD} = 5nF		15		ns
High-side Driver Fall Time (1)	t_{HFALL}	C_{LOAD} = 5nF		12		ns
Low-side Driver Rise Time (1)	t_{LRISE}	C_{LOAD} = 5nF		15		ns
Low-side Driver Fall Time (1)	t_{LFALL}	C_{LOAD} = 5nF		10		ns
Boot Switch						
Bootstrap Switch Voltage Drop	V_{BDFWD}	I_{BST} = 5mA		0.035		V
Remote Sense						
Input Offset Voltage	$V_{IOFFSET}$	V_{ROUT} = 0.9V	-6		6	mV
Differential Gain	A_{RS}		0.995		1.005	V/V
Close Loop Bandwidth (1)	f_{RS0}		2			MHz
Output Voltage at ROUT Pin	V_{ROUT}				V_{VDD6V} - 0.2	V
Output Source Current	I_{SRC}				1	mA
Output Sink Current	I_{SNK}				1	mA
Power Good						
Feedback Voltage Limit for PGOOD	V_{OV}		650	675	700	mV
Feedback Voltage Limit for PGOOD	V_{UV}		505	525	545	mV
PGOOD Hysteresis Voltage at FB	$V_{PGD-HYST}$			25	45	mV
PGOOD Pull Down Resistance	R_{RGD}			35	55	Ω
PGOOD Leakage Current	$I_{PGD-LEAK}$				0.5	μA
Thermal Shutdown						
Junction Shutdown Temperature (1)	T_{SD}			155		℃
Hysteresis (1)	$T_{SD-HYST}$			20		℃

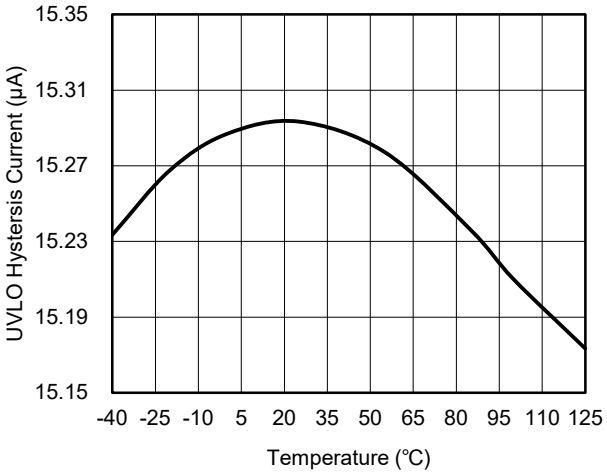
NOTE: 1. Specified by design. Not production tested.

TYPICAL PERFORMANCE CHARACTERISTICS

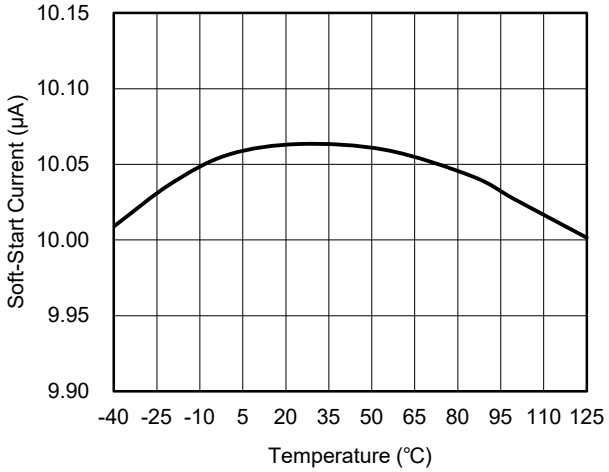
UVLO Turn-on Voltage vs. Temperature



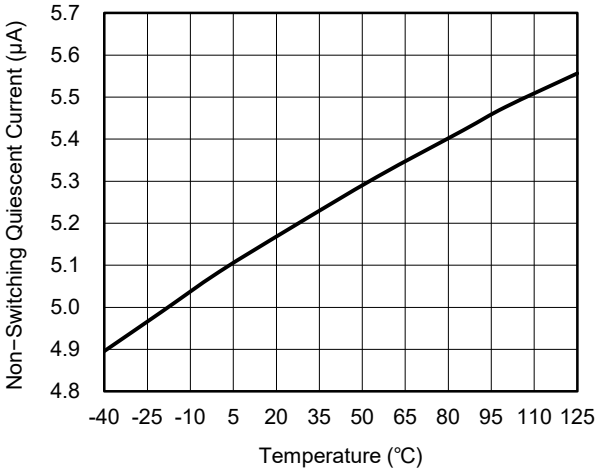
UVLO Hystersis Current vs.Temperature



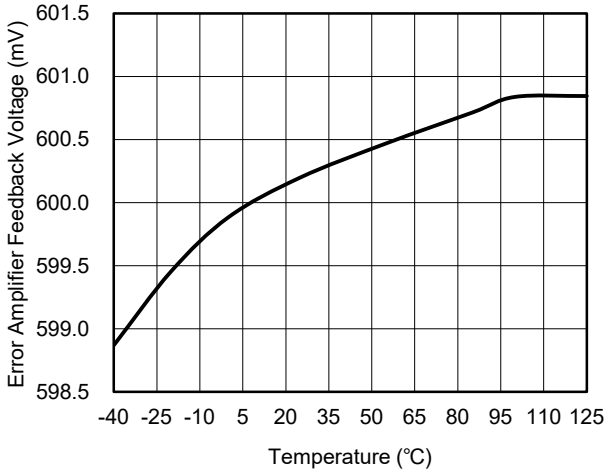
Soft-Start Current vs. Temperature



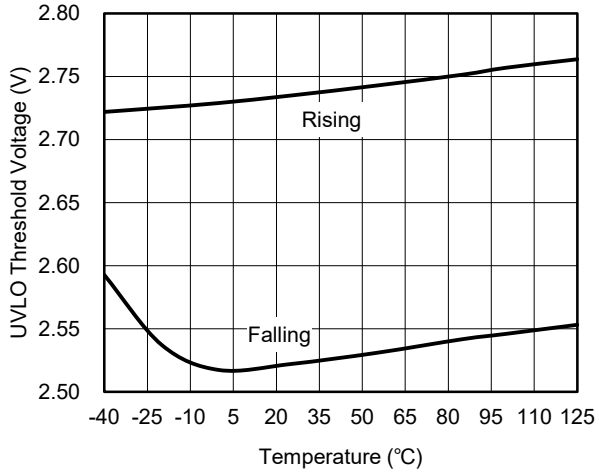
Non-Switching Quiescent Current vs. Temperature



Error Amplifier Feedback Voltage vs. Temperature

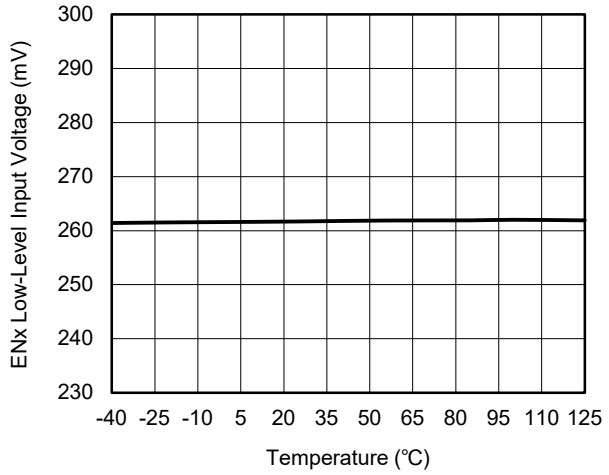


BP UVLO Threshold vs. Temperature

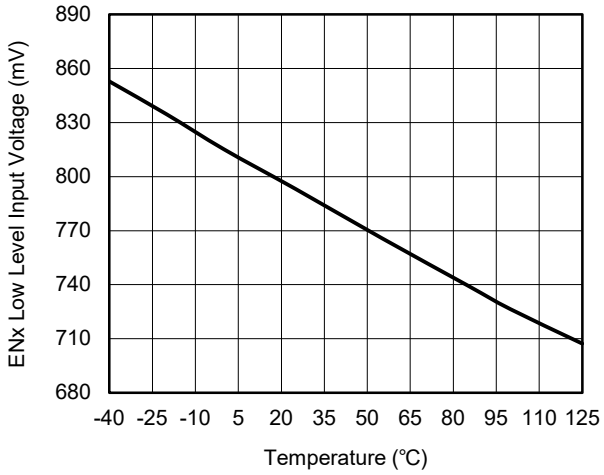


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

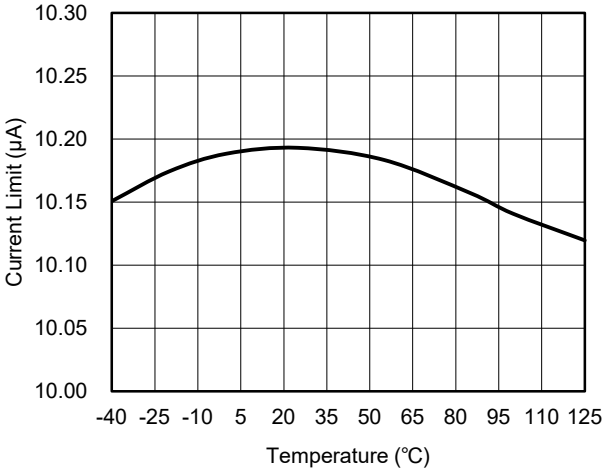
ENx Low-Level Input Voltage vs. Temperature



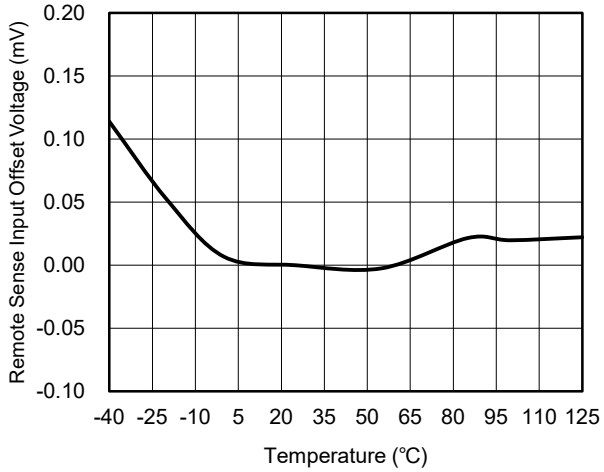
ENx High-Level Input Voltage vs. Temperature



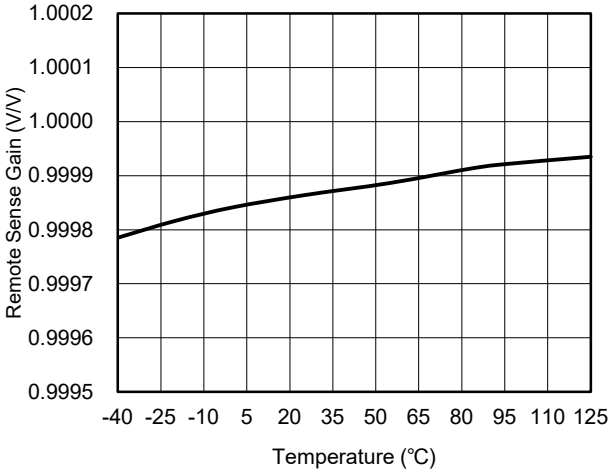
Current Limit vs. Temperature



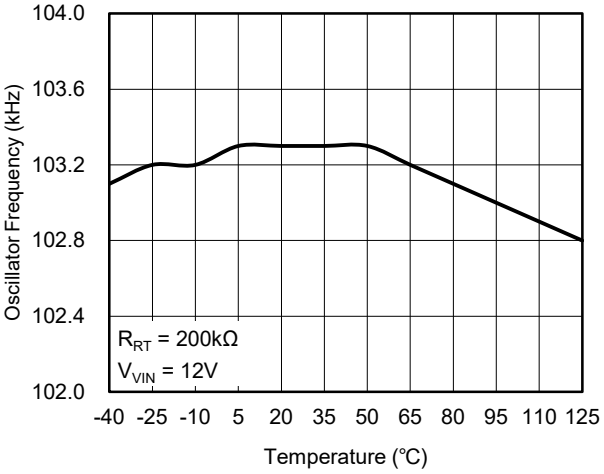
Remote Sense Input Offset Voltage vs. Temperature



Remote Sense Gain vs. Temperature

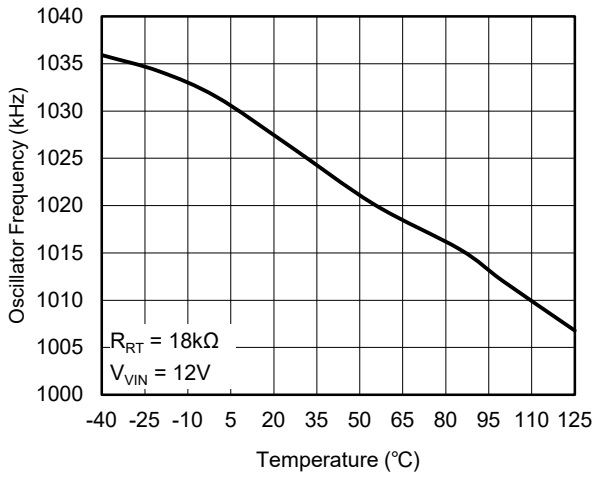


Oscillator Frequency vs. Temperature

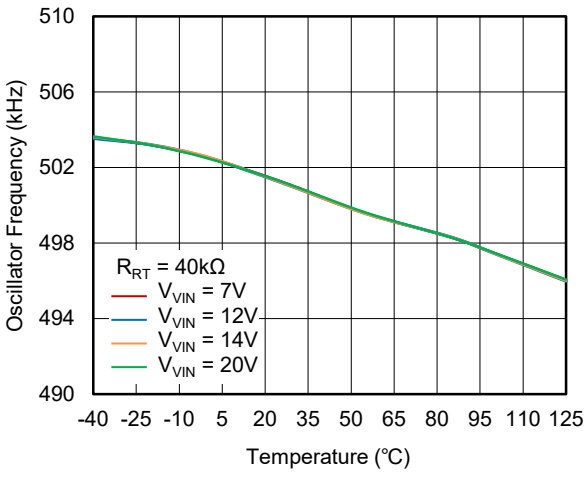


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

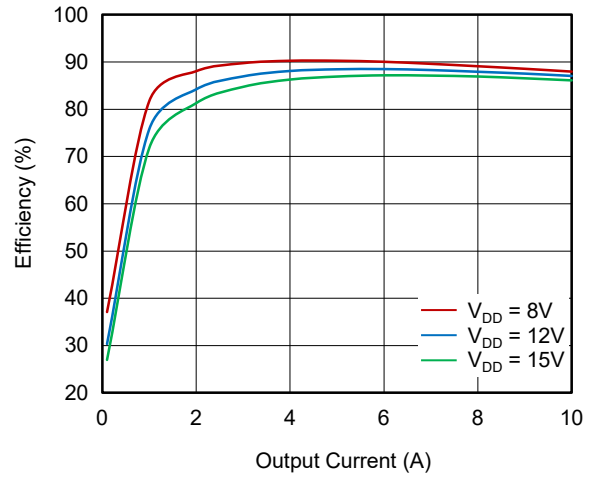
Oscillator Frequency vs. Temperature



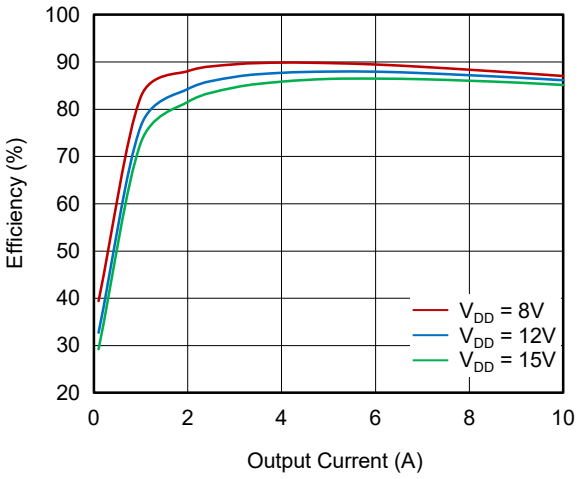
Oscillator Frequency vs. Temperature



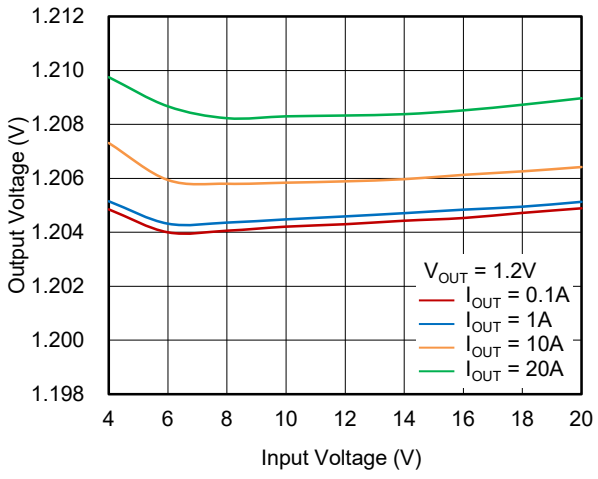
Efficiency vs Load Current (8V to 15V to 1.2V at 10A, Example 1)



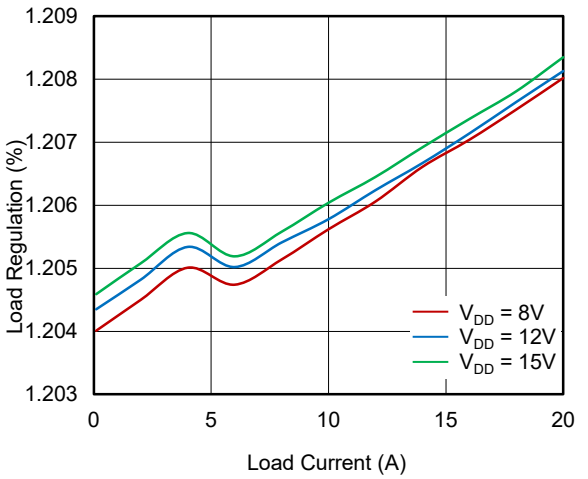
Efficiency vs Load Current (8V to 15V to 1.8V at 10A, Example 1)



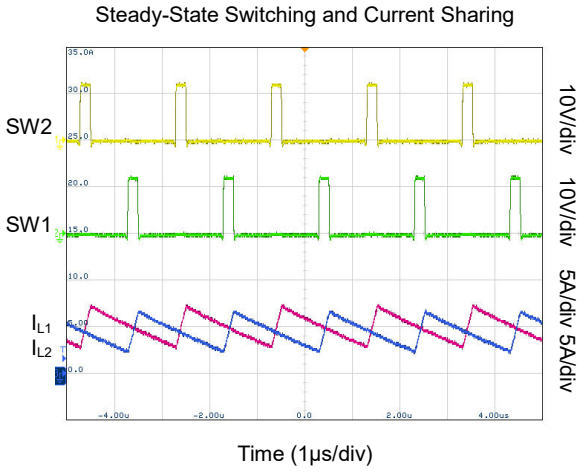
Line Regulation



Load Regulation



TYPICAL PERFORMANCE CHARACTERISTICS (continued)



TYPICAL APPLICATION CIRCUIT

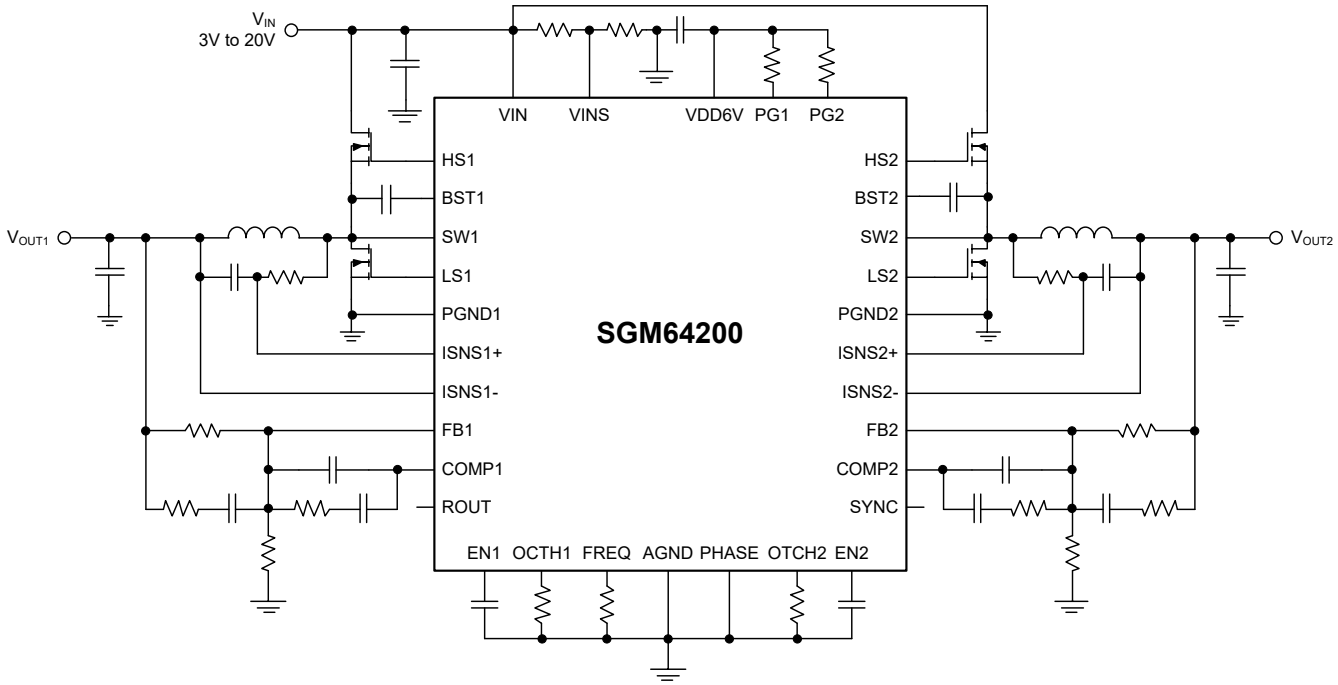


Figure 1. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

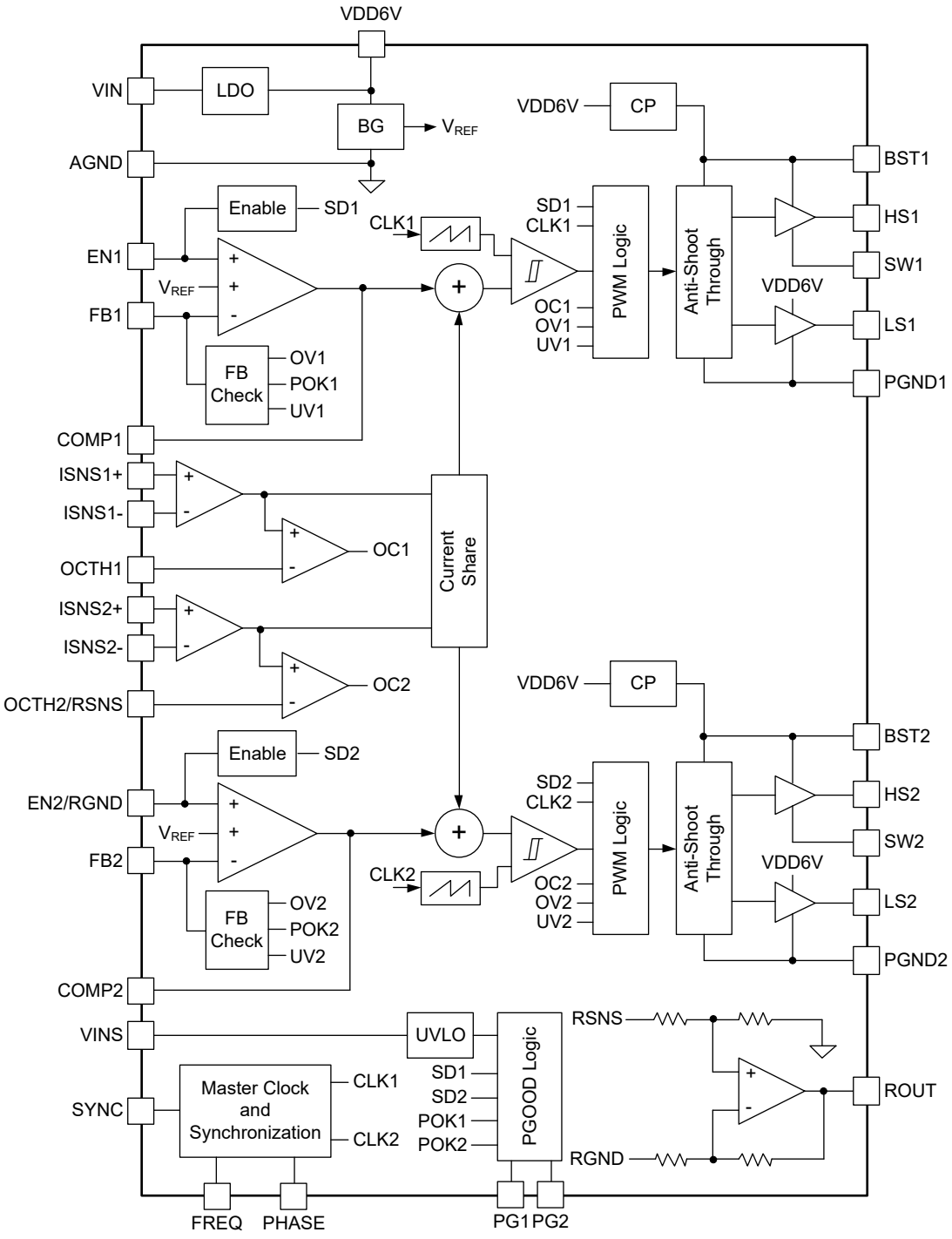


Figure 2. Block Diagram

DETAILED DESCRIPTION

The SGM64200 is a two-phase single output/two-way output Buck controller. The input voltage range is 3V to 20V, and the minimum output voltage is 600mV.

In the case of two outputs, the controller is in voltage control mode with input voltage feedforward. Its advantage is that it is insensitive to noise, and there is no control instability in DCR applications. Besides, it has a small minimum on-time, which can produce lower output voltage.

Under the condition of two-phase single output, two-phase current sharing can be achieved, so as to balance two-phase heating. Since the detected current sharing error signal is relatively small, the whole loop can be modeled according to the voltage mode with feedforward.

When the device operates under two outputs, the ROUT pin must leave floating.

Voltage Reference

The 600mV bandgap reference is connected to the positive input end of the amplifier. This reference voltage can be adjusted in a unity gain configuration, thereby eliminating the voltage cheapness in applications. The reference voltage with a tolerance of 0.5% allows the customer to design a very precise power supply.

Output Voltage Setting

The output voltage of SGM64200 is regulated by external resistance, as shown in Figure 3. The regulated voltage is obtained by Equation 1.

$$V_{OUT} = 0.6V \times \left(1 + \frac{R_A}{R_{BIAS}}\right) \quad (1)$$

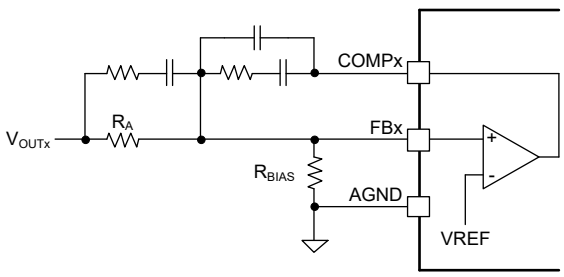


Figure 3. Setting the Output Voltage

Input Voltage Feedforward

By adding voltage feedforward, the SGM64200 keeps the power stage gain constant when the input voltage changes, and has a fast response to line transition. At the same time, the simple power stage also simplifies the loop design. From the model, the front-end gain from COMP to LC is 8.5V/V.

Current Sensing

The SGM64200 uses differential current detection to detect the output current. It can be DCR of the inductor or precision current detection resistance, which should be added separately. When DCR is used to detect current in Figure 4, parallel RC filter is required to filter out AC voltage component of inductor.

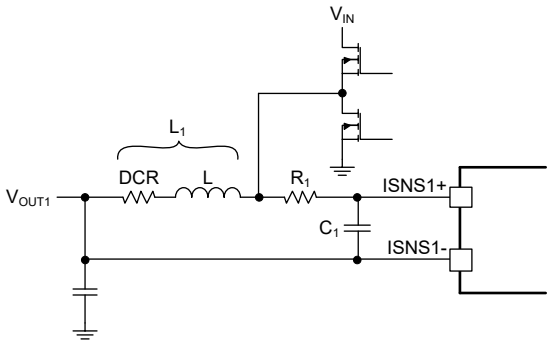


Figure 4. Inductor DCR Current Sensing

Use Equation 2 to calculate R_1 and C_1 for an ideal design.

$$R_1 \times C_1 = \frac{L_1}{DCR} \quad (2)$$

The RC time constant needs to be equal to the time constant of the inductor itself. When their time constants are the same, the voltage on C_1 is equal to the product of the current in the inductor and DCR. At this time, it is generally recommended to select a capacitor of 0.1μF as the value of C_1.

DETAILED DESCRIPTION (continued)

Over-Current Protection

When the SGM64200 operates on two outputs, each channel has an OCTH pin to monitor the current. When operating in two-phase mode, the two channels set the same over-current threshold through OCTH1. The current detection method is to set the over-current threshold voltage by connecting the resistance between the OCTHx pin and AGND in series. The detected current is amplified 15 times internally by the amplifier, and then compare with the over-current threshold to determine whether an over-current fault occurs, as shown in Figure 5 below.

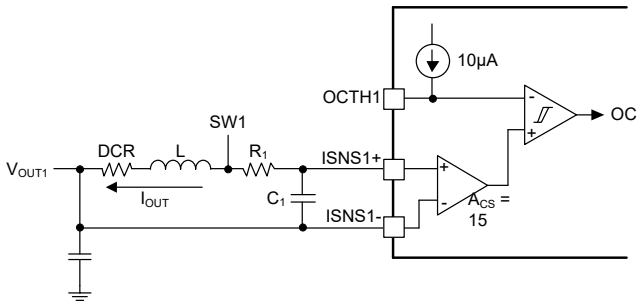


Figure 5. Over-Current Protection

Use Equation 3 to calculate the current limit resistance (R_{OCTH}) of desired over-current limit.

$$R_{OCTH} = \frac{\left(I_{OC} + \frac{I_{RIPPLE}}{2}\right) \times DCR \times A_{CS}}{I_{OCTH}} \quad (3)$$

Where:

I_{OC} is the desired DC over-current limit level.

I_{RIPPLE} is the inductor peak-peak ripple current.

DCR is the inductor DC resistance.

A_{CS} is 15 (TYP). It is the current sensing amplifier gain.

I_{OCTH} is 10μA (TYP). It is the internal source current out of OCTHx pin.

When the inductance current exceeds the set threshold, the SGM64200 will limit the current cycle by cycle. When three times of continuous over-current conditions occur, the high-side MOSFET and low-side MOSFET are turned off, and the controller starts to hiccup. The chip will enter into restart mode after six soft-start processes. When the over-current condition disappears, it works normally, otherwise repeat the above operation.

Two-Phase Mode, Remote Sense Amplifier, and Current Sharing Loop

The SGM64200 can work in the high current two-phase mode. When the appropriate external MOSFET is selected, the system can output the current up to 50A. As shown in Figure 6, when the configuration is in two-phase mode, FB2 is connected to VDD6V, and COMP1 and COMP2 are connected at the same time. For applications with large current, the remote compensation amplifier is used to compensate output voltage drop, so as to adjust the remote voltage to the set value. EN2/RGND and OCTH2 are multiplexing pins, which are used as RSNS and RGND in two-phase mode. ROUT is the output terminal of the compensation amplifier, which is connected to the output voltage divider.

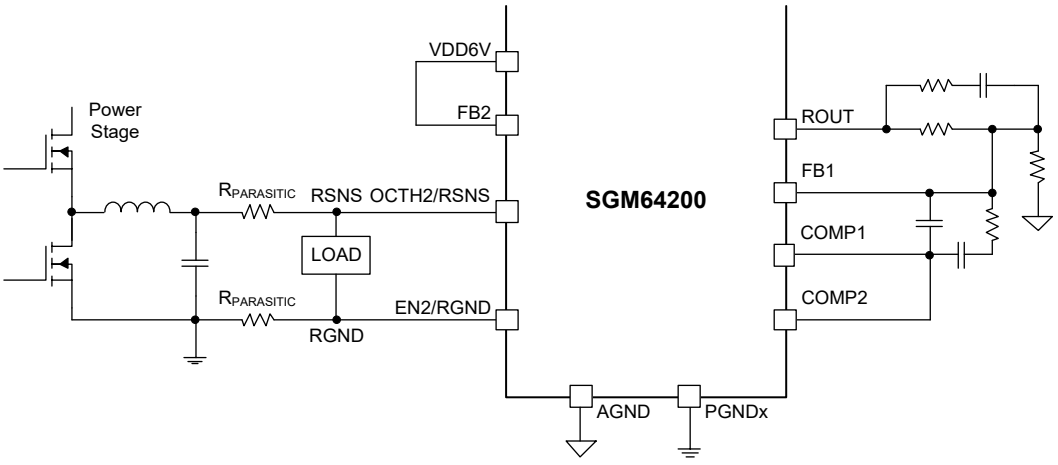


Figure 6. Two Phase Voltage Loop Diagram

DETAILED DESCRIPTION (continued)

The VDD6V supplies power to the remote sense amplifier. Under normal application, the set output voltage must be 0.2V lower than the VDD6V voltage, otherwise, it cannot be adjusted to a proper value. If the output voltage is below 2.2V, the remote sense amplifier can be used. If the output exceeds 2.2V, the amplifier can be omitted, and the remote voltage is directly connected to the resistance voltage divider network.

When the device operates in two-phase mode, the current sharing loop shown in Figure 7 is used to balance two-phase current. The two phases have the same COMP value. Compare to the current of the two phases in the current sharing loop and generate an error signal. The signal acts with the COMP signal to generate their own error signals and compare them with the slope to generate their own PWM pulses.

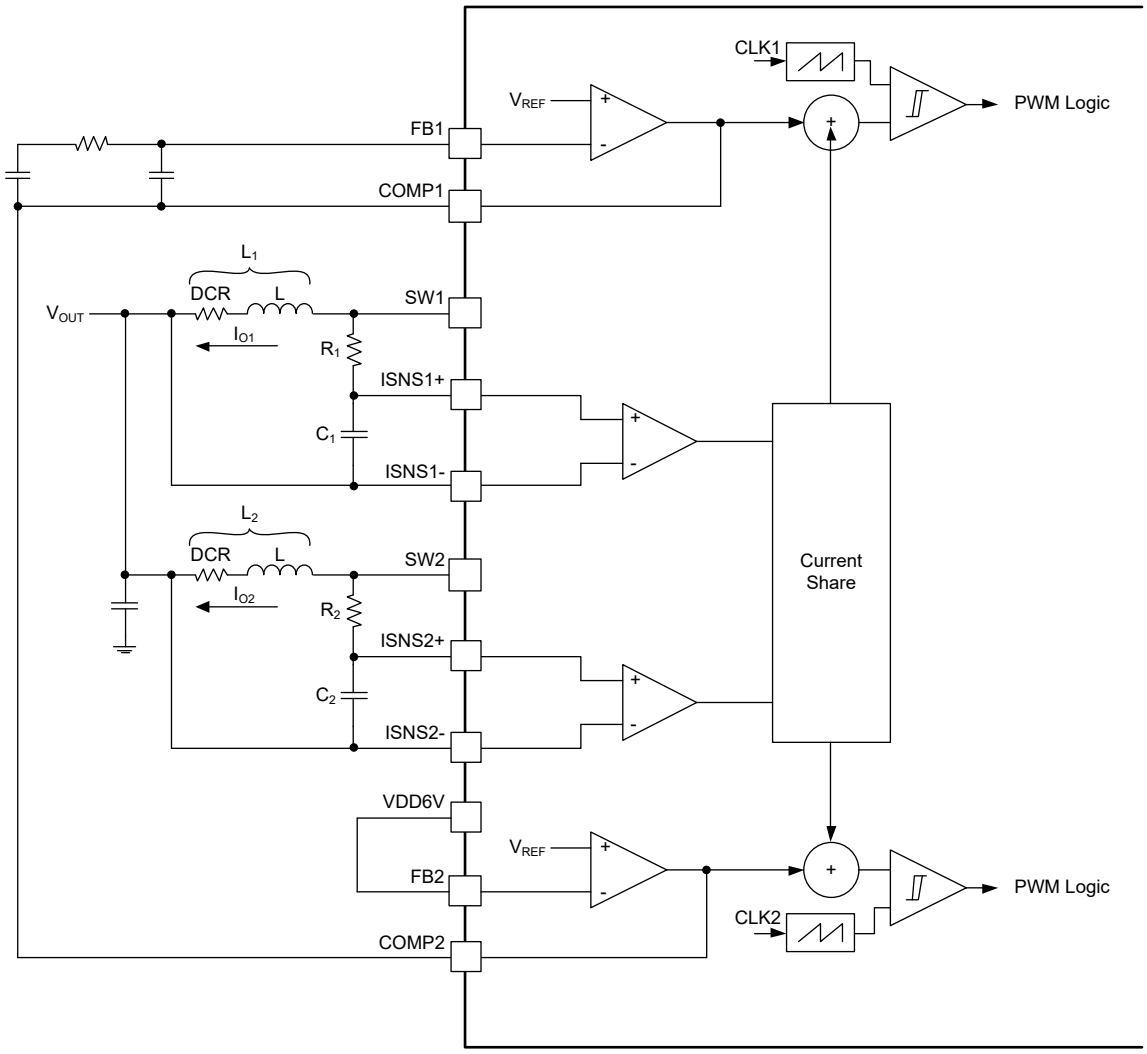


Figure 7. Two Phase Current Sharing Loop Diagram

DETAILED DESCRIPTION (continued)

Start-Up and Shutdown

Start-Up Sequence

When ENx is pulled down below 0.3V, the corresponding channel is turned off, and when ENx is released, the 40μA current source inside the device begins to charge the soft-start capacitor and clamps to 1.3V. When the voltage across the soft-start capacitor exceeds 0.7V, the internal VDD6V linear regulator is enabled. When the VIN, VDD6V, PG, and clock signals are confirmed, ENx is pulled down to 0.4V by the 140μA current source and then charged by the internal 10μA current source. V_{SS_INT} is the voltage of the shifted soft-start capacitor, connected to the non-inverting terminal end of the error amplifier.

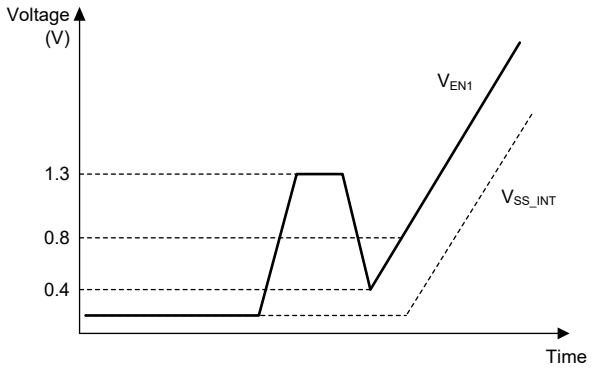


Figure 8. EN Start-up Waveform

The external soft-start capacitor and the charge current source determine the soft-start time together, which is the actual output ramp rise time when the soft-start capacitor is charged up by 600mV. Due to the offset (800mV, TYP) from the actual ENx pin voltage to the V_{SS_INT}, there is some initial hysteresis. The soft-start sequence occurs in a closed-loop fashion, which means that the error amplifier continuously controls the output voltage during soft-start. And the feedback loop remains closed, as happens in a duty cycle limited soft-start design. The error amplifier has two positive inputs. One is connected to the 600mV reference while the other is to V_{SS_INT}. The error amplifier regulates the output voltage to whichever the lower value. When the voltage of the EN pin is raised to 1.4V, the 600mV reference becomes the main input to the error amplifier, and the converter has reached the final regulation voltage. Use equation 4 to calculate the soft-start capacitor, C_{SS}.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{600mV} \quad (4)$$

Where:
t_{SS} is the desired soft-start time,
I_{SS} is 10μA (TYP). It is the internal soft-start current.

Prebiased Output Start-Up

The SGM64200 supports pre-biased startup. During soft-start, it does not generate any PWM pulse until V_{SS_INT} exceeds the FB voltage. Once V_{SS_INT} exceeds the FB voltage, PWM pulses are initiated with very short on-time of synchronous rectifier. The on-time is then gradually increased cycle after cycle to meet the duration determined by (1-D)/f_{SW} where D is the duty cycle. This scheme can prevent sinking of current from the pre-biased output, and support a smooth and controllable ramping of output voltage.

During a soft-start sequence, pulse skipping occurs when the PWM pulse width is shorter than the minimum controllable on-time (typically caused by PWM comparator and gate driver delays) and the output may show a large ripple voltage.

Shutdown

VDD6V is controlled by EN during shutdown, and if the EN pins of both channels are pulled low, VDD6V is disabled regardless of whether the input voltage exceeds the programmed UVLO.

Switching Frequency and Master or Slave Synchronization

The switching frequency is determined by the resistance of the FREQ pin connected to GND, as Equation 5 follows.

$$R_{FREQ} = \frac{20 \times 10^9}{f_{SW}} \quad (5)$$

Where:
R_{FREQ} is the resistor from FREQ pin to AGND in Ω.
f_{SW} is the desired switching frequency in Hz.

DETAILED DESCRIPTION (continued)

The SGM64200 can also be synchronized through an external clock, which can be ±20% of the master clock frequency, please refer to Table 1 to configure the master/slave and phase shift of the SGM64200 by the level of the PHASE pin.

Figure 9 implements a method to reduce the ripple of the input voltage by averaging the phase shift between two SGM64200 devices.

Table 1. Phase Shift Angle Selection

PHASE		Mode	Phase Angle (°)	
Connection	Range (V)		CH1	CH2
AGND	< 0.5	Master	0	180
Floating	0.6 to 2	Slave	0	180
High	> 2.1	Slave	90	270

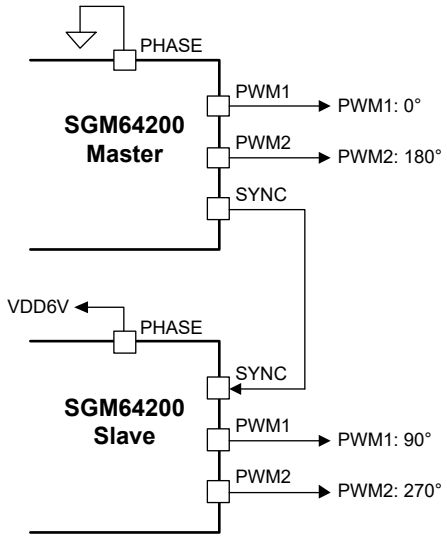


Figure 9. Synchronization Diagram

Over-Voltage and Under-Voltage Fault Protection

The SGM64200 achieves over-voltage/under-voltage detection by sensing the voltage sampled by the FB pin. The compensation network is connected to the FB pin and the COMP pin affects the rate at which the output voltage is sensed. The error amplifier attempts to adjust the output to match the FB to the reference voltage, and if the error amplifier is unable to do so, it triggers over-voltage/under-voltage protection. Please refer to the Electrical Characteristics for more details.

If under-voltage occurs, the device will enter into hiccup mode and keep trying to restart until the fault is recovered.

If over-voltage occurs, the device will shut down the high-side MOSFET and lock the low-side MOSFET to release the output current to the regulated level within the power good window.

In the mode of two outputs, the fault of a single channel does not affect the normal operation of the other, and only the voltage value of the FB1 pin is detected in the two-phase mode, so both channels will take action after the fault is detected.

Input Under-Voltage Lockout (UVLO)

The required threshold voltage can be programmed by a resistor divider through the VINS pin as shown in Figure 10.

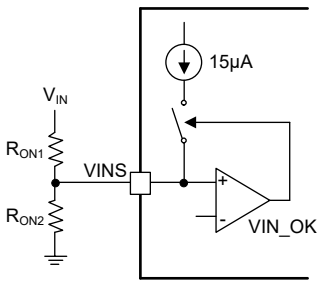


Figure 10. Input UVLO Diagram

Refer to Equation 6 and Equation 7 to calculate the actual required UVLO threshold and hysteresis value.

$$V_{IN\_UVLO} = 1.24 \times \frac{(R_{ON1} + R_{ON2})}{R_{ON2}} \quad (6)$$

$$V_{IN\_HYS} = 15\mu A \times R_{ON1} \quad (7)$$

DETAILED DESCRIPTION (continued)

Power Good

The SGM64200 has pins for each channel to indicate a good output. These pins are open-drain outputs, and the PG pin is pulled low when the feedback voltage (V_{FB}) is not within ±12.5% from nominal or when the soft-start function is active.

Thermal Shutdown

When the junction temperature of the device reaches the thermal shutdown threshold of +150℃, the PWM oscillator shuts down, then the high-side and low-side drivers shut down. The device recovers to a hysteresis value of approximately 20℃, that is, the PWM begins soft-start when the device cools to +130℃.

Connection of Unused Pins

If the application uses only one channel, then some pins of the other channel also need to be properly connected, please refer to Table 2.

Table 2. Phase Shift Angle Selection

Pin Name	Connection
BSTx	Floating.
COMPx	Floating.
ISNSx-	Connect to a voltage between 0V and 5.6V, short to ISNSx+.
ISNSx+	Short to ISNSx-.
ROUT	Floating.
EN1	Connect to ground.
EN2/RGND	Connect to ground.
FBx	Connect to ground.
HSx	Floating.
OCTH1	Connect to ground through a 100kΩ resistor.
OCTH2/RSNS	Connect to ground through a 100kΩ resistor.
LSx	Floating.
PGx	Connect to ground.
PHASE	Connect to ground.
SWx	Connect to ground.
SYNC	Floating.

Device Functional Modes

In dual-output mode, EN1 and EN2/RGND are used to control the enable and shutdown of their channels, respectively. Floating the pins enables the channels and pulling down the pins disables the channels. In a two-phase output configuration, the EN1 pin is used to simultaneously configure the enable and shutdown of both outputs.

APPLICATION INFORMATION

The SGM64200 can be configured as a two-phase output mode or dual output mode.

Dual-Output Mode

This section describes the design calculations and device selection for dual output applications of the controller. Table 3 shows the design objectives. Only the calculation of channel 1 is listed, and the calculation of channel 2 is similar to that of channel 1.

The schematic diagram is shown as Figure 11.

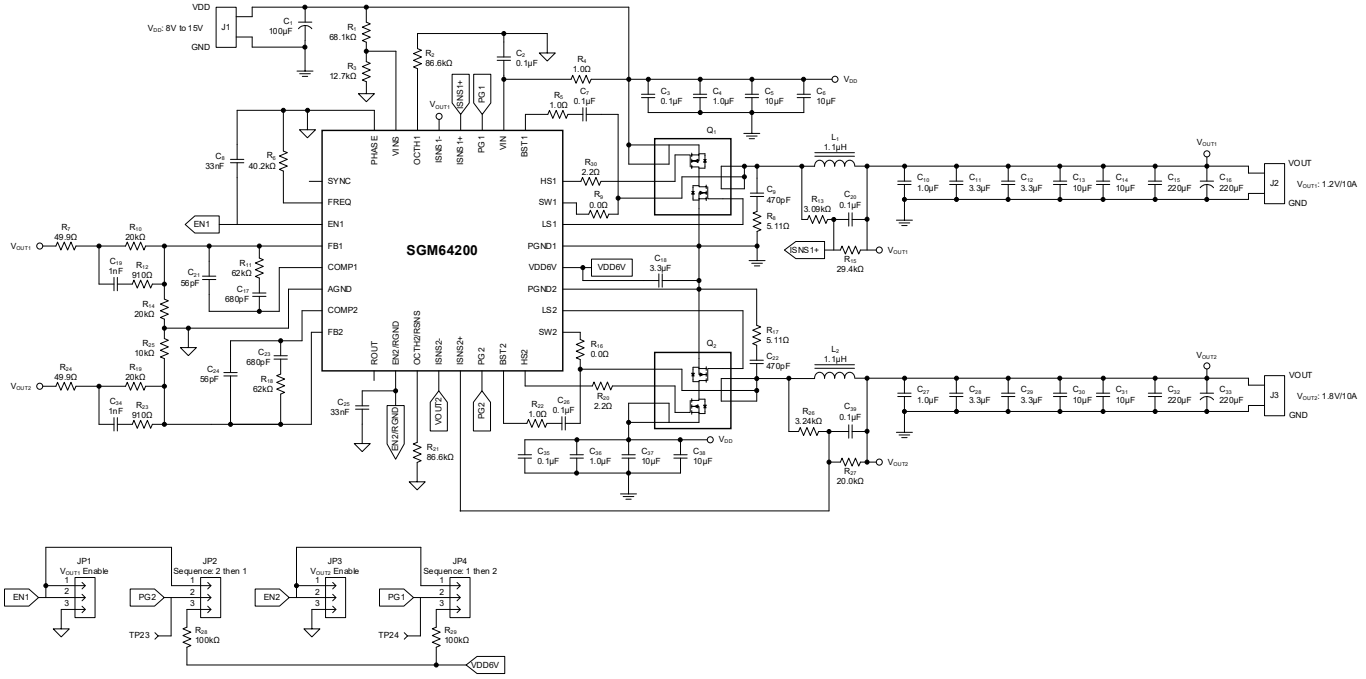


Figure 11. Design Example 1, Dual Output Converter Schematic

Table 3. SGM64200 Dual Output Design Example Specification

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics						
Input Voltage	V_{IN}		8	12	15	V
Input Ripple	V_{IN_RIPPLE}	$I_{OUT1} = I_{OUT2} = 10A$			0.25	V
Output 1 Characteristics						
Output Voltage	V_{OUT1}	$I_{OUT1\_MIN} \le I_{OUT1} \le I_{OUT1\_MAX}$		1.2		V
Line Regulation		$V_{IN\_MIN} \le V_{IN} \le V_{IN\_MAX}$			0.5	%
Load Regulation		$I_{OUT1\_MIN} \le I_{OUT1} \le I_{OUT1\_MAX}$			0.5	%
Output Ripple	$V_{RIPPLE1}$	$I_{OUT1} = I_{OUT1\_MAX}$			24	mV
Output Overshoot	V_{OVER1}	$\Delta I_{OUT1} = 5A$		40		mV
Output Undershoot	V_{UNDER1}	$\Delta I_{OUT1} = 5A$		40		mV
Output Current	I_{OUT1}	$V_{IN\_MIN} \le V_{IN} \le V_{IN\_MAX}$	0		10	A
Short Circuit Current Trip Point	I_{SCP1}			15		A

APPLICATION INFORMATION (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output 2 Characteristics						
Output Voltage	V_{OUT2}	$I_{OUT2\_MIN} \le I_{OUT2} \le I_{OUT2\_MAX}$		1.8		V
Line Regulation		$V_{IN\_MIN} \le V_{IN} \le V_{IN\_MAX}$			0.5	%
Load Regulation		$I_{OUT2\_MIN} \le I_{OUT2} \le I_{OUT2\_MAX}$			0.5	%
Output Ripple	$V_{RIPPLE2}$	$I_{OUT2} = I_{OUT2\_MAX}$			36	mV
Output Overshoot	V_{OVER2}	ΔI_{OUT2} = 5A		40		mV
Output Undershoot	V_{UNDER2}	ΔI_{OUT2} = 5A		40		mV
Output Current	I_{OUT2}	$V_{IN\_MIN} \le V_{IN} \le V_{IN\_MAX}$	0		10	A
Short Circuit Current Trip Point	I_{SCP2}			15		A
General Characterstics						
Soft-Start Time	t_{SS}	V_{IN} = 12V		2		ms
Efficiency	η	V_{IN} = 12V, $I_{OUT1} = I_{OUT2}$ = 10A		88		%
Switching Frequency	f_{SW}			500		kHz

Switching Frequency Selection

500kHz switching frequency is selected as the trade off between efficiency and size of passive components.

Inductor Selection (L_1)

The selection of synchronous Buck inductor is usually based on the design criteria of 20% to 40% of the inductance current ripple. At the maximum load current, the inductance can be obtained by Equation 8.

$$L_1 \approx \frac{V_{IN\_MAX} - V_{OUT1}}{0.3 \times I_{OUT\,1}} \times \frac{V_{OUT1}}{V_{IN\_MAX}} \times \frac{1}{f_{SW}} = \frac{15V - 1.2V}{0.3 \times 10A} \times \frac{1.2V}{15V} \times \frac{1}{500kHz} = 0.736\mu H \quad (8)$$

Select a standard inductance. The inductance is 0.88μH under 10A load, and the ripple current $I_{RIPPLE1}$ = 2.5A.

Output Capacitor Selection (C_{10} through C_{16})

The selection of output capacitance needs to consider the transient response. Equations 10 and 11 leave a margin when estimating the voltage deviation, so as to consider the response delay in the loop, and thus determine the output capacitance:

$$V_{OVER1} < \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \Delta t = \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \frac{\Delta I_{OUT1} \times L1}{V_{OUT1}} = \frac{(\Delta I_{OUT1})^2 \times L_1}{V_{OUT1} \times C_{OUT1}} \quad (10)$$

$$V_{UNDER1} < \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \Delta t = \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \frac{\Delta I_{OUT1} \times L1}{V_{IN} - V_{OUT1}} = \frac{(\Delta I_{OUT1})^2 \times L_1}{(V_{IN} - V_{OUT1}) \times C_{OUT1}} \quad (11)$$

When V_{IN_MIN} > 2 × V_{OUT1}, use Equation V_{OVER1} to calculate the minimum output capacitance. When V_{IN_MIN} < 2 × V_{OUT1}, calculate the value using Equation V_{UNDER1}. In this design example, the V_{IN_MIN} is much larger than 2 × V_{OUT1}, so Equation 12 is used for calculation.

$$C_{OUT1\_MIN} = \frac{(\Delta I_{OUT1})^2 \times L_1}{V_{OUT} \times V_{OVER1}} = \frac{5^2 \times 0.88\mu H}{1.2 \times 40mV} = 458\mu F \quad (12)$$

When the capacitance is minimum, the maximum ESR is determined by the maximum ripple, as shown in Equation 13.

$$E_{ER\_MAX} = \frac{V_{RIPPLE1} - V_{RIPPLE\_CAP}}{I_{RIPPLE1}} = \frac{V_{RIPPLE1} - \left(\frac{I_{RIPPLE1}}{8 \times C_{OUT1} \times f_{SW}}\right)}{I_{RIPPLE1}} = \frac{24mV - \left(\frac{2.5A}{8 \times 458\mu F \times 500kHz}\right)}{2.5A} = 9m\Omega \quad (13)$$

Two 220μF, 4V aluminum electrolytic capacitors are selected according to the requirements of ripple and output response. In addition, two 0805 10μF, two 0603 3.3μF and one 1μF ceramic capacitors are selected to filter high-frequency noise.

APPLICATION INFORMATION (continued)

Peak Current Rating of Inductor

Equations 14 and 15 are used to calculate the charging current at startup and the current peak value of the inductor, respectively, to determine the minimum saturation current of the inductor.

$$I_{CHARGE} = \frac{V_{OUT\,1} \times C_{OUT1}}{t_{SS}} = \frac{1.2V \times (2 \times 220\mu F + 2 \times 10\mu F + 2 \times 3.3\mu F + 1\mu F)}{2ms} = 0.281A \quad (14)$$

$$L_{L1\_PEAK} = I_{OUT1\_MAX} + (1/2 \times I_{RIPPLE1}) + I_{CHARGE} = 10A + (1/2 \times 2.5A) + 0.281A = 11.53A \quad (15)$$

Table 4. Design Example 1, Dual-Output List of Materials

Parameter	Symbol	Value	Units
Inductance	L_1	0.88	μH
RMS Current (Thermal Rating)	I_{L1_RMS}	10.026	A
Peak Current (Saturation Rating)	I_{L1_PEAK}	11.53	A

Wurth744314110 inductance is selected, and the inductance is 1.1μH. Under 10A load current, the inductance value drops to about 0.88uH. The DCR is 3.15mΩ and the size is 7mm × 7mm.

Input Capacitor Selection (C_3 through C_6)

Input capacitor ripple and ESR ripple should be considered for input voltage ripple. Use the following formulas to calculate.

$$IC_{IN1\_MIN} = \frac{I_{OUT1} \times V_{OUT1}}{V_{RIPPLE\_CAP} \times V_{IN\_MIN} \times f_{SW}} = \frac{10A \times 1.2V}{200mV \times 8V \times 500kHz} = 15\mu F \quad (16)$$

$$ESR_{MAX} = \frac{V_{RIPPLE\_ESR}}{I_{OUT1} + (1/2 \times I_{RIPPLE1})} = \frac{50mV}{11.25A} = 4.44m\Omega \quad (17)$$

$$I_{RMS\_CIN1} = I_{OUT\,1} \times \sqrt{D \times (1-D)} = 10A \times \sqrt{0.15 \times (1-0.15)} = 3.57A \quad (18)$$

$$D = \frac{V_{OUT\,1}}{V_{IN\_MIN}} \quad (19)$$

Place two 0805, 10μF capacitors, one 0605, 1.0μF capacitor and one 0402, 0.1μF ceramic capacitor on the power input.

MOSFET Selection (Q_1)

Select the CSD86330. The device integrates two MOS at the size of 3mm × 3mm, and flows through 20A. The R_{ON} of the high side mos is 8.8mΩ, and the R_{ON} of the low side mos is 4.6mΩ. Each high side mos drive pin is connected with a 2.2Ω resistor to reduce driving noise.

ILIM Resistor (R_2)

Use the time constant relationship between the inductance L_1 and DCR and the resistance capacitance connected in parallel to extract the current information on the inductance. The capacitance value is taken as 0.1μF, and the resistance value can be calculated by the following equation.

$$R_{13} = \frac{L_1}{C \times R_{DCR}} = \frac{0.88\mu H}{0.1\mu F \times 3.15m\Omega} = 2.8k\Omega \quad (20)$$

The design limits the maximum input voltage of the detection current operational amplifier to 50mV. If the detected voltage exceeds this value, a series resistance is required to divide the voltage, and the dividing resistance R_{15} is calculated by the following formula.

$$R_{15} = \frac{R_{13} \times V_{CS\_MAX}}{V_{DCR} - V_{CS\_MAX}} \quad (21)$$

Where: $V_{DCR} = (DCR \times 1.2) \times (I_{L\_PEAK} \times 1.2)$

The maximum DCR voltage drop is calculated as follows.

$$V_{OC} = \left[\left(I_{OUT1} + \frac{I_{RIPPLE}}{2}\right) \times 1.2\right] \times (DCR \times 1.2) = \left[\left(10A + \frac{2.5A}{2}\right) \times 1.2\right] \times (3.15m\Omega \times 1.2) = 51.05mV \quad (22)$$

The current limiting resistance is calculated as follows. At this time, it is assumed that the input bias voltage V_{OS} of the current detection operational amplifier is equal to -3mV.

$$R_{LIM} = \frac{(V_{OC} - V_{OS\_MIN}) \times A_{CS}}{I_{LIM\_MIN}} = \frac{[51.05mV - (-3mV)] \times 15V/V}{9.5\mu A} = 85.3k\Omega \cong 86.6k\Omega \quad (23)$$

APPLICATION INFORMATION (continued)

Feedback Divider (R_{10}, R_{14})

The SGM64200 uses an operational amplifier with an internal reference voltage of 0.6V. The value of voltage divider is 10kΩ to 50kΩ, which is a compromise between static current and noise resistance. The calculation formula is as follows when R_{10} is 20kΩ.

$$R_{14} = \frac{V_{FB} \times R_{10}}{V_{OUT1} - V_{FB}} = \frac{0.600V \times 20.0k\Omega}{1.2V - 0.600V} = 20k\Omega \quad (24)$$

Compensation: (R_{11}, R_{12}, C_{17}, C_{19}, C_{21})

Use the SGM64200 loop calculation tool, set the 50kHz bandwidth and 50° phase margin, measured the calculated results in the experimental values and modified the parameters to obtain the following values: C_{21} = 56pF, C_{17} = 680pF, C_{19} = 1nF, R_{12} = 910Ω, R_{11} = 62kΩ.

Boot-Strap Capacitor (C_7)

In order to drive high side FET normally, the ripple of BST capacitor is limited to less than 100mV.

$$C_{BOOST} = \frac{Q_{G1}}{V_{BST\_RIPPLE}} = \frac{7nC}{100mV} = 70nF \approx 100nF \quad (25)$$

General Device Components

Synchronization (SYNC Pin):

The SYNC pin must be left open for independent dual outputs.

RT Resistor (R_6):

The switching frequency is determined by RT resistance, which is calculated by the following formula.

$$R_{RT} = \frac{20^9}{f_{SW}} = \frac{20^9}{500kHz} = 40k\Omega \approx 40.2k\Omega \quad (26)$$

Differential Amplifier Out (ROUT Pin)

In dual output configuration the ROUT pin is not used and must remain open (unconnected).

EN Timing Capacitors (C_8)

The soft start capacitor voltage is the reference voltage slope of the operational amplifier. Equation 27 calculates the capacitor value.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{FB}} = \frac{2ms \times 10\mu A}{0.6V} \approx 33nF \quad (27)$$

Power Good (PG1, PG2 Pins)

PG1 and PG2 are pulled up to VDD6V through 100kΩ resistance.

Phase Set (PHASE Pin)

The PHASE pin can be connected to ground or connected to the VDD6V pin.

VIN Bypass Capacitor (C_2)

As shown in the Pin Configuration section, use a 0.1μF, 50V, X7R capacitor for VIN bypass.

VDD6V Bypass Capacitor (C_{18})

Connect the VDD6V to a low ESR capacitor with a capacitance of 4.7uF or higher.

Application Curves

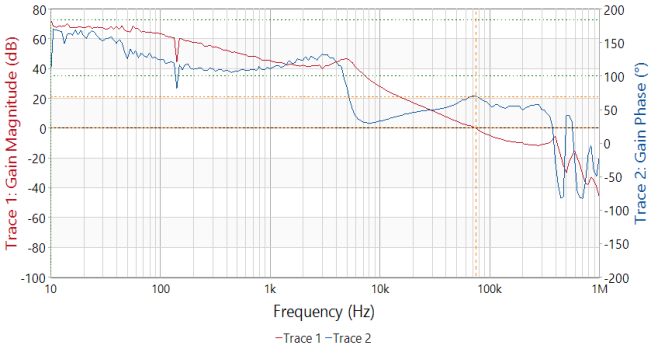


Figure 12. Design Example 1 Loop Response (V_{DD} = 12V, V_{OUT1} = 1.2V, I_{OUT1} = 10A, 80kHz Bandwidth, 50° Phase Margin)

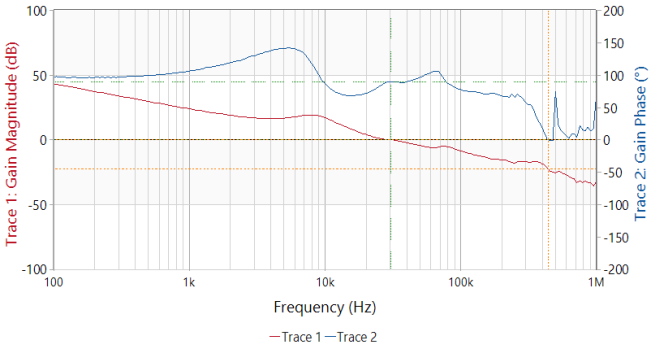


Figure 13. Design Example 1 Loop Response (V_{DD} = 12V, V_{OUT1} = 1.8V, I_{OUT1} = 10A, 80kHz Bandwidth, 50° Phase Margin)

APPLICATION INFORMATION (continued)

Two Phase Mode Configuration from 12V to 1.2V for SGM64200

Figure 14 is a schematic diagram of the two-phase single output configuration mode. Table 5 is the design objective.

Table 5. Channel 2 Pin Connections in Two-Phase Mode

Pin	Connection
COMP2	Connect to COMP1.
EN2/RGND	Use as RGND pin, connect to the output ground.
FB2	Connect to VDD6V.
OCTH2/RSNS	Use as RSNS pin, connect to output.
PG2	Floating or connect to ground.

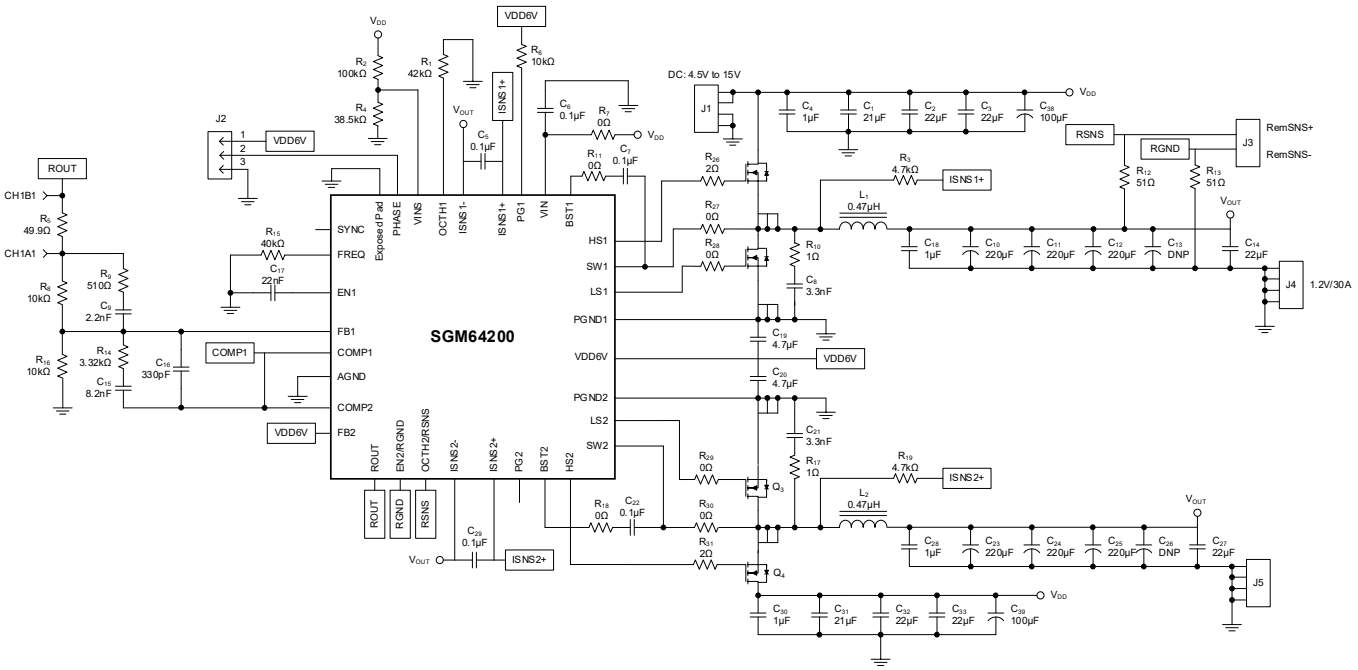


Figure 14. Design Example 2, Two-Phase Converter Schematic Table 6.

Table 6. SGM64200 Design Example 2 Specification

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		4.5		15	V
Output Voltage	V_{OUT1}	$I_{OUT\_MIN} \le I_{OUT} \le I_{OUT1\_MAX}$		1.2		V
Line Regulation		$V_{IN\_MIN} \le V_{IN} \le V_{IN\_MAX}$			0.5	%
Load Regulation		$I_{OUT\_MIN} \le I_{OUT} \le I_{OUT1\_MAX}$			0.5	%
Output Ripple	$V_{RIPPLE1}$	$I_{OUT} = I_{OUT\_MAX}$			12	mV
Output Overshoot	V_{OVER1}	ΔI_{OUT} = 5A		40		mV
Output Undershoot	V_{UNDER1}	ΔI_{OUT} = 5A		40		mV
Output Current	I_{OUT1}	$V_{IN\_MIN} \le V_{IN} \le V_{IN\_MAX}$	0		10	A
Soft-Start Time	t_{SS}	V_{IN} = 12V		2		ms
Efficiency	η	V_{IN} = 12V, $I_{OUT1} = I_{OUT2}$ = 10A		88		%
Switching Frequency	f_{SW}			500		kHz

LAYOUT

Layout Guidelines

Power Stage

The BUCK power stage has two current loops. One of them is the input loop with high-frequency AC discontinuous current, and the other is the output loop with high-frequency continuous current. In order to make the input loop as small as possible, the input ceramic capacitor should be as close to the main switch mos and synchronous rectifier mos as possible. Like the input loop, the output capacitor in the output loop also needs to be closer to the inductor and PGND to reduce the area of the output loop. The SW node needs to be very small to reduce the radiation area. HS and LS require short and thick trace to be placed between the chip and mos.

Device Peripheral

SGM64200 needs to distinguish signal ground (AGND) from power ground (PGND). It is necessary to correctly distinguish the grounding in the circuit. All the pins related to the power stage are connected to PGND, and other pins related to the signal stage (such as FB1, FB2, FREQ, OCTH1 and OCTH2) are connected to AGND. When DCR is applied to detect current, Kelvin connection is required. The detection capacitance needs to be close to the ISNS+ and ISNS- pins. In two-phase mode, OCTH2/RSN and EN2/RGND need to be directly connected to the load point where the voltage needs to be adjusted, and the leads need to be wired in parallel and away from the switching elements.

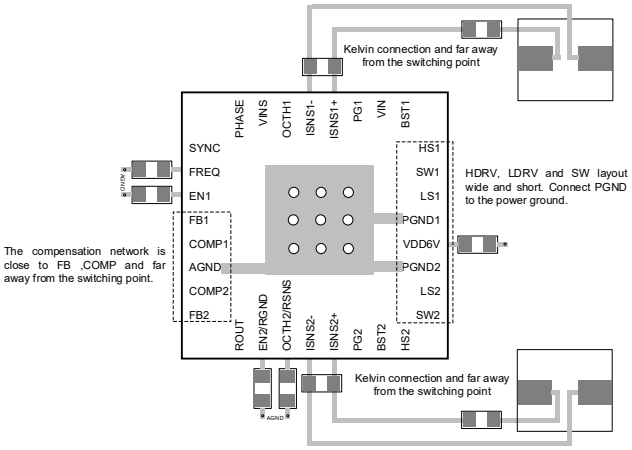


Figure 15. Layout Example

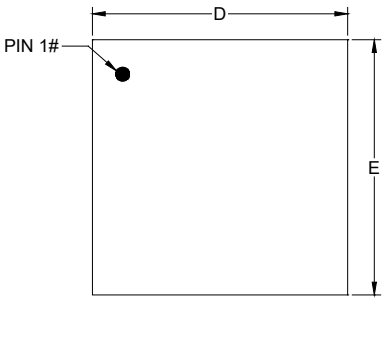
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

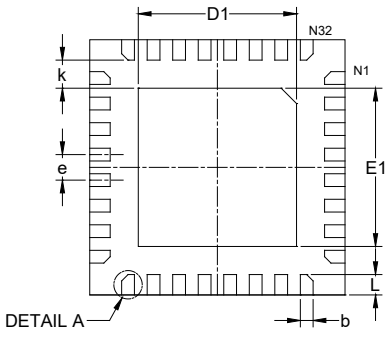
Changes from Original (DECEMBER 2022) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

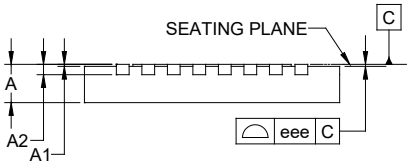
TQFN-5×5-32AL



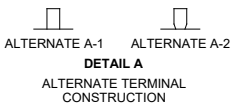
TOP VIEW

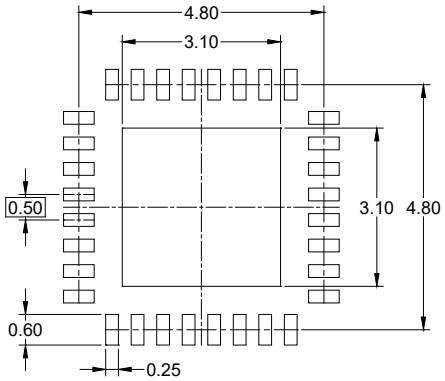


BOTTOM VIEW



SIDE VIEW





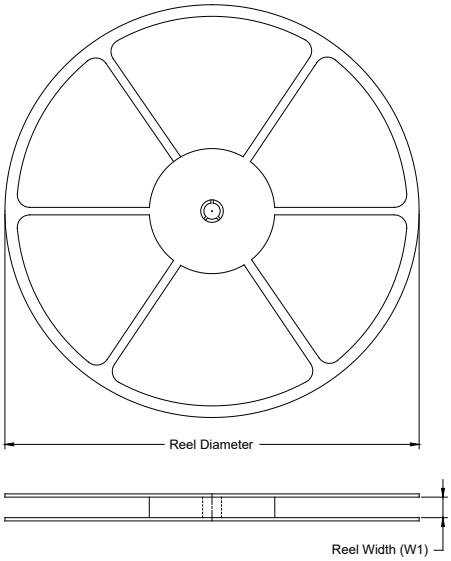
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2	0.203 REF		
b	0.200	-	0.300
D	4.900	-	5.100
E	4.900	-	5.100
D1	3.000	-	3.200
E1	3.000	-	3.200
e	0.500 BSC		
k	0.550 REF		
L	0.300	-	0.500
eee	0.080		

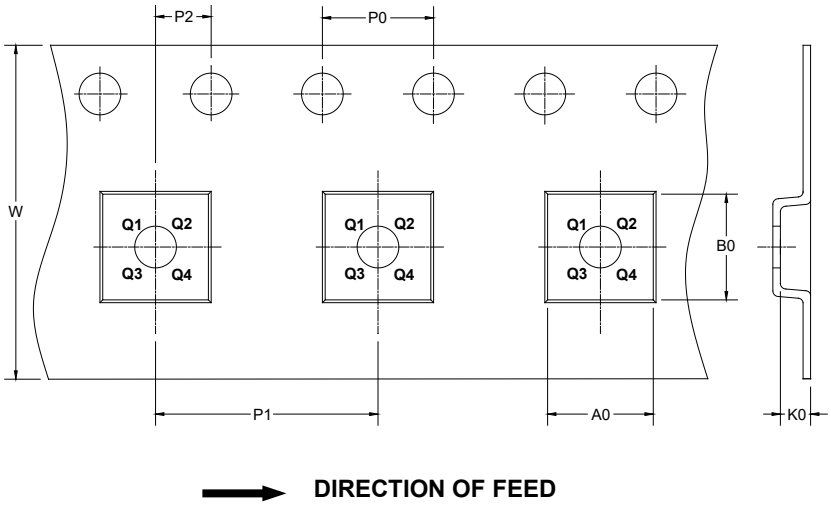
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



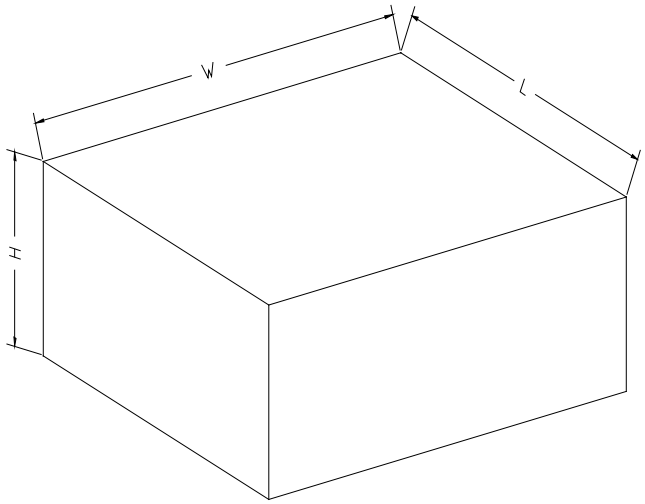
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-5×5-32AL	13″	12.4	5.30	5.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002