SGM41538/SGM41538B
1- to 4-Cell Battery Charge Controller with Hybrid Power Boost and Battery-Only-Boost Modes, Power Monitoring and SMBus

GENERAL DESCRIPTION

The SGM41538 and SGM41538B are efficient synchronous multi-chemistry chargers for 1- to 4-cell batteries optimized for high density applications with minimum number of external components.

Hybrid Power Boost mode (HPB) is supported in which the battery can assist the adapter when the system demand is higher than the adapter rated power. It also features an ultra-fast changeover from charging to discharging and does not crash when switching between different operating modes.

If the adapter is not present and V_{BAT} is above the minimum operation system voltage (V_{SYSMIN}), BATFET will directly connect the battery to the system. Battery-Only-Boost mode is also supported when V_{BAT} drops close to V_{SYSMIN} or lower. In this case, the Boost converter is activated to boost the low battery voltage and regulate the system voltage until battery stored energy is completely utilized and depleted.

Device supply source is automatically selected between battery or adapter. The integrated gate drivers for the external N-MOSFETs (ACFET, RBFET and BATFET) are powered by two internal charge pumps.

The integrated SMBus interface of the SGM41538 and SGM41538B allows the power management controller to accurately set and regulate the input current, charge current, discharge current, and the charge voltage. It also provides a comprehensive set of programmable protection features.

Adapter current, battery discharge current, and system power are monitored through their respective pins (IADP, IDCHG, PMON) such that the host can throttle the CPU and reduce system power whenever needed.

The SGM41538 and SGM41538B are available in a Green TQFN-4×4-28BL package and can operate in the -40℃ to +125℃ junction temperature range.

APPLICATIONS

Systems with Battery/Capacitor Backup
Notebooks, Ultra-Books, Detachable, and Tablet PCs
Industrial and Medical Equipment
Portable Equipment

FEATURES

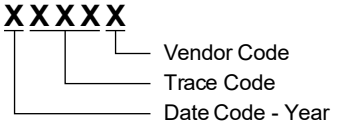
- **Hybrid Power Boost Mode (HPB) Allows System Powering from Adapter and Battery Together**
  - **Ultra-Fast 80μs Response for Entering HPB**
- **Battery-Only-Boost Mode Allows Powering the System in Low Battery State without Adapter**
- **Two-Level Input Current Limiting for Maximum Adapter Power Utilization and Minimal Battery Discharge**
- **Charges 1- to 4-Cell Packs from 4.5V to 24V Adapters**
- **Accurate Power/Current Monitoring for CPU Throttling**
  - **-1.7%~2.3% Current Monitor Accuracy**
  - **-5%~5% System Power Monitoring Accuracy (PMON)**
- **Comprehensive nPROCHOT Protection Profile**
- **Automatic Adapter/Battery Source Selection by NMOS**
  - **Fast ACFET Turn-On (100μs)**
- **Accurate Input Current, Charge Voltage, Charge Current and Discharge Current Limit Programming**
  - **-0.3%~0.35% Charge Voltage (16mV/Step)**
  - **-2.2%~2.5% Input Current (64mA/Step)**
  - **-1.5%~3.5% Charge Current (64mA/Step)**
  - **-3.5%~1.5% Discharge Current (512mA/Step)**
- **Comprehensive Integrated Charging Functions**
  - **Battery LEARN Function**
  - **Battery Presence Monitor**
  - **Boost Mode Indicator**
  - **Internal Loop Compensation**
  - **Bootstrap (BTST) Diode**
- **Improve Safety Protections for Over-Voltage, Over-Current, Battery, Inductor, and MOSFET Short-Circuit**
- **4 Switching Frequencies: 300kHz, 400kHz, 600kHz and 800kHz**
- **Real-Time System Control with ILIM Pin Current Limit**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41538	TQFN-4×4-28BL	-40℃ to +125℃	SGM41538XTSX28G/TR	SGM41538 XTSX28 XXXXX	Tape and Reel, 3000
SGM41538B	TQFN-4×4-28BL	-40℃ to +125℃	SGM41538BXTSX28G/TR	SGM0D7 XTSX28 XXXXX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range
SRN, SRP, ACN, ACP, CMSRC, VCC, BATSRC ..... -0.3V to 30V
PHASE ..... -2V to 30V
ACDET, SDA, SCL, LODRV, IADP, IDCHG, PMON, ILIM, ACOK, CMPIN, CMPOUT, nPROCHOT, nBATPRES, nBST_STAT ..... -0.3V to 6V
REGN ..... -0.3V to 7V
BTST, HIDRV, ACDRV, BATDRV ..... -0.3V to 36V
Differential Voltage
BTST-PHASE, HIDRV-PHASE, ACDRV-CMSRC, BATDRV-BATSRC ..... -0.3V to 7V
ACP-ACN, SRP-SRN ..... -0.5V to 0.5V
Transient Voltage
LODRV (2% Duty Cycle) ..... -4V to 6.5V
HIDRV (2% Duty Cycle) ..... -4V to 36V
PHASE (2% Duty Cycle) ..... -4V to 30V
Output Sink Current
ACOK, nBST_STAT, nPROCHOT 6mA
Package Thermal Resistance
TQFN-4×4-28BL, θ_{JA} ..... 36.8℃/W
TQFN-4×4-28BL, θ_{JB} ..... 14.4℃/W
TQFN-4×4-28BL, $\theta_{JC\ (TOP)}$ ..... 26.2℃/W
TQFN-4×4-28BL, $\theta_{JC\ (BOT)}$ ..... 4.1℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±2000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Voltage Range
SRN, SRP, ACN, ACP, CMSRC, VCC, BATSRC ..... 0V to 24V
PHASE ..... -2V to 24V
ACDET, SDA, SCL, LODRV, IADP, IDCHG, PMON, ILIM, ACOK, CMPIN, CMPOUT, nPROCHOT, nBATPRES, nBST_STAT ..... 0V to 5V
REGN ..... -0.3V to 6V
BTST, HIDRV, ACDRV, BATDRV ..... 0V to 30V
Differential Voltage
ACP-ACN, SRP-SRN ..... -0.4V to 0.4V
Transient Voltage
LODRV (2% Duty Cycle) ..... -4V to 6.5V
HIDRV (2% Duty Cycle) ..... -4V to 36V
PHASE (2% Duty Cycle) ..... -4V to 30V
Output Sink Current
ACOK, nBST_STAT, nPROCHOT 6mA
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

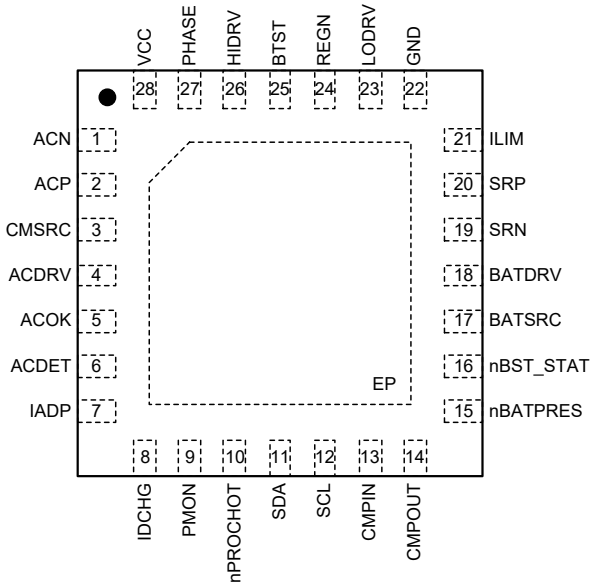
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-4×4-28BL

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	ACN	Input Current Sense Resistor Negative Terminal. A 0.1μF ceramic capacitor between ACN and GND pins for common-mode filtering and a 0.1μF between ACN and ACP pins for differential mode filtering are recommended.
2	ACP	Input Current Sense Resistor Positive Terminal. A 0.1μF ceramic capacitor between ACP and GND pins for common-mode filtering and a 0.1μF between ACN and ACP pins for differential mode filtering are recommended.
3	CMSRC	ACDRV Gate Drive Source Pin (Charge Pump). Connect it to the common source of ACFET (Q1) and RBFET (Q2) through a 4kΩ resistor (for CMSRC pin inrush current limiting).
4	ACDRV	Gate Drive Output (Charge Pump) for Adapter (ACFET) and Reverse Blocking (RBFET) N-MOSFETs. When ACOK is high, ACDRV is driven 6V above CMSRC to turn on ACFET and RBFET. Use a series 4kΩ resistor between ACDRV and common gates of the ACFET and RBFET to limit the ACDRV inrush current.
5	ACOK	Active-High Open-Drain Adapter Detection Output. It should be pulled up with an external resistor (like 10kΩ) to a positive voltage rail. It is released to go high if a good input adapter is detected (V_{ACDET} > V_{ACOK}, V_{VCC} < V_{ACOV}, V_{VCC} > V_{VCC_UVLOZ} and V_{VCC} > V_{BAT} + V_{SLEEP}). Otherwise, the ACOK output will be pulled low.
6	ACDET	Adapter Voltage Detection Input. A resistor driver from the input adapter positive line is connected to this pin to program the detection voltage threshold. The ACDET adapter detection threshold is 2.4V. If V_{ACDET} > V_{WAKEUP_RISE} and V_{VCC} > V_{VCC_UVLOZ}, then REGN LDO is present, then ACOK comparator, independent comparator, input current buffer (IADP), discharge current buffer (IDCHG), and power monitor buffer (PMON) can be enabled by SMBus.
7	IADP	Sensed Adapter Current Buffered Output. Differential amplifier output of the input current. V_{IADP} = G_A × (V_{ACP} - V_{ACN}) where the gain G_A can be set to 20 or 40 by SMBus. Place a small ceramic capacitor (100pF or less) to decouple IADP pin to GND. If the buffer is not needed the output can be left floating.
8	IDCHG	Sensed Discharge Current Buffered Output. Differential amplifier output of the discharge current V_{IDCHG} = G_D × (V_{SRN} - V_{SRP}) in which the G_D gain can be set to 8 or 16 by SMBus. Place a small ceramic capacitor (100pF or less) to decouple IDCHG pin to GND. If the buffer is not needed the output can be left floating.
9	PMON	Buffered Output for the Measured System Power. PMON provides an analog current proportional to the total system power (adapter power plus battery power) that with an external resistor between PMON and GND pins is converted to the PMON voltage. The buffer gain is selectable through SMBus. Place a small ceramic capacitor (100pF or less) to decouple PMON pin to GND.
10	nPROCHOT	Processor Hot Output (Open-Drain, Active Low Indicator Output). Several events are monitored such as over-current in the adapter input or battery discharge and if any of them occurs, a pulse with at least 10ms width is sent to this pin. Pull this pin up with a 10kΩ resistor to the pull-up rail.

PIN DESCRIPTION (continued)

PIN	NAME	FUNCTION
11	SDA	SMBus Open-Drain Data Line (I/O). Connect the SDA pin to the host/smart battery SDA line. SMBus communication can start when V_{VCC} > $V_{VCC\_UVLOZ\_RISE}$. Use a 10kΩ pull-up resistor and follow the SMBus specifications.
12	SCL	SMBus Open-Drain Clock Input. Connect to SCL pin to the host/smart battery SCL line. SMBus communication can start when V_{VCC} > $V_{VCC\_UVLOZ\_RISE}$. Use a 10kΩ pull-up resistor and follow the SMBus specifications.
13	CMPIN	Independent Comparator Input. Comparator parameters such as the internal reference (comparison threshold), output polarity and deglitch time are programmable through SMBus. The hysteresis can be adjusted by placing an external resistor between CMPIN and CMPOUT pins when the polarity is high. If this comparator is not needed, connect the CMPIN pin to ground and leave the CMPOUT floating.
14	CMPOUT	Independent Comparator Open-Drain Output. Pull this pin up with a 10kΩ resistor to the pull-up rail. Comparator parameters such as the internal reference (comparison threshold), output polarity and deglitch time are programmable through SMBus. The comparator is active only when REGN is available. If this comparator is not needed, connect the CMPIN to ground and leave the CMPOUT floating.
15	nBATPRES	Active-Low Battery Present Input Signal. A low on this input informs the device that the battery is present, and a high means battery is not connected. If this input goes high the device ends the LEARN function and turns on the ACFET/RBFET, however, to protect adapter to battery short, the ACFET/RBFET will not turn on until BATFET is turned off. A low-to-high on this pin disables battery charging and Hybrid Power Boost mode. When nBATPRES is high, the host can still enable charge or Hybrid Power Boost mode by writing to the REG0x14 and REG0x15.
16	nBST_STAT	Active-Low Open-Drain Boost Mode Indicator Output. Pull this pin up with a 10kΩ resistor to the pull-up rail. When the device is in Boost mode, this pin is pulled low, otherwise it is released and goes high.
17	BATSRC	Source Connection Pin for the BATFET (the N-MOSFET switch that connects the battery and system).
18	BATDRV	Gate Driving Output (Charge Pump) for the BATFET. BATDRV is driven 6V above BATSRC to turn on BATFET and power the system from battery. To turn of BATFET BATDRV is shorted to BATSRC. Use a series 4kΩ resistor between BATDRV and BATFET gate to limit the BATDRV inrush current.
19	SRN	Charge Current Sense Resistor Negative Terminal and Battery Voltage Sensing Pin. Connect a 0.1μF ceramic capacitor (SRN to GND) for common-mode filtering and another 0.1μF ceramic capacitor (SRN to SRP) for differential mode filtering.
20	SRP	Charge Current Sense Resistor Positive Terminal and Battery Voltage Sensing Pin. Connect a 0.1μF ceramic capacitor (SRP to GND) for common-mode filtering and another 0.1μF ceramic capacitor (SRN to SRP) for differential mode filtering.
21	ILIM	Program Pin for Charge and Discharge Current Limits. The voltage of the ILIM pin can set the charge current limit to the corresponding value given by V_{ILIM} = 20 × (V_{SRP} - V_{SRN}) and the discharge current limit by V_{ILIM} = 5 × (V_{SRN} - V_{SRP}). To set the ILIM voltage, A resistor divider from the 3.3V reference rail can be used. The actual current limit is the lower of the ILIM and REG0x14 (for charge) and REG0x39 (for discharge). The minimum ILIM voltage that allows charge or discharge current regulation is 100mV.
22	GND	Device Ground Return. Connect this pin to the analog ground plane of the PCB and also to the PCB power ground plane only at one point (at the thermal pad under the device).
23	LODRV	Low-side (LS) Switching N-MOSFET Gate Driving Output.
24	REGN	6.07V Output of the Internal LDO Powered from VCC. The REGN LDO is only available if V_{ACDET} > V_{WAKEUP_RISE} and V_{VCC} is above V_{VCC_UVLOZ}. Decouple REGN pin to GND with at least 2.2μF (0603) ceramic capacitor. The integrated bootstrap diode for the high-side gate driver is placed between REGN and BTST pins.
25	BTST	High-side (HS) Switching N-MOSFET Gate Driver Power Supply. Connect BTST and PHASE pins with a 47nF bootstrap capacitor from BTST to PHASE. The bootstrap diode is integrated.
26	HIDRV	High-side (HS) Switching N-MOSFET Gate Driving Output.
27	PHASE	High-side (HS) Switching MOSFET Source Connection. PHASE is connected to the switching node of the converter.
28	VCC	Device Supply Pin. It is powered from adapter or battery. Use a 10Ω (1206 size is recommended) and a 1μF low pass filter on VCC to limit inrush current. Connect VCC to the system and adapter lines with a Schottky diode.
Exposed Pad	EP	Exposed Thermal Pad (under the device). Analog and power grounds are star-connected only at this point (exposed pad plane). Solder this pad to the PCB copper plane and consider sufficient number of thermal vias under the device connected to other layers ground planes to facilitate heat relief.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, parameters are given with $V_{VCC\_UVLOZ} < V_{VCC} < V_{ACOV}$, $V_{VCC} > V_{SRN} + V_{SLEEP}$, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Currents						
Battery-Only Quiescent Current (through SRP, SRN, BATSRC, PHASE, VCC, ACP and ACN Pins) (T_J = 0℃ to +85℃)	I_{Q_BAT}	V_{BAT} = 16.8V, VCC disconnected from battery, EN_LWPWR = 1 (low power mode enabled)			0.5	μA
		V_{BAT} = 16.8V, VCC connected to battery, EN_LWPWR = 1 (low power mode enabled)		20	32	μA
		V_{BAT} = 16.8V, VCC connected to battery, BATFET on, EN_LWPWR = 0 (low power mode disabled), REGN on, comparator and nPROCHOT enabled, PMON and Boost mode disabled		900	1110	μA
		V_{BAT} = 16.8V, VCC connected to battery, BATFET on, EN_LWPWR = 0 (low power mode disabled), REGN on, comparator, nPROCHOT and PMON enabled, Boost mode disabled		1110	1340	μA
		V_{BAT} = 13.5V, VCC connected to battery, BATFET on, EN_LWPWR = 0 (low power mode disabled), REGN on, comparator, nPROCHOT, PMON and Boost mode enabled, converter not switching		1.40		mA
VCC/VBAT Supply						
VCC Operating Range	V_{VCC_OP}		4.5		24	V
Input Under-Voltage Rising Threshold	$V_{VCC\_UVLOZ\_RISE}$	V_{VCC} rising	2.36	2.56	2.76	V
Input Under-Voltage Falling Threshold	$V_{VCC\_UVLOZ\_FALL}$	V_{VCC} falling	2.16	2.36	2.56	V
Input Under-Voltage Falling Hysteresis	$V_{VCC\_UVLOZ\_HYS}$	V_{VCC} falling		200		mV
Sleep Falling Threshold to Turn-Off ACFET	V_{SLEEP_FALL}	(V_{VCC} - V_{SRN}) falling	-40	25	120	mV
Sleep Rising Threshold to Turn-On ACFET	V_{SLEEP_RISE}	(V_{VCC} - V_{SRN}) rising	270	460	670	mV
ACDET Wakeup Rising Threshold	V_{WAKEUP_RISE}	$V_{VCC} > V_{VCC\_UVLOZ}$, V_{ACDET} rising		0.59	0.67	V
ACDET Wakeup Falling Threshold	V_{WAKEUP_FALL}	$V_{VCC} > V_{VCC\_UVLOZ}$, V_{ACDET} falling	0.42	0.49		V
ACOK Rising Threshold	V_{ACOK_RISE}	$V_{VCC} > V_{VCC\_UVLOZ}$, V_{ACDET} rising	2.355	2.4	2.455	V
ACOK Falling Threshold	V_{ACOK_FALL}	$V_{VCC} > V_{VCC\_UVLOZ}$, V_{ACDET} falling	2.3	2.35	2.4	V
VCC Over-Voltage Rising Threshold	V_{ACOV_RISE}	V_{VCC} rising	24.5	25.7	27	V
VCC Over-Voltage Falling Threshold	V_{ACOV_FALL}	V_{VCC} falling	23.6	24.8	26	V
ACN to BAT Falling Threshold to Turn-On BATFET	V_{ACNSRN_FALL}	(V_{ACN} - V_{SRN}) falling	110	200	310	mV
ACN to BAT Rising Threshold to Turn-Off BATFET	V_{ACNSRN_RISE}	(V_{ACN} - V_{SRN}) rising	180	290	420	mV
Battery Depletion Falling Threshold, given as Percentage of the Voltage Regulation Limit. Results in Exit from Boost Mode and LEARN Mode.	$V_{BATDEPL\_FALL}$	BAT_DEPL_VTH[1:0] = 00	57.5	60	62.5	%
		BAT_DEPL_VTH[1:0] = 01	62.5	65	67.5	%
		BAT_DEPL_VTH[1:0] = 10	65.5	68	70.5	%
		BAT_DEPL_VTH[1:0] = 11	69.5	72	74.5	%
Battery Depletion Rising Hysteresis	$V_{BATDEPL\_RISE}$	BAT_DEPL_VTH[1:0] = 00	140	300	460	mV
		BAT_DEPL_VTH[1:0] = 01	145	315	480	mV
		BAT_DEPL_VTH[1:0] = 10	145	315	480	mV
		BAT_DEPL_VTH[1:0] = 11	180	355	535	mV
Battery LOWV Falling Threshold	$V_{BATLOWV\_FALL}$	V_{SRN} falling	2.3	2.5	2.7	V
Battery LOWV Rising Threshold	$V_{BATLOWV\_RISE}$	V_{SRN} rising		2.67		V
Battery LOWV Charge Current Limit	$I_{BATLOWV}$	R_{SR} = 10mΩ		570		mA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, parameters are given with V_{VCC_UVLOZ} < V_{VCC} < V_{ACOV}, V_{VCC} > V_{SRN} + V_{SLEEP}, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACFET/RBFET and BATFET Gate Drivers						
ACDRV Charge Pump Current Limit	I_{ACFET}	V_{ACDRV} - V_{CMSRC} = 4V	150	210		μA
Gate Drive Voltage on ACFET	V_{DRV_ACFET}	V_{ACDRV} - V_{CMSRC} when V_{VCC} > V_{VCC_UVLOZ}	5.5	5.97	6.5	V
ACDRV Turn-Off Resistance	R_{ACDRV_OFF}		4	5.9	7.6	kΩ
Minimum ACDRV Gate to Source Load	R_{ACDRV_GS}		200			kΩ
BATDRV Charge Pump Current Limit	I_{BATFET}	V_{BATDRV} - V_{BATSRC} = 4V	80	105		μA
Gate Drive Voltage on BATFET, V_{BATDRV} - V_{BATSRC}	V_{DRV_BATFET}	V_{BATDRV} – V_{BATSRC} when V_{VCC} > V_{VCC_UVLOZ} and EN_LWPWR = 0	5.2	5.8	6.3	V
BATDRV Turn-Off Resistance	R_{BATDRV_OFF}		4	5.9	7.6	kΩ
Minimum BATDRV Gate to Source Load	R_{BATDRV_LOAD}		700			kΩ
Battery Charger						
Typical Charge Voltage Regulation Range	V_{REG_RANGE}		1.024		19.2	V
Typical Charge Voltage Setting Step Size	V_{REG_STEP}			16		mV
Charge Voltage Initial Accuracy	V_{REG_ACC}	ChargeVoltage register = 41A0h		16.800		V
		-20℃ to +85℃	-0.5		0.35	%
		-40℃ to +125℃	-0.55		0.4	%
		ChargeVoltage register = 3130h		12.592		V
		-20℃ to +85℃	-0.3		0.35	%
		-40℃ to +125℃	-0.4		0.45	%
		ChargeVoltage register = 20D0h		8.400		V
		-20℃ to +85℃	-0.55		0.65	%
		-40℃ to +125℃	-0.6		0.7	%
		ChargeVoltage register = 1060h		4.192		V
		-20℃ to +85℃	-1		1.15	%
		-40℃ to +125℃	-1.05		1.2	%
Typical Charge Current Regulation Range	I_{CHG_RANGE}	R_{SR} = 10mΩ	0		8128	mA
Typical Charge Current Regulation Setting Step Size	I_{CHG_STEP}	R_{SR} = 10mΩ		64		mA
Charge Current Regulation Initial Accuracy (V_{SRN} > 2V, R_{SR} = 10mΩ)	I_{CHG_ACC}	ChargeCurrent register = 1000h		4096		mA
			-1.5		3.5	%
		ChargeCurrent register = 0800h		2048		mA
			-2.5		5	%
		ChargeCurrent register = 0400h		1024		mA
			-5.5		10.5	%
		ChargeCurrent register = 0200h		512		mA
			-8		18.5	%
		ChargeCurrent register = 0100h		256		mA
		ChargeVoltage register = 20D0h, 3031h, 41A0h	-17		37	%
		ChargeVoltage register = 1060h	-17		33	%
		ChargeCurrent register = 00C0h		192		mA
			-22		40	%
SRP and SRN Leakage Mismatch	$I_{LEAK\_SRP-SRN}$		-7		10	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, parameters are given with $V_{VCC\_UVLOZ} < V_{VCC} < V_{ACOV}$, $V_{VCC} > V_{SRN} + V_{SLEEP}$, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current Regulation						
Typical Input Current Regulation Range	I_{INDPM_RANGE}	R_{AC} = 10mΩ	0		8064	mA
Typical Input Current Regulation Step	I_{INDPM_STEP}	R_{AC} = 10mΩ		64		mA
Input Current Regulation Initial Accuracy	I_{INDPM_ACC}	InputCurrent register = 1000h		4096		mA
			-2.2		2.5	%
		InputCurrent register = 0800h		2048		mA
			-3.5		3.7	%
		InputCurrent register = 0400h		1024		mA
			-6.3		6.3	%
		InputCurrent register = 0200h		512		mA
			-11		11	%
ACP and ACN Leakage Mismatch	$I_{LEAK\_ACP-ACN}$		-3		4	μA
Peak Power Mode						
Input Peak Power Overload Duration	$t_{OVERLOAD}$	PKPWR_TOVLD[1:0] = 00	0.65		1.05	ms
		PKPWR_TOVLD[1:0] = 01	1.3		2.1	
		PKPWR_TOVLD[1:0] = 10	3.5		5.3	
		PKPWR_TOVLD[1:0] = 11	7		10.5	
Peak Power Cycle Period	t_{MAX}	PKPWR_TMAX[1:0] = 00	17.5	20	22	ms
		PKPWR_TMAX[1:0] = 01	35	40	44	
		PKPWR_TMAX[1:0] = 10	70	80	88	
		PKPWR_TMAX[1:0] = 11	1120	1300	1410	
Peak Current Limit Initial Accuracy	$ILIM2_{ACC}$	InputCurrent register = 1000h, ILIM2_VTH[3:0] = 1001 (150%)		6144		mA
			98.3		102.3	%
		InputCurrent register = 0800h, ILIM2_VTH[3:0] = 1001 (150%)		3072		mA
			97.2		103	%
		InputCurrent register = 0400h, ILIM2_VTH[3:0] = 1001 (150%)		1536		mA
			94.5		105.5	%
		InputCurrent register = 0200h, ILIM2_VTH[3:0] = 1001 (150%)		768		mA
			90.5		108.5	%
Battery Discharge Current Regulation (Hybrid Power Boost Mode)						
Typical Discharge Current Regulation Range	V_{IDCHG_RNG}	R_{SR} = 10mΩ	0		32256	mA
Typical Discharge Current Regulation Setting Step Size	I_{IDCHG_STEP}	R_{SR} = 10mΩ		512		mA
Discharge Current Regulation Initial Accuracy	I_{DCHG_ACC}	DisChargeCurrent register = 2000h		8192		mA
			-3.5		1.5	%
		DisChargeCurrent register = 1000h		4096		mA
			-2.5		2	%
		DisChargeCurrent register = 0800h		2048		mA
			-5		3.5	%
		DisChargeCurrent register = 0400h		1024		mA
			-8.5		6.5	%
		DisChargeCurrent register = 0200h		512		mA
			-14.5		9.5	%

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, parameters are given with V_{VCC_UVLOZ} < V_{VCC} < V_{ACOV}, V_{VCC} > V_{SRN} + V_{SLEEP}, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery-Only-Boost Mode						
Typical System Voltage Regulation Range	V_{SYS_RNG}		5.632		13.568	V
Typical System Voltage Regulation Step Size Setting	V_{SYS_STEP}			128		mV
System Voltage Regulation Accuracy	V_{SYS_ACC}	VsysMin register = 2600h		9.728		V
			-2.6		2	%
		VsysMin register = 1980h		6.528		V
			-2.8		2.2	%
System Voltage Falling Threshold to Enter Battery Boost (in % of VsysMin)	$V_{SYS\_BST\_ENTER}$			100		%
System Over-Voltage to Exit Battery Boost (in % of System Regulation Voltage)	$V_{SYS\_BST\_EXIT}$			120		%
Current Sense Amplifiers						
IADP Output Voltage Range	V_{IADP}		0		3.3	V
IADP Output Current	I_{IADP}				1	mA
IADP Sense Amplifier Gain	A_{IADP}	$V_{IADP}/V_{ACP-ACN}$, IADP_GAIN = 0		20		V/V
Input Current Sense Amplifier Gain Accuracy	V_{IADP_ACC}	$V_{ACP-ACN}$ = 40mV	-1.7		2.3	%
		$V_{ACP-ACN}$ = 20mV	-3		4	
		$V_{ACP-ACN}$ ≥ 10mV	-5		6	
		$V_{ACP-ACN}$ ≥ 5mV	-9		11	
		$V_{ACP-ACN}$ ≥ 2.5mV	-15		20	
		$V_{ACP-ACN}$ ≥ 1.5mV	-25		35	
IADP Upper Clamp Voltage	V_{IADP_CLAMP}		3		3.3	V
IADP Output Load Capacitance	C_{IADP}	With 0mA to 1mA load			100	pF
IDCHG Output Voltage Range	V_{IDCHG}		0		3.6	V
IDCHG Output Current	I_{IDCHG}				1	mA
Current Sense Amplifier Gain	A_{IDCHG}	$V_{IDCHG}/V_{SRN-SRP}$, IDCHG_GAIN = 1		16		V/V
Current Sense Output Accuracy	V_{IDCHG_ACC}	$V_{SRN-SRP}$ = 81.28mV, IDCHG_GAIN = 0	-5.8		6	%
		$V_{SRN-SRP}$ = 40mV	-3.5		2.5	
		$V_{SRN-SRP}$ = 20mV	-6		4.5	
		$V_{SRN-SRP}$ = 10mV	-10		8	
		$V_{SRN-SRP}$ = 5mV	-20		15	
IDCHG Upper Clamp Voltage	V_{IDCHG_CLAMP}		2.45		3.6	V
IDCHG Output Load Capacitance	C_{IDCHG}	With 0mA to 1mA load			100	pF
PMON Output Voltage Range	V_{PMON}		0		3.7	V
PMON Output Current	I_{PMON}		0		100	μA
PMON System Gain (R_{AC} = R_{SR} = 10mΩ)	A_{PMON}	$V_{PMON}/(P_{IN} + P_{BAT})$, PMON_RATIO = 1		1		μA/W
PMON Gain Accuracy (with PMON_RATIO = 1 and R_{AC} = R_{SR} = 10mΩ)	V_{PMON_ACC}	Adapter-only, system running at 19.5V/45W	-5.5		5.5	%
		Adapter-only, system running at 12V/24W	-6		6	
		Adapter-only, system running at 5V/9W	-9.5		9.5	
		Battery-only, system running at 11V/44W	-5		5	
		Battery-only, system running at 7.4V/29.8W	-5.5		5.5	
		Battery-only, system running at 3.7V/14.4W	-7.5		7.5	
PMON Clamp Voltage	V_{PMON_CLAMP}		2.5		3.7	V

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, parameters are given with $V_{VCC\_UVLOZ} < V_{VCC} < V_{ACOV}$, $V_{VCC} > V_{SRN} + V_{SLEEP}$, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Converter Driving						
PWM Switching Frequency	f_{SW}	PWM_FREQ[1:0] = 00	530	600	670	kHz
		PWM_FREQ[1:0] = 01	690	800	880	
		PWM_FREQ[1:0] = 10	275	300	345	
		PWM_FREQ[1:0] = 11	360	400	460	
PWM Duty Cycle Range, Buck Mode	D_{BUCK}		20		100	%
PWM Duty Cycle Range, Boost Mode	D_{BOOST}		0		80	%
High-side Driver Turn-On Resistance	$R_{DS\_HI\_ON}$	V_{BTST} - V_{PH} = 5.5V		4.3	7.5	Ω
High-side Driver Turn-Off Resistance	$R_{DS\_HI\_OFF}$	V_{BTST} - V_{PH} = 5.5V		0.94	1.45	Ω
Bootstrap Comparator Refresh Threshold (V_{BTST} - V_{SW}) at which LS MOSFET Refresh Pulse is Requested	$V_{BTST\_REFRESH}$	V_{VCC} = 5V	3	3.6	4.2	V
Low-side Driver Turn-On Resistance	$R_{DS\_LO\_ON}$			7.5	11.5	Ω
Low-side Driver Turn-Off Resistance	$R_{DS\_LO\_OFF}$			0.85	1.3	Ω
Bootstrap Diode Forward Voltage (V_F)	V_{BTST_VF}	I_F = 10mA, LODRV turn on, measured between REGN and BTST		0.07		V
Soft-Start Current Rise Step Size	I_{STEP}			64		mA
Soft-Start Current Rise Step Time	t_{STEP}			480		μs
Input Over-Current Protection						
Rising Threshold (% of ICRIT Current Limit)	V_{ACOC}	ACOC_VTH = 1	185.5	200	210	%
ACOC Threshold Range	V_{ACOC_CLAMP}	V_{ACP} - V_{ACN}	48		185	mV
Battery Over-Voltage Protection						
OV Rising Threshold (% of V_{BAT_REG})	V_{BAT_OVP}	V_{SRN} rising	102	104	106	%
OV Falling Threshold (% of V_{BAT_REG})		V_{SRN} falling	100	102	104	%
SRP Discharge Current (Sinking)	I_{BAT_OVP}	V_{SRN} > 6V		15		mA
		V_{SRN} = 4.6V		12		mA
Cycle-by-Cycle Over-Current Limit (I_{OCP_LIMIT} = V_{OCP_LIMIT}/R_{SR} where the Voltage is Measured between SRP and SRN)	V_{OCP_LIMIT}	ChargeCurrent register = 0xxxh	51	60	70.5	mV
		ChargeCurrent register = 1000h to 17C0h	79	90	104.5	
		ChargeCurrent register = 1800h to 1FC0h	106	120	138.5	
Charge Current Cycle-by-Cycle Under-Current Falling Threshold	V_{UCP_FALL}	(V_{SRP} - V_{SRN}) falling	0.8	5.4	10	mV
Light Load Falling Threshold in Buck Mode	$V_{LL\_FALL\_BUCK}$	(V_{SRP} - V_{SRN}) falling, enter light charge current		1.25		mV
Light Load Rising Threshold in Buck Mode	$V_{LL\_RISE\_BUCK}$	(V_{SRP} - V_{SRN}) rising, exit light charge current		2.5		mV
Light Load Falling Threshold in Boost Mode	$V_{LL\_FALL\_BOOST}$	(V_{SRN} - V_{SRP}) falling, enter light discharge current		3		mV
Light Load Rising Threshold in Boost Mode	$V_{LL\_RISE\_BOOST}$	(V_{SRN} - V_{SRP}) rising, exit light discharge current		5.5		mV
ACP to PH Voltage Rising Threshold	V_{ACP-PH_RISE}	IFAULT_HI = 1 (HS short-circuit detection enabled)	580	780	980	mV
PH to GND Voltage Initial Rising Threshold	$V_{IFAULT\_LO\_RISE}$	IFAULT_LO = 1 (LS short-circuit detection enabled)	175	260	340	mV
Thermal Shutdown						
Thermal Shutdown Rising threshold	T_{SHUT_RISE}	Temperature increasing		150		℃
Thermal Shutdown Falling threshold	T_{SHUT_FALL}	Temperature decreasing		130		℃

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, parameters are given with V_{VCC_UVLOZ} < V_{VCC} < V_{ACOV}, V_{VCC} > V_{SRN} + V_{SLEEP}, typical values are measured at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REGN LDO						
REGN Regulator Output Voltage	V_{REGN_REG}	V_{VCC} = 10V, V_{ACDET} > V_{WAKEUP_RISE}	5.77	6.07	6.37	V
REGN Short-Circuit (GND) Current Limit when in Charging Mode	$I_{REGN\_LIM\_Charging}$	V_{REGN} = 0V, V_{VCC} > V_{UVLO}, in charging mode (CHRG_INHIBIT = 0)	78	110.0		mA
REGN Voltage when Current Limiting in Charging Mode	I_{REGN}	V_{VCC} = 5V, I_{LOAD} = 20mA	4.64	4.84	4.99	V
REGN Short-Circuit (GND) Current Limit when not in Charging	$I_{REGN\_LIM\_No\_Charging}$	V_{REGN} = 0V, V_{VCC} > V_{UVLO}, not in charging mode (CHRG_INHIBIT = 1)	15			mA
REGN Output during Thermal Shutdown	I_{REGN_TSHUT}	V_{REGN} = 5V	15	24		mA
REGN Output Filter Capacitor	C_{REGN}	I_{LOAD} = 100μA to 50mA		2		μF
PROCHOT Comparator Thresholds						
ICRIT Comparator Initial Threshold (in % of input Current Limit)	V_{ICRIT}	ILIM2_VTH[3:0] = 1001 (150%), I_{IN} limit = 4096mA (InputCurrent register = 1000h)	161	165	169.5	%
INOM Comparator Initial Threshold (in % of input Current Limit)	V_{INOM}	INOM_VTH = 0 (110%), I_{IN} limit = 4096mA (InputCurrent register = 1000h)	107.5	110	113	%
		INOM_VTH = 1 (106%), I_{IN} limit = 4096mA (InputCurrent register = 1000h)	103.5	106	109	
IDCHG Comparator Threshold (Voltage between SRN and SRP)	V_{IDCHG}	IDCHG_VTH[5:0] = 100000	157	163.84	168	mV
		IDCHG_VTH[5:0] = 001000	39.4	40.96	42.5	
VSYS Comparator Threshold to Trigger PROCHOT	V_{VSYS}	VSYS_VTH[1:0] = 00		5.75		V
		VSYS_VTH[1:0] = 01 (default)	5.83	6	6.17	
		VSYS_VTH[1:0] = 10		6.25		
		VSYS_VTH[1:0] = 11		6.5		
Miscellaneous Comparators						
Independent Comparator Input Common Mode	V_{CMP_CM}		0		5.0	V
Independent Comparator Reference Voltage (CMPIN Falling)	V_{CMP_REF}	CMP_REF = 0 (2.3V)	2.26	2.3	2.33	V
		CMP_REF = 1 (1.2V)	1.18	1.2	1.22	V
Independent Comparator Reference Hysteresis	$V_{CMP\_RISE\_HYST}$	CMP_POL = 0 (polarity: CMPIN high leads to CMPOUT low)		100		mV
V_{ILIM} Falling Threshold as Converter Enable	V_{ILIM_FALL}	V_{ILIM} falling	56	76	103	mV
V_{ILIM} Rising Threshold as Converter Enable	V_{ILIM_RISE}	V_{ILIM} rising	80	100	127	mV
Analog and Digital I/O						
Input Bias Current (Analog Pins)	V_{AIN_LEAK}	V_{BIAS} = 6V	-0.5		0.5	μA
Input Low Threshold (SDA, SCL)	V_{IN_LO}	SDA and SCL pins			0.73	V
Input High Threshold (SDA, SCL)	V_{IN_HI}	SDA and SCL pins	2.33			V
Input Bias Current (SDA, SCL)	V_{DIN_LEAK}	V = 6V, SDA and SCL pins	-0.5		0.5	μA
Output Saturation Voltage (ACOK, SDA, CMPOUT, nBST_STAT)	V_{OUT_LO}	5mA drain current (sink)			200	mV
Leakage Current (ACOK, SDA, CMPOUT, nBST_STAT)	V_{OUT_LEAK}	V = 6V	-0.5		0.5	μA
Output Saturation Voltage (nPROCHOT)	$V_{OUT\_LO\_PROCHOT}$	17mA drain current (sink)			400	mV
Leakage Current (nPROCHOT)	$V_{OUT\_LEAK\_PROCHOT}$	V = 6V	-0.5		0.5	μA

TIMING REQUIREMENTS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Comparators Deglitch Times						
ACOK Rising Deglitch to Turn-On ACFET	$t_{ACOK\_RISE\_DEG}$	ACOK_DEG = 0	110	150	190	ms
		ACOK_DEG = 1	0.8	1.2	1.6	s
ACOK Falling Deglitch to Turn-Off ACFET	$t_{ACOK\_FALL\_DEG}$				3	μs
Deglitch Time to Latch Off ACFET	t_{ACOC_DEG}		4.3	5.5	7	ms
Battery Depletion Rising Deglitch to Turn-Off ACFET and Turn-On BATFET	$t_{BATDEPL\_RISE\_DEG}$			600		ms
Battery Depletion Falling Threshold to Turn-Off BATFET and Turn-On ACFET	$t_{BATDEPL\_FALL\_DEG}$			2		μs
PWM Driver Timing						
Driver Dead Time from Low-side to High-side	$t_{DEADTIME\_RISE}$			20		ns
Driver Dead Time from High-side to Low-side	$t_{DEADTIME\_FALL}$			20		ns
SMBus Timing Characteristics						
Clock Frequency	f_{S_CL}		10		100	kHz
SCL/SDA Rise Time	t_R				1	μs
SCL/SDA Fall Time	t_F				300	ns
SCL Pulse Width High	t_{W_H}		4		50	μs
SCL Pulse Width Low	t_{W_L}		4.7			μs
Setup Time for START Condition	t_{SU_STA}		4.7			μs
Start Condition Hold Time before Generating the First Clock Pulse	t_{H_STA}		4			μs
Data Setup Time	t_{SU_DAT}		250			ns
Data Hold Time	t_{H_DAT}		300			ns
Setup Time for STOP Condition	t_{SU_STOP}		4			μs
Bus Free Time between START and STOP Conditions	t_{BUF}		4.7			μs
Host Communication Failure						
SMBus Bus Release Timeout	$t_{TIMEOUT}$		25		35	ms
Watchdog Timeout Period	t_{WDI}	WDTMR_ADJ[1:0] = 01	4	5	6	s
		WDTMR_ADJ[1:0] = 10	68	78	88	s
		WDTMR_ADJ[1:0] = 11	135	155	175	s

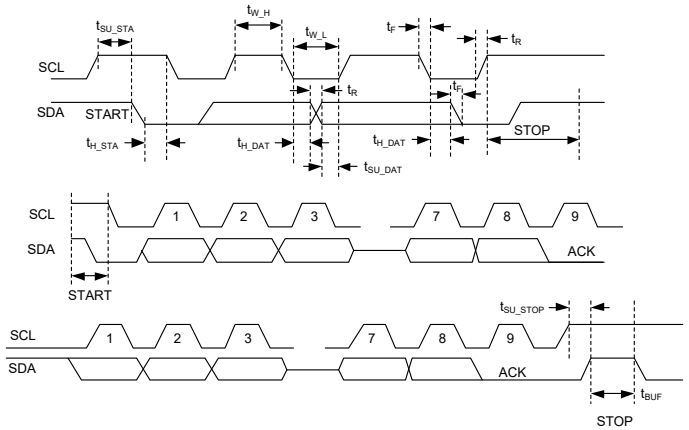
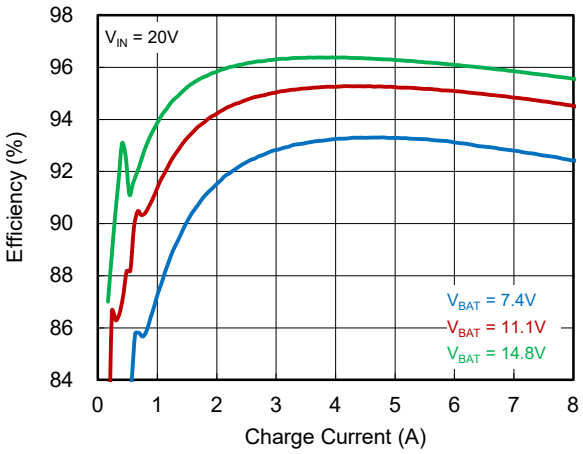


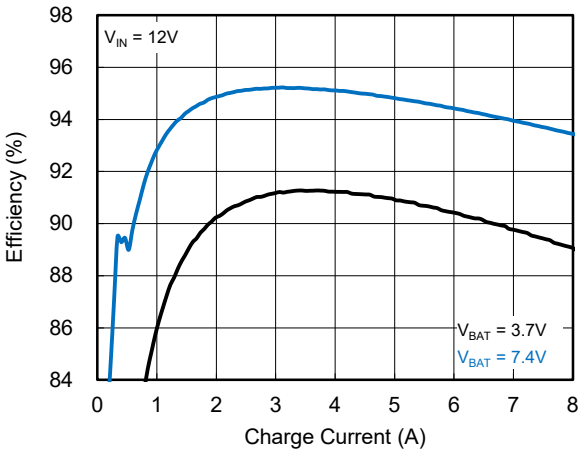
Figure 1. SMBus Key Waveforms and Timings

TYPICAL PERFORMANCE CHARACTERISTICS

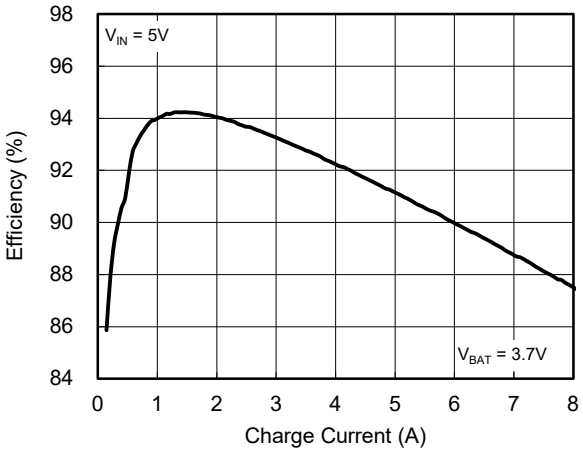
Efficiency during Charging



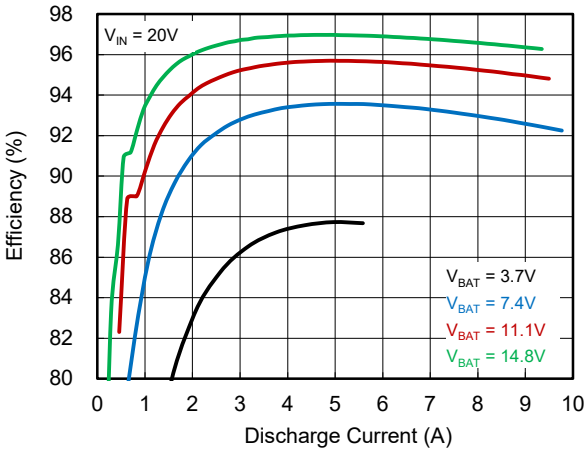
Efficiency during Charging



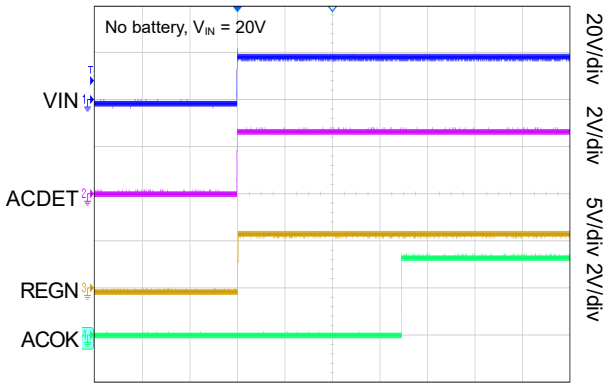
Efficiency during Charging



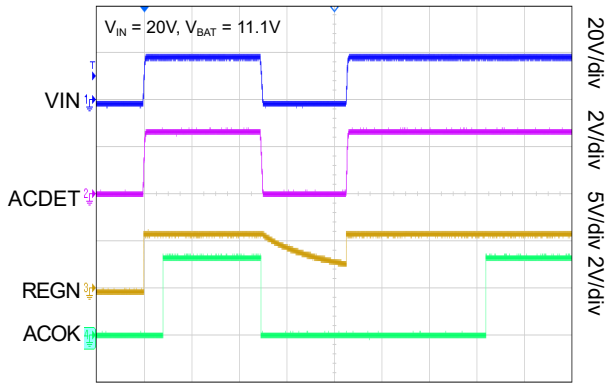
Efficiency during Boost



VCC, ACDET, REGN, and ACOK during Power-Up

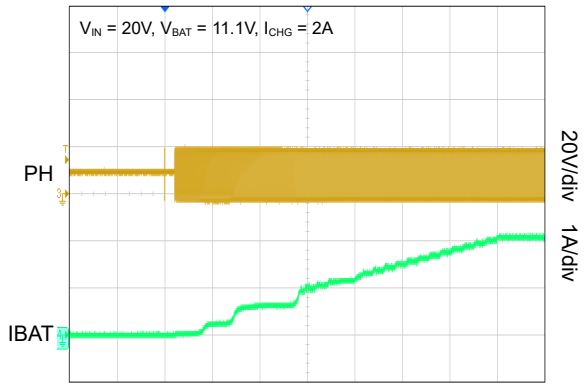


Power On ACOK Delay at 1st and 2nd Adapter Plug-in

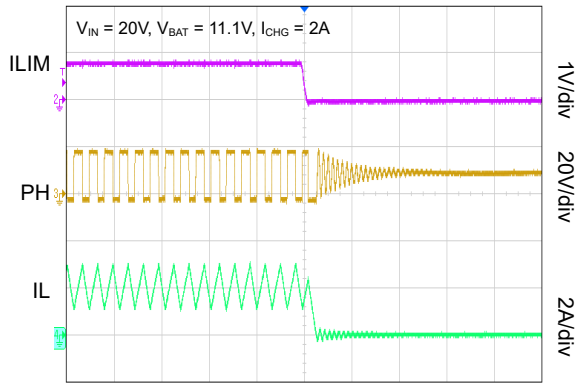


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

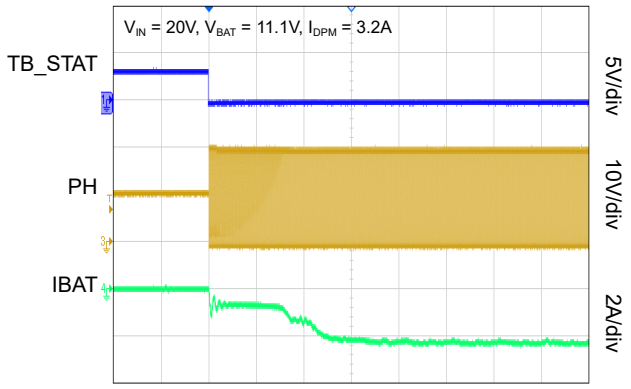
Charge Enable with Soft-Start



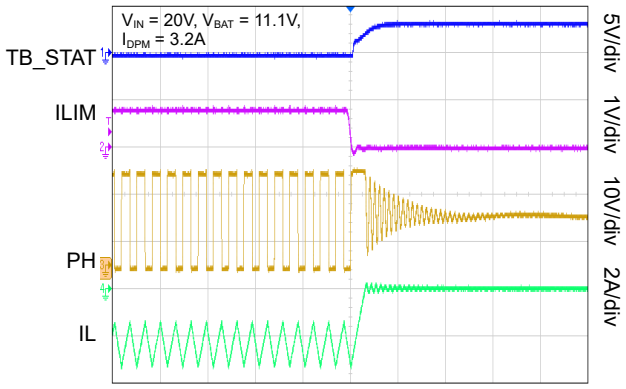
Charge Disabled by ILIM



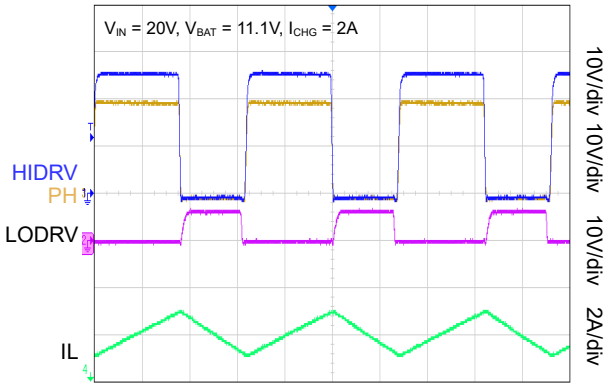
Hybrid Power Boost Mode Enabled



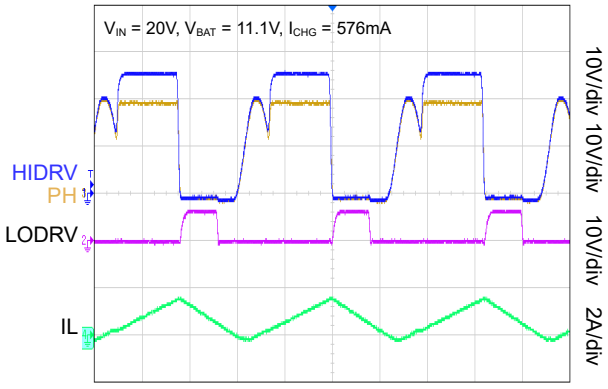
Hybrid Power Boost Mode Disabled by ILIM



CCM during Charging

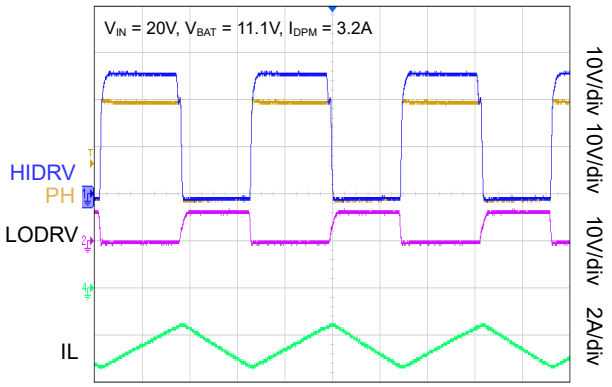


DCM during Charging

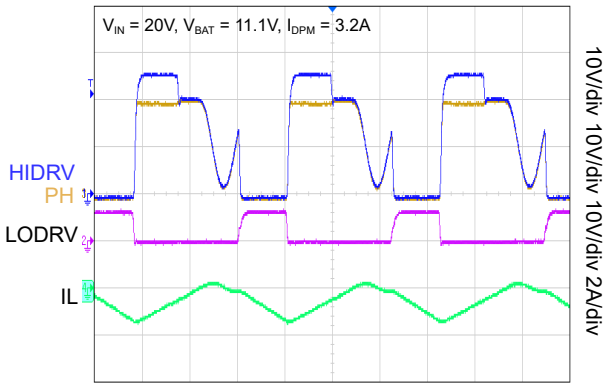


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

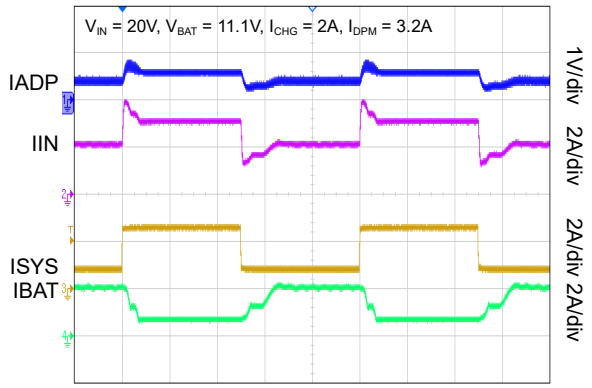
CCM during Hybrid Power Boost Mode



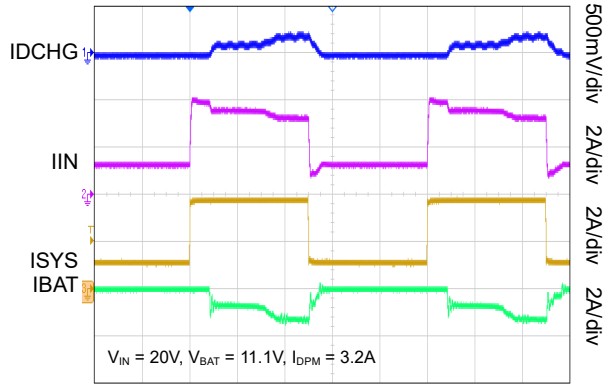
DCM during Hybrid Power Boost Mode



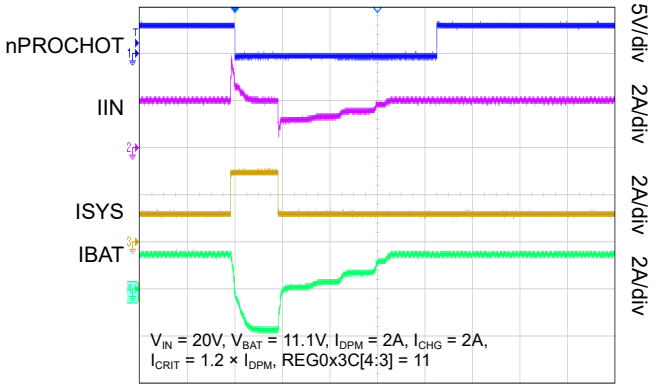
Input Current Regulation during System Load Transient



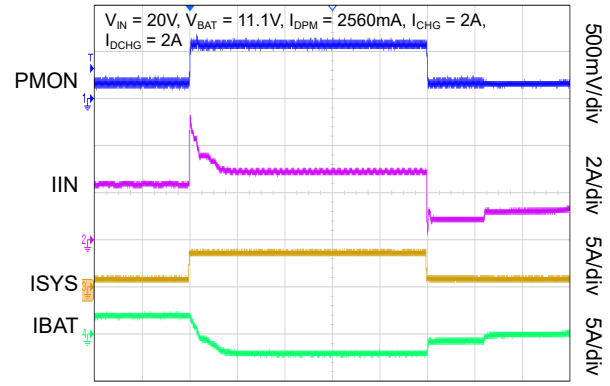
Hybrid Power Boost Mode with Charge Enable



Hybrid Power Boost Mode with Charge Enable, nPROCHOT Asserted



Hybrid Power Boost Mode with Discharge Current Regulation



FUNCTIONAL BLOCK DIAGRAM

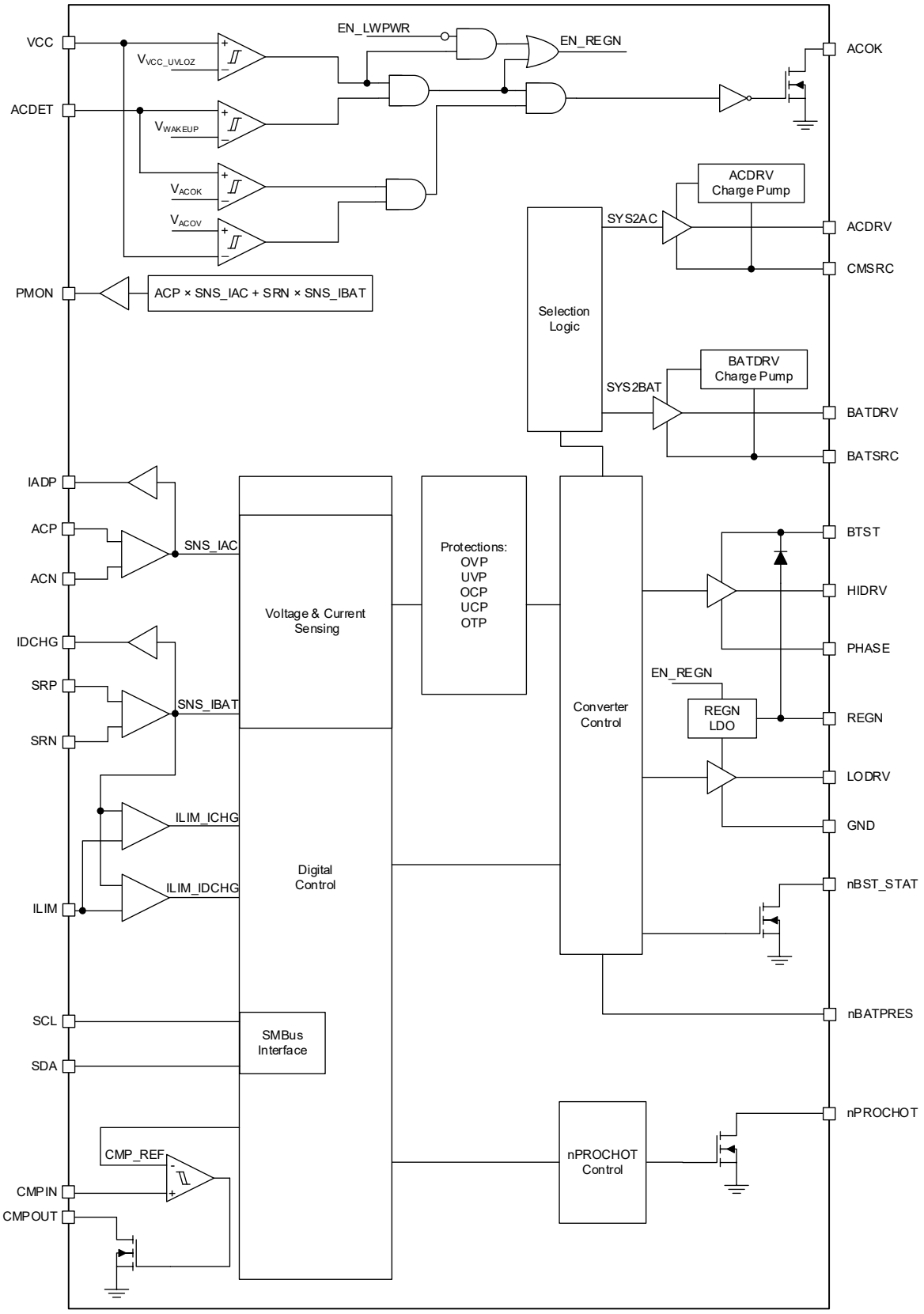


Figure 2. Functional Block Diagram

DETAILED DESCRIPTION

Overview

The SGM41538 is a multi-chemistry battery charging controller with automatic power source selection (adapter or battery) and 4.5V to 24V input voltage range. This device is an ideal choice for space-limited portable applications with 1- to 4-cell batteries such as notebook and detachable ultra-books. The power source selection is implemented through separate drivers for the external N-MOSFETs (ACFET, RBFET and BATFET) that control connection of those sources.

Dynamic Power Management (DPM) is included to prevent adapter overloads by limiting the input power while maximizing the utilization of adapter power rating. Adapter is loaded close to its maximum power for system load and battery charging. With DPM, if during the battery charging the system power demand is increased, the charge current is decreased accordingly to keep the total adapter current below its rating. If the system power is increased above the adapter rating, the Hybrid Power Boost mode (called "Turbo Boost mode" previously) will start to assist the adapter by discharging battery to the system.

With the integrated accurate current sense amplifiers (analog outputs), system power (PMON), input current (IADP) and battery discharge current (IDCHG) can be constantly monitored. If an over-current is detected, the adapter or battery will be disconnected and an nPROCHOT (processor hot) alert signal is sent to the CPU. The CPU should then re-adjust and optimize the charge parameters to get the best system performance with the available power.

The SGM41538 SMBus interface allows accurate adjustments of the input current, charge voltage and charge current. The nPROCHOT timings and thresholds are also SMBus adjustable for maximum adaptation to the system requirements.

Power-On Reset (POR)

The SGM41538 is powered by an adapter or battery. Typically, they are connected to VCC by external Schottky diodes (OR). If VCC voltage exceeds its UVLO threshold, the device will awake with a power-on reset (POR) and then SMBus communication can be started.

Battery-Only Operation

When adapter is not present, BATFET (Q3 in Figure 7) is turned on when the device is powered up (from battery) if $V_{VCC} > V_{VCC\_UVLOZ}$. After reset, the SGM41538 remains in low power mode with the lowest quiescent current by default (EN_LWPWR bit is set to 1). Resetting EN_LWPWR to 0 by SMBus enables the performance mode. In this mode the IDCHG and PMON buffers, nPROCHOT protection functions, Battery-Only-Boost mode and independent comparator can be enabled by SMBus. To have accurate references, the REGN LDO is enabled (except when only IDCHG buffer) in battery-only performance mode.

Adapter Detection and ACOK Output

The ACDET input senses the adapter voltage through an external resistor divider. The AC detection threshold is typically set higher than the maximum battery voltage, but less than the minimum acceptable adapter voltage. All internal bias circuits are enabled when $V_{ACDET} > V_{WAKEUP\_RISE}$.

ACOK is an open-drain output that goes high (external pull-up) when an adapter is detected. The conditions for ACOK = high are:

- $V_{VCC\_UVLOZ} < V_{VCC} < V_{ACOV}$
- $V_{ACDET} > 2.4V$
- $V_{VCC} - V_{SRN} > V_{SLEEP\_RISE}$ (Note that V_{SRN} is the sensed battery voltage or V_{BAT})

The ACOK_STAT bit represents the status of ACOK pin. The deglitch time for ACOK is set by ACOK_DEG bit (150ms or 1.2s), and its POR default value is 1.2s, however, it will be 150ms for the first time that the adapter is plugged in, if no write to ACOK_DEG bit has occurred since POR. For all subsequent adapter detections (after the first one), the deglitch time is set by ACOK_DEG bit (150ms or 1.2s). So, if this bit is not overwritten after POR, only after the first adapter plug-in, the deglitch time is 150ms and for any other plug-in, deglitch will be 1.2s. If the battery has been present already and ACOK_DEG bit is re-written to 1.2s before the first adapter plug-in, the ACOK deglitch will be 1.2s for the first plug-in as well.

Adapter Over-Voltage (ACOV)

An adapter over-voltage is detected if V_{VCC} exceeds 25.7V. Upon detection of an ACOV charge will be disabled, ACOK goes low, ACFET/RBFET turn off (to disconnect the high voltage from the system), and BATFET turns on if the turn-on conditions are valid. The ACOV event is cleared when V_{VCC} returns below 24.8V (normal range). In this case, the device releases the ACOK to go high, turns the BATFET off, and turns the ACFET and RBFET on again to power the system from the adapter.

DETAILED DESCRIPTION (continued)

REGN LDO

The REGN is an LDO regulator that also serves as an internal voltage reference. This LDO is enabled whenever V_{ACDET} is higher than V_{WAKEUP_RISE} and is disabled when the adapter is removed and low power mode is enabled (EN_LWPWR = 1) regardless of other registers and settings. It will be enabled if the low power mode is disabled (EN_LWPWR = 0) and one of the following functions is enabled:

- Power Monitor Function (PMON)
- Processor Hot Function (nPROCHOT)
- Independent Comparator
- Battery-Only-Boost (EN_BATT_BOOST)

System Power Selection

The switch between the adapter and battery as power source for the SGM41538 is automatic and with a break-before-make logic to avoid shoot-through between the two sources during transitions.

Two common source N-MOSFETs (ACFET and RBFET, named as Q1 and Q2 in Figure 7 or Figure 8) are placed between the adapter and ACP pin. Their common gates are driven by the ACDRV output and both sources are connected to the CMSRC pin.

The ACFET is used to disconnect adapter from system and battery. It also limits the inrush current rise (di/dt) by controlling the turn-on time when the adapter is plugged in. The ACFET also protects the adapter if a short-circuit occurs in the battery or system.

The RBFET blocks negative voltage if a reverse input voltage is accidentally applied and also protects the battery discharge to the input if a short occurs on the adapter side. Compared to a reverse blocking Schottky diode, the RBFET has much lower power dissipation thanks to its low R_{DSON}.

The ACDET input is used to detect the presence of the adapter. If V_{ACDET} is below 2.4V, it means that a valid adapter is not present and the device isolates the system from the adapter input by pulling the ACDRV to CMSRC and keeping ACFET and RBFET off. In this situation, if all following conditions are valid, the system will be connected to the battery through BATFET (N-MOSFET) by bringing its gate voltage to V_{BATSRC} + 6V on the BATDRV output:

- $V_{VCC} > V_{VCC\_UVLOZ}$
- V_{ACN} (System Voltage) < V_{SRN} (Battery Voltage) + 200mV
- ACFET and RBFET are off

A valid adapter is detected when V_{ACDET} is above 2.4V. If all following conditions are valid, the ACDRV will go high to turn the ACFET and RBFET on, and change the system power source from battery to adapter:

- ACOK is high.
- Device is not in LEARN mode, or if it is in LEARN mode, the V_{SRN} is below the battery depletion threshold.

The gate drive voltage for the ACFET/RBFET is V_{CMSRC} + 6V. If after 20ms of turning the ACFET/RBFET on, the gate-source voltage is still below 5.7V, the ACFET/RBFET will be turned off. A turn-on retry will repeat after a 1.2s delay, and if the same failure occurs for seven times within a 90s period, the ACFET/RBFET will latch off. In this case, it is necessary to remove the adapter and shut down the system to reset the device by forcing V_{ACDET} below V_{ACOK_FALL} (2.35V TYP). The ACFET/RBFET can turn on again after reset. The failure counter is reset to zero after 90s to avoid false latch off.

At least one of the following conditions must be valid to turn off ACFET and RBFET:

- If the device is in LEARN mode, V_{SRN} is higher than battery depletion threshold.
- ACOK is low.

Two external capacitors (C_{GS} and C_{GD}) must be carefully selected based on the following considerations and placed on the ACFET for limiting the adapter inrush current during turn-on:

- Try to minimize the total system bus capacitance.
- Choose C_{GS} at least 40 times higher than C_{GD} to prevent ACFET false turn-on during adapter hot plug-in.
- ACFET must be fully turned on within 20ms, otherwise a turn-on failure will be detected.
- MOSFET peak current rating must be high enough.
- Use 4kΩ gate drive current limiting and slow-down resistors in series with ACDRV, CMSRC and BATDRV pins to increase the gate voltage rise time and limit inrush and fault currents.

DETAILED DESCRIPTION (continued)

Battery Charging in Buck Mode

This device controls charging of the batteries or super-capacitor stacks with Buck switching converters. A complete charge cycle includes constant-current (CC) and constant-voltage (CV) phases. In constant-current phase, the charge current is regulated to a limit which is set in ChargeCurrent Register. The charger enters CV mode to regulate the battery voltage when SRN voltage reaches the voltage level set in ChargeVoltage Register. The following conditions must be met to start charging in the charge mode:

- Charge is enabled (CHRG_INHIBIT bit is 0, and charge is enabled by default).
- ILIM pin voltage is above V_{ILIM_RISE} (100mV TYP).
- Valid values are set through SMBus in ChargeCurrent register and ChargeVoltage register.
- ACOK is high (valid adapter) - see Adapter Detection and ACOK Output section.
- ACFET and RBFET are on (with sufficient gate voltage) - see System Power Selection section.
- V_{SRN} is below BATOVP threshold.
- Device junction temperature is below TSHUT threshold.
- Device is not in ACOC condition - see Protections Functions section.

The charge will stop if any of the following events occur:

- Charge is inhibited (set CHRG_INHIBIT bit to 1 through SMBus).
- ILIM pin voltage falls below V_{ILIM_FALL} (76mV TYP).
- Setting one of the ChargeCurrent register and ChargeVoltage register to 0.
- ACOK goes low (invalid adapter voltage).
- ACFET is turned off.
- V_{SRN} exceeds BATOVP threshold (battery over-voltage).
- Thermal shutdown.
- ACOC is detected (adapter over-current).
- Short-circuit is detected (see MOSFETs and Inductor Short-Circuit Protections section).
- Watchdog timer expires (if watchdog timer is enabled, see Watchdog Timer section).

Automatic Charge Current Soft-Start

After charging is enabled, the charge current will start to rise with an automatic soft-start to prevent stress or over-current/overshoot on the converter and output capacitors. With a 10mΩ sense resistor the charge current starts at 128mA and in CCM mode rises with 64mA steps in each ~480μs until it reaches the programmed value. While the converter is in DCM mode, the step size is larger and lasts longer due to the slower converter response.

Hybrid Power Boost Mode (HPB)

When the required system power is higher than the adapter power, the Hybrid Power Boost feature can be turned on to allow discharging battery to system and prevent adapter and system fail. After power-up, the HPB feature is disabled by default (EN_HYBRID_BOOST bit is 0). Set this bit to 1 to enable HPB feature. The status of HPB is indicated on the nBST_STAT output pin and can also be read from the BOOST_STAT bit through SMBus.

For HPB, the input current must be set to a value above 1536mA (with a R_{AC} = 10mΩ input current sensing resistor). The input current threshold for entering HPB can be set to 104% or 107% of the input current limit by the FDPM_RISE bit (0 = 107% and 1 = 104%). If the peak power mode is not enabled (see Peak Power Mode or Two-Level Adapter Current Limiting section), the input current limit is I_{LIM1} (set in InputCurrent register). If the peak power mode is enabled and the device is in the t_{OVLD} duration of the of peak power mode cycle, the input current limit is I_{LIM2}, and the HPB threshold is 107% of the I_{LIM2}. In the rest of a peak power mode cycle, the input current limit will be I_{LIM1}. When input current exceeds 107% of the input current limit, the controller begins battery discharge by changing the converter from Buck mode to Boost mode. During HPB, the adapter current will be regulated to the input current limit level. Use watchdog timer to prevent too long operation in HPB mode.
Any of the following conditions will stop the HPB mode:

- Power demand reduction (battery discharge current drops to 0A).
- Light load on adapter (adapter current fall below 750mA).
- Disabling HPB (EN_HYBRID_BOOST is reset to 0).
- Removing adapter.
- Low battery voltage (V_{BAT} falls below depletion threshold, set in BAT_DEPL_VTH[1:0] bits).
- ACFET turn-off.
- Thermal shutdown.
- Short-circuit detection (see MOSFETs and Inductor Short-Circuit Protections section).
- Watchdog timer expires (if watchdog is enabled).

DETAILED DESCRIPTION (continued)

Battery-Only-Boost Mode

This mode is enabled if EN_BATT_BOOST = 1. When Battery-Only-Boost mode is enabled, if there is no adapter, system is powered from the battery and the converter operates in Boost mode to regulate the system voltage when the battery voltage is lower than the minimum system voltage (set in REG0x3E). In Battery-Only-Boost mode, the supply rail voltage is regulated to V_{SYSMIN} plus an offset value which is set in the VBOOST bit. This offset is + 1.6V (if VBOOST = 0, default) or + 2.4V (if VBOOST = 1). The Boost mode keeps the system running until complete depletion of the battery. While the device is operating in this mode, the BOOST_STAT bit is 1 and nBST_STAT indicator output pin is low.

Battery-Only-Boost mode will terminate if any of the following occurs:

- Disabling Battery-Only-Boost mode (EN_BATT_BOOST bit is reset to 0).
- Enabling battery low power mode (EN_LWPWR bit is set to 1).
- Adapter is plugged in (resulting in ACOK go high).
- Battery depletion (V_{BAT} falls below depletion threshold, set in BAT_DEPL_VTH[1:0] bits).
- Thermal shutdown.
- Short-circuit detection (Refer to MOSFETs and Inductor Short-Circuit Protections section).
- Watchdog timer expires (if watchdog is enabled).

In the Battery-Only-Boost mode, the minimum ACOK falling ACDET threshold (2.30V) must be higher than the regulation level (V_{SYSMIN} + 1.6V or + 2.4V) and the lowest supported adapter voltage must be higher than that for smooth changeover during adapter plug in or removal. For example, if V_{SYSMIN} = 6.656V and VBOOST = 1 (2.4V), the input detection threshold must be above 9.056V plus some additional margin, like 10V for this example. If the selected ACOK falling threshold is the minimum (2.3V), the ACDET divider ratio (ground-side resistor to the total divider resistance) should be lower than 2.3V/10V.

Power and Current Monitoring

Accurate Current Sense Amplifiers (for IADP and IDCHG)

Two accurate current sense amplifiers (CSA) monitor the input current (IADP) and the discharge current (IDCHG). These outputs are commonly used in industry for charger monitoring. The IADP voltage is 20 (default) or 40 times the ACP-ACN differential voltage (set in IADP_GAIN bit). The IDCHG voltage is 8 or 16 (default) times the SRN-SRP differential voltage (set in IDCHG_GAIN bit). IADP output is valid only if $V_{VCC} > V_{VCC\_UVLOZ}$ and $V_{ACDET} > V_{WAKEUP}$.

- V_{IADP} = 20 or 40 × (V_{ACP} - V_{ACN}) in charge and Hybrid Power Boost modes.
- V_{IDCHG} = 8 or 16 × (V_{SRN} - V_{SRP}) in discharge mode (Hybrid Power Boost or Battery-Only-Boost modes).

It is recommended to place a small capacitor (100pF MAX) on these outputs to decouple high frequency noise. An RC filter can also be added if more filtering is desired, but lower cutoff frequency results in CSA slower response. Use a resistor divider at the CSA output can reduce the voltage of current monitoring and keep the high accuracy against temperature variations.

Accurate Power Sense Amplifier (for PMON)

Total available power from adapter and battery together is monitored in the SGM41538. The ratio factor (K_{PMON} defined as the ratio of the PMON pin voltage to the total system power) is set by the gain (programmed in PMON_RATIO bit, default 1μA/W) and the connected PMON resistor to GND for current to voltage conversion. The input sense resistor (R_{AC}) can be selected 2× or 0.5× the charge sense resistor (R_{SR}) by setting RSNS_RATIO[1:0] bits to 01 or 10.

$$I_{PMON} = K_{PMON} (V_{IN} \times I_{IN} - V_{BAT} \times I_{BAT}) \quad (1)$$

Note that in charge $I_{BAT} > 0$ and in discharge $I_{BAT} < 0$.

Like CSA, a small capacitor (100pF MAX) is recommended on PMON output to decouple high frequency noise. An additional RC filter may also be used if needed, considering that lower cutoff frequency increases the amplifier response delay.

DETAILED DESCRIPTION (continued)

CPU Throttling and Processor Hot Indication

The CPU peak power may go too high and exceed the total available power from the adapter and battery when it is operating in turbo mode. The signs of such over-power are adapter high current, overshoot in battery discharge current, or system bus voltage drop. Also, without the adapter or battery, the power may not be sufficient for the CPU turbo mode peak power. Such events are grouped and monitored by the processor-hot function with programmable thresholds and deglitch times for each event. If one of the events is triggered, an nPROCHOT pulse will be asserted. The following 7 events are included in the nPROCHOT profile of the SGM41538:

- ICRIT: Programmed adapter critical current (I_{CRIT} = 1.1 × I_{LIM2}) is exceeded (programmable threshold and deglitch time).
- INOM: Adapter average current exceeds 110% of the input current limit (programmable threshold and deglitch time).
- IDCHG: Programmed battery discharge over-current is exceeded (programmable threshold and deglitch time).
- VSYS: Battery voltage (V_{SRN}) (for 2-cell to 4-cell batteries) falls below programmed threshold (programmable threshold).
- CMPOUT (independent comparator output) transition from high to low (programmable deglitch time).
- ACOK falling edge (high to low transition upon adapter removal).
- nBATPRES input rising edge (transition from low to high upon battery removal).

All events can be individually enabled/disabled in PROCHOT_PROFILE[6:0]. The I_{CRIT} threshold is set as a percentage of the input IDPM (regulation) current. The InputCurrent register (or IDPM) is set with 7 bits in REG0x3F, and its default value is 4096mA. I_{LIM2} can be set to 110% to 250% of I_{DPM}. If I_{DPM} is set too small, the I_{CRIT} can trigger nPROCHOT upon adapter connection due to the inrush current, especially if a short deglitch time like 10μs or 100μs is used. The exact settings that potentially may cause a trip, depend on the system rail capacitance and the difference between the adapter and battery voltages. Larger capacitance or larger voltage difference increase the inrush current. A false trigger is more expected to occur if I_{CRIT} is below 512mA.

With any nPROCHOT event, the nPROCHOT output is pulled low for at least 10ms (PROCHOT_WIDTH[1:0] = 10 by default). This low pulse will be extended if at the end of the 10ms period the event is still present.

During an nPROCHOT cycle, if any new triggering event occurs, it will be saved in the PROCHOT_STAT[6:0] status register. They can be used for design tests and system optimization.

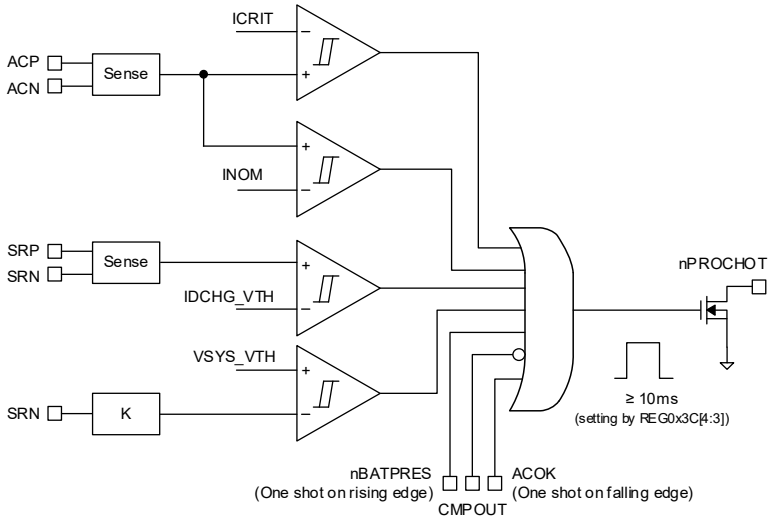


Figure 3. nPROCHOT Logic and Events Profile

DETAILED DESCRIPTION (continued)

Dynamic Power Management and Input Current

Dynamic power management is used to adjust the charge current such that adapter current remains close to its maximum limit (I_{LIM1}) which is set in InputCurrent register. If the system demands a current above this limit, the peak power mode (if enabled) will be activated (see Peak Power Mode or Two-Level Adapter Current Limiting in the next section). If this mode is not enabled, then HPB will be activated (if it is enabled and all conditions are valid). Adapter current may exceed the I_{LIM1} limit if none of these modes are active. Exceeding I_{LIM1} may result in INOM, nPROCHOT or ACOC events. I_{LIM1} and FDPM_RISE (input current HPB entry threshold) are measured with high precision. I_{LIM1} can be set in 64mA increments in InputCurrent register, and FDPM_RISE threshold can be set to 104% or 107% of the I_{LIM1}. The high precision allows the following combinations of settings:

- If InputCurrent register is set as a multiple of 128mA (bit [6] = 0), the FDPM_RISE can be set to 107% for any I_{LIM1} value.
- If InputCurrent register is set as a multiple of 128mA (bit [6] = 0) the FDPM_RISE can be set to the tighter 104% threshold for I_{LIM1} values above 2.5A (that is for I_{LIM1} > 2560mA only).
- The InputCurrent register can be set with the higher 64mA precision (bit [6] = 1) for I_{LIM1} > 2.5A if FDPM_RISE = 107%.

Peak Power Mode or Two-Level Adapter Current Limiting

An adapter is usually able to tolerate load currents above its rating for short periods (less than a few tens of milliseconds). This ability can be utilized for two-level input current limiting (or peak power mode) to reduce discharge when CPU is running in turbo mode. EN_PKPWR is the enable bit for the peak power mode. I_{LIM1} current limit is the adapter DC current in DPM and is set in InputCurrent register (below but near adapter rating) while I_{LIM2} (short time increases overloading limit) is set as a percentage of I_{LIM1} (or DPM current) through the ILIM2_VTH[3:0] bits in the 110% to 250% range.

A load transient can cause a surge in the input current or battery discharge (when both adapter and battery supply the system together), or a drop in the system voltage (when the system is supplied by adapter only). Upon detection of such events, if the peak power mode is enabled, firstly the I_{LIM2} input current limit will be in effect for a period of t_{OVLD} (set by PKPWR_TOVLD[1:0] in the 1ms to 10ms range), and then if high load continues, adapter current will be limited to I_{LIM1} for a duration up to t_{MAX} - t_{OVLD}. The t_{MAX} value is set by PKPWR_TMAX[1:0] in the 20ms to 1300ms range (20ms by default). If the load current remains high after the t_{MAX} period, another peak power cycle will begin. Otherwise, the charge will resume after the expiry of t_{MAX}.

The timing parameters (t_{OVLD} and t_{MAX}) cannot be modified while the device is in this mode (peak power mode is enabled if EN_PKPWR = 1) and any attempt to write to these registers (PKPWR_TOVLD[1:0] and PKPWR_TMAX[1:0]) is ignored. For any change in t_{OVLD} or t_{MAX}, this mode must be disabled (reset EN_PKPWR to 0) and then re-enabled.

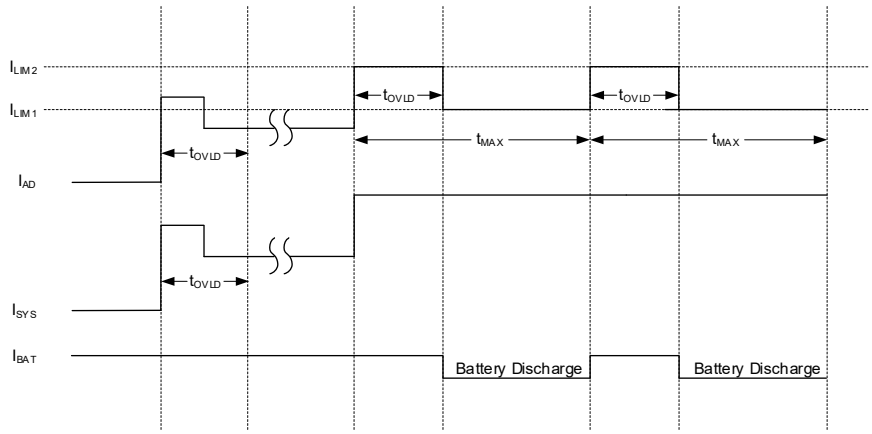


Figure 4. Timings of the Peak Power Mode Two-Level Adapter Current (IAD-Current through R_{AC}) Limiting after System Current (I_{SYS}) Surge

DETAILED DESCRIPTION (continued)

Converter in Buck Mode (Charging)

In Buck mode (charging), the converter operates as a fixed frequency, voltage mode control synchronous PWM Buck converter with a type III internal compensation. The resonance frequency determined by the output LC filter is given by Equation 2:

$$f_O \approx \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

Choose this frequency such that with the internal compensation, converter has sufficient phase margin. For the best performance choose the LC filter such that the nominal f_O frequency falls in the 10kHz to 20kHz range. Some recommended LC components are given in Table 1 for the selectable switching frequencies of 300kHz to 800kHz and for different charge current configurations. Note that the output capacitor (C_O) is the total capacitance present at the battery connection (place it on the SRN node of the charge current sense resistor). To calculate these tables, the inductance is first selected to set the current ripple in the 20% to 40% of the desired charge current and then the capacitance is selected such that the resonant frequency falls between 10kHz and 20kHz.

The DC bias voltage of ceramic capacitors significantly reduces the effective capacitance of them especially at higher output voltages and for smaller size packages. Consider the proper capacitance derating for C_O based on the manufacturer recommendations. A rated voltage much higher than the operating voltage may be required to minimize such derating.

Table 1. Suggested LC Filters for Some Common Charge Currents

Default Switching Frequency	LC Parameters	Charge Current				
		2A	3A	4A	6A	8A
800kHz	L (μH)	6.8 or 8.2	5.6 or 6.8	3.3 or 4.7	3.3	2.2
	C_O (μF)	20	20	20	30	40
	R_{SR} (mΩ)	10	10	10	10	10
600kHz	L (μH)	x	6.8	5.6	3.3 or 4.7	3.3
	C_O (μF)	x	20	20	30	30
	R_{SR} (mΩ)	x	10	10	10	10
400kHz	L (μH)	x	x	6.8 or 8.2	5.6	4.7
	C_O (μF)	x	x	20	20	20
	R_{SR} (mΩ)	x	x	10	10	10
300kHz	L (μH)	x	x	8.2	6.8	5.6
	C_O (μF)	x	x	20	20	20
	R_{SR} (mΩ)	10	10	10	10	10

NOTE: R_{SR}: Charge Sense Resistor, x: Not Recommended.

DETAILED DESCRIPTION (continued)

Battery-Only: Converter in Boost Mode Discharging

In Battery-Only-Boost mode, the converter operates as a fixed frequency voltage mode control synchronous Boost PWM converter with internal type III compensation. In this mode the output LC filter resonant frequency is given by Equation 3:

$$f_O \approx \frac{1}{2\pi\sqrt{LC}} \times \frac{V_{IN}}{V_O} \quad (3)$$

Use Equation 3 to design the LC filter, such that the internal compensation can achieve enough phase margin. For the best performance, choose the nominal LC resonant frequency in the 3.5kHz to 6.0kHz range. Some suggested output capacitances for the recommended inductor values at various V_{SYS}/V_{BAT} Boost ratios are given in Table 2. In this table, C_O is the system node capacitance that must be connected to the ACN side of the adapter sense resistor for the Battery-Only-Boost configuration. The inductance is calculated based on the Buck charging current (Buck mode). The selected inductance determines the system capacitance such that the output resonant frequency is 6.0kHz. Use the lowest Boost ratio in the supported range for selecting the components. For example, if V_{SYSMIN} = 6.7V and VBOOST = 0 (1.6V), the converter boosts when the V_{BAT} is in the 6.0V to 6.7V range and the lowest Boost ratio will be (6.7 + 1.6)/6.7 = 1.24, so for this example the V_{SYS}/V_{BAT} = 1.25 row should be used to select the system capacitance. The minimum recommended system capacitance is 60μF for proper transient response, therefore larger inductors are not recommended at higher Boost ratios.

Table 2. Suggested LC Value for the Battery-Only-Boost Operation (x: Not Recommended)

System Capacitor C_O (μF)	Boost Inductor L_O (μH)					
Boost Ratio (V_{SYS}/V_{BAT})	2.2	3.3	4.7	5.6	6.8	8.2
1.25	200	135	95	80	66	60
1.5	140	95	66	60	x	x
2.0	80	60	x	x	x	x

Continuous Conduction Mode (CCM)

Inductor current will be continuous (CCM operation) if the charge current is large enough and stays above zero during each switching cycle. At the beginning of each cycle, the ramp signal starts from 600mV, and the high-side switch (HS MOSFET) is turned on while the error amplifier output (EAO) voltage is higher than the ramp. The HS switch turns off and after a short dead time the low-side switch (LS MOSFET) turns on when the ramp rises above the EAO voltage. At the end of the cycle, the ramp resets to 600mV and the LS switch turns off to prepare for a new cycle. A break-before-make logic always provides a short dead time in which both switches are off during transition to prevent shoot-through. During dead time, the inductor current is circulated through the LS MOSFET body-diode. In CCM, the converter acts as a system with two fixed poles. By keeping the LS MOSFET on during the off times (synchronous rectification), the power dissipation remains low and allows safe high current charging.

DCM (Discontinuous Conduction Mode) Converter Operation

Inductor current (I_L) has a downward slope when HS MOSFET is off (LS MOSFET on). If I_L reaches zero, the converter enters DCM. To prevent system voltage from being boosted by the HS MOSFET body diode, the under-current protection (UCP) prevents negative current and turns off the LS MOSFET if its current falls below 0.54A (in other words, the R_{SR} = 10mΩ voltage drops below 5.4mV). In DCM the system response changes to a single-pole system. The pole location is proportional to the load current.

Light Load Detection (Comparator) and Non-Synchronous Operation Mode

Light load is detected when the charge current drops below 125mA (sensed on the R_{SR} = 10mΩ). In light load status, the controller keeps LS MOSFET off to prevent negative current (and boost back), and converter enters non-synchronous mode. When charge current increases above 250mA, converter exits the light load status and LS MOSFET can turn on again.

Likewise, in Boost mode light load status (discharge current below 300mA), the HS MOSFET is kept off and converter enters the non-synchronous mode to prevent negative inductor current and current back flow to the battery. When the charge current exceeds 550mA, the HS MOSFET can turn on again.

DETAILED DESCRIPTION (continued)

Switching Frequency Selection

The switching frequency can be selected between 300kHz, 400kHz, 600kHz and 800kHz (default) by setting PWM_FREQ[1:0] bits through SMBus. This feature can be used to help solve EMI problems.

LEARN Cycle for Battery

To calibrate the battery gas gauge, a full discharge and charge cycle can be completed through the LEARN function. A LEARN cycle is started by setting the EN_LEARN bit to 1. After enabling the LEARN, the system is only powered from battery and not the adapter by turning ACFET/RBFET off and BATFET on. The LEARN cycle is automatically terminated when the battery voltage falls below the depletion threshold and then the controller turns BATFET off and ACFET/RBFET on to switch back to the normal power input from adapter. The EN_LEARN bit automatically resets to 0 after completing a LEARN cycle.

If during a LEARN cycle the adapter is removed, LEARN mode is terminated by clearing EN_LEARN to 0 and BATFET remains on without any glitches. To start a new LEARN cycle when the adapter is reconnected, the host needs to set the EN_LEARN bit again.

If during a LEARN cycle the battery is removed, the nBATPRES input will go from low to high that terminates LEARN mode and within 100μs the ACFET/RBFET turns on quickly to avoid system crash. An ACFET/RBFET turn-on triggerd by nBATPRES is faster than turning on caused by battery depletion comparator.

Watchdog Timer

A watchdog timer is included in this device that can suspend operation (charging, Hybrid Power Boost mode or Battery-Only-Boost mode) if it is timed out and not reset by ChargeVoltage register or ChargeCurrent register write commands within a timer setting. The timer is adjustable in WDTMR_ADJ[1:0] to 155s (default), 78s, 5s or disabled. A change to these two bits also resets the watchdog timer.

After a watchdog timeout, the register values are not affected, but converter will suspend. The converter does not resume until watchdog is reset by a write to ChargeVoltage register or ChargeCurrent register or a change is made in the WDTMR_ADJ[1:0] bits.

Protections Functions

Adapter Input OCP (ACOC)

The input over-current (ACOC) can be set to 1.25 × I_{CRIT} or 2 × I_{CRIT} (selectable through ACOC_VTH bit). This function can be disabled through the EN_ACOC bit. If it is enabled and the input current exceeds the ACOC limit for more than 6ms (deglitch time) the ACFET/RBFET will latch off and cannot be turned on again unless the adapter is removed and reinserted such that ACDET voltage falls below V_{ACOK_FALL} (2.35V TYP) to completely reset the SGM41538. Note that the SGM41538 cannot keep the input current level at its regulated value if the charge current has been already reduced to 0 and system is the only adapter load.

Charging OCP (CHGOCP)

By monitoring the R_{SR} sense resistor voltage (V_{SRP} - V_{SRN}), cycle-by-cycle peak charge over-current protection is implemented to keep the charge current below OCP threshold. With R_{SR} = 10mΩ, the OCP threshold is set to 6A, 9A or 12A automatically based on the charge current setting in the ChargeCurrent register. This automatic setting prevents too low or too high OCP settings that can result in unwanted protection trigger or unsafe settings. If the I_{SR} peak current exceeds the OCP limit, the gate driver of the HS switch turns off for the rest of the cycle (until the beginning of the next cycle). Selected inductor must have sufficient saturation current such that peak current remains in the desired ripple range.

Battery Over-Voltage Protection (BATOVP)

If in charge mode, the sensed battery voltage (V_{SRN}) rises 4% or more above regulation set point (BATOVP event), both MOSFET switches will be kept off. If this situation lasts for more than 30ms, the charger will be disabled completely. This feature provides a quick response to over-voltage conditions, for example when the load or battery is removed. During BATOVP event an internal 15mA current sink is connected to SRP to discharge any stored energy in the output inductor and the output capacitors.

If a BATOVP is detected during Boost operation (Battery-Only-Boost or Hybrid Power Boost), the device continues the Boost mode.

Battery Short Protection

If the battery voltage (V_{SRN}) goes too low and drops below 2.5V (BATLOWV event), the converter will reset for 1ms and then if all required charge conditions are valid, charging will restart. With this feature, current overshoot is avoided that otherwise could cause inductor saturation and damage to the MOSFETs. During the BATLOWV condition, the charge current will be limited to 0.57A (with R_{SR} = 10mΩ). If BATLOWV continues, the LS MOSFET remains off and only turns on for short pulses to refresh bootstrap (BTST) capacitor.

DETAILED DESCRIPTION (continued)

Thermal Shutdown (TSHUT)

The device TQFN package provides very good junction to ambient thermal conduction to keep the device cool. To prevent damage to the device in case of overheating, if the junction temperature (T_J) exceeds 150℃ the device will turn off converter and shut down itself. It does not turn on again until T_J drops below 130℃, where the charge can resume with a soft-start. During TSHUT, the REGN LDO current limit is reduced to 24mA and the ACFET and RBFET remain on to power the system.

MOSFETs and Inductor Short-Circuit Protections

A special short-circuit protection method is used in SGM41538 by cycle-by-cycle current monitoring of the MOSFETs R_{DSON} voltage drops that are sensed after a short blanking time from the beginning of each cycle. If an inductor or MOSFET short is detected by an over-current comparator, a counter will be incremented (1 per each cycle). Each MOSFET has its own comparator and counter. If any counter reaches 7, the charger will latch off and ACFET/RBFET are turned off to disconnect the adapter. The BATFET will also turn on to connect the battery to the system. The counters will reset when the power stage exits latch-off and is enabled again. To reset latch-off status, pull the V_{VCC} below V_{VCC_UVLOZ} or the V_{ACDET} below V_{WAKEUP}. V_{DS} monitoring of the MOSFETs can be disabled independently. The low-side V_{DS} monitor has a 260mV over-current threshold and is enabled by IFAULT_LO bits. The high-side V_{DS} monitor threshold is 780mV and is enabled by IFAULT_HI bits. In Battery-Only-Boost mode, the low-side switch V_{DS} short-circuit threshold monitoring is only used for cycle-by-cycle current limiting and the latch-off does not happen.

Note that the cycle-by-cycle charge over-current protection circuit may detect the over-current firstly and turn off the switch before the short-circuit protection circuit can detect it. It can happen due to the short-circuit detection blank time that is considered to avoid influence of MOSFET transient noises during turn-on. Note that the MOSFET is forced to turn off by the over-current protection before the end of blanking time and in this condition, the device cannot detect short-circuit and the counters may not reach 7 to latch off. Therefore, the charger keeps switching with very small duty cycle for cycle-by-cycle current limiting. Even in this situation the charger and MOSFETs remain in their safe operation area due to very short on-time.

Due to the same reason (blanking times), during soft-start the short-circuit protection trigger may take much longer than 7 cycles.

Programming

SMBus Write-Word or Read-Word charger protocol commands are supported by SGM41538/SGM41538B. The charger can be identified by the 16-bit ManufacturerID and DeviceID registers located at 0FEh and 0FFh respectively. The ManufacturerID always returns 38h. The Device ID for the SGM41538 is 66h, and for the SGM41538B it is 68h. All registers of the SGM41538/SGM41538B are 16-bit which are divided into a high byte and a low byte.

SMBus Interface

The SGM41538 is a slave device with the 7-bit address of 09h (0000 1001b) and for the SGM41538B it is 49h (0100 1001b). As a slave device, it will not initiate a communication on the bus. A host is needed to control and program communications through the SMBus. A simplified subgroup of the System Management Bus Specification V1.1 commands (available from www.smbus.org) is supported for communication with the smart battery using read-word and write-word protocols.

Both data (SDA) and clock (SCL) pins use Schmitt-trigger inputs to allow slow pulse edges. Use 10kΩ pull-ups on both lines to provide the required SMBus rise/fall times. The master (usually the host) starts a communication by creating a START condition on the bus and terminates it by creating a STOP condition. Then the bus will be free for a new transaction. START condition is created by an SDA high-to-low transition while SCL is high, and a STOP condition is issued by an SDA low-to-high transition while SCL is high. See Figure 5 and Figure 6 for the timing diagrams of the SMBus interface signals. The address, command, and data bytes are all exchanged between the START and STOP conditions. During transactions, the SDA state only can change when the SCL is low, except for the START and STOP conditions. Data is transmitted bit by bit from MSB to LSB and one byte (8-bits) at a time. Data bits are sampled from SDA line at the rising edges of the SCL. A 9th acknowledge bit is also transmitted by receiver, so nine clock cycles are required for transferring each byte. The write-word and read-word command protocols are provided in Table 3 and Table 4.

DETAILED DESCRIPTION (continued)

SMBus Write-Word and Read-Word Protocols

Table 3. Write-Word Format

Bits	S/SR	Slave Addr	Write Bit	ACK	Cmnd. Byte	ACK	Low Data Byte	ACK	High Data Byte	ACK	STOP (P)
Creator	MTR	MTR	MTR	SLV	MTR	SLV	MTR	SLV	MTR	SLV	MTR
# of Bits		7	1	1	8	1	8	1	8	1	
Order		MSB LSB			MSB LSB		MSB LSB		MSB LSB		

Table 4. Read-Word Format

Bits	S/SR	Slave Addr	Write Bit	ACK	Cmnd. Byte	ACK	S/SR	Slave Addr	Read Bit	ACK	Low Data Byte	ACK	High Data Byte	NCK	STOP (P)
Creator	MTR	MTR	MTR	SLV	MTR	SLV	MTR	MTR	MTR	SLV	SLV	MTR	SLV	MTR	MTR
# of Bits		7	1	1	8	1		7	1	1	8	1	8	1	
Order		MSB LSB			MSB LSB			MSB LSB			MSB LSB		MSB LSB		

NOTES:
1. MTR: Master, SLV: Slave.
2. S = START condition, SR = Repeated START condition, P = STOP condition.
3. Write bit ($\overline{W}$) and ACK are logic low.
4. Read bit (R) and NCK (Not acknowledge) are logic high.

Timing Diagrams

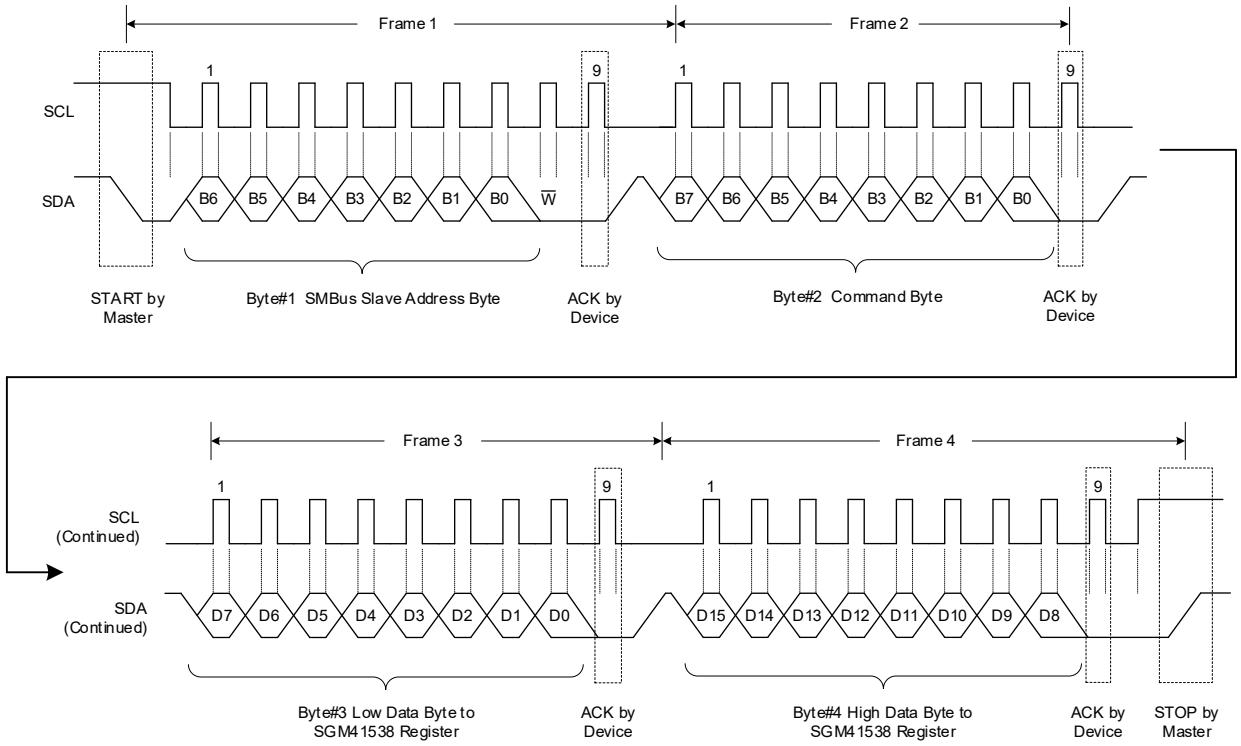


Figure 5. SMBus Write Timing

DETAILED DESCRIPTION (continued)

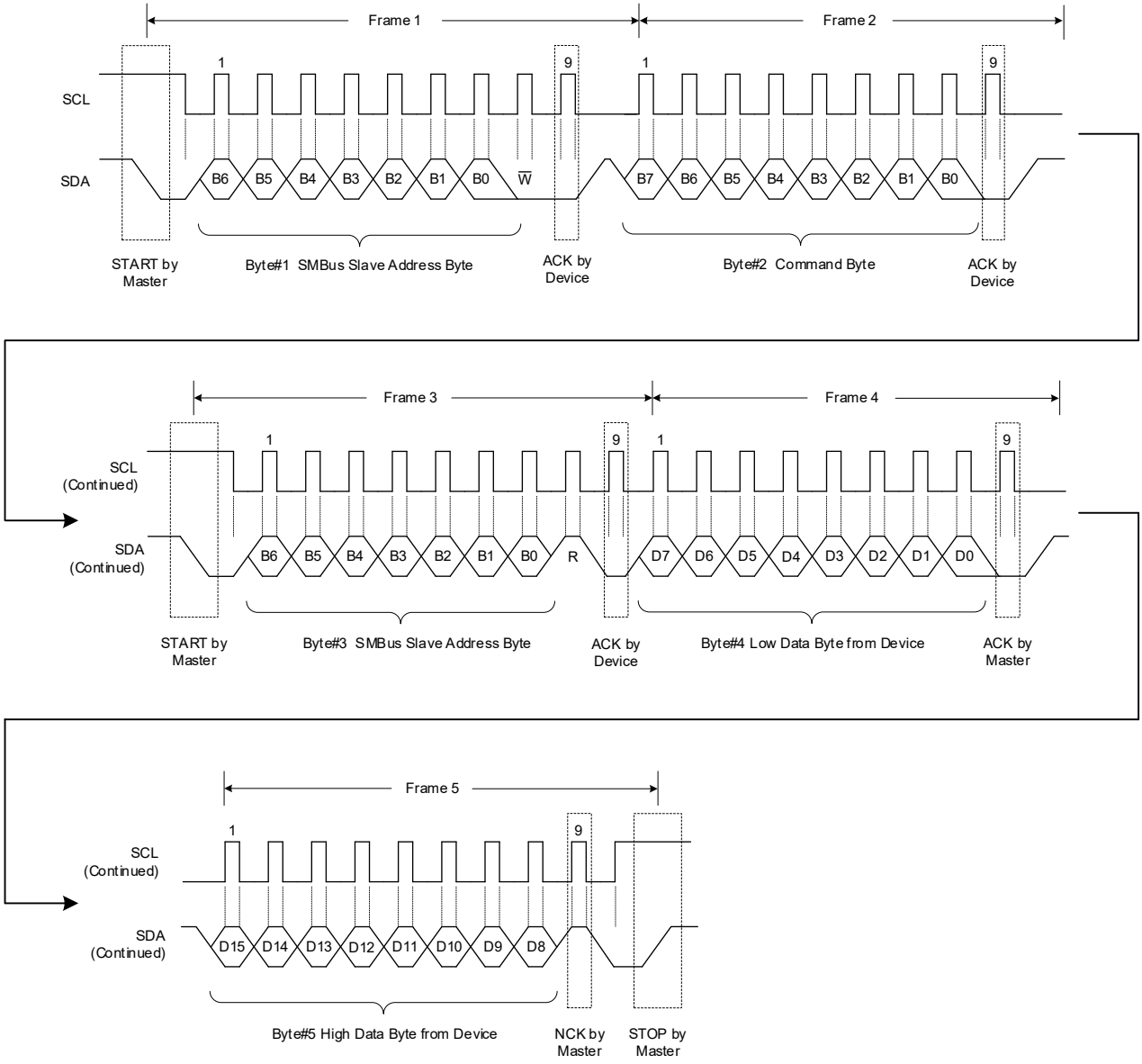


Figure 6. SMBus Read Timing

REGISTER MAPS

Table 5. SGM41538/SGM41538B Battery Charger Command Summary

16-Bit Register Address	Command Name	Description	POR State	Type	Links
12h	ChargeOption0 Register	Charge Options Control 0	E108h	Read/Write	Go
3Bh	ChargeOption1 Register	Charge Options Control 1	C220h	Read/Write	Go
38h	ChargeOption2 Register	Charge Options Control 2	0080h	Read/Write	Go
37h	ChargeOption3 Register	Charge Options Control 3	1240h or 1A40h	Read/Write	Go
3Ch	ProchotOption0 Register	nPROCHOT Options Control 0	4A54h	Read/Write	Go
3Dh	ProchotOption1 Register	nPROCHOT Options Control 1	8120h	Read/Write	Go
3Ah	ProchotStatus Register	nPROCHOT Status	0000h	Read Only	Go
14h	ChargeCurrent Register	7-Bit Charge Current Setting	0000h	Read/Write	Go
15h	ChargeVoltage Register	11-Bit Charge Voltage Setting	0000h	Read/Write	Go
39h	DisChargeCurrent Register	6-Bit Discharge Current Setting	1800h (6144mA)	Read/Write	Go
3Fh	InputCurrent Register	7-Bit Input Current Setting	1000h (4096mA)	Read/Write	Go
3Eh	VsysMin Register	7-Bit Minimum System Voltage Setting	2300h	Read/Write	Go
FEh	ManufacturerID Register	Manufacturer ID	0038h	Read Only	—
FFh	DeviceID Register	Device ID	0066h (for SGM41538) 0068h (for SGM41538B)	Read Only	—

SGM41538/SGM41538B Supported SMBus Commands

Table 5 summarizes the 12 battery-charger/smart battery commands that are supported by the SGM41538/41538B and can be use through write-word or read-word protocols. The other 2 listed commands, ManufacturerID register and DeviceID register, can be used to identify the device (reading REG0xFE and REG0xFF registers respectively). The ManufacturerID register command returns 0038h for both devices. The DeviceID register command returns 0066h for the SGM41538 and 0068h for the SGM41538B.

REGISTER MAPS (continued)

Bit Types:

R: Read only

R/W: Read/Write

n: Parameter code formed by the bits as an unsigned binary number.

REG0x12: ChargeOption0 Register [Reset = 0xE108]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	EN_LWPWR	1	R/W	Enable Low Power Mode 0 = Device is set to performance mode (in battery-only). The nPROCHOT, current/power monitor buffers, Battery-Only-Boost mode, and independent comparator can follow their respective register settings 1 = Device is set to the low power mode with battery-only. IC draws the lowest quiescent current. nPROCHOT, discharge current monitor buffer, power monitor buffer, Battery-Only-Boost mode and independent comparator are disabled (default)
D[14:13]	WDTMR_ADJ[1:0]	11	R/W	Watchdog Timer Setting Set the maximum time interval between two consecutive SMBus writes (to the charge voltage and/or charge current register) to reset the timer and avoid watchdog reset. If a write to REG0x14 or REG0x15 is not done within the watchdog interval, the converter will stop and Buck or Boost mode is disabled. Device will resume upon a write to these registers and the charge or Boost mode will resume if all the other conditions are valid. 00 = Disable watchdog timer 01 = 5 seconds 10 = 78 seconds 11 = 155 seconds (default)
D[12:10]	Reserved	000	R	Reserved.
D[9:8]	PWM_FREQ[1:0]	01	R/W	Set Converter Switching Frequency 00 = 600kHz 01 = 800kHz (default) 10 = 300kHz 11 = 400kHz
D[7:6]	Reserved	00	R	Reserved.
D[5]	EN_LEARN	0	R/W	Enable Battery LEARN Mode If enabled, the ACFET and RBFET are turned off and BATFET turns on. But if nBATPRES input goes high (battery removal), LEARN mode is terminated and this bit resets to 0. If the battery is depleted, LEARN mode cannot be enabled. 0 = Disable LEARN mode (default) 1 = Enable LEARN mode
D[4]	IADP_GAIN	0	R/W	IADP (Input Adapter Current Amplifier) Gain Setting This bit determines the ratio of the IADP pin voltage to the V_{ACP} - V_{ACN} differential voltage. 0 = ×20 (default) 1 = ×40
D[3]	IDCHG_GAIN	1	R/W	IDCHG (Discharge Current Amplifier) Gain Setting This bit determines the ratio of the IDCHG pin voltage to the V_{SRN} - V_{SRP} differential voltage. 0 = ×8 (if the discharge current regulation range is 0A to 32A range) 1 = ×16 (with discharge current regulation range 0A to 16A) (default)
D[2:1]	Reserved	00	R	Reserved.
D[0]	CHRG_INHIBIT	0	R/W	Charge Inhibit Battery charging is enabled if this bit is 0 (If REG0x14 and REG0x15 values are valid) 0 = Enable charge (default) 1 = Inhibit charge

REGISTER MAPS (continued)

REG0x3B: ChargeOption1 Register [Reset = 0xC220]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:14]	BAT_DEPL_VTH[1:0]	11	R/W	Battery Depletion (Over-Discharge) Detector Falling Threshold Setting If in LEARN or Boost modes battery voltage falls below this threshold, the LEARN or Boost mode will be terminated. It is given as percentage of the voltage regulation setting in REG0x15. 00 = 60% (~2.52V/cell) 01 = 65% (~2.73V/cell) 10 = 68% (~2.856V/cell) 11 = 72% (~3.024V/cell) (default)
D[13:12]	RSNS_RATIO[1:0]	00	R/W	Define the Ratio of the Selected R_{AC} and R_{SR} External Current Sense Resistors Used for PMON calculation for input (R_{AC}) and charge (R_{SR}) current sense resistors. 00 or 11 = R_{AC} = R_{SR} (default) 01 = R_{AC} = 2 × R_{SR} 10 = R_{AC} = 0.5 × R_{SR}
D[11]	EN_IDCHG	0	R/W	Enable IDCHG Pin Output Buffer 0 = Disable IDCHG output (to minimize I_Q) (default) 1 = Enable IDCHG output
D[10]	EN_PMON	0	R/W	Enable PMON Pin Output Buffer 0 = Disable PMON output (to minimize I_Q) (default) 1 = Enable PMON output
D[9]	PMON_RATIO	1	R/W	Set PMON (Power Monitoring) Gain Ratio of the PMON output current to the total input and battery power. 0 = 0.25μA/W (R_{AC} = R_{SR} = 10mΩ) or 0.5μA/W (R_{AC}/R_{SR} = 20mΩ/10mΩ, 10mΩ/20mΩ, 20/20mΩ) 1 = 1μA/W (R_{AC} = R_{SR} = 10mΩ) or 2μA/W (R_{AC}/R_{SR} = 20mΩ/10mΩ, 10mΩ/20mΩ, 20mΩ/20mΩ) (default)
D[8]	Reserved	0	R	Reserved.
D[7]	CMP_REF	0	R/W	Internal Reference Voltage for the Independent Comparator 0 = 2.3V (default) 1 = 1.2V
D[6]	CMP_POL	0	R/W	Set the Polarity of the Independent Comparator Output 0 = When CMPIN is above threshold, CMPOUT is low. Hysteresis is 100mV (default) 1 = When CMPIN is above threshold, CMPOUT is high. Hysteresis is set by the resistor placed between CMPIN and CMPOUT
D[5:4]	CMP_DEG[1:0]	10	R/W	Enable and Deglitch Time for the Independent Comparator Only applies to the falling edge of the CMPOUT (No rising deglitch). 00 = Independent comparator is disabled 01 = Enabled with 1μs output deglitch time 10 = Enabled with 2ms output deglitch time (default) 11 = Enabled with 5s output deglitch time
D[3]	EN_FET_LATCHOFF	0	R/W	Enable Power Path Latch-off If enabled, upon triggering of the independent comparator, the ACFET and RBFET will turn off. Latch off will be cleared by disabling this bit or a POR. This function is only available with 2ms and 5s deglitch times (CMP_DEG[1:0] =10 or 11). 0 = No latch off if independent comparator is triggered (default) 1 = Power path latches off if the independent comparator is triggered
D[2]	Reserved	0	R	Reserved.
D[1]	EN_SHIP_DCHG	0	R/W	Enable Shipping Mode Discharge 0 = Disable discharge mode (default) 1 = Enable discharge mode (Discharges SRN pin at least 20mA for 140ms)
D[0]	Reserved	0	R	Reserved.

REGISTER MAPS (continued)

REG0x38: ChargeOption2 Register [Reset = 0x0080]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:14]	PKPWR_TOVLD[1:0]	00	R/W	Set the Maximum Over-load Time (Increase Input Current Limit to I_{LIM2}) in Peak Power Mode 00 = 1ms (default) 01 = 2ms 10 = 5ms 11 = 10ms
D[13]	EN_PKPWR	0	R/W	Enable Peak Power Mode 0 = Disable peak power mode (default) 1 = Enable peak power mode
D[12:10]	Reserved	000	R	Reserved.
D[9:8]	PKPWR_TMAX[1:0]	00	R/W	Peak Power Mode Maximum Cycle Time (TMAX) (The relax time that input current limit is back to I_{LIM1} is TMAX – TOVLD). 00 = 20ms (default) 01 = 40ms 10 = 80ms 11 = 1300ms
D[7]	EN_EXTILIM	1	R/W	Enable External Current Limit Adjustment Enable the External ILIM pin setting to set the charge and discharge current limits. 0 = Limits are set by REG0x14 and REG0x39 registers only 1 = Limits are set by the lower of ILIM pin and REG0x14 and REG0x39 registers respectively (default)
D[6]	EN_BATT_BOOST	0	R/W	Enable Battery-Only-Boost Mode 0 = Disable Battery-Only-Boost mode (default) 1 = Enable Battery-Only-Boost mode
D[5]	VBOOST	0	R/W	Battery-Only-Boost Mode System Regulation Voltage (VsysMin_SET is set in REG0x3E) 0 = 1.6V + VsysMin_SET (default) 1 = 2.4V + VsysMin_SET
D[4:0]	Reserved	00000	R	Reserved.

REGISTER MAPS (continued)

REG0x37: ChargeOption3 Register [Reset = 0x1240 or 0x1A40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	EN_IDCHG_REG	0	R/W	Enable Current Regulation for Battery Discharge 0 = Disable current regulation in discharge (default) 1 = Enable discharge current regulation
D[14]	Reserved	0	R	Reserved.
D[13]	ACDRV_OFF	0	R/W	Disable ACDRV Output It can be used to turn off ACFET and RBFET, even if a good adapter is present. 0 = ACFET and RBFET are allowed to turn on based on "System Power Selection" (default) 1 = ACFET and RBFET are kept off
D[12]	ACOK_DEG	1	R/W	Set ACOK Rising Edge Deglitch Time for the Adapter Input After POR, when the adapter is inserted for the first time, the deglitch time is always 150ms regardless of this bit, but in the next insertions the deglitch time set by that: 0 = 150ms 1 = 1.2s (default)
D[11]	ACOK_STAT	x	R	Indicator Bit for Adapter Present Shows the presence of the input adapter (sets to 1 when V_{ACDET} > 2.4V). 0 = AC adapter is not present 1 = AC adapter is present
D[10]	EN_ACOC	0	R/W	Enable ACOC (Input OCP) Input current is monitored through V_{ACP}-V_{ACN} voltage for ACOC protection. If input current peak exceeds the ACOC threshold (adjustable to 1.25 or 2 times ICRIT setting), the ACFET/RBFET will latch off (with a 6ms allowance deglitch). 0 = Disable ACOC (default) 1 = Enable ACOC
D[9]	ACOC_VTH	1	R/W	ACOC Threshold Limit Setting 0 = 125% of I_{CRIT} 1 = 200% of I_{CRIT} (default)
D[8]	PKPWR_ENCHRG	0	R/W	Allow Battery Charging during t_{MAX} Peak Power Cycle 0 = Not Allowed. The adapter only supports system load (minimize chance of AC overload) (default) 1 = Allowed. The adapter current capability of I_{LIM1} and I_{LIM2} is fully utilized
D[7]	IFAULT_HI	0	R/W	Enable the High-side MOSFET V_{DS} Threshold for Short-Circuit Protection 0 = Protection disabled (default) 1 = Protection enabled and threshold is 780mV
D[6]	IFAULT_LO	1	R/W	Enable the Low-side MOSFET V_{DS} Threshold for Short-Circuit Protection It is also used as the cycle-by-cycle current limit protection threshold in Boost mode. 0 = Protection disabled 1 = Protection enabled and threshold is 260mV (default)
D[5]	FDPM_RISE	0	R/W	Input Current Threshold to Enter Hybrid Power Boost Mode or Peak Power Mode This bit sets the fast DPM comparator threshold to enter Hybrid Power Boost mode. (Minimum DPM current setting for Boost mode is 1536mA). It is set as percentage of the input current limit. If peak power mode is not enabled, the input current limit is I_{LIM1} (set in REG0x3F), else if the input current limit is I_{LIM2} and the HPB entry threshold is 107% of I_{LIM2} if the device is in t_{OVLD} of peak power mode cycle. In the rest of the peak power mode cycle, input current limit is I_{LIM1}. 0 = 107% (default) 1 = 104%
D[4:3]	FDPM_DEG[1:0]	00	R/W	Deglitch Time for the Fast DPM Set the response time from the moment that system current exceeds Fast DPM threshold until the start of battery discharging in Boost mode. 00 = 80μs (default) 01 = 150μs 10 or 11 = 25μs

REGISTER MAPS (continued)

REG0x37: ChargeOption3 Register [Reset = 0x1240 or 0x1A40] (continued)

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[2]	EN_HYBRID_BOOST	0	R/W	Enable Bit for Hybrid Power Boost Mode Reset to 0 by battery removal (a low to high on nBATPRES input) to disable Boost mode. 0 = Disable Hybrid Power Boost mode (default) 1 = Enable Hybrid Power Boost mode
D[1]	BOOST_STAT	0	R	Boost Mode Indicator Bit 0 = Device is not in Hybrid Power Boost or Battery-Only-Boost mode (default) 1 = Device is in Hybrid Power Boost or Battery-Only-Boost mode (note that the nBST_STAT is an active-low pin and with opposite state compared to this bit.)
D[0]	FDPM_FALL	0	R/W	Exit Threshold for the Hybrid Power Boost Mode Set the fast DPM comparator threshold to exit HPB mode as percentage of the input current limit setting (DPM current) in REG0x3F. 0 = 93% (default) 1 = 96%

REGISTER MAPS (continued)

REG0x3C: ProchotOption0 Register [Reset = 0x4A54]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	Reserved	0	R	Reserved.
[14:11]	ILIM2_VTH[3:0]	1001	R/W	I_{LIM2} Threshold Setting (as Percentage of I_{LIM1} in REG0x3F) Current is measured through the R_{AC} voltage (V_{ACP} - V_{ACN}). 0001 to 1000 = 110% ~ 145%, in 5% steps 1001 = 150% (default) 1010 = 160% 1011 = 170% 1100 = 180% 1101 = 200% 1110 = 220% 1111 = 250% (clamps to 230% if I_{DPM} ≥ 3.648A) Note: I_{CRIT} = 110% of I_{LIM2}.
D[10:9]	ICRIT_DEG[1:0]	01	R/W	ICRIT Deglitch Time Setting (Typical) 00 = 10μs 01 = 100μs (default) 10 = 400μs 11 = 800μs
D[8]	Reserved	0	R	Reserved.
D[7:6]	VSYS_VTH[1:0]	01	R/W	System Voltage Threshold Selection to Trigger nPROCHOT nPROCHOT triggers if SRN voltage falls below VSYS_VTH with 20μs deglitch time. It is recommended not to enable VSYS in nPROCHOT profile if REG0x15 is programmed below VSYS_VTH threshold. 00 = 5.75V 01 = 6.0V (default) 10 = 6.25V 11 = 6.5V
D[5]	EN_PROCHOT_EXT	0	R/W	Enable nPROCHOT Pulse Extension If enabled, nPROCHOT pin remains in low voltage until host writes a 0 on the PROCHOT_CLEAR bit (in 0x3C[2]). 0 = Disable pulse extension (default) 1 = Enable pulse extension
D[4:3]	PROCHOT_WIDTH[1:0]	10	R/W	nPROCHOT Pulse Width Setting Minimum nPROCHOT pulse width when pulse extension is disabled (REG0x3C[5] = 0) 00 = 100μs 01 = 1ms 10 = 10ms (default) 11 = 5ms
D[2]	PROCHOT_CLEAR	1	R/W	nPROCHOT Pulse Clear Clear nPROCHOT pulse when pulse extension is enabled (0x3C[5] = 1). 0 = Clear nPROCHOT pulse and set nPROCHOT pin to high 1 = No effect (default)
D[1]	INOM_DEG	0	R/W	INOM Trigger Deglitch Time Maximum INOM deglitch time. 0 = 1ms (MAX) (default) 1 = 15ms (MAX)
D[0]	INOM_VTH	0	R/W	INOM Threshold INOM event occurs If the average input current exceeds INOM_VTH. INOM threshold is given as percentage of the Input Current Limit (IDPM) in REG0x3F. 0 = 110% (default) 1 = 106%

REGISTER MAPS (continued)

REG0x3D: ProchotOption1 Register [Reset = 0x8120]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:10]	IDCHG_VTH[5:0]	100000	R/W	IDCHG Threshold Setting (6-Bit Value) Discharge current is measured through the V_{SRN} -V_{SRP} differential voltage across R_{SR}. An IDCHG PROCHOT event is triggered if the discharge current exceeds IDCHG_VTH. Range: 0A to 32256mA Steps: 512mA Discharge Threshold = n × 512mA (n = 0 to 63). (Default: n = 100000b or 16384mA).
D[9:8]	IDCHG_DEG[1:0]	01	R/W	IDCHG Typical Deglitch Time 00 = 1.6ms 01= 100μs (default) 10 = 6ms 11 = 12ms
D[7]	Reserved	0	R	Reserved.
D[6:0]	PROCHOT_PROFILE[6:0]	0100000	R/W	Enable Functions in the nPROCHOT Profile (7 Bits) Adapter removal automatically disables ICRIT, INOM, nBATPRES and ACOK functions in the nPROCHOT profile but comparator, IDCHG, and VSYS function settings are not affected. If adapter is present, the nPROCHOT function is enabled by the following bits. (The nPROCHOT function is disabled when all bits are 0.) Bit 6: Independent comparator 0 = Disable (default) 1 = Enable Bit 5: ICRIT 0 = Disable 1 = Enable (default) Bit 4: INOM 0 = Disable (default) 1 = Enable Bit 3: IDCHG 0 = Disable (default) 1 = Enable Bit 2: VSYS 0 = Disable (default) 1 = Enable Bit 1: nBATPRES 0 = Disable (default) 1 = Enable (one-shot triggered on rising edge) Bit 0: ACOK 0 = Disable (default) 1 = Enable (one-shot triggered on falling edge)

REGISTER MAPS (continued)

REG0x3A: ProchotStatus Register [Reset = 0x0000]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:8]	Reserved	00000000	R	Reserved.
D[7]	Reserved	0	R/W	Reserved and writing “1” is not recommended.
D[6:0]	PROCHOT_STAT[6:0]	0000000	R	nPROCHOT Events Status (7 Bits) The status bits of all nPROCHOT events that are triggered during the same nPROCHOT pulse are set to 1. This register resets to 0 if one of the following occurs. 1. After the first host read from this register (after nPROCHOT pin goes high) 2. When nPROCHOT goes low to start another pulse Bit 6: Independent Comparator Bit 5: ICRIT Bit 4: INOM Bit 3: IDCHG Bit 2: VSYS Bit 1: nBATPRES Bit 0: ACOK For Each Bit: 0 = Not occurred 1 = Occurred

REGISTER MAPS (continued)

REG0x14: ChargeCurrent Register [Reset = 0x0000]

The charge current (CC phase) can be set in the 128mA to 8.128A range in 64mA steps when a 10mΩ sense resistor is used by writing a 7-bit value in the 16-bit REG0x14 register (ChargeCurrent register command) with the format given in Table 6. Writing 0 or 64mA to this register terminates the current charge cycle. After a power-on reset (POR), the charge current will reset to 0A. If due to V_{ACDET} < 2.35V the adapter is not working properly (resulting in ACOK going low), the ChargeCurrent register will reset to 0A. As an additional protection level, user can set the maximum charge current by setting the ILIM pin voltage. The actual charge current limit will be the lower setting between ChargeCurrent register and the ILIM pin setting. This feature can be disabled by pulling ILIM above 2V externally (2V is the maximum charge current regulation limit). If ILIM voltage is pulled below 76mV, charging will be disabled.

Use Equation 4 to set the ILIM pin charge current limit:

$$I_{CHG} = \frac{V_{ILIM}}{20 \times R_{SR}} \quad (4)$$

The SRP and SRN pins are used to measure the voltage drop across the charge current sense resistor (R_{SR}). The default R_{SR} value is 10mΩ, however, other values may also be used that will scale the currents in Table 6 by the 10mΩ/R_{SR} ratio. For example, the (1000h) code used for 4096mA charge current with 10mΩ will result in 2048mA current if a 20mΩ sense resistor is used. Generally, a larger resistor provides better measurement accuracy and regulation but increases the conduction losses. The current ripple peaks may also trigger over-current with a large R_{SR}. To reduce ripple and avoid unwanted over-current trigger, a larger inductance or higher frequency setting is needed. It is recommended to choose an R_{SR} not higher than 20mΩ.

Table 6. Charge Current Register with R_{SR} = 10mΩ Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15:13]	Reserved	000	R/W	Reserved and writing “1” is not recommended.
D[12]	Charge Current, DACICHG 6	0	R/W	0 = Add 0mA of charger current 1 = Add 4096mA of charger current
D[11]	Charge Current, DACICHG 5	0	R/W	0 = Add 0mA of charger current 1 = Add 2048mA of charger current
D[10]	Charge Current, DACICHG 4	0	R/W	0 = Add 0mA of charger current 1 = Add 1024mA of charger current
D[9]	Charge Current, DACICHG 3	0	R/W	0 = Add 0mA of charger current 1 = Add 512mA of charger current
D[8]	Charge Current, DACICHG 2	0	R/W	0 = Add 0mA of charger current 1 = Add 256mA of charger current
D[7]	Charge Current, DACICHG 1	0	R/W	0 = Add 0mA of charger current 1 = Add 128mA of charger current
D[6]	Charge Current, DACICHG 0	0	R/W	0 = Add 0mA of charger current 1 = Add 64mA of charger current
D[5:0]	Reserved	000000	R/W	Reserved and writing “1” is not recommended.

REGISTER MAPS (continued)

REG0x15: ChargeVoltage Register [Reset = 0x0000]

The charge regulation voltage (CV phase) can be set within the 1.024V to 19.200V range in 16mV steps by writing an 11-bit value in the 16-bit register (ChargeVoltage register command) using the format given in Table 7. After POR, the charge voltage setting is 0 and the converter is off. Writing 0 to the ChargeVoltage register disables battery charging, Hybrid Power Boost or Battery-Only-Boost modes.

The SRN pin senses the battery voltage for regulation. This pin must be decoupled (0.1μF recommended) as close as possible to the device and connected close to the battery.

Table 7. Charge Voltage Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	Reserved	0	R/W	Reserved and writing “1” is not recommended.
D[14]	Charge Voltage, DACV 10	0	R/W	0 = Add 0mV of charger voltage 1 = Add 16384mV of charger voltage
D[13]	Charge Voltage, DACV 9	0	R/W	0 = Add 0mV of charger voltage 1 = Add 8192mV of charger voltage
D[12]	Charge Voltage, DACV 8	0	R/W	0 = Add 0mV of charger voltage 1 = Add 4096mV of charger voltage
D[11]	Charge Voltage, DACV 7	0	R/W	0 = Add 0mV of charger voltage 1 = Add 2048mV of charger voltage
D[10]	Charge Voltage, DACV 6	0	R/W	0 = Add 0mV of charger voltage 1 = Add 1024mV of charger voltage
D[9]	Charge Voltage, DACV 5	0	R/W	0 = Add 0mV of charger voltage 1 = Add 512mV of charger voltage
D[8]	Charge Voltage, DACV 4	0	R/W	0 = Add 0mV of charger voltage 1 = Add 256mV of charger voltage
D[7]	Charge Voltage, DACV 3	0	R/W	0 = Add 0mV of charger voltage 1 = Add 128mV of charger voltage
D[6]	Charge Voltage, DACV 2	0	R/W	0 = Add 0mV of charger voltage 1 = Add 64mV of charger voltage
D[5]	Charge Voltage, DACV 1	0	R/W	0 = Add 0mV of charger voltage 1 = Add 32mV of charger voltage
D[4]	Charge Voltage, DACV 0	0	R/W	0 = Add 0mV of charger voltage 1 = Add 16mV of charger voltage
D[3:0]	Reserved	0000	R/W	Reserved and writing “1” is not recommended.

REGISTER MAPS (continued)

REG0x3F: InputCurrent Register [Reset = 0x1000]

To keep the adapter cost, weight and size small, its power rating cannot be unlimited. Adapter is usually not designed to provide the maximum system power and charge current at the same time. System power has large fluctuations depending on the power requirements of the CPU and other subsystems and may vary from near zero (in sleep mode) to a maximum. Therefore, to optimize adapter rating, Dynamic Power Mode (DPM) is used in which the charge current is continuously adjusted based on the available adapter current and the system load. The battery current may even be reversed (discharged) during system high power peaks (typically short term) to support adapter such that they both provide power to the system (battery assists the adapter). With DPM, the AC adapter current (primary input current) is limited and regulated close to its maximum rating for maximum utilization of the adapter. This is the current that in the normal system condition is available to power the system load and for charging the battery at the same time. Normally, the total input current, is equal to the sum of the system and charge currents (plus charger IC current, I_{BIAS}). When this sum tends to exceed the input current limit, the device reduces the charge current to give priority to the system load. If the system current demand continues to increase, the charge current is reduced linearly to 0. If the system demand increases even further, the charger enters Hybrid Power Boost (HPB) mode and discharges battery to assist the adapter for powering the heavy system load. During HPB mode, the input current remains in regulation. The regulated input current value (I_{DPM}) is set in the InputCurrent register.

During DPM regulation, the total input current is the sum of the device supply current I_{BIAS}, the charger input current, and the system load current I_{LOAD}, that can be estimated from Equation 5:

$$I_{INPUT} = I_{LOAD} + \left(\frac{I_{BAT} \times V_{BAT}}{V_{IN} \times \eta} \right) + I_{BIAS} \quad (5)$$

where η is the converter efficiency and I_{BAT} is the battery current (I_{BAT} > 0 for charging, I_{BAT} < 0 for discharging). The converter operates in Buck mode when charging and in Boost mode (HPB) when discharging.

The input current limit (I_{DPM}) can be set within the 64mA to 8.128A range in 64mA steps by writing a 7-bit value in the 16-bit register (InputCurrent register command) using the format given in Table 8 (If R_{AC} = 10mΩ is used). After POR, the input current limit is set to default (4096mA with R_{AC} = 10mΩ). Writing 0 or a value above 8.128A is considered invalid and will be ignored.

Other R_{AC} resistor values can be used, however, the actual current will be scaled by 10mΩ/R_{AC} ratio. For example, the (1000h) code for setting the input current setting to 4096mA with a 10mΩ results in 2048mA current if R_{AC} = 20mΩ is used. A larger resistor provides better measurement accuracy and regulation but increases the conduction loss.

Table 8. InputCurrent Register Details, Using R_{AC} = 10mΩ Sense Resistor

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	EN_HIZ	0	R/W	0 = The converter can switch if other conditions met (default) 1 = The converter can't switch except for Battery-Only-Boost Mode. This bit can reduce the quiescent current of input by about 500μA. Such as this condition: default mode, no battery, V_{IN} = 20V (satisfy V_{ACDET} > V_{ACOK} and V_{VCC} > V_{VCC_UVLO}), the input current is about 1.5mA if EN_HIZ = 0, and reduce to about 1mA if EN_HIZ = 1.
D[14:13]	Reserved	00	R/W	Reserved and writing "1" is not recommended.
D[12]	Input Current, DACIIN 6	1	R/W	0 = Add 0mA of input current 1 = Add 4096mA of input current
D[11]	Input Current, DACIIN 5	0	R/W	0 = Add 0mA of input current 1 = Add 2048mA of input current
D[10]	Input Current, DACIIN 4	0	R/W	0 = Add 0mA of input current 1 = Add 1024mA of input current
D[9]	Input Current, DACIIN 3	0	R/W	0 = Add 0mA of input current 1 = Add 512mA of input current
D[8]	Input Current, DACIIN 2	0	R/W	0 = Add 0mA of input current 1 = Add 256mA of input current
D[7]	Input Current, DACIIN 1	0	R/W	0 = Add 0mA of input current 1 = Add 128mA of input current
D[6]	Input Current, DACIIN 0	0	R/W	0 = Add 0mA of input current 1 = Add 64mA of input current
D[5:0]	Reserved	000000	R/W	Reserved and writing "1" is not recommended.

REGISTER MAPS (continued)

REG0x39: DisChargeCurrent Register [Reset = 0x1800]

The battery discharge current limit can be set within the 0.512A to 32.256A range in 512mA steps by writing a 6-bit value to the 16-bit register (DisChargeCurrent register command) using the format given in Table 9 (with R_{SR} = 10mΩ). After POR, the discharge current limit is set to the default which is 6144mA (with R_{SR} = 10mΩ).

To provide a higher level of protection during battery discharge, the ILIM pin can be used for hardware programming of the maximum discharge current. Typically, the user should set this limit below (but not far from) the battery pack over-current protection (OCP) threshold for maximum battery discharge capacity. Refer to the battery specification for OCP information. Actual discharge current limit is the lower of the hardware limit (set by the ILIM pin voltage) and the software limit (set by DisChargeCurrent register). To disable the discharge hardware limit, ILIM pin can be pulled above 1.6V, which corresponds to the maximum adjustable discharge current regulation limit. When ILIM voltage is below 76mV, battery discharge is disabled. To set the discharge current limit with ILIM pin, Equation 6 can be used.

$$I_{DCHG} = \frac{V_{ILIM}}{5 \times R_{SR}} \quad (6)$$

R_{SR} default value is 10mΩ, however, other values may also be used. The actual current is scaled by the ratio of 10mΩ and R_{SR}. For example, the discharge current setting used for 4096mA with a 10mΩ resistor will result in 2048mA limit with a 20mΩ resistor. A larger sense resistor provides higher regulation accuracy but at the expense of higher conduction loss. If current sensing resistor value is too high, it may trigger an over-current protection threshold because the peak of the current ripple results in a voltage that is too high. In such a case, either a higher inductance value or a lower current sensing resistor value should be used to limit the current ripple voltage level. A current sensing resistor value no more than 20mΩ is recommended.

In battery Boost mode, the battery is the only power source in the system and limiting the battery discharge current can cause a system voltage drop when the load demand is higher than the discharge limit. In this mode, the battery discharge current is higher than system current. It is not uncommon that the battery current is twice as big as the system current with heavy load, therefore, the discharge limit should be set to the largest current that the battery and switching components can support. It should be considered for protection against fatal currents such as a short-circuit. It should not be set below 9A, because in some system conditions, the discharge current cannot be regulated if it is set below 9A during Boost mode.

Table 9. DisChargeCurrent Register with R_{SR} = 10mΩ Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	Reserved	0	R/W	Reserved and writing “1” is not recommended.
D[14]	Discharge Current, DACIIN 5	0	R/W	0 = Add 0mA of input current 1 = Add 16384mA of discharge current
D[13]	Discharge Current, DACIIN 4	0	R/W	0 = Add 0mA of input current 1 = Add 8192mA of discharge current
D[12]	Discharge Current, DACIIN 3	1	R/W	0 = Add 0mA of input current 1 = Add 4096mA of discharge current
D[11]	Discharge Current, DACIIN 2	1	R/W	0 = Add 0mA of input current 1 = Add 2048mA of discharge current
D[10]	Discharge Current, DACIIN 1	0	R/W	0 = Add 0mA of input current 1 = Add 1024mA of discharge current
D[9]	Discharge Current, DACIIN 0	0	R/W	0 = Add 0mA of input current 1 = Add 512mA of discharge current
D[8:0]	Reserved	000000000	R/W	Reserved and writing “1” is not recommended.

REGISTER MAPS (continued)

REG0x3E: VsysMin Register (Setting the Minimum System Voltage during Battery-Only- Boost Mode) [Reset = 0x2300]

The Battery-Only-Boost mode minimum system voltage can be set between 5.632V (1600h) to 13.568V (3500h) in 128mV steps at VsysMin_SET = 0, by writing a 7-bit value in the 16-bit register (VsysMin register command) using the format given in Table 10 and 16V at VsysMin_SET = 1. After POR, the Battery-Only-Boost mode minimum system voltage is set to default (8.96V, 2300h).

Note that the Battery-Only-Boost mode regulation voltage is set separately by VBOOST bit to 1.6V + VsysMin_SET (if VBOOST = 0, default) or 2.4V + VsysMin_SET (if VBOOST = 1).

The system voltage is sensed through the ACN pin voltage for regulation. Place a decoupling capacitor (0.1μF recommended) on this pin as close as possible to the device to remove high frequency noise.

Table 10. Minimum System Voltage (VsysMin) Register Details

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[15]	Reserved	0	R/W	Reserved and writing “1” is not recommended.
D[14]	VsysMin_SET	0	R/W	0 = VsysMin[13:7] (default) 1 = 16V The Battery-Only-Boost mode regulation voltage is set separately by VBOOST + VsysMin_SET.
D[13]	Minimum System Voltage, DACVS6	1	R/W	0 = Add 0mV of charger voltage 1 = Add 8192mV of charger voltage
D[12]	Minimum System Voltage, DACVS5	0	R/W	0 = Add 0mV of charger voltage 1 = Add 4096mV of charger voltage
D[11]	Minimum System Voltage, DACVS4	0	R/W	0 = Add 0mV of charger voltage 1 = Add 2048mV of charger voltage
D[10]	Minimum System Voltage, DACVS3	0	R/W	0 = Add 0mV of charger voltage 1 = Add 1024mV of charger voltage
D[9]	Minimum System Voltage, DACVS2	1	R/W	0 = Add 0mV of charger voltage 1 = Add 512mV of charger voltage
D[8]	Minimum System Voltage, DACVS1	1	R/W	0 = Add 0mV of charger voltage 1 = Add 256mV of charger voltage
D[7]	Minimum System Voltage, DACVS0	0	R/W	0 = Add 0mV of charger voltage 1 = Add 128mV of charger voltage
D[6:5]	REGN_SET	00	R/W	The REGN voltage is set to 5V, 5.5V or 6V. 00 = 6V (default) 01 or 10 = 5V 11 = 5.5V
D[4:0]	Reserved	00000	R/W	Reserved and writing “1” is not recommended.

REGISTER MAPS (continued)

Registers Affected by Other Events

Certain events, such as adapter or battery removal, result in a change in some register values, such as resetting some fields to their POR value. Table 11 lists those especial events and their affected bit fields.

Table 11. Event Affected Registers and Bit Fields (Exceptions)

Affected Register Field	Affecting Event / Affected Field Name	Adapter Removal (ACDET < 2.4V)	Battery Removal (nBATPRES = High)	Batdepl	EN_PKPWR = 1	Writing Out of Range (Undervalue)	Writing Out of Range (Overvalue)
0x12[5]	EN_LEARN	Get POR Value (Write Ignored)					
0x38[6]	EN_BATT_BOOST			Get POR Value if Boost is Active			
0x37[2]	EN_HYBRID_BOOST		Get POR Value				
0x38[15:14]	PKPWR_TOVLD[1:0]				Write Ignored		
0x38[9:8]	PKPWR_TMAX[1:0]				Write Ignored		
0x14	ICHG	Get POR Value	Get POR Value			64mA is treated as 0mA	Write Ignored
0x15	VCHG		Get POR Value			Write Ignored	
0x39	IDCHG						
0x3E	VsysMin						
0x3F	IDPM						

APPLICATION INFORMATION

Typical Applications

In this section, two typical applications of the SGM41538 are provided. Figure 7 (S→System+) shows a battery charging system with Battery-Only-Boost mode support and in Figure 7 (S→Battery+) shows the schematic of a battery charging system without Battery-Only-Boost mode support. Refer to the details provided in this document to understand the Battery-Only-Boost mode operation.

In applications with Battery-Only-Boost function, VCC must be able to get power from either the adapter or the system rail by a diode selector (S→System+ in Figure 7). Note that VCC is powered from the system rail and not directly from the battery in such applications. The reason is that in Battery-Only-Boost mode with heavy system load, the battery voltage (sensed at SRN) may drop below the minimum requirement due to the high battery current, resulting in an insufficient voltage for the switching converter operation. But the higher system rail voltage is sufficient for converter operation in such conditions. Note also that during the initial power-up, the battery voltage reaches D2 after a forward voltage drop across the Q3 body diode. The drop across D2 (Schottky) is small, however, for a partially charged single-cell (1-cell) Li-Ion battery, the additional voltage drop across the Q3 body diode may result in a VCC voltage below UVLO. Therefore, using Battery-Only-Boost feature it is not recommended for systems with 1-cell battery.

If the system does not need the Battery-Only-Boost mode feature, the requirements are a little bit relaxed compared to the previous case and the schematic shown in Figure 7 (S→Battery+) can be used. The VCC power source selector (D1 and D2) is now connected to adapter and battery, and it is suitable for 1-cell applications. The required system bus capacitance (C_{SYS}) is also lower.

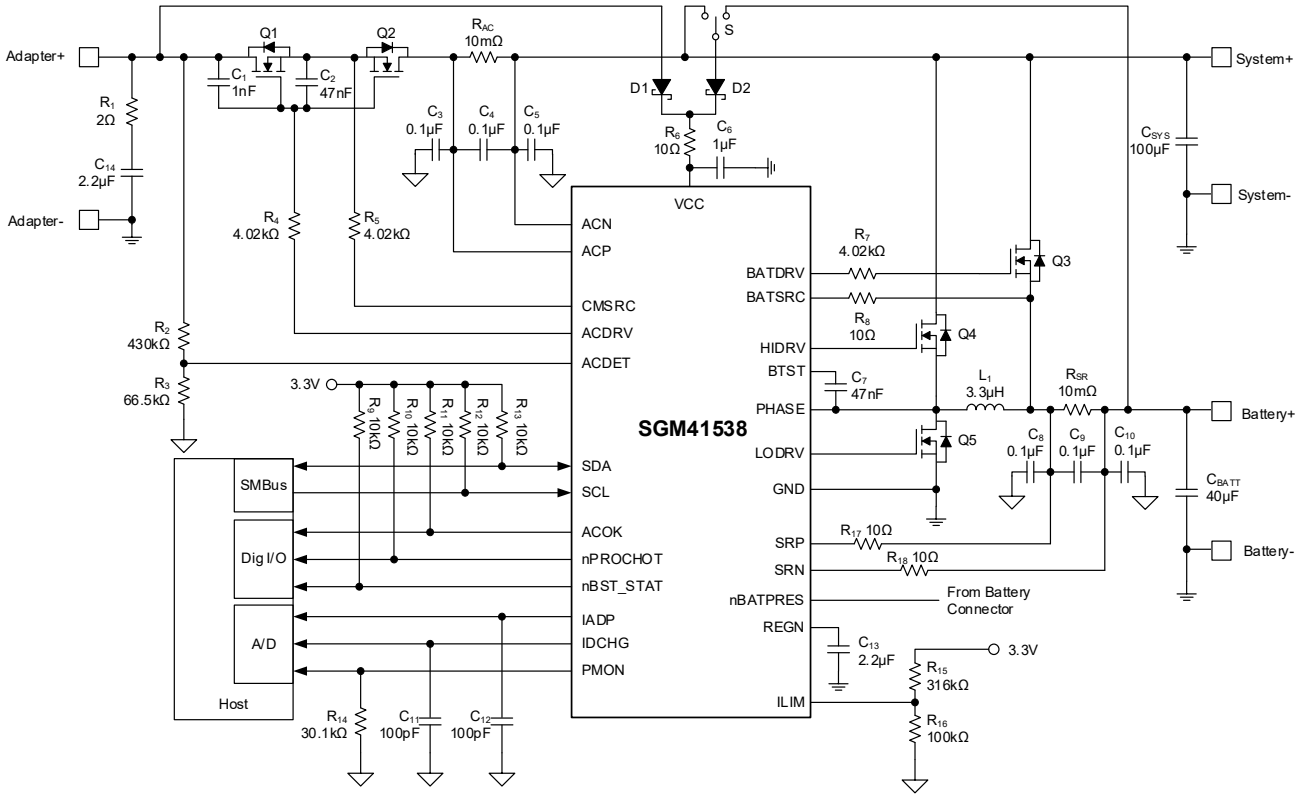


Figure 7. Typical SGM41538 Battery Charging Application

APPLICATION INFORMATION (continued)

Design Requirements

Table 12 lists the parameters that must be determined before designing the charger, with some example values.

Table 12. Design Requirements

Design Parameter	Desired Value (Example)
Input Voltage (1)	17.7V < Adapter Voltage < 24V
Input Current Limit (1)	3.2A (65W adapter)
Battery Charge Voltage (2)	12592mV (3-cell battery)
Battery Charge Current (2)	4096mA (3-cell battery)
Battery Discharge Current (2)	6144mA (3-cell battery)

NOTES:
1. Refer to adapter specification to find the input voltage range and input current limit requirements.
2. Refer to battery specification to find the charge voltage, charge current and discharge current recommended levels.

Design Procedure

Figure 7 shows the simplified application circuits with the minimum required capacitances on each pin. In this section, design and selection of the main external components including inductor, capacitors and MOSFETs along with additional protection circuits along with minimum loss considerations will be discussed.

Protecting the Device against Negative Output Voltage (Reverse Battery Connection)

If by accident or a production failure the battery pack is inserted with reverse polarity or if a short occurs on the battery connections, negative voltages can appear on the SRP, SRN, and BATSRC pins. The device internal electrostatic-discharge (ESD) protection diodes (from GND pin to SRP or SRN pins) and the two internal anti-parallel (AP) diodes that are placed between SRP and SRN pins, will be forward biased by such negative voltage that can cause high negative current through those diodes. Placing small series resistors (10Ω) between SRP, SRN pin and R_{SR} sense terminals respectively can limit these currents and save the device.

Protecting Against Negative Input Voltage (Reverse Adapter Connection)

Applying a reverse voltage to the input can damage the device and system permanently. Figure 8 provides a solution for protection against reverse input polarity using a small N-MOSFET (Q6) and two resistors (R_{12} and R_{13}). When adapter is connected correctly, Q6 remains off due to the negative gate-source voltage (V_{GS}). If the adapter is connected in reverse polarity, the V_{GS} will be positive and Q6 turns on and shorts Q1/Q2 (ACFET/RBFET) gate and source together and keeps it off. The body diode of Q2 blocks the negative voltage from reaching to the device and the system. However, the device CMSRC and ACDRV pins need current limiting resistors (R_3 and R_4) to limit their ESD diode currents caused by the negative voltage. A low V_{GS} threshold MOSFET should be selected for Q6 with low Q_{GS} gate charge for quick turn-on (before Q2) upon negative voltage connection. The R_3 and R_4 resistances must be small enough for quick response of ACFET/RBFET (to avoid slow turn-on/turn-off). R_3 and R_4 power rating must be large enough to dissipate losses at maximum adapter voltage without overheating.

Battery Quiescent Current Reduction

When adapter is disconnected and VCC is powered from the battery (through a direct or indirect path resulting in V_{VCC} > V_{VCC_UVLOZ}), the internal BATFET charge pump will constantly run to drive the BATFET by keeping BATDRV voltage at 6V above V_{SRN}. The additional quiescent current caused by the charge pump is not necessary because BATFET does not need to be turned on at light load or shutdown state and its body diode can conduct the small system current without significant loss. To extend the system run time with battery, BATFET needs to be turned on only at high current to reduce the loss and voltage drop across its source and drain (channel conduction rather than body diode conduction). Therefore, host can turn off the battery pack switches to disconnect the battery from the system when the system is in shutdown. Some battery packs may awake again if the SRN voltage remains above the battery UVLO for a long time (like in shipping mode). By setting EN_SHIP_DCHG bit in ChargeOption1 register to 1, a current source is enabled inside the device to discharge the SRN quickly and pull the VCC voltage (and system rail voltage) low. With the V_{SYS} discharged to zero and V_{VCC} < V_{VCC_UVLOZ}, the quiescent current will be minimized.

APPLICATION INFORMATION (continued)

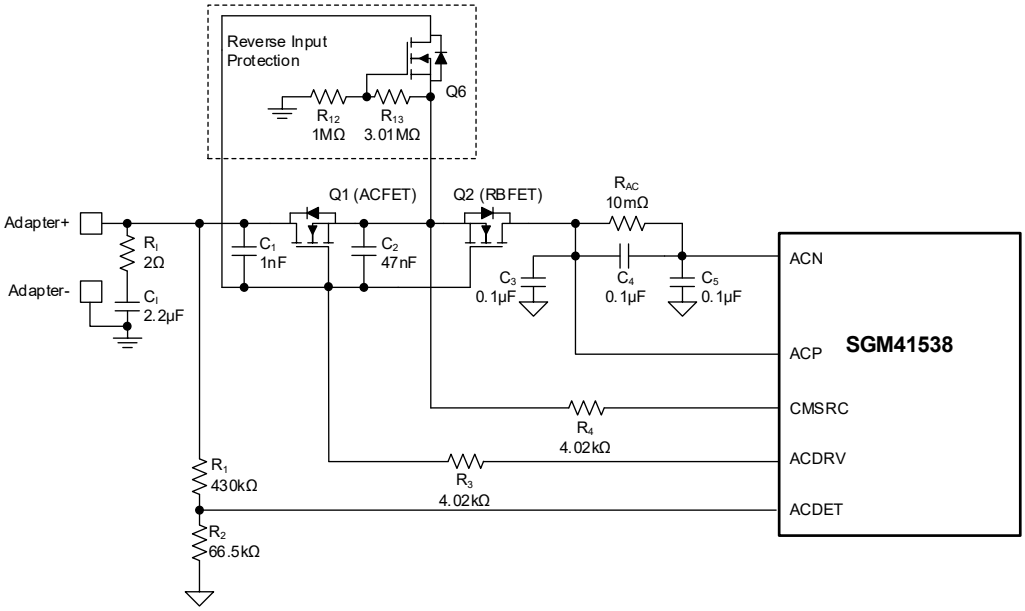


Figure 8. Additional Circuit (Q6, R_{12}, R_{13}) for Reverse Input Voltage Protection

Inductor (L) Design

Several parameters need to be considered to design the inductor. Higher switching frequency reduces the required inductance and capacitances. The SGM41538 provides 4 fixed frequency choices. The inductor saturation current must be higher than the highest peak current that is the sum of charging current (I_{CHG}) and half of the peak to peak ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + \frac{1}{2} \times I_{RIPPLE} \quad (7)$$

The inductor ripple is determined by the input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), frequency (f_S) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{f_S \times L} \quad (8)$$

To design the inductor from Equation 8 and for a reasonable tradeoff between size and efficiency, the inductor current ripple is usually considered in the range of 20% to 40% of the maximum charge current.

The maximum ripple current happens at around 50% duty cycle (D = 0.5). For example, for a 3-cell pack the charge voltage varies from 9V to 12.6V and if a 20V adapter is used, the ripple is maximum when the battery voltage is around 10V. For a 4-cell battery, the voltage varies from 12V to 16.8V and 12V will generate the highest inductor current ripple with a 20V adapter.

Cycle-by-cycle charge under-current protection (UCP) is provided by monitoring the current sensing resistor (R_{SR}). The typical UCP falling edge threshold is 5mV (that is 0.5A with R_{SR} = 10mΩ). If the average charge current falls below 125mA, the LS switch turns off and remains off until BTST capacitor needs a new refresh. LS body diode freewheels the inductor current in off-time.

Input Capacitor (C_{IN}) Selection

C_{IN} must be able to circulate all input current ripple and high frequency switching currents and keep them away from the input line and adapter. When the converter is providing I_{CHG} charge current the resulting RMS ripple current in the input can be estimated from Equation 9. The worst case occurs around D = 50%. If the converter operates in a range away from 50% duty cycle, the worst case will be at the duty cycle which is closest to 50%:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (9)$$

It is recommended to use low ESR ceramic capacitor like X7R or X5R for input decoupling. These capacitors must be placed close to the drain of the HS MOSFET and source of the LS MOSFET. DC bias voltage derating must be considered for the ceramic capacitors. For a 19V to 20V adapter, at least a 25V capacitor is needed. For a typical 3A to 4A charge current, a 10μF to 20μF ceramic capacitance is recommended for C_{IN}.

DC-bias effect can lead to significant capacitance drop, especially at higher input voltages and for small capacitor package sizes. It is recommended to refer to the capacitor datasheet to evaluate the DC bias performance. It may be needed to select a higher voltage and higher value capacitor to get the required capacitance at the operating voltage.

APPLICATION INFORMATION (continued)

Output Capacitor (C_{OUT}) Selection

C_{OUT} must also be able to carry the inductor ripple current and store enough energy for stable operation against system load transients. The output capacitor RMS current can be estimated from Equation 10:

$$I_{COUT} = \frac{I_{RIPPLE}}{2\times\sqrt{3}} \approx 0.29\times I_{RIPPLE} \quad (10)$$

The SGM41538 uses an internal compensator. For good loop stability, the output LC filter resonant frequency should be set between 10kHz to 20kHz. A 25V, X7R or X5R ceramic capacitor is recommended for the output capacitor. For a typical 3A to 4A charger, a 10μF to 20μF capacitance should be sufficient. C_{OUT} must be placed after R_{SR} resistor for the best accuracy in the charge current regulation.

MOSFET Selection

The converter needs two N type MOSFETs for synchronous switching. The internal gate drivers provide 5V gate drive voltage. Choose at least 30V MOSFETs for 19V to 20V input voltage rating.

Switching MOSFETs are usually selected based on a figure-of-merit (FOM) to tradeoff between the conduction and switching losses. For the high-side MOSFET, it is defined as the product of on-resistance (R_{DSON}) and the gate-to-drain charge (Q_{GD}). For the low-side MOSFET, it is defined as the product of the on-resistance (R_{DSON}) and the total gate charge, Q_G.

$$FOM_{HS} = R_{DS(ON)}\times Q_{GD};\quad FOM_{LS} = R_{DS(ON)}\times Q_G \quad (11)$$

A MOSFET with lower FOM value generates lower total loss. Lower R_{DSON} usually costs more with the same package size.

The HS MOSFET loss can be estimated form Equation 12 in which t_{ON} is the turn-on time and turn-off time is represented by t_{OFF}:

$$P_{HS} = D\times I_{CHG}{}^2\times R_{DS(ON)} + \frac{1}{2}\times V_{IN}\times I_{CHG}\times(t_{ON}+t_{OFF})\times f_S \quad (12)$$

Conduction and switching losses are represented by the first and second terms respectively. Note that R_{DSON} typically increases by 50% with 100°C rise in junction temperature. The MOSFET turn-on and turn-off times can be estimated by Equation 13:

$$t_{ON} = \frac{Q_{SW}}{I_{ON}};\quad t_{OFF} = \frac{Q_{SW}}{I_{OFF}} \quad (13)$$

where I_{ON} and I_{OFF} are the turn-on and turn-off gate driving currents and Q_{SW} is the switching charge. If Q_{SW} is not given in datasheet, Equation 14 can be used to estimate it based on the gate-drain charge (Q_{GD}) and gate-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + 0.5\times Q_{GS} \quad (14)$$

Gate driving currents can also be estimated from REGN voltage (V_{REGN}), plateau voltage of the MOSFET (V_{PLT}), and the total gate driver turn-on and turn-off gate resistances (R_{ON} and R_{OFF}):

$$I_{ON} = \frac{V_{REGN}-V_{PLT}}{R_{ON}};\quad I_{OFF} = \frac{V_{PLT}}{R_{OFF}} \quad (15)$$

The LS MOSFET conduction loss is given by Equation 16 when operating in continuous synchronous conduction mode:

$$P_{LS} = (1-D)\times I_{CHG}{}^2\times R_{DS(ON)} \quad (16)$$

When the charger operates in non-synchronous mode, the LS MOSFET is off, and the inductor current freewheels through its body-diode. The body diode power loss is given by Equation 17 in which V_F represents its forward voltage drop and $I_{NONSYNC}$ represents the non-synchronous mode charging current (maximum 0.25A with R_{SR} = 10mΩ, or 0.5A if V_{BAT} < 2.5V):

$$P_D = V_F\times I_{NONSYNC}\times(1-D) \quad (17)$$

P_D is maximum at the lowest duty cycle (when V_{BAT} is minimum). It is recommended to choose a MOSFET with an internal Schottky diode or one with sufficient body diode rating to carry the maximum non-synchronous charge current.

Input Filter

An input filter is necessary to prevent damage to the device due to the voltage spikes cause by the adapter hot plug-in. These spikes are generated by resonance of the cable parasitic inductance and the input capacitor. This filter should be properly designed and tested to avoid over-voltage damage.

Various technics can be used for damping or limiting the voltage spikes during adapter hot plug, such that the peak is adequately less than the VCC maximum voltage rating. One simple method is using a large electrolytic capacitor at the input. The high ESR of this kind of capacitors can damp the resonance and reduce the spike peak significantly. Another common method is using high current TVS Zener diodes for clamping the spikes to a safe level. These methods may need too much space and can be costly.

APPLICATION INFORMATION (continued)

A more cost-effective and compact solution is presented in Figure 9. R_1 and C_1 form an RC network to damp the resonance and limit the spike to a safe level. D_1 is added to protect VCC from reverse voltage caused by oscillations. C_2 is placed as close as possible to VCC for decoupling and must be smaller than C_1 such that R_1 is the dominant component of the circuit equivalent ESR to get sufficient damping. R_2 limits the D_1 inrush current and saves D_1 during adapter hot plug-in. $R_2 \times C_2$ time constant should be around 10μs to limit the dV/dt of the VCC pin and the hot plug inrush current (R_1 carries the high inrush current). R_1 package size must be large enough (with minimal parasitic inductance) to tolerate the inrush current power loss (check the resistor data sheet). This filter must be tested in the real application for verification and any required adjustment after completing the design.

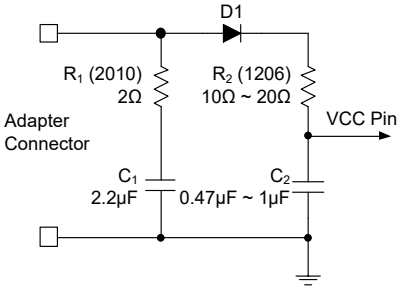


Figure 9. Input Filter Design

Power Supply

When a good adapter is plugged in and detected by the ACDET input, the device ACOK output goes high and the ACFET/RBFET are turned on to connect the adapter to the system. Adapted voltage is detected by the ACDET through an external resistor divider. The detection threshold must normally be programmed such that a good adapter is detected when its voltage is above the maximum battery voltage and below the maximum allowed input/system voltage (ACOV).

When the adapter is disconnected, BATFET connects the system to the battery. The battery depletion threshold is typically higher than the minimum system voltage such that the battery capacity can be fully utilized for maximum run time.

Layout

PCB layout is an important part of the charger design. A weak layout can result in poor performance, resistive losses, EMI issues and instability problems. The following guidelines are helpful for designing a good layout.

1. To reduce the switching losses, try to minimize the switching rise and fall times. By selecting component with right sizes, and proper placement and routing, the high frequency current path (loop) can be minimized as explained in Figure 10. At the same time, the switching node and connected conductors must have minimal areas to minimize radiation and electrical and magnetic coupling to the nearby traces and elements. For a proper PCB layout, follow the next guidelines in the specified priority order.

2. Place input ceramic capacitor as close as possible to switching MOSFET's (HS drain and LS source) with the shortest copper connections. MOSFETS and capacitor must be on the same layer of the PCB (Do not use vias for these connections).

3. Place the IC close to the switching MOSFET's gate pins to minimize the gate drive path. The IC can be placed on the other side of the PCB.

4. Place one inductor terminal close to the MOSFETS switching node with a short and wide trace and minimum copper area to minimize radiation. Do not use multiple layer parallel traces for this connection. Try to minimize parasitic capacitance coupling from the switching node to any other trace, plane, or component.

5. Place the R_{SR} (charging current sensing resistor) right next to the inductor other terminal (output pin) and route its sense leads with Kelvin connections, as shown in Figure 11, to the IC on the same layer. Keep the sense traces close to each other to minimize loop area and do not route them through or shared with a high-current path. Place a decoupling capacitor on the sense traces next to the IC.

6. Place output capacitor close to the R_{SR} output pin. Place its GND pin close to the LS switch and C_{IN} ground retunes.

7. Input and output capacitor ground connections must be tied together and connected to the same copper area before connection to the system ground.

8. Connect and tie charger power ground and analog ground only in a single point. Pour an analog ground plane under the device but keep it away from power pins to minimize inductive and capacitive noise coupling.

9. Always route analog and power grounds separately. Connect analog and power grounds only at one point either using the IC power pad or with a tiny 0Ω jumper resistor (in the latter case, tie the power pad to the analog ground if possible).

APPLICATION INFORMATION (continued)

10. Place any decoupling capacitor close to the respective IC pin and IC GND with the shortest trace lengths.

11. Soldering the IC exposed power pad to the PCB ground is necessary. Consider enough thermal vias under the IC, to connect it to other ground planes for better heat conduction and improved thermal performance.

12. Consider enough vias with proper sizes based on the maximum current in the path.

PCB Layout Consideration for Short-Circuit Protection

Figure 12 shows the block diagram of the SGM41538 special short-circuit protection scheme. The R_{DSON} voltage drop of the MOSFETs is monitored after a certain blanking time from the beginning of each cycle through the COMP1 and COMP2 comparators. If a MOSFET or inductor short occurs, the corresponding comparator will increment its counter. The charger will latch off if a counter reaches to 7 short-circuit detections and will not be released unless the adapter is removed and re-inserted.

Normally the LS MOSFET current flows from source to drain resulting in a negative voltage V_{DS} drop and the over-current comparator cannot be triggered. But if a short occurs across the HS MOSFET or the inductor, a large current will flow from the drain to the source of the LS MOSFET that can be detected by the COMP2 comparator. The LS switch voltage drop is sensed between the PHASE and GND pins.

A short on the HS MOSFET is detected by the voltage drop between the ACP and PHASE pins by COMP1. Therefore, it monitors the total drop on the HS MOSFET, R_{AC} (adapter sense resistor) and PCB traces from ACN pin of the R_{AC} to the HS MOSFET drain pin. There is usually a relatively long path from the R_{AC} sense resistor to the converter positive supply (HS MOSFET drain) and its effect must be minimized by a proper PCB layout. To avoid unwanted shutdowns by false short-circuit detection, good layout and careful R_{DSON} selection for MOSFETs are critical. In a bad layout, the system current is drawn at a point after the charger input point. In such case all drops cause by system current are included in COMP1 over-current sensing. An improved layout with the above mentioned considerations is provided in Figure 13 in which the system and charger input current paths are not separated after ACN, and the PCB voltage drop caused by the system current is coupled to the voltage sensed by COMP1.

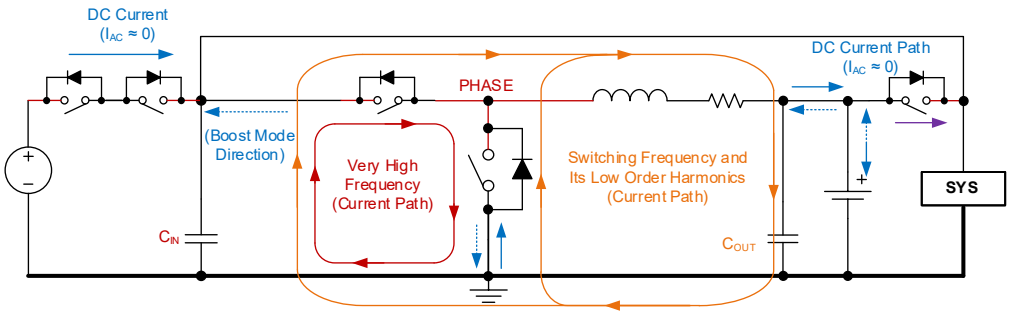


Figure 10. The High Frequency Switching Current Loop

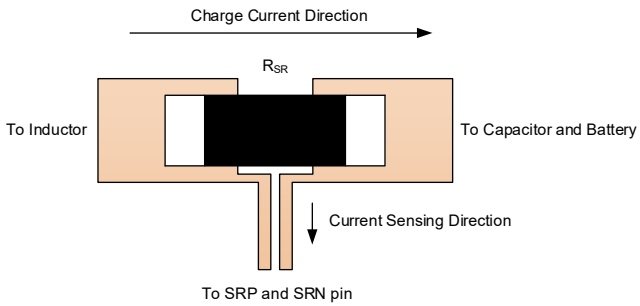


Figure 11. Kelvin Connection Layout for Improved Measurement Accuracy with Current Sensing Resistors

APPLICATION INFORMATION (continued)

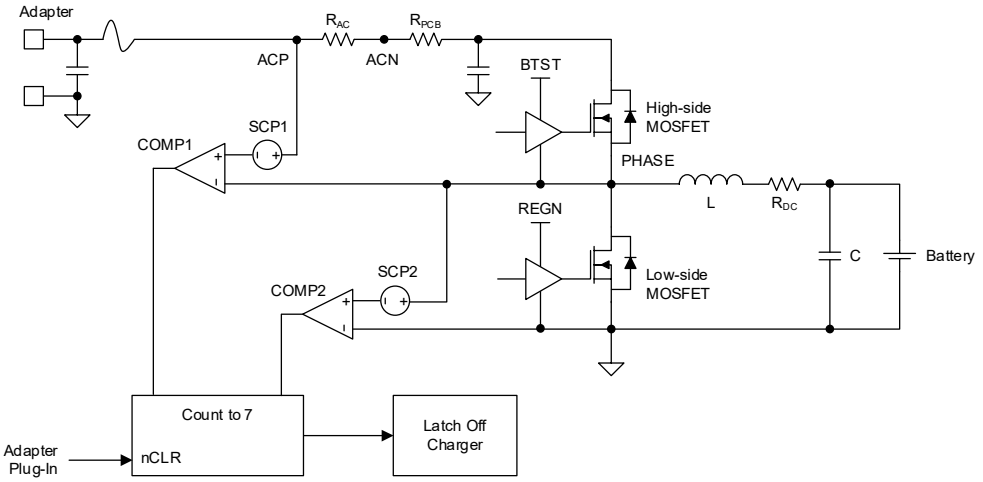


Figure 12. SGM41538 Short-Circuit Protection Scheme

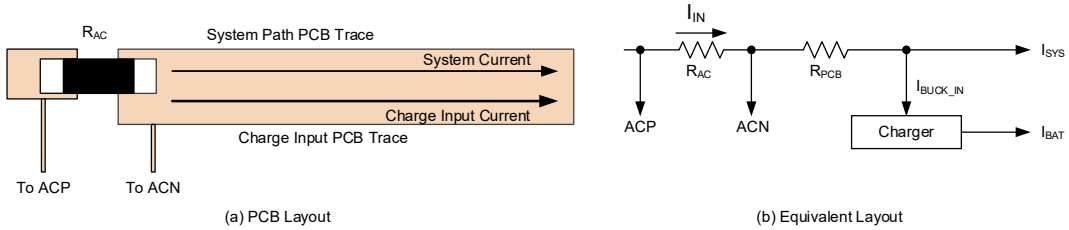


Figure 13. PCB Layout Example to Minimize False Short-Circuit Detection

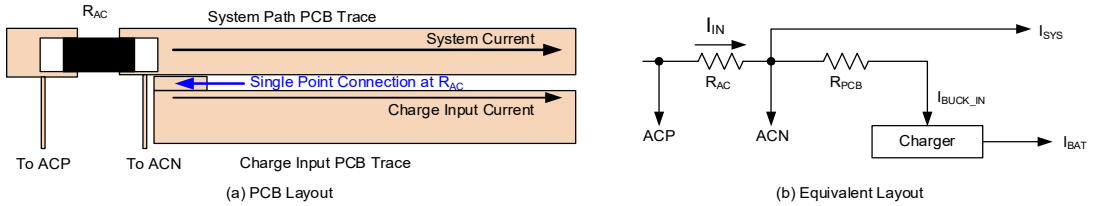


Figure 14. Optimized PCB Layout Example to Minimize False Short-Circuit Detection

The same concept with an optimized PCB layout is provided in Figure 14. The system and charger input current paths are separated and only the charger input current PCB drops sensed by COMP1 will minimize the risk of charger shutdown due to false charger short-circuit detection. It also simplifies the layout design for applications with high system current.

Equation 18 provides the total sensed voltage drop by the short-circuit comparator in Figure 14:

$$V_{HS} = R_{AC} \times I_{IN} + R_{PCB} \times \left(I_{BUCK\_IN} + k \times \left(I_{IN} - I_{BUCK\_IN}\right)\right) + R_{DS(ON)} \times I_{PEAK} \quad (18)$$

R_{AC} is the input sense resistance (adapter current sense), I_{IN} is the input current, R_{PCB} is the PCB parasitic resistance between R_{AC} and the converter, I_{BUCK_IN} is the charger input current, R_{DSON} is the HS MOSFET on-resistance and I_{PEAK} is the peak inductor current. The k represents a PCB factor that varies from k = 0 for the well decoupled layout (Figure 14) in which the PCB traces for system and charge currents are completely separated, to k = 1 for the fully coupled layout (Figure 13) in which one trace carries both currents (whole I_{DMP} current). The total voltage drop (V_{HS}) must remain below the HS short-circuit comparator threshold to avoid false triggering of the short-circuit shutdown.

The LS comparator threshold can be disabled or set to 250mV by programming the IFAULT_LO bit in the ChargeOption3 register to 0 or 1 respectively. The HS short-circuit threshold can be disabled or set to 750mV by programming the IFAULT_HI bit in the same register to 0 or 1 respectively.

Proper short-circuit detection thresholds should be programmed by the host when the PCB layout is known, to avoid false protection triggers.

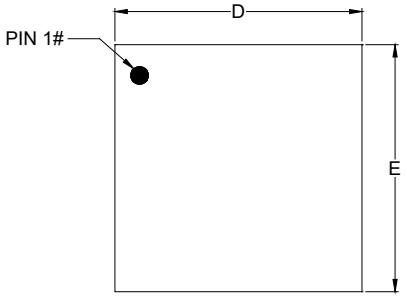
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

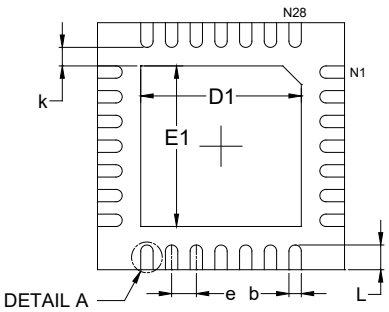
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

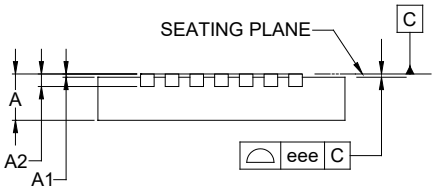
TQFN-4×4-28BL



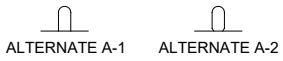
TOP VIEW



BOTTOM VIEW

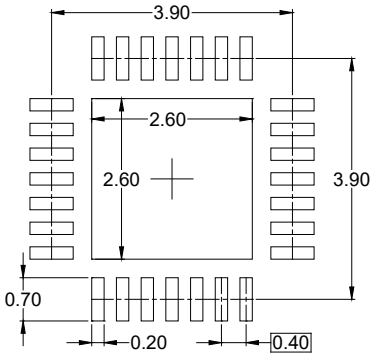


SIDE VIEW



DETAIL A

ALTERNATE TERMINAL CONSTRUCTION



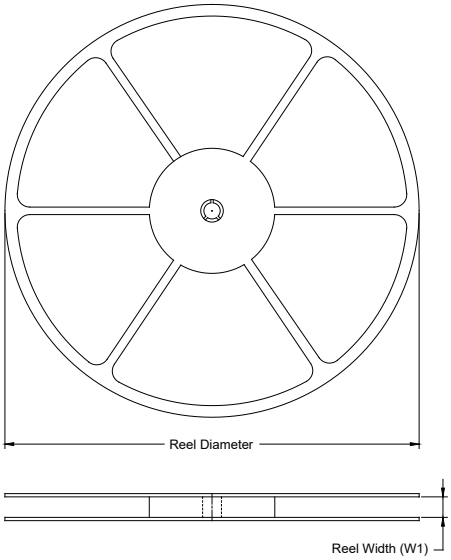
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.150	-	0.250
D	3.900	-	4.100
E	3.900	-	4.100
D1	2.500	-	2.700
E1	2.500	-	2.700
e		0.400 BSC	
k		0.300 REF	
L	0.300	-	0.500
eee		0.080	

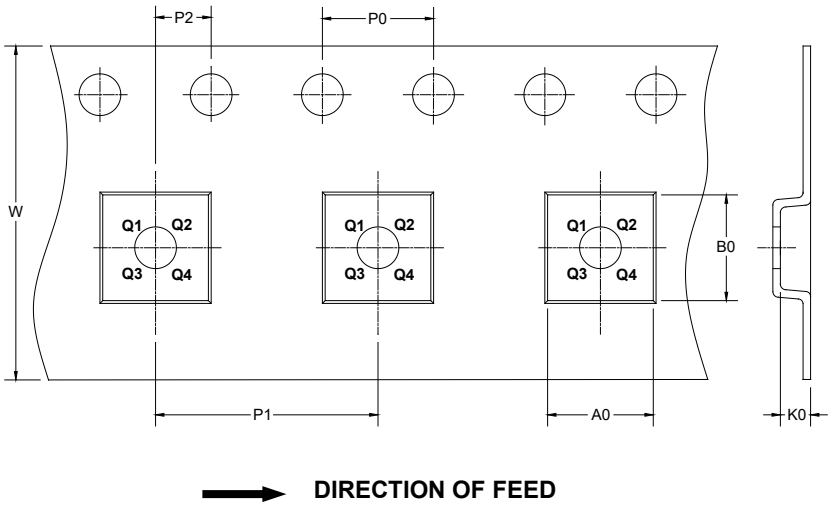
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



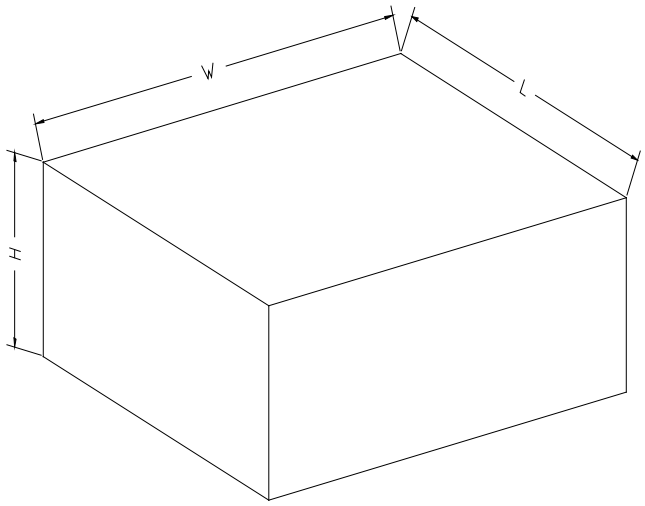
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-4×4-28BL	13"	12.4	4.30	4.30	1.10	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002