SGM41600T
I²C Controlled Single Cell 8A Switched Cap Charger with Bypass Mode

GENERAL DESCRIPTION

The SGM41600T is an efficient 8A switched-capacitor battery charging device with I²C control that can operate either in charge-pump voltage divider mode or in bypass mode. It can charge single-cell Li-Ion or Li-polymer battery in a wide 3.6V to 11.5V input voltage range (VBUS) from smart wall adapters or power banks. The switched-capacitor architecture is optimized for 50% duty cycle to cut the input current to one-half of the battery current and reduce the wiring drops, losses and temperature rise in the application.

A two-channel switched-capacitor topology is used to reduce the required input capacitors, improve efficiency and minimize the output ripple. Necessary protection features for safe charging performance including input over-voltage protection by external OVPFET (Q_{OVP}) and input reverse blocking (using an internal NFET) are provided.

The SGM41600T is available in a Green WLCSP-2.95×2.95-36B package and can operate in the -40℃ to +85℃ ambient temperature range.

FEATURES

- **Efficiency Optimized Switched-Capacitor Architecture**
  - **Up to 8A Output Current**
  - **3.6V to 11.5V Input Voltage Range**
  - **300kHz to 1.5MHz Switching Frequency Setting**
  - **Above 96.6% Voltage Divider Mode Efficiency (when V_{BAT} = 4V, I_{BAT} = 6A, C_{FLY} = 3 × 22μF per Phase)**
- **Comprehensive Integrated Protection Features**
  - **External OVP Control and Regulation**
  - **Input Over-Voltage Protection (VBUS_OVP)**
  - **Input Short-Circuit Protection (VBUS_SC)**
  - **Input Over-Current Protection (IBUS_OCP)**
  - **Input Under-Current Protection (IBUS_UCP)**
  - **Battery Over-Voltage Protection (VBAT_OVP)**
  - **Output Short-Circuit Protection (VOUT_SC)**
  - **IBAT Over-Current Protection (IBAT_OCP)**
  - **C_{FLY} Short-Circuit Protection (CFLY_SC)**
  - **Switch Peak Over-Current Protection (PEAK_OCP)**
  - **Die Over-Temperature Protection (TDIE_OTP)**
- **6-Channel 12-Bit (Effective) ADC Converter**
  - **VBUS, IBUS, VBAT, IBAT, VOUT, TDIE for Monitoring**

APPLICATIONS

Smart Phone, Tablet PC

TYPICAL APPLICATION

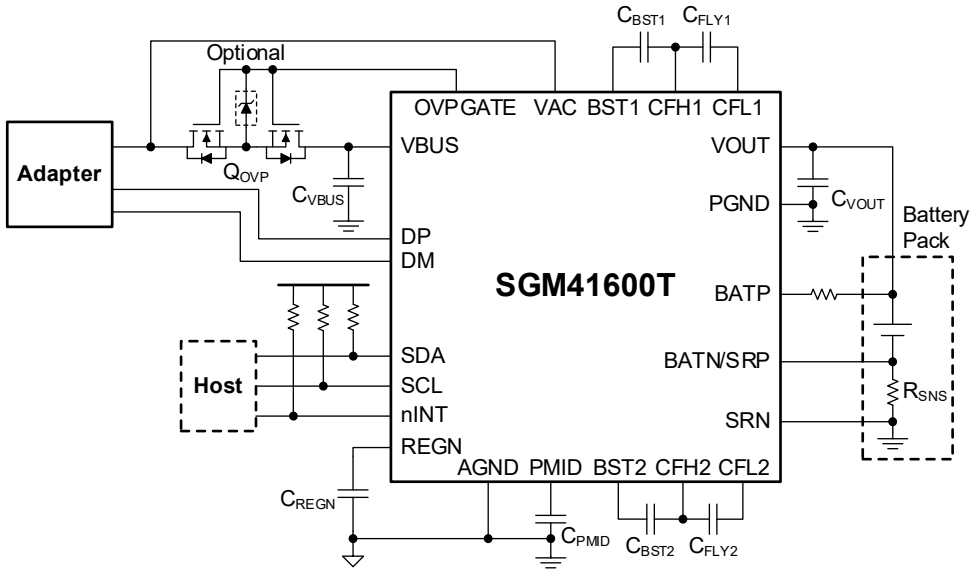


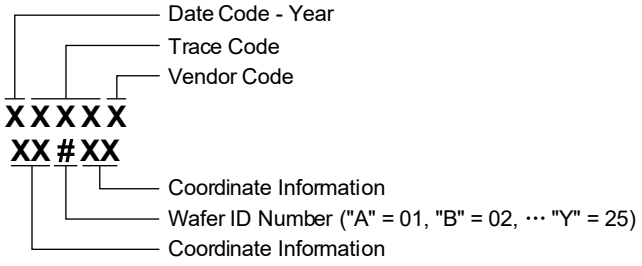
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41600T	WLCSP-2.95×2.95-36B	-40℃ to +85℃	SGM41600TYG/TR	07K XXXXX XX#XX	Tape and Reel, 1500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VAC (Converter Not Switching) ..... -0.3V to 38V
OVPGATE to VBUS ..... -22V to 6V
VBUS, PMID (Converter Not Switching) ..... -0.3V to 22V
BST1, BST2 ..... -0.3V to V_{PMID} + 5.5V
VOUT ..... -0.3V to 6V
CFH1, CFH2 to VOUT ..... -0.3V to 6V
CFL1, CFL2 ..... -0.3V to 6V
DP, DM, REGN, BATP, SDA, SCL, nINT ..... -0.3V to 6V
BATN/SRP, SRN ..... -0.3V to 1.8V
SRP to SRN ..... -0.5V to 0.5V
Package Thermal Resistance
WLCSP-2.95×2.95-36B, θ_{JA} ..... 33℃/W
WLCSP-2.95×2.95-36B, θ_{JB} ..... 4.3℃/W
WLCSP-2.95×2.95-36B, θ_{JC} ..... 12.4℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

RECOMMENDED OPERATING CONDITIONS

VAC ..... 3.5V to 18V
(OVPGATE - VBUS) ..... 4.5V to 5.1V
VBUS (Bypass Mode) ..... 3.6V to 5.5V
VBUS (Voltage Divider Mode) ..... 5.5V to 11.5V
VOUT, BATP ..... 3V to 5.5V
I_{VOUT} (Bypass Mode) ..... 0A to 5A
I_{VOUT} (Voltage Divider Mode) ..... 0A to 8A
PMID - VOUT (Voltage Divider Mode) ..... 0V to 5.5V
(CFH1 - VOUT), CFL1 ..... 0V to 5.5V
(CFH2 - VOUT), CFL2 ..... 0V to 5.5V
BATN/SRP, SRN ..... 0V to 1.5V
(SRP - SRN) ..... -0.05V to 0.05V
SDA, SCL, nINT ..... 0V to 5V
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

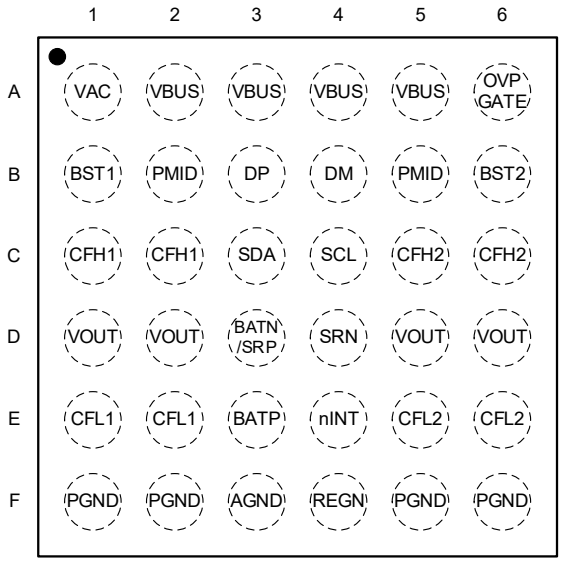
Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-2.95×2.95-36B

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
A1	VAC	AI	Adapter DC Voltage Sense Input Pin. Connect it to the drain of the external OVPFET (Q_{OVP}).
A2, A3, A4, A5	VBUS	P	Device Power Input Pins. Use a 10μF or larger ceramic capacitor between VBUS and PGND pins close to the device.
A6	OVPGATE	AO	External N-FET Gate Control Pin. Connect to the gate of the external OVPFET (Q_{OVP}). (Note: The REG_RST bit does not affect the output of OVPGATE.)
B1	BST1	P	Channel-1 Bootstrap Pin. It is the BST pin to supply Q_{CH1} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CFH1 pin.
B2, B5	PMID	P	Power Stage Supply Input Pins. Bypass them with at least two 4.7μF ceramic capacitors to PGND.
B3	DP	AIO	USB Communication Interface Positive Line. Connect to the USB D+ data line.
B4	DM	AIO	USB Communication Interface Negative Line. Connect to the USB D- data line.
B6	BST2	P	Channel-2 Bootstrap Pin. It is the BST pin to supply Q_{CH2} gate driver. Use a 0.1μF or larger MLCC capacitor from this pin to CFH2 pin.
C1, C2	CFH1	P	Channel-1 Flying Capacitor Positive Pins. Connect two 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close as possible to the device.
C3	SDA	DIO	I^2C Interface Data Line. The SDA line is forced to release when the 25ms I^2C timeout fault occurs.
C4	SCL	DI	I^2C Interface Clock Input Line. The device I^2C controller block is forced to reset when receiving 9 clock pulses on the SCL line.
C5, C6	CFH2	P	Channel-2 Flying Capacitor Positive Pins. Connect two 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close as possible to the device.
D1, D2, D5, D6	VOUT	P	Output Pins. Connect to the battery pack positive terminal. Two 10μF capacitors between VOUT and PGND pins are recommended.
D3	BATN/SRP	AI	Battery Voltage Sensing Negative Input or Battery Current Sensing Positive Input. Short this pin and SRN together if R_{SNS} is not used.
D4	SRN	AI	Battery Current Sensing Negative Input. Place a 2mΩ or 5mΩ (R_{SNS}) shunt resistor between SRN and BATN/SRP pins.
E1, E2	CFL1	P	Channel-1 Flying Capacitor Negative Pins. Connect two 22μF or larger parallel capacitors between CFH1 and CFL1 pins as close as possible to the device.
E3	BATP	AI	Battery Voltage Sensing Positive Input. Connect a 100Ω resistor between BATP and positive terminal of the battery pack.
E4	nINT	DO	Open-Drain Interrupt Output Pin. Use a 10kΩ pull-up to the logic high rail. It is normally high but generates a low 256μs pulse when a charge status or fault occurs to inform the host.
E5, E6	CFL2	P	Channel-2 Flying Capacitor Negative Pins. Connect two 22μF or larger parallel capacitors between CFH2 and CFL2 pins as close as possible to the device.
F1, F2, F5, F6	PGND	P	Power Ground Pin.
F3	AGND	P	Analog Ground Pin (reference for low current signals).
F4	REGN	AO	Internal 3.3V LDO Output. Connect a 4.7μF MLCC capacitor between this pin and AGND.

NOTE:
1. P = power, AI = analog input, AO = analog output, AIO = analog input/output, DI = digital input, DO = digital output, DIO = digital input/output.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents						
VAC Quiescent Current	I_{Q_VAC}	ADC disabled, charge disabled, Q_{OVP} used, $V_{VAC\_OVP\_R}$ = 12V (AC_OVP[3:0] bits = 1000) V_{VAC} = 13V, V_{VBUS} = 0V, V_{VOUT} = 0V VAC_OVP activated		350	520	μA
VBUS Quiescent Current	I_{Q_VBUS}	ADC disabled, charge disabled, Q_{OVP} used, V_{VBUS} = 8V, V_{VAC} = 8V (excluding the pull-down current at VBUS pin)		60	100	μA
		ADC enabled, charge enabled, Q_{OVP} used, V_{VBUS} = 8V > (2 × V_{VOUT}), f_{SW} = 500kHz		10		mA
Battery Only Quiescent Current	I_{Q_VOUT}	ADC disabled, charge disabled, VBUS not present, V_{VAC} = 0V, V_{VOUT} = 4.5V		15	27	μA
		ADC enabled, charge disabled, (after 1-shot ADC conversion complete), VBUS not present, V_{VAC} = 0V, V_{VOUT} = 4.5V		15		μA
VBUS Present Rising Threshold	$V_{BUS\_PRESENT\_R}$	V_{VBUS} rising		3.1	3.6	V
VBUS Present Falling Threshold	$V_{BUS\_PRESENT\_F}$	V_{VBUS} falling		2.9		V
VBUS Present Hysteresis	$V_{BUS\_PRESENT\_HYS}$			200		mV
VOUT Present Rising Threshold	$V_{OUT\_PRESENT\_R}$	V_{VOUT} rising to allow enter charge		2.8		V
VOUT Present Falling Threshold	$V_{OUT\_PRESENT\_F}$	V_{VOUT} falling		2.7		V
VOUT Present Hysteresis	$V_{OUT\_PRESENT\_HYS}$			100		mV
External OVP Control						
VAC Present Rising Threshold	$V_{VAC\_PRESENT\_R}$	V_{VAC} rising		3.1	3.5	V
VAC Present Falling Threshold	$V_{VAC\_PRESENT\_F}$	V_{VAC} falling		2.9		V
VAC Present Hysteresis	$V_{VAC\_PRESENT\_HYS}$			200		mV
VAC Present Rising Threshold Deglitch Time	$t_{VAC\_IN\_DEG}$	Deglitch between V_{VAC} rising above $V_{VAC\_PRESENT\_R}$ and starting external OVPFET turn-on		20		ms
VAC OVP Rising Threshold Range	$V_{VAC\_OVP\_R}$	I²C programmable, 1V per step, 12V by default	4		19	V
VAC OVP Threshold Accuracy	$V_{VAC\_OVPR\_ACC}$	$V_{VAC\_OVP\_R}$ = 5V, initial accuracy, T_J = +25℃	4.7	4.9	5.15	V
		$V_{VAC\_OVP\_R}$ = 12V, initial accuracy, T_J = +25℃	11.3	11.8	12.3	V
VAC OVP Rising Deglitch Time	$t_{VAC\_OVPR\_DEG}$	$V_{VAC\_OVP\_R}$ = 12V, V_{VAC} = 11V to 13V, by 5V/μs		100		ns
VBUS Pull-Down Resistor	R_{PDN_VBUS}	VBUS pin, BUS_PDN_EN = 1, V_{VBUS} = 2.6V		3	5	kΩ
VAC Pull-Down Resistor	R_{PDN_VAC}			200	300	Ω
VAC Pull-Down Timeout	t_{VAC_PD}	AC_PDN_EN = 1		400		ms
VBAT Regulation Range	V_{BAT_REG}	I²C programmable, 50mV per step	$V_{BAT\_OVP\_R}$ - 200mV		$V_{BAT\_OVP\_R}$ - 50mV	
VBAT Regulation Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT_REG} = 4.3V		±0.5		%
VBAT Regulation Entry Deglitch Time	$t_{VBAT\_REG\_IN}$			500		μs
IBAT Regulation Range	I_{BAT_REG}	I²C programmable, 100mA per step	I_{BAT_OCP} - 500mA		I_{BAT_OCP} - 200mA	
IBAT Regulation Accuracy	$I_{BAT\_REG\_ACC}$	I_{BAT} = 7A, R_{SNS} = 2mΩ		±2		%
IBAT Regulation Entry Deglitch Time	$t_{IBAT\_REG\_IN}$			500		μs
Switched Cap Chargers						
VBUS to VOUT Resistance	$R_{DROPOUT}$	Bypass mode		15		mΩ
R_{DSON} of Reverse Blocking FET	R_{DS_QRB}	V_{VBUS} = 8V, V_{VOUT} = 4V, I_{BAT} = 0.5A		6		mΩ
R_{DSON} of $Q_{CH1/2}$	R_{DS_QCH}	V_{VBUS} = 8V, V_{VOUT} = 4V, I_{BAT} = 0.5A		14		mΩ
R_{DSON} of $Q_{DH1/2}$	R_{DS_QDH}	V_{VBUS} = 8V, V_{VOUT} = 4V, I_{BAT} = 0.5A		8		mΩ
R_{DSON} of $Q_{CL1/2}$	R_{DS_QCL}	V_{VBUS} = 8V, V_{VOUT} = 4V, I_{BAT} = 0.5A		8		mΩ
R_{DSON} of $Q_{DL1/2}$	R_{DS_QDL}	V_{VBUS} = 8V, V_{VOUT} = 4V, I_{BAT} = 0.5A		8		mΩ

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Protection						
nINT Low Pulse duration when a Protection Occurs	t_{INT}			256		μs
VBUS OVP Rising Threshold Range	$V_{BUS\_OVP\_R}$	I²C programmable, 100mV per step, 11.5V by default	4		14	V
VBUS OVP Threshold Accuracy	$V_{BUS\_OVPR\_ACC}$	$V_{BUS\_OVP\_R}$ = 5V, initial accuracy, T_J = +25℃	4.7	4.9	5.15	V
		$V_{BUS\_OVP\_R}$ = 11.5V, initial accuracy, T_J = +25℃	10.6	11.1	11.7	V
IBUS OCP Threshold Range	I_{BUS_OCP}	Voltage divider mode; I²C programmable, 100mA per step, 4A by default	1.5		4.6	A
		Bypass mode; I²C programmable, 100mA per step, 5A by default	2.5		5.6	
IBUS OCP Threshold Accuracy	$I_{BUS\_OCP\_ACC}$	I_{BUS_OCP} = 3A, initial accuracy, T_J = +25℃	-5		5	%
IBUS UCP Rising Threshold	$I_{BUS\_UCP\_R}$	Rising, set by REG0x07[6] = 0	220	300	380	mA
		Rising, set by REG0x07[6] = 1	410	500	590	
IBUS UCP Falling Threshold	$I_{BUS\_UCP\_F}$	Falling, set by REG0x07[6] = 0	80	150	220	mA
		Falling, set by REG0x07[6] = 1	170	250	320	
IBUS UCP Falling Deglitch Time	$t_{IBUS\_UCPF\_DEG}$	Deglitch between I_{BUS} falling below $I_{BUS\_UCP\_F}$ and triggering protection action, I²C programmable, 64ms by default	0.01		256	ms
VBAT OVP Rising Threshold Range	$V_{BAT\_OVP\_R}$	I²C programmable, 25mV per step, 4.35V by default	4		5	V
VBAT OVP Threshold Accuracy	$V_{BAT\_OVPR\_ACC}$	$V_{BAT\_OVP\_R}$ = 4.35V, initial accuracy, T_J = +25℃	4.31	4.35	4.37	V
VBAT OVP Rising Deglitch Time	$t_{VBAT\_OVPR\_DEG}$	Deglitch between V_{BAT} rising above $V_{BAT\_OVP\_R}$ and triggering protection action		50		μs
IBAT OCP Threshold Range	I_{BAT_OCP}	I²C programmable, 100mA per step, 8.2A by default	3		9.3	A
IBAT OCP Threshold Accuracy	$I_{BAT\_OCP\_ACC}$	I_{BAT_OCP} = 5.2A, R_{SNS} = 2mΩ, initial accuracy, T_J = +25℃	-2.2		2.2	%
IBAT OCP Deglitch Time	$t_{IBAT\_OCP\_DEG}$	Deglitch between I_{BAT} rising above I_{BAT_OCP} and triggering protection action		50		μs
VDRP OVP Threshold Range	V_{DRP_OVP}	I²C programmable, 50mV per step, 300mV by default, V_{DRP} = V_{VAC} - V_{VBUS}	50		400	mV
TDIE OTP Rising Threshold	$T_{DIE\_OTP\_R}$			150		℃
Watchdog Timeout Range	t_{WDT}	I²C programmable, 0.5s by default		0.5		s
ADC Specification						
ADC Resolution	ADC_{RES}			12		bits
ADC Conversion Time	t_{ADC_CONV}	Report data for each channel		4		ms
ADC VBUS Voltage Readable in REG0x14 and REG0x15	V_{BUS_ADC}	Effective range	3		12	V
		LSB		4		mV
VBUS ADC Accuracy	$V_{BUS\_ADC\_ACC}$	V_{VBUS} = 8V, initial accuracy, T_J = +25℃	-2		2	%
ADC IBUS Current Readable in REG0x16 and REG0x17	I_{BUS_ADC}	Effective range	0		6	A
		LSB		2		mA
IBUS ADC Accuracy	$I_{BUS\_ADC\_ACC}$	I_{BUS} = 2A, initial accuracy, T_J = +25℃	-5		5	%
		I_{BUS} = 4A, initial accuracy, T_J = +25℃	-5		5	%
ADC VBAT Voltage Readable in REG0x18 and REG0x19	V_{BAT_ADC}	Effective range	3		5	V
		LSB		2		mV
VBAT ADC Accuracy	$V_{BAT\_ADC\_ACC}$	V_{BAT} = 4V, initial accuracy, T_J = +25℃	-0.5		0.5	%
ADC IBAT Current Readable in REG0x1A and REG0x1B	I_{BAT_ADC}	Effective range	0		9	A
		LSB		2.5		mA

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IBAT ADC Accuracy	$I_{BAT\_ADC\_ACC}$	I_{BAT} = 2A, R_{SNS} = 2mΩ, initial accuracy, T_J = +25℃	-5		5	%
		I_{BAT} = 7A, R_{SNS} = 2mΩ, initial accuracy, T_J = +25℃	-2		2	%
ADC DIE Temperature Readable in REG0x1E	T_{DIE_ADC}	Effective range	-40		150	℃
		LSB		1		℃
TDIE ADC Accuracy	$T_{DIE\_ADC\_ACC}$			±3		℃
ADC VOUT Voltage Readable in REG0x1C and REG0x1D	V_{OUT_ADC}	Effective range	2.7		5	V
		LSB		2		mV
VOUT ADC Accuracy	$V_{OUT\_ADC\_ACC}$	V_{VOUT} = 4V, initial accuracy, T_J = +25℃	-0.5		0.5	%
Logic I/O Threshold (SCL, SDA and nINT Pins)						
High Level Input Voltage	V_{IH_I2C}	SCL and SDA pins	0.825			V
Low Level Input Voltage	V_{IL_I2C}	SCL and SDA pins			0.4	V
Low Level Output Voltage	V_{OL_I2C}	Sink 2mA, SDA and nINT pins			0.4	V
SCL Clock Frequency	f_{CLK}		100		1000	kHz
BC1.2 Detection (DP and DM Pins)						
Data Contact Detect Current Source	I_{DP_SRC}	DP pin, T_J = +25℃	10.5	12.5	14.5	μA
DM Pull-Down Resistance	$R_{DM\_DWN\_BC}$	DM pin, T_J = +25℃	17	20	23	kΩ
Data Contact Detect Logic Low Threshold	V_{LGC_LOW}	DP pin			0.8	V
Data Contact Detect Debounce Time	t_{DCD_DBNC}			15		ms
DP Force Detect Voltage	V_{DP_SRC}	DP pin, T_J = +25℃	0.55	0.60	0.65	V
DM Sink Current	I_{DM_SNK}	DM pin	70	100	130	μA
DP Voltage Source On Time	t_{VDPSRC_ON}	DP pin		60		ms
Pull-Down Detect Threshold	V_{DAT_REF}		0.25	0.325	0.4	V
DM Force Detect Voltage	V_{DM_SRC}	DM pin, T_J = +25℃	0.55	0.60	0.65	V
DP Sink Current	I_{DP_SNK}	DP pin	70	100	130	μA
DM Voltage Source On Time	t_{VDMSRC_ON}	DM pin		60		ms
UFCS Detection (DP and DM Pins)						
High Level Input Voltage	V_{IH_DP}	DP pin	2.31			V
Low Level Input Voltage	V_{IL_DP}	DP pin			0.54	V
High Level Output Voltage	V_{OH_DM}	DM pin, source 0.5mA, V_{VAC} = 3.5V	1.44			V
Low Level Output Voltage	V_{OL_DM}	DM pin, sink 0.5mA			0.5	V
High Level Output Rise Time	t_{RISE}	DM pin, from 20% to 80%, C_L = 200pF		1		μs
Low Level Output Fall Time	t_{FALL}	DM pin, from 80% to 20%, C_L = 200pF		1		μs
Duration of Handshake Detection 1st Signal	t_{DET1}		1.5	2	2.5	ms
Duration of Handshake Detection 2nd Signal	t_{DET2}		6	8	10	ms
Duration of Handshake Detection 3rd Signal	t_{DET3}		1.5	2	2.5	ms
Duration of Handshake Detection 4th Signal	t_{DET4}		6	8	10	ms
Timer for DP Line Pull-up Detection	t_{DpDet}		11		15	ms
Delay Time to Restart DP Line Pull-up Detection	$t_{DetRetry}$	After DP line pull-up detection failed and the detection counter is less than 3	0		10	ms
Delay Time to Output Ping Signal	$t_{SendPing}$	After successful UFCS handshake			100	ms
Data Pin Role Switching Time	$t_{DataRoleSwitch}$	DM pin			1	ms

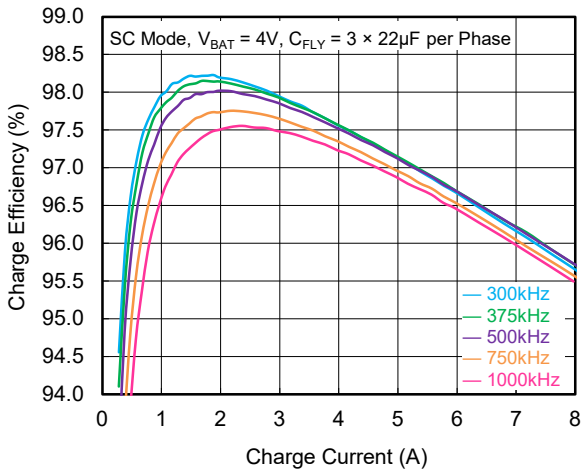
ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +85℃, typical values are at T_J = +25℃, unless otherwise noted.)

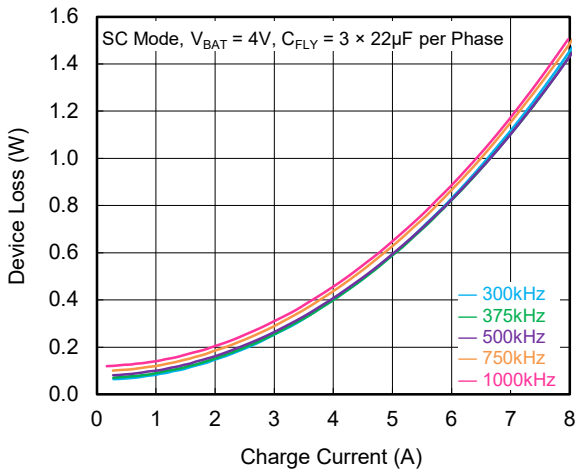
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Frame Receiving Timeout Time	$t_{FrameReceive}$		500	600	700	μs
Duration of Cable Hard Reset Signal	$t_{ResetCable}$		1		1.5	ms
Duration of Source Device Hard Reset Signal	$t_{ResetSource}$		2			ms
Duration of Charging Device Hard Reset Signal	$t_{ResetSink}$		2			ms
ACK Message Receiving Timeout Time	$t_{ACKReceive}$				10	ms
Delay Time to Transmit ACK Message	$t_{ACKTransmit}$		100			μs
Delay Time to Restart Message Transmission	t_{Retry}	After $t_{ACKReceive}$ timeout and the retry conditions are met			500	μs
Response Message Receiving Timeout Time	$t_{SenderRespone}$				50	ms
Delay Time to Transmit Response Message	$t_{ReceiverRespone}$				40	ms
Power_Ready Message Receiving Timeout Time	$t_{PowerSupply}$	Duration from charging device receiving ACK message to receiving power ready message and obtaining the desired voltage and current			550	ms
Cable_Information Message Receiving Timeout Time	$t_{CableInfoRespone}$				1200	ms
End_Cable_Detect Message Receiving Timeout Time	$t_{RestartTrans}$				1100	ms
Delay Time to Transmit Message to Cable	$t_{CableTrans}$	After cable responding Cable_Information message			1000	ms
Delay Time before Transmitting Next Message	$t_{MsgTransDelay}$	After transmitted a message (Note: should not longer than $t_{ACKReceive}$ and $t_{ReceiverRespone}$)	2			ms

TYPICAL PERFORMANCE CHARACTERISTICS

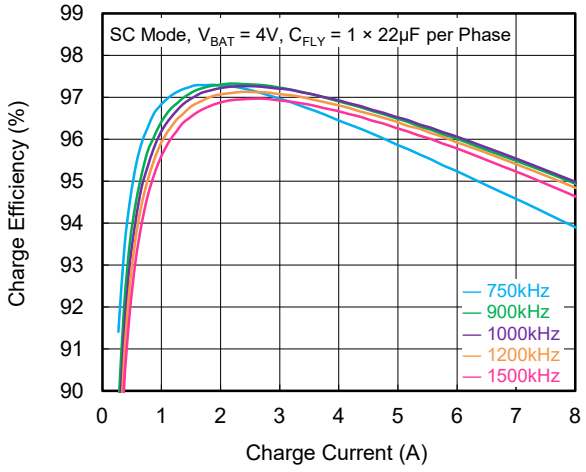
Charge Efficiency vs. Charge Current



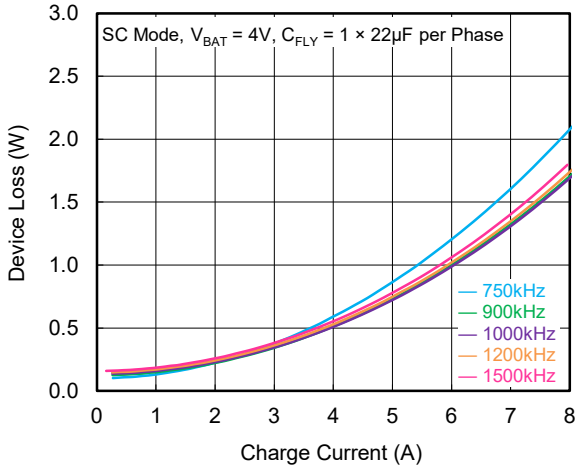
Device Loss vs. Charge Current



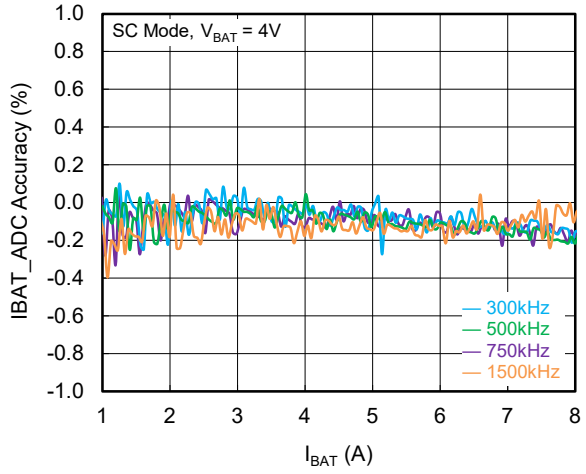
Charge Efficiency vs. Charge Current



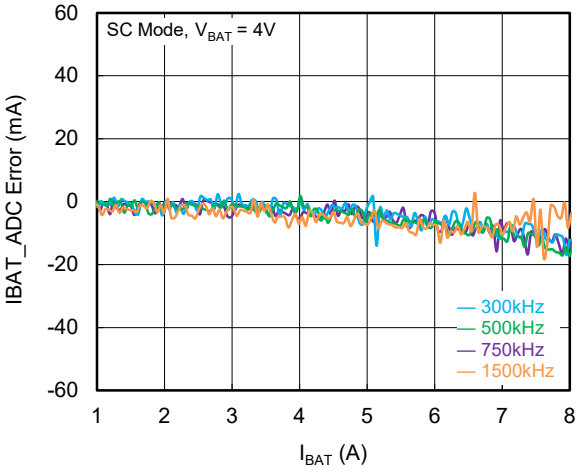
Device Loss vs. Charge Current



IBAT_ADC Accuracy vs. BAT Current

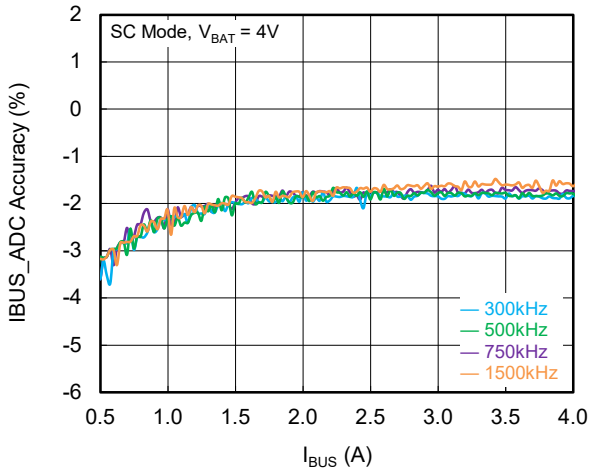


IBAT_ADC Error vs. BAT Current

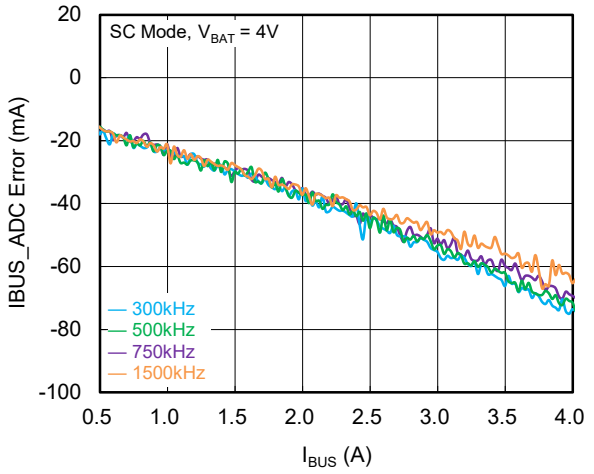


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

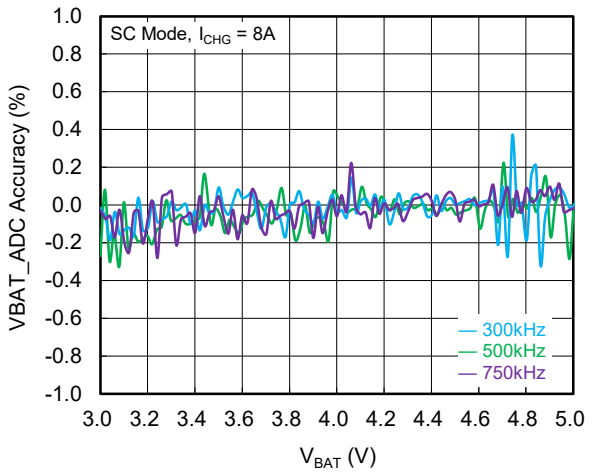
IBUS_ADC Accuracy vs. BUS Current



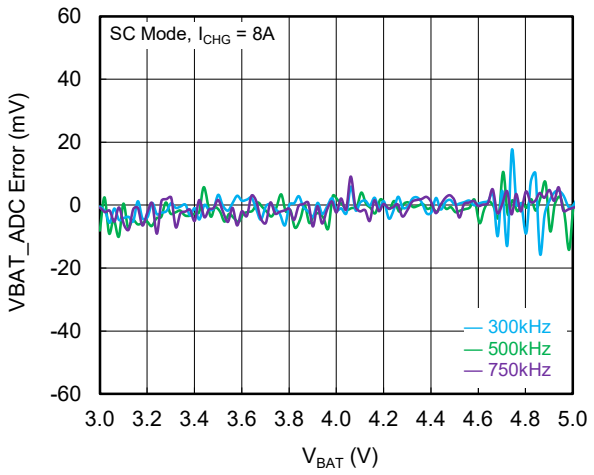
IBUS_ADC Error vs. BUS Current



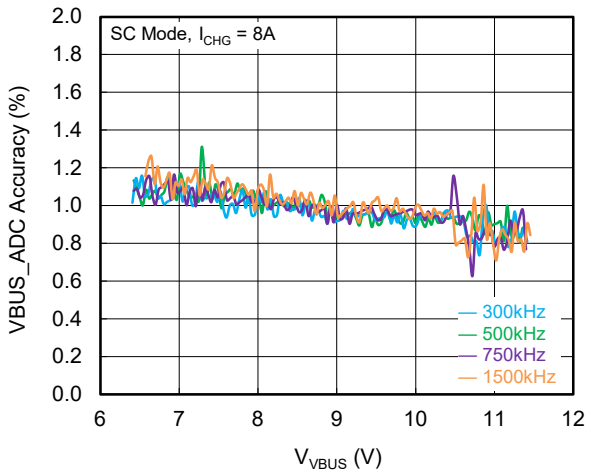
VBAT_ADC Accuracy vs. BAT Voltage



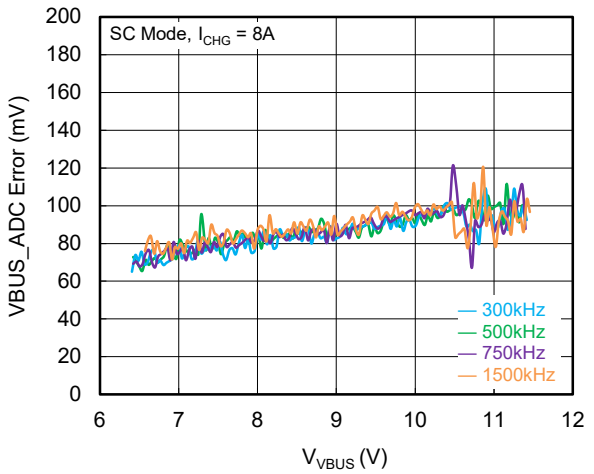
VBAT_ADC Error vs. BAT Voltage



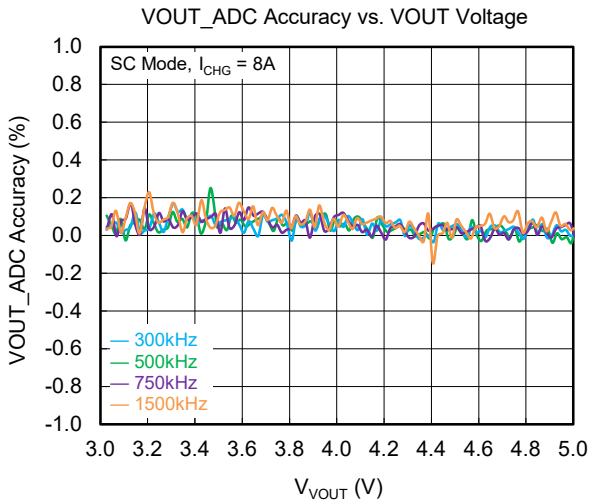
VBUS_ADC Accuracy vs. BUS Voltage

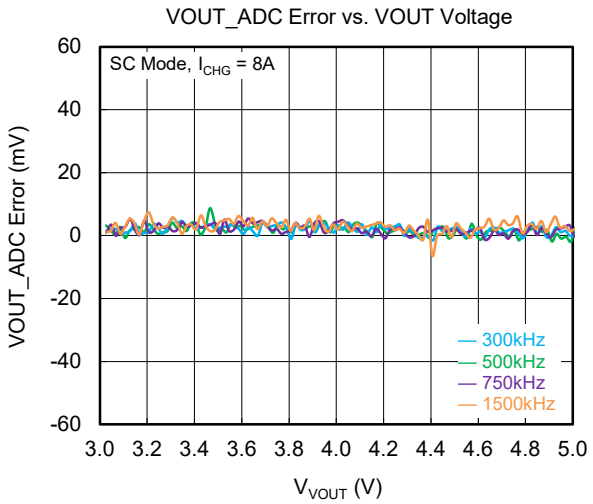


VBUS_ADC Error vs. BUS Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (continued)





TYPICAL APPLICATION CIRCUIT

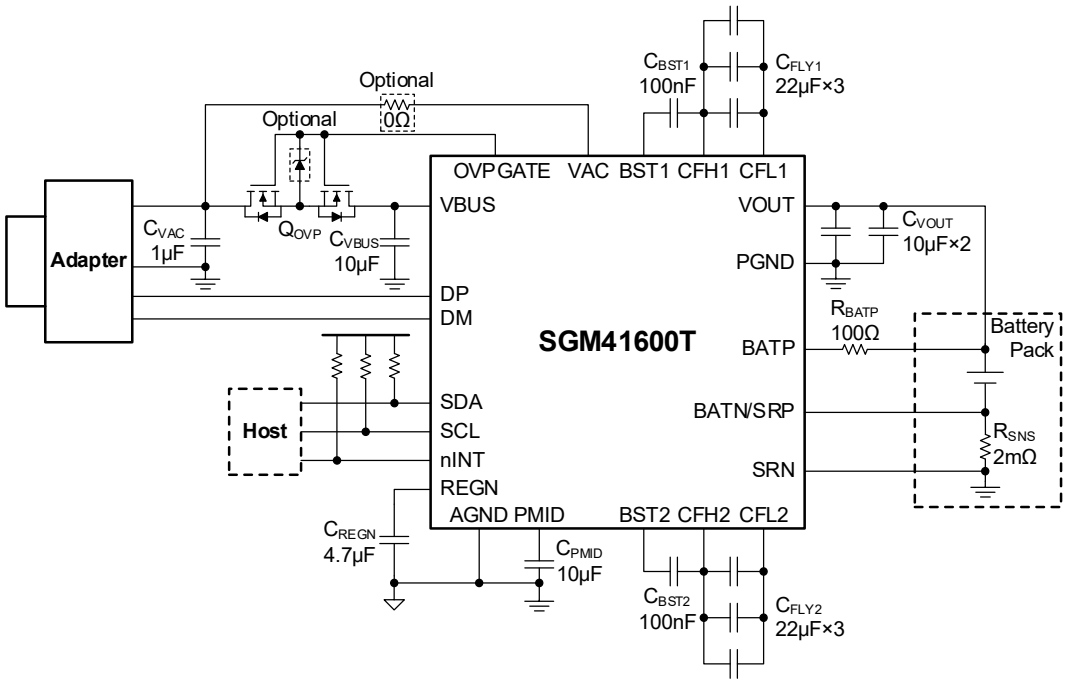


Figure 2. Typical Application Circuit

FUNCTIONAL BLOCK DIAGRAM

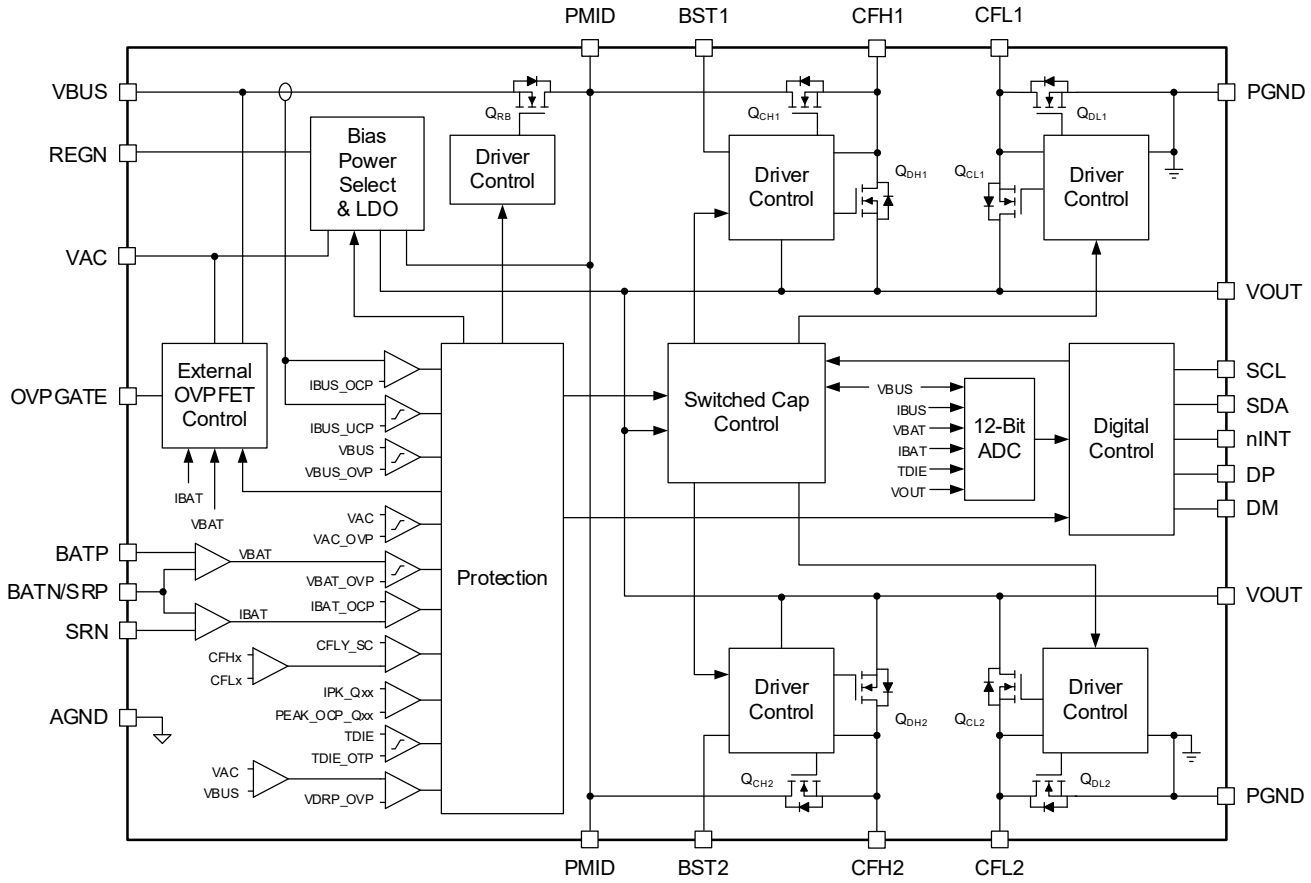


Figure 3. Functional Block Diagram

REGISTER ADDRESS MAPPING

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

Slave Device Address: 0x6E (0b1101 110 + W/R)

FUNCTION	FLAG	MASK	THRESHOLD SETTING	ENABLE	DEGLITCH
DEVICE_REV	—	—	0x03[7:4]	—	—
DEVICE_ID	—	—	0x03[3:0]	—	—
REG_RST	—	—	0x00[7]	—	—
CHG_MODE	—	—	0x00[6:4]	—	—
WD_TIMEOUT	0x11[5]	0x12[5]	0x00[2:0]	0x00[3]	—
FSW_SET	—	—	0x01[7:5]	—	—
FSW_SHIFT	—	—	0x01[4:3]	—	—
FSW_DITHER	—	—	—	0x01[2]	—
OVPGATE	—	—	—	0x04[5] & 0x05[6]	—
VAC_OVP	0x0D[7]	0x0E[7]	0x04[3:0]	0x04[4]	
AC_PDN	0x0D[6]	0x0E[6]	—	0x05[7]	—
VAC_ABSENT	0x11[4]	0x12[4]	—	—	—
VDRP_OVP	0x0D[4]	0x0E[4]	0x05[2:0]	0x05[5]	0x05[4]
VBUS_OVP	0x0D[3]	0x0E[3]	0x06[6:0]	0x06[7]	—
BUS_PDN	0x0D[5]	0x0E[5]	—	0x05[6]	—
VBUS_INSERT	0x11[7]	0x12[7]	—	—	—
VBUS_ABSENT	0x11[3]	0x12[3]	—	—	—
VBUS_HI	0x0F[1]	0x10[1]	0x02[1:0]	0x02[4]	0x08[5]
VBUS_LO	0x0F[2]	0x10[2]	0x02[3:2]	0x02[5]	0x08[4]
IBUS_UCP_TIMEOUT	0x0D[1]	0x0E[1]	0x08[3:2]	0x07[7]	—
IBUS_UCP_FALL	0x0D[0]	0x0E[0]	0x07[6]	0x07[7]	0x08[1:0]
IBUS_OCP	0x0D[2]	0x0E[2]	0x07[4:0]	0x07[5]	—
VOUT_OVP	0x11[2]	0x12[2]	0x0C[2:1]	0x0C[3]	0x0C[0]
VOUT_INSERT	0x11[6]	0x12[6]	—	—	—
VBAT_OVP	0x0F[7]	0x10[7]	0x09[5:0]	0x09[7]	—
VBAT_REG	0x0F[5]	0x10[5]	0x0B[1:0]	0x0B[2]	—
IBAT_OCP	0x0F[6]	0x10[6]	0x0A[5:0] & 0x0A[6]	0x0A[7]	—
IBAT_REG	0x0F[4]	0x10[4]	0x0B[4:3]	0x0B[5]	—
REG_TIMEOUT	—	—	—	0x0B[6]	—
PEAK_OCP	0x0F[0]	0x10[0]	0x01[1] & 0x01[0]	—	—
PIN_DIAG (CFLY_SC & VOUT_SC)	0x11[0]	0x12[0]	—	0x02[7]	—
TDIE_OTP	0x0F[3]	0x10[3]	—	—	—
ADC	0x11[1]	0x12[1]	0x13[6]	0x13[7]	—

REGISTER AND DATA

Bit Types:
R: Read only
R/W: Read/Write
RC: Read clears the bit
R/WC: Read/Write. Writing a '1' clears the bit. Writing a '0' has no effect.

REG0x00: CONTROL1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	REG_RST	0	R/WC	Register Reset Bit 0 = No register reset (default) 1 = Reset registers to their default values. When enabled, the associated register bits are reset to their default value and then this bit is automatically reset to 0.	REG_RST
D[6:4]	CHG_MODE[2:0]	000	R/W	Charge Mode Control Bits 000 = Off mode (default) 001 = Forward bypass mode 010 = Forward Charge-pump voltage divider mode 011 ~ 111 = Off mode Note: It is not allowed to change charge mode during charging.	REG_RST or WDT
D[3]	WDT_DIS	0	R/W	Watchdog Enable Bit 0 = Watchdog enabled (default) 1 = Watchdog disabled	REG_RST
D[2:0]	WDT_TIMER[2:0]	000	R/W	Watchdog Timer Setting Bits 000 = 0.5sec (default) 001 = 1sec 010 = 2sec 011 = 5sec 100 = 10sec 101 = 20sec 110 = 40sec 111 = 80sec	REG_RST

REG0x01: CONTROL2 Register [reset = 0x40]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:5]	FSW_SET[2:0]	010	R/W	Voltage Divider Switching Frequency Setting Bits 000 = 300kHz 001 = 375kHz 010 = 500kHz (default) 011 = 600kHz 100 = 750kHz 101 = 1000kHz 110 = 1200kHz 111 = 1500kHz Note: support switching frequency change during charging.	REG_RST
D[4:3]	FSW_SHIFT[1:0]	00	R/W	Bits of Adjusting Switching Frequency for EMI 00/11 = Nominal frequency (default) 01 = Nominal frequency +10% 10 = Nominal frequency -10%	REG_RST
D[2]	FSW_DITHER_EN	0	R/W	Switching Frequency Dithering Enable Bit 0 = Disabled (default) 1 = Enabled. Dither varies switching frequency ±10%	REG_RST
D[1]	PEAK_OCP_QCH	0	R/W	Q_{CHx} Peak OCP Threshold Setting Bit 0 = 9.5A (default) 1 = 13A	REG_RST
D[0]	PEAK_OCP_QDL	0	R/W	Q_{DLx} Bidirectional Peak OCP Threshold Setting Bit 0 = 9.5A (default) 1 = 13A	REG_RST

REGISTER AND DATA (continued)

REG0x02: CONTROL3 Register [reset = 0xBC]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	PIN_DIAG_EN	1	R/W	Pin Diagnosis Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5]	VBUS_LO_EN	1	R/W	Low VBUS Error Detection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[4]	VBUS_HI_EN	1	R/W	High VBUS Error Detection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[3:2]	VBUS_LO[1:0]	11	R/W	Low VBUS Error Reference Setting Bits 00 = 1.01 01 = 1.02 10 = 1.03 11 = 1.04 (default)	REG_RST
D[1:0]	VBUS_HI[1:0]	00	R/W	High VBUS Error Reference Setting Bits 00 = 1.10 (default) 01 = 1.15 10 = 1.20 11 = 1.25	REG_RST

REG0x03: DEVICE_INFO Register [reset = 0x12]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	DEVICE_REV[3:0]	0001	R	Device Revision 0001 = NTO-A SGM41600T	N/A
D[3:0]	DEVICE_ID[3:0]	0010	R	Device ID 0010 = SGM41600T	N/A

REG0x04: AC_OVP Register [reset = 0x18]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	OVPGATE_EN	0	R/W	When VAC is not present but VBUS is present, turn on/off OVPFET by OVPGATE pin. 0 = Turn off OVPFET when VAC is not present (default) 1 = Turn on OVPFET even when VAC is not present Note: when OVPGATE_EN = 1, OVPFET cannot be turned off by BUS_PDN_EN = 1; While OVPGATE_EN = 0, OVPFET can be turned off by BUS_PDN_EN = 1.	REG_RST
D[4]	AC_OVP_EN	1	R/W	VAC OVP Protection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[3:0]	AC_OVP[3:0]	1000	R/W	VAC OVP Protection Rising Threshold Setting Bits VAC OVP Rising Threshold Value: = 4V + AC_OVP[3:0] × 1V Offset: 4V Range: 4V (0000) - 19V (1111) Default: 12V (1000)	REG_RST

REGISTER AND DATA (continued)

REG0x05: PULL-DOWN & VDRP_OVP Register [reset = 0x25]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	AC_PDN_EN	0	R/WC	VAC Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, the VAC is pulled down for 400ms and then this bit is automatically reset to 0.	N/A
D[6]	BUS_PDN_EN	0	R/W	VBUS Pull-Down Resistor Enable Bit 0 = Pull-down disabled (default) 1 = Pull-down enabled. When enabled, it will turn off the external OVPFET and discharge VBUS and PMID with R_{PDN_VBUS} and R_{PDN_PMID}. This action is important during a hot-plug event to prevent transient over-voltages.	REG_RST
D[5]	VDRP_OVP_EN	1	R/W	VDRP OVP Protection Enable Bit, $V_{DRP} = (V_{VAC} - V_{VBUS})$ 0 = Disabled 1 = Enabled (default)	REG_RST
D[4]	VDRP_OVP_DEG	0	R/W	VDRP OVP Protection Deglitch Time Setting Bit This is deglitch time ($t_{DRP\_OVP\_DEG}$) between the moment V_{DRP} exceeding V_{DRP_OVP} threshold and triggering the protection action. 0 = 10μs (default) 1 = 5ms	REG_RST
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	VDRP_OVP[2:0]	101	R/W	VDRP OVP Protection Threshold Setting Bits VDRP OVP Threshold Value: = 50mV + VDRP_OVP[2:0] × 50mV Offset: 50mV Range: 50mV (000) - 400mV (111) Default: 300mV (101)	REG_RST

REG0x06: BUS_OVP Register [reset = 0xCB]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUS_OVP_EN	1	R/W	VBUS OVP and Peak OVP Protection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[6:0]	BUS_OVP[6:0]	100 1011	R/W	Setting Bits of VBUS OVP Protection Rising Threshold VBUS OVP Rising Threshold Value: = 4V + BUS_OVP[6:0] × 100mV Offset: 4V Range: 4V (000 0000) - 14V (110 0100) Default: 11.5V (100 1011) If BUS_OVP[6:0] ≥ 110 0100, V_{BUS_OVP} = 14V	REG_RST

REGISTER AND DATA (continued)

REG0x07: IBUS_OCP & UCP Register [reset = 0xB9]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBUS_UCP_EN	1	R/W	IBUS UCP Protection Enable Bit 0 = Disabled 1 = Enabled (default) Note: Including IBUS_UCP_TIMEOUT and IBUS_UCP_FALL protections.	REG_RST
D[6]	IBUS_UCP	0	R/W	IBUS UCP Threshold Setting 0 = $I_{BUS\_UCP\_R}$ = 300mA rising, $I_{BUS\_UCP\_F}$ = 150mA falling (default) 1 = $I_{BUS\_UCP\_R}$ = 500mA rising, $I_{BUS\_UCP\_F}$ = 250mA falling The system should control the I_{BUS} current to rise above $I_{BUS\_UCP\_R}$ before $t_{IBUS\_UCP\_BLK}$ time expires. Note: This bit can only be changed before enabling switching.	REG_RST
D[5]	IBUS_OCP_EN	1	R/W	IBUS OCP Protection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[4:0]	IBUS_OCP[4:0]	1 1001	R/W	IBUS OCP Threshold Setting Voltage Divider Mode: I_{BUS_OCP} = 1.5A + IBUS_OCP[4:0] × 100mA Offset: 1.5A Range: 1.5A (0 0000) - 4.6A (1 1111) Default: 4A (1 1001) Bypass Mode: I_{BUS_OCP} = 2.5A + IBUS_OCP[4:0] × 100mA Offset: 2.5A Range: 2.5A (0 0000) - 5.6A (1 1111) Default: 5A (1 1001)	REG_RST

REG0x08: BUS_PROT_DEG Register [reset = 0x06]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VBUS_HI_DEG	0	R/W	High VBUS Error Detection Deglitch Time Setting Bit This is deglitch time ($t_{VBUS\_HI\_DEG}$) between the moment V_{PMID} rising above n × (V_{BUS_HI} × V_{VOUT} + 100mV) and triggering protection action (n = 1 or 2, depending on the operation mode) 0 = 100ns (default) 1 = 100μs	REG_RST
D[4]	VBUS_LO_DEG	0	R/W	Low VBUS Error Detection Deglitch Time Setting Bit This is deglitch time ($t_{VBUS\_LO\_DEG}$) between the moment V_{PMID} falling below n × (V_{BUS_LO} × V_{VOUT} - 100mV) and triggering protection action (n = 1 or 2, depending on the operation mode) 0 = 10μs (default) 1 = 1ms	REG_RST
D[3:2]	IBUS_UCP_BLK[1:0]	01	R/W	IBUS UCP Protection Blanking Time Setting Bits After soft-start timer, $t_{IBUS\_UCP\_BLK}$ = 100ms × 2 ^ IBUS_UCP_BLK[1:0] 00 = 100ms 01 = 200ms (default) 10 = 400ms 11 = 800ms	REG_RST
D[1:0]	IBUS_UCP_FALL_DEG[1:0]	10	R/W	IBUS UCP Protection Falling Deglitch Time Setting Bit This is deglitch time ($t_{IBUS\_UCPF\_DEG}$) between the moment I_{BUS} falling below $I_{BUS\_UCP\_F}$ threshold and triggering protection action. 00 = 10μs 01 = 8ms 10 = 64ms (default) 11 = 256ms	REG_RST

REGISTER AND DATA (continued)

REG0x09: BAT_OVP Register [reset = 0x8E]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BAT_OVP_EN	1	R/W	VBAT OVP Protection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[6]	Reserved	0	R	Reserved	N/A
D[5:0]	BAT_OVP[5:0]	00 1110	R/W	VBAT OVP Rising Threshold Setting VBAT OVP Rising Threshold Value: = 4V + BAT_OVP[5:0] × 25mV Offset: 4V Range: 4V (00 0000) - 5V (10 1000) Default: 4.35V (00 1110) When BAT_OVP[5:0] ≥ 10 1000, V_{BAT_OVP} = 5V	REG_RST

REG0x0A: IBAT_OCP Register [reset = 0xB4]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	IBAT_OCP_EN	1	R/W	IBAT OCP Protection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[6]	IBAT_RSNS	0	R/W	External IBAT Current Sense Resistor Setting Bit 0 = 2mΩ (default) 1 = 5mΩ	REG_RST
D[5:0]	IBAT_OCP[5:0]	11 0100	R/W	IBAT OCP Threshold Setting Bits IBAT OCP Threshold Value: = 3A + IBAT_OCP[5:0] × 100mA Offset: 3A Range: 3A (00 0000) to 9.3A (11 1111) Default: 8.2A (11 0100)	REG_RST

REGISTER AND DATA (continued)

REG0x0B: REGULATION Register [reset = 0x24]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	REG_TIMEOUT_DIS	0	R/W	Regulation Timeout Disable 0 = Enabled (default) 1 = Disabled When enabled, charging will be disabled if the regulation lasts longer than 650ms.	REG_RST
D[5]	IBAT_REG_EN	1	R/W	IBAT Regulation Enable 0 = Disabled 1 = Enabled (default) When enabled, $t_{IBAT\_OCP\_DEG}$ is increased to 500μs to avoid unwanted triggering of IBAT_OCP during regulation.	REG_RST
D[4:3]	IBAT_REG[1:0]	00	R/W	IBAT Regulation Threshold Setting 00 = 200mA below IBAT_OCP[5:0] register setting (default) 01 = 300mA below IBAT_OCP[5:0] register setting 10 = 400mA below IBAT_OCP[5:0] register setting 11 = 500mA below IBAT_OCP[5:0] register setting The margin below IBAT_OCP[5:0] register at which IBAT regulation starts.	REG_RST
D[2]	VBAT_REG_EN	1	R/W	VBAT Regulation Enable 0 = Disabled 1 = Enabled (default) When enabled, $t_{VBAT\_OVPR\_DEG}$ is increased to 500μs to avoid unwanted triggering of VBAT OVP during regulation.	REG_RST
D[1:0]	VBAT_REG[1:0]	00	R/W	VBAT Regulation Threshold Setting 00 = 50mV below BAT_OVP[5:0] register setting (default) 01 = 100mV below BAT_OVP[5:0] register setting 10 = 150mV below BAT_OVP[5:0] register setting 11 = 200mV below BAT_OVP[5:0] register setting The margin below BAT_OVP[5:0] register at which VBAT regulation starts.	REG_RST

REG0x0C: VOUT_OVP Register [reset = 0x0B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3]	VOUT_OVP_EN	1	R/W	VOUT OVP Protection Enable Bit 0 = Disabled 1 = Enabled (default)	REG_RST
D[2:1]	VOUT_OVP[1:0]	01	R/W	VOUT OVP Protection Rising Threshold Setting Bits $V_{VOUT\_OVP\_R}$ = 4.6V + VOUT_OVP[1:0] × 200mV 00 = 4.6V 01 = 4.8V (default) 10 = 5V 11 = 5.2V	REG_RST
D[0]	VOUT_OVP_DEG	1	R/W	VOUT OVP Protection Deglitch Time Setting Bit This is deglitch time ($t_{VOUT\_OVP\_DEG}$) between the moment V_{VOUT} exceeding $V_{VOUT\_OVP\_R}$ threshold and triggering protection action. 0 = 100μs 1 = 1ms (default)	REG_RST

REGISTER AND DATA (continued)

REG0x0D: FLT_FLAG1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	AC_OVP_FLAG	0	RC	VAC OVP Fault Flag 0 = No VAC OVP fault 1 = VAC OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VAC OVP fault is cleared, a read on this bit will reset it to 0.	N/A
D[6]	AC_PDN_FLAG	0	RC	VAC Pull-Down Event Flag 0 = No VAC pull-down event 1 = VAC pull-down event has occurred. It generates an interrupt on nINT pin if unmasked. After the VAC pull-down event is complete, a read on this bit will reset it to 0.	N/A
D[5]	BUS_PDN_FLAG	0	RC	VBUS Pull-Down Event Flag 0 = No VBUS pull-down event 1 = VBUS pull-down event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS pull-down event is complete, a read on this bit will reset it to 0.	REG_RST
D[4]	VDRP_OVP_FLAG	0	RC	VDRP OVP Fault Flag 0 = No VDRP OVP fault 1 = VDRP OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[3]	BUS_OVP_FLAG	0	RC	VBUS OVP Fault Flag 0 = No VBUS OVP fault 1 = VBUS OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS OVP fault is cleared, a read on this bit will reset it to 0.	N/A
D[2]	IBUS_OCP_FLAG	0	RC	IBUS OCP Fault Flag 0 = No IBUS OCP fault 1 = IBUS OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[1]	IBUS_UCP_ TIMEOUT_FLAG	0	RC	IBUS UCP Timeout Fault Flag 0 = No IBUS UCP timeout fault 1 = IBUS UCP timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	IBUS_UCP_FALL_ FLAG	0	RC	IBUS UCP Fall Event Flag 0 = No IBUS UCP fall event 1 = IBUS UCP fall event has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	REG_RST

REGISTER AND DATA (continued)

REG0x0E: FLT_INT_MASK1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	AC_OVP_MASK	0	R/W	Mask VAC OVP Fault Interrupt 0 = VAC OVP fault interrupt can work (default) 1 = Mask VAC OVP fault interrupt. AC_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[6]	AC_PDN_MASK	0	R/W	Mask VAC Pull-Down Event Interrupt 0 = VAC pull-down event interrupt can work (default) 1 = Mask VAC pull-down event interrupt. AC_PDN_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	BUS_PDN_MASK	0	R/W	Mask VBUS Pull-Down Event Interrupt 0 = VBUS pull-down event interrupt can work (default) 1 = Mask VBUS pull-down event interrupt. BUS_PDN_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	VDRP_OVP_MASK	0	R/W	Mask VDRP OVP Fault Interrupt 0 = VDRP OVP fault interrupt can work (default) 1 = Mask VDRP OVP fault interrupt. VDRP_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	BUS_OVP_MASK	0	R/W	Mask BUS OVP Fault Interrupt 0 = BUS OVP fault interrupt can work (default) 1 = Mask BUS OVP fault interrupt. BUS_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	IBUS_OCP_MASK	0	R/W	Mask IBUS OCP Fault Interrupt 0 = IBUS OCP fault interrupt can work (default) 1 = Mask IBUS OCP fault interrupt. IBUS_OCP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	IBUS_UCP_ TIMEOUT_MASK	0	R/W	Mask IBUS_UCP_TIMEOUT Fault Interrupt 0 = IBUS_UCP_TIMEOUT fault interrupt can work (default) 1 = Mask IBUS_UCP_TIMEOUT fault interrupt. IBUS_UCP_TIMEOUT_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	IBUS_UCP_FALL_ MASK	0	R/W	Mask IBUS UCP Fall Event Interrupt 0 = IBUS UCP fall event interrupt can work (default) 1 = Mask IBUS UCP fall event interrupt. IBUS_UCP_FALL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REGISTER AND DATA (continued)

REG0x0F: FLT_FLAG2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BAT_OVP_FLAG	0	RC	VBAT OVP Fault Flag 0 = No VBAT OVP fault 1 = VBAT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT OVP fault is cleared, reading this bit will reset it to 0.	N/A
D[6]	IBAT_OCP_FLAG	0	RC	IBAT OCP Fault Flag 0 = No IBAT OCP fault 1 = IBAT OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[5]	VBAT_REG_FLAG	0	RC	VBAT Regulation Event Flag 0 = No VBAT regulation event 1 = VBAT regulation event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBAT regulation event is complete, reading this bit will reset it to 0.	N/A
D[4]	IBAT_REG_FLAG	0	RC	IBAT Regulation Event Flag 0 = No IBAT regulation event 1 = IBAT regulation event has occurred. It generates an interrupt on nINT pin if unmasked. After the IBAT regulation event is complete, reading this bit will reset it to 0.	N/A
D[3]	TDIE_OTP_FLAG	0	RC	TDIE OTP Fault Flag (Die Over-Temperature) 0 = No TDIE OTP fault 1 = TDIE OTP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the TDIE OTP fault is cleared, reading this bit will reset it to 0.	N/A
D[2]	VBUS_LO_FLAG	0	RC	VBUS Under-Voltage Fault Flag It is set to 1 if $V_{VBUS}/V_{VOUT} < 2 \times V_{BUS\_LO}$ in voltage divider mode, or $V_{VBUS}/V_{VOUT} < V_{BUS\_LO}$ in bypass mode. 0 = No VBUS under-voltage fault 1 = VBUS under-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS under-voltage fault is cleared, reading this bit will reset it to 0.	N/A
D[1]	VBUS_HI_FLAG	0	RC	VBUS Over-Voltage Fault Flag It is set to 1 if $V_{VBUS}/V_{VOUT} > 2 \times V_{BUS\_HI}$ in voltage divider mode, or $V_{VBUS}/V_{VOUT} > V_{BUS\_HI}$ in bypass mode. 0 = No VBUS over-voltage fault 1 = VBUS over-voltage fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS over-voltage fault is cleared, reading this bit will reset it to 0.	N/A
D[0]	PEAK_OCP_FLAG	0	RC	Switching FETs Peak OCP Fault Flag It is set to 1 if at least one of the internal switching FETs Q_{CHx} and Q_{DLx} reaches its peak OCP threshold. 0 = No switching FETs peak OCP fault 1 = Switching FETs peak OCP fault has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x10: FLT_INT_MASK2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BAT_OVP_MASK	0	R/W	Mask VBAT OVP Fault Interrupt 0 = VBAT OVP fault interrupt can work (default) 1 = Mask VBAT OVP fault interrupt. BAT_OVP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[6]	IBAT_OCP_MASK	0	R/W	Mask IBAT OCP Fault Interrupt 0 = IBAT OCP fault interrupt can work (default) 1 = Mask IBAT OCP fault interrupt. IBAT_OCP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	VBAT_REG_MASK	0	R/W	Mask VBAT Regulation Event Interrupt 0 = VBAT regulation event interrupt can work (default) 1 = Mask VBAT regulation event interrupt. VBAT_REG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	IBAT_REG_MASK	0	R/W	Mask IBAT Regulation Event Interrupt 0 = IBAT regulation event interrupt can work (default) 1 = Mask IBAT regulation event interrupt. IBAT_REG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	TDIE_OTP_MASK	0	R/W	Mask TDIE OTP Fault Interrupt 0 = TDIE OTP fault interrupt can work (default) 1 = Mask TDIE OTP fault interrupt. TDIE_OTP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	VBUS_LO_MASK	0	R/W	Mask VBUS Under-Voltage Fault Interrupt 0 = VBUS under-voltage fault interrupt can work (default) 1 = Mask VBUS under-voltage fault interrupt. VBUS_LO_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[1]	VBUS_HI_MASK	0	R/W	Mask VBUS Over-Voltage Fault Interrupt 0 = VBUS over-voltage fault interrupt can work (default) 1 = Mask VBUS over-voltage fault interrupt. VBUS_HI_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	PEAK_OCP_MASK	0	R/W	Mask PEAK OCP Fault Interrupt 0 = PEAK OCP fault interrupt can work (default) 1 = Mask PEAK OCP fault interrupt. PEAK_OCP_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REGISTER AND DATA (continued)

REG0x11: FLT_FLAG3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUS_INSERT_FLAG	0	RC	VBUS Insert Event Flag This bit is set to 1 if V_{VBUS} > $V_{BUS\_PRESENT\_R}$. 0 = No VBUS insert event 1 = VBUS insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS is absent, reading this bit will reset it to 0.	N/A
D[6]	VOUT_INSERT_FLAG	0	RC	VOUT Insert Event Flag If ADC_EN bit = 1 or V_{VAC} > $V_{VAC\_PRESENT\_R}$ or V_{VBUS} > $V_{BUS\_PRESENT\_R}$, this bit will set to 1 when V_{VOUT} > $V_{OUT\_PRESENT\_R}$. 0 = No VOUT insert event 1 = VOUT insert event has occurred. It generates an interrupt on nINT pin if unmasked. After the VOUT is absent, reading this bit will reset it to 0.	N/A
D[5]	WD_TIMEOUT_FLAG	0	RC	Watchdog Timeout Fault Flag 0 = No watchdog timeout fault 1 = Watchdog timeout fault has occurred. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	REG_RST
D[4]	VAC_ABSENT_FLAG	0	RC	VAC Absent Fault Flag This bit is set to 1 if V_{VAC} < $V_{VAC\_PRESENT\_F}$. 0 = No VAC absent fault 1 = VAC absent fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VAC is present, a read on this bit will reset it to 0.	N/A
D[3]	BUS_ABSENT_FLAG	0	RC	VBUS Absent Fault Flag It is set to 1 if V_{VBUS} < $V_{BUS\_PRESENT\_F}$. 0 = No VBUS absent fault 1 = VBUS absent fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VBUS is present, a read on this bit will reset it to 0.	N/A
D[2]	VOUT_OVP_FLAG	0	RC	VOUT OVP Fault Flag 0 = No VOUT OVP fault 1 = VOUT OVP fault has occurred. It generates an interrupt on nINT pin if unmasked. After the VOUT OVP fault is cleared, reading this bit will reset it to 0.	N/A
D[1]	ADC_DONE_FLAG	0	RC	ADC Conversion Complete Flag In 1-shot conversion mode, this bit is set to 1 after ADC conversion of all enabled channels is completed. 0 = Normal 1 = ADC conversion complete. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	N/A
D[0]	PIN_DIAG_FLAG	0	RC	Pin Diagnosis Fail Fault Flag When switching is enabled, certain conditions are checked on the C_{FLY} and VOUT pins to assure proper operation. 0 = Normal 1 = C_{FLY} short or VOUT pin short fault has occurred. It generates an interrupt on nINT pin. Reading this bit will reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x12: FLT_INT_MASK3 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	BUS_INSERT_MASK	0	R/W	Mask BUS_INSERT Event Interrupt 0 = BUS_INSERT event interrupt can work (default) 1 = Mask BUS_INSERT event interrupt. BUS_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[6]	VOUT_INSERT_MASK	0	R/W	Mask VOUT_INSERT Event Interrupt 0 = VOUT_INSERT event interrupt can work (default) 1 = Mask VOUT_INSERT event interrupt. VOUT_INSERT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[5]	WD_TIMEOUT_MASK	0	R/W	Mask WD_TIMEOUT Fault Interrupt 0 = WD_TIMEOUT fault interrupt can work (default) 1 = Mask WD_TIMEOUT fault interrupt. WD_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[4]	VAC_ABSENT_MASK	0	R/W	Mask VAC_ABSENT Fault Interrupt 0 = VAC_ABSENT fault interrupt can work (default) 1 = Mask VAC_ABSENT fault interrupt. VAC_ABSENT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[3]	BUS_ABSENT_MASK	0	R/W	Mask BUS_ABSENT Fault Interrupt 0 = BUS_ABSENT fault interrupt can work (default) 1 = Mask BUS_ABSENT fault interrupt. BUS_ABSENT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[2]	VOUT_OVP_MASK	0	R/W	Mask VOUT OVP Fault Interrupt 0 = VOUT OVP fault interrupt can work (default) 1 = Mask VOUT OVP fault interrupt. VOUT_OVP_FLAG bit is set after the fault, but the interrupt signal is not generated.	REG_RST
D[1]	ADC_DONE_MASK	0	R/W	Mask ADC Complete Event Interrupt 0 = ADC_DONE event interrupt can work (default) 1 = Mask ADC_DONE event interrupt. ADC_DONE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST
D[0]	PIN_DIAG_MASK	0	R/W	Mask Pin Diagnosis Fail Interrupt 0 = Pin diagnosis fail interrupt can work (default) 1 = Mask pin diagnosis fail interrupt. PIN_DIAG_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST

REGISTER AND DATA (continued)

REG0x13: ADC_CTRL Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	ADC_EN	0	R/W	ADC Conversion Enable 0 = Disabled (default) 1 = Enabled Note: In 1-shot mode when the selected channel conversions are completed, the ADC_EN bit is automatically reset to 0. All channel conversions except IBUS_ADC and IBAT_ADC can be enabled even when the device is not during charging (CHG_MODE[2:0] = 000).	REG_RST or WDT
D[6]	ADC_RATE	0	R/W	ADC Conversion Mode Control 0 = Continuous conversion (default) 1 = 1-shot conversion	REG_RST
D[5]	VBUS_ADC_DIS	0	R/W	VBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[4]	IBUS_ADC_DIS	0	R/W	IBUS ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[3]	VBAT_ADC_DIS	0	R/W	VBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[2]	IBAT_ADC_DIS	0	R/W	IBAT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[1]	TDIE_ADC_DIS	0	R/W	TDIE ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST
D[0]	VOUT_ADC_DIS	0	R/W	VOUT ADC Control 0 = Enable conversion (default) 1 = Disable conversion	REG_RST

REG0x14: VBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBUS_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VBUS Data (4mV resolution) MSB<3:0>: 8192mV, 4096mV, 2048mV, 1024mV	REG_RST

REG0x15: VBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBUS_ADC[7:0]	0000 0000	R	Low Byte of the ADC VBUS Data (4mV resolution) LSB<7:0>: 512mV, 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV	REG_RST

REG0x16: IBUS_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBUS_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC IBUS Data (2mA resolution) MSB<3:0>: 4096mA, 2048mA, 1024mA, 512mA	REG_RST

REG0x17: IBUS_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBUS_ADC[7:0]	0000 0000	R	Low Byte of the ADC IBUS Data (2mA resolution) LSB<7:0>: 256mA, 128mA, 64mA, 32mA, 16mA, 8mA, 4mA, 2mA	REG_RST

REGISTER AND DATA (continued)

REG0x18: VBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VBAT_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VBAT Data (2mV resolution) MSB<3:0>: 4096mV, 2048mV, 1024mV, 512mV	REG_RST

REG0x19: VBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VBAT_ADC[7:0]	0000 0000	R	Low Byte of the ADC VBAT Data (2mV resolution) LSB<7:0>: 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV	REG_RST

REG0x1A: IBAT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	IBAT_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit IBAT Data (2.5mA resolution) MSB<3:0>: 5120mA, 2560mA, 1280mA, 640mA	REG_RST

REG0x1B: IBAT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	IBAT_ADC[7:0]	0000 0000	R	Low Byte of ADC IBAT Data (2.5mA resolution) LSB<7:0>: 320mA, 160mA, 80mA, 40mA, 20mA, 10mA, 5mA, 2.5mA	REG_RST

REG0x1C: VOUT_ADC1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:4]	Reserved	0000	R	Reserved	N/A
D[3:0]	VOUT_ADC[11:8]	0000	R	Higher 4 bits of the 12-bit ADC VOUT Data (2mV resolution) MSB<3:0>: 4096mV, 2048mV, 1024mV, 512mV	REG_RST

REG0x1D: VOUT_ADC0 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	VOUT_ADC[7:0]	0000 0000	R	Low Byte of the ADC VOUT Data (2mV resolution) LSB<7:0>: 256mV, 128mV, 64mV, 32mV, 16mV, 8mV, 4mV, 2mV	REG_RST

REG0x1E: TDIE_ADC Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TDIE_ADC[7:0]	0000 0000	R	ADC TDIE Data (8-bit, 1℃ resolution) LSB<7:0>: 128℃, 64℃, 32℃, 16℃, 8℃, 4℃, 2℃, 1℃ T_{DIE} = TDIE_ADC[7:0] × 1℃ - 40℃	REG_RST

REGISTER AND DATA (continued)

REG0x21: BC1.2_FLAG1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VAC_CHG_FLAG	0	RC	Event Flag of VAC Voltage Change 0 = No VAC voltage change event 1 = VAC voltage change event has occurred, namely that VAC present or absent event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[4]	USB_DEVICE_CHG_FLAG	0	RC	Event Flag of USB BC1.2 Device Status Bits Change 0 = No USB_DEVICE_STAT[2:0] bits change event 1 = USB_DEVICE_STAT[2:0] bits change event has occurred. It generates an interrupt on nINT pin if unmasked. Reading this bit will reset it to 0.	N/A
D[3:0]	Reserved	0000	R	Reserved	N/A

REG0x22: BC1.2_MASK1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5]	VAC_CHG_MASK	0	R/W	Mask Interrupt of VAC Voltage Change Event 0 = Interrupt of VAC voltage change event can work. (default) 1 = Mask interrupt of VAC voltage change event. VAC_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin.	N/A
D[4]	USB_DEVICE_CHG_MASK	0	R/W	Mask Interrupt of USB BC1.2 Device Status Bits Change Event 0 = Interrupt of USB_DEVICE_STAT[2:0] bits change event can work. (default) 1 = Mask interrupt of USB_DEVICE_STAT[2:0] bits change event. USB_DEVICE_CHG_FLAG bit sets after the fault, but this bit suppresses the interrupt signal on nINT pin.	N/A
D[3:0]	Reserved	0000	R	Reserved	N/A

REG0x23: DPDM_DETC Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	DPDM_DETC_EN	0	R/W	Enable Bit of DP/DM Detection for Debug 0 = Disabled (default) 1 = Enabled. The DP/DM detection results are updated every 8ms.	N/A
D[6:4]	DP_RSLT[2:0]	000	R	DP Pin Voltage Detection Result Bits 000 = 0V. The DP pin voltage is in the range of 0 to 0.05V. 001 = 0.2V. The DP pin voltage is in the range of 0.15V to 0.25V. 010 = 0.6V. The DP pin voltage is in the range of 0.55V to 0.65V. 011 = 1.8V. The DP pin voltage is in the range of 1.65V to 1.95V. 100 = 3.3V.The DP pin voltage is in the range of 3V to 3.6V. 111 = Error. The DP pin voltage is not listed above. Only valid when DPDM_DETC_EN bit is set to 1.	N/A
D[3]	Reserved	0	R	Reserved	N/A
D[2:0]	DM_RSLT[2:0]	000	R	DM Pin Voltage Detection Result Bits 000 = 0V. The DM pin voltage is in the range of 0 to 0.05V. 001 = 0.2V. The DM pin voltage is in the range of 0.15V to 0.25V. 010 = 0.6V. The DM pin voltage is in the range of 0.55V to 0.65V. 011 = 1.8V. The DM pin voltage is in the range of 1.65V to 1.95V. 100 = 3.3V.The DM pin voltage is in the range of 3V to 3.6V. 111 = Error. The DM pin voltage is not in the ranges listed above. Only valid when DPDM_DETC_EN bit is set to 1.	N/A

REGISTER AND DATA (continued)

REG0x24: BC1.2_CTRL Register [reset = 0x18]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	DCD_TIMER[1:0]	01	R/W	DCD Timer $t_{DCD\_TIMEOUT}$ Setting Bits 00 = The DCD detection is disabled. 01 = 600ms (default) 10 = 900ms 11 = The DCD timer is infinite. The BC1.2 detection cannot step forward until DP voltage is detected below V_{LGC_LOW}.	N/A
D[3]	DCD_DELAY	1	R/W	DCD Detection Delay Time Setting Bit for BC1.2 This is delay time (t_{DCD_DLY}) from when BC1.2 is enabled and VBUS is present to when the DCD detection starts. 0 = 150ms 1 = 300ms (default)	N/A
D[2]	BC_AUTO_EN	0	R/W	BC1.2 Automatic Detection Enable Bit 0 = Disabled (default) 1 = Enabled. When V_{VAC} is present, it will automatically start BC1.2 detection.	N/A
D[1:0]	Reserved	00	R	Reserved	N/A

REG0x25: DPDM_CTRL Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	Reserved	00	R	Reserved	N/A
D[5:4]	DP_DAC[1:0]	00	R/W	DP Pin Output Driver Voltage Setting Bits 00 = HiZ mode (default) 01 = 0V (V_{0P0_VSRC}) 10 = 0.6V (V_{0P6_VSRC}) 11 = 3.3V (V_{3P3_VSRC}) Note: The bit configurations are invalid during BC1.2 detection.	N/A
D[3:2]	DM_DAC[1:0]	00	R/W	DM Pin Output Driver Voltage Setting Bits 00 = HiZ mode (default) 01 = 0V (V_{0P0_VSRC}) 10 = 0.6V (V_{0P6_VSRC}) 11 = 3.3V (V_{3P3_VSRC}) Note: The bit configurations are invalid during BC1.2 detection.	N/A
D[1]	DPDM_DAC_EN	0	R/W	Enable Bit of DP/DM DAC 0 = Disabled (default) 1 = Enabled	N/A
D[0]	Reserved	0	R	Reserved	N/A

REG0x28: USB_STAT Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6:4]	USB_DEVICE_STAT[2:0]	000	R	Status Bit of USB BC1.2 Device Detection 000 = No input 001 = BC1.2 detection in progress 010 = SDP device detected 011 = Non-standard adapter detected 100 = DCP device detected 101 = CDP device detected 110 ~ 111 = Reserved	N/A
D[3:1]	Reserved	000	R	Reserved	N/A
D[0]	DCD_TIMEOUT_FLAG	0	RC	BC1.2 DCD Timeout Fault Flag Bit 0 = No BC1.2 DCD timeout fault 1 = BC1.2 DCD timeout fault has occurred. Generate an interrupt on nINT pin. Read this bit to reset it to 0.	N/A

REGISTER AND DATA (continued)

REG0x50: UFCS_CTL1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:6]	EN_PROTOCOL[1:0]	00	R/W	UFCS Protocol Enable Bits 00 = Disabled UFCS protocol (default) 10 = Enabled UFCS protocol When EN_PROTOCOL[1:0] = 00, the associated register bits are reset to their default value and can be read-only.	REG_RST or rising edge of VAC_ABSENT_ FLAG bit
D[5]	EN_UFCS_HANDSHAKE	0	R/W	UFCS Protocol Handshake Enable Bit 0 = Disable UFCS protocol handshake. The DP and DM pins are high impedance. (default) 1 = Enable UFCS protocol handshake. It enables the pulse train output on the DM line after a DCP source is qualified, and then it enables the DP high level detection circuit. If the initial handshake or ping is failed, master quits UFCS mode, and this bit is automatically cleared to 0.	REG_RST or WDT or EN_ PROTOCOL = 00 or falling edge of SOURCE_ HARDRESET bit or rising edge of HARD_RESET_ FLAG bit
D[4:3]	BAUD_RATE[1:0]	00	R/W	UFCS Communication Baud Rate Setting Bits 00 = 115200bps (default) 01 = 57600bps 10 = 38400bps 11 = reserved	REG_RST or WDT or EN_ PROTOCOL = 00
D[2]	SND	0	R/WC	Master Transmission Start Bit 0 = Not transmission (default) 1 = Start transmission When transmission is completed, this bit is automatically reset to 0.	REG_RST or WDT or EN_ PROTOCOL = 00
D[1]	CABLE_HARDRESET	0	R/WC	Send Reset Command to Cable 0 = Do not send reset command (default). 1 = Send reset command. The DM pin is pulled low for $t_{ResetCable}$. It is automatically reset to 0 after RST CMD is complete.	REG_RST or WDT or EN_ PROTOCOL = 00
D[0]	SOURCE_HARDRESET	0	R/WC	Send Reset Command to Source 0 = Do not send reset command (default). 1 = Send reset command. The DM pin is pulled low for $t_{ResetSource}$. It is automatically reset to 0 after RST CMD is complete, and EN_UFCS_HANDSHAKE bit is also reset to 0.	REG_RST or WDT or EN_ PROTOCOL = 00

REG0x51: UFCS_CTL2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:3]	Reserved	00 0000	R	Reserved	N/A
D[2]	UFCS_DP_PULLUP_EN	0	R/W	Hardware Reset Disable Bit 0 = disabled, (default) 1 = enabled, pull up DP to 3.3V by 50kΩ resistor. Configure this bit before change recipient device address to ignore hardware reset when DP is floating during recipient device changed.	REG_RST or WDT or EN_ PROTOCOL = 00
D[1]	DEV_ADDRESS_ID	0	R/W	Setting Bit of Recipient Device Address ID 0 = Source. The recipient device address ID bits in the message header are 001. (default) 1 = Cable. The recipient device address ID bits in the message header are 011.	REG_RST or WDT or EN_ PROTOCOL = 00
D[0]	EN_DM_HIZ	0	R/W	DM Pin HiZ-Mode Enable Bit 0 = Disable DM pin Hi-Z mode (default) 1 = Enable DM pin Hi-Z mode. During cable detection, the DM pin should be set to Hi-Z mode.	REG_RST or WDT or EN_ PROTOCOL = 00

REGISTER AND DATA (continued)

REG0x52: UFCS_ISR1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_HANDSHAKE_FAIL_FLAG	0	RC	Error Flag of UFCS Failed Handshake with Master 0 = UFCS handshake success or is not complete. 1 = UFCS handshake failed. The device auto resets EN_UFCS_HANDSHAKE bit to 0, and then generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[6]	UFCS_HANDSHAKE_SUCC_FLAG	0	RC	Event Flag of UFCS Successful Handshake with Master 0 = UFCS handshake failed or is not complete. 1 = UFCS handshake success. After a successful initial handshake, this bit is set. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. Then the AP can set the SND bit to start ping transmission.	EN_PROTOCOL = 00
D[5]	BAUD_RATE_ERROR_FLAG	0	RC	Error Flag of UFCS Baud Rate 0 = No baud rate error has occurred. 1 = Baud rate error is out of ±20% tolerance. It discards the received data, and generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[4]	CRC_ERRO_FLAG	0	RC	Error Flag of UFCS Cyclic Redundancy Check (CRC) 0 = No CRC error has occurred. 1 = CRC mismatch occurred in the last received data. It discards the received data, and generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[3]	SENT_PACKET_COMPLETE_FLAG	0	RC	Event Flag of UFCS Data Packet Transmission Complete 0 = Data packet transmission error occurred; or it is not complete. 1 = Data packet transmission complete. After master completes data packet transmission and pulls the DM line high, this flag bit is set. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[2]	DATA_READY_FLAG	0	RC	Received Slave Data is Ready for I²C Read by Master 0 = Not Ready 1 = Ready. After slave completes data packet transmission and pulls the DP line high, if no CRC error occurs, this bit is set. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[1]	HARD_RESET_FLAG	0	RC	Event Flag of UFCS Receiving Hard Reset Signal 0 = Hard reset signal is not received. 1 = Hared reset signal received. The device immediately performs UFCS hard reset by clearing EN_UFCS_HANDSHAKE bit to 0, and then generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[0]	ACK_RECEIVE_TIMEOUT_FLAG	0	RC	Error Flag of Receiving ACK Signal Timeout 0 = No receiving ACK signal timeout fault 1 = Receiving ACK signal timeout fault has occurred. Master did not receive ACK signal in $t_{ACKReceive}$. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00

REGISTER AND DATA (continued)

REG0x53: UFCS_ISR2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	RX_BUFFER_OVERFLOW_FLAG	0	RC	Error Flag of UFCS Receive Buffer Overflow 0 = Receive buffer has not overflowed. 1 = Received buffer has overflowed. It discards the received data, and generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[5]	Reserved	0	R	Reserved	N/A
D[4]	BAUD_RATE_CHANGE_FLAG	0	RC	Event Flag of UFCS Baud Rate Reference Level Change 0 = UFCS baud rate reference level is not changed. 1 = UFCS baud rate reference level is changed. After receiving the ping message and the correct CRC, it will generate an interrupt on nINT pin if unmasked. Read this bit to reset it to 0. Then it will send data with the new baud rate.	EN_PROTOCOL = 00
D[3]	FRAME_RECEIVE_TIMEOUT_FLAG	0	RC	Error Flag of Data Frame Reception Timeout 0 = No data frame reception timeout fault. 1 = Reception timeout fault has occurred in a data frame or between data frames. Master did not receive next data bit in $t_{FrameReceive}$. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[2]	RX_BUFFER_BUSY_FLAG	0	RC	Event Flag of Non-Empty RX_Buffer when Receiving Message 0 = The RX_Buffer is empty. 1 = The RX_Buffer is not empty when receiving a new message. It discards the new message, and generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[1]	MSG_TRANSFER_FAIL_FLAG	0	RC	Error Flag of UFCS Failed Data Transmission 0 = Normal 1 = Data transmission failed. For master's nMsgRetryCount consecutive data transmissions, master has never received slave's ACK signal in $t_{ACKReceive}$. It generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00
D[0]	TRAINING_BYTE_ERROR_FLAG	0	RC	Error Flag of UFCS Receiving Training Byte 0 = No training byte error has occurred. 1 = Training byte error occurred in the last received data. The error includes data error or baud rate error. It discards the received data, and generates an interrupt on nINT pin if unmasked. Read this bit to reset it to 0.	EN_PROTOCOL = 00

REGISTER AND DATA (continued)

REG0x54: UFCS_MASK1 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	UFCS_HANDSHAKE_FAIL_MASK	0	R/W	Mask UFCS Failed Handshake Interrupt 0 = UFCS failed handshake interrupt can work (default). 1 = Mask UFCS failed handshake interrupt. UFCS_HANDSHAKE_FAIL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[6]	UFCS_HANDSHAKE_SUCC_MASK	0	R/W	Mask UFCS Successful Handshake Interrupt 0 = UFCS successful handshake interrupt can work (default). 1 = Mask UFCS successful handshake interrupt. UFCS_HANDSHAKE_SUCC_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[5]	BAUD_RATE_ERROR_MASK	0	R/W	Mask UFCS Baud Rate Error Interrupt 0 = Baud rate error interrupt can work (default). 1 = Mask baud rate error interrupt. BAUD_RATE_ERROR_ FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[4]	CRC_ERRO_MASK	0	R/W	Mask UFCS Cyclic Redundancy Check (CRC) Error Interrupt 0 = CRC error interrupt can work (default). 1 = Mask CRC error interrupt. CRC_ERRO_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[3]	SENT_PACKET_COMPLETE_MASK	0	R/W	Mask UFCS Data Packet Transmission Complete Interrupt 0 = Data packet transmission complete interrupt can work (default). 1 = Mask data packet transmission complete interrupt. SENT_PACKET_COMPLETE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[2]	DATA_READY_MASK	0	R/W	Mask Received Slave Data Ready Interrupt 0 = Received slave data ready interrupt can work (default). 1 = Mask received slave data ready interrupt. DATA_READY_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[1]	HARD_RESET_MASK	0	R/W	Mask UFCS Receiving Hard Reset Signal Interrupt 0 = Receiving hard reset signal interrupt can work (default). 1 = Mask receiving hared reset signal interrupt. HARD_RESET_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[0]	ACK_RECEIVE_TIMEOUT_MASK	0	R/W	Mask Receiving ACK Signal Timeout Error Interrupt 0 = Receiving ACK signal timeout error interrupt can work (default). 1 = Mask receiving ACK signal timeout error interrupt. ACK_RECEIVE_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00

REGISTER AND DATA (continued)

REG0x55: UFCS_MASK2 Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7]	Reserved	0	R	Reserved	N/A
D[6]	RX_BUFFER_OVERFLOW_MASK	0	R/W	Mask UFCS Receive Buffer Overflow Interrupt 0 = UFCS receive buffer overflow interrupt can work (default). 1 = Mask UFCS receive buffer overflow interrupt. RX_BUFFER_OVERFLOW_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[5]	Reserved	0	R	Reserved	N/A
D[4]	BAUD_RATE_CHANGE_MASK	0	R/W	Mask UFCS Baud Rate Reference Level Change Interrupt 0 = UFCS baud rate reference level change interrupt can work (default). 1 = Mask UFCS baud rate reference level change interrupt. BAUD_RATE_CHANGE_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[3]	FRAME_RECEIVE_TIMEOUT_MASK	0	R/W	Mask Data Frame Reception Timeout Interrupt 0 = Data frame reception timeout interrupt can work (default). 1 = Mask data frame reception timeout interrupt. FRAME_RECEIVE_TIMEOUT_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[2]	RX_BUFFER_BUSY_MASK	0	R/W	Mask UFCS Non-Empty RX_Buffer Interrupt 0 = UFCS non-empty RX_buffer interrupt can work (default). 1 = Mask UFCS non-empty RX_buffer interrupt. RX_BUFFER_BUSY_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[1]	MSG_TRANSFER_FAIL_MASK	0	R/W	Mask UFCS Failed Data Transmission Interrupt 0 = UFCS failed data transmission interrupt can work (default). 1 = Mask UFCS failed data transmission interrupt. MSG_TRANSFER_FAIL_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00
D[0]	TRAINING_BYTE_ERROR_MASK	0	R/W	Mask UFCS Receiving Training Byte Error Interrupt 0 = Training byte error interrupt can work (default). 1 = Mask training byte error interrupt. TRAINING_BYTE_ERROR_FLAG bit is set after the event, but the interrupt signal is not generated.	REG_RST or EN_PROTOCOL = 00

REG0x56: DURATION_PER_BIT Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	DURATION_PER_BIT[7:0]	0000 0000	R	Slave Baud Rate Detection Result (250ns Resolution) LSB<7:0>: 32000ns, 16000ns, 8000ns, 4000ns, 2000ns, 1000ns, 500ns, 250ns t_{BAUD} = DURATION_PER_BIT[7:0] × 250ns	REG_RST or WDT or EN_PROTOCOL = 00

REG0x57: TX_LENGTH Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	TX_LENGTH[7:0]	0000 0000	R/WC	UFCS Transmitter Length Configuration Register The length is the number of bytes in the transmitted data packet, excluding training byte and CRC byte. It is automatically reset to 0000 0000 when transmission is completed.	REG_RST or WDT or EN_PROTOCOL = 00

REGISTER AND DATA (continued)

REG0x58 ~ REG0x96: TX_BUFFER Registers [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
REG0x58[7:0]	TX_BUFFER_0[7:0]	0000 0000	R/WC	TX_BUFFER is a 63-byte transmitted buffer. It includes all bytes in the transmitted data packet except the training byte and CRC byte. All of the 63-byte data are automatically reset to 0000 0000 when transmission is completed.	REG_RST or WDT or EN_PROTOCOL = 00
REG0x59[7:0]	TX_BUFFER_1[7:0]	0000 0000	R/WC		
……	……	……	……		
REG0x96[7:0]	TX_BUFFER_62[7:0]	0000 0000	R/WC		

REG0x97: RX_LENGTH Register [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
D[7:0]	RX_LENGTH[7:0]	0000 0000	RC	UFCS Receiver Data Length Register The length is the number of bytes in the received data packet, excluding training byte and CRC byte. Read these bits to reset them to 0000 0000.	REG_RST or WDT or EN_PROTOCOL = 00 or one of the rising edges of BAUD_RATE_ERROR_FLAG, CRC_ERRO_FLAG, RX_BUFFER_OVERFLOW_FLAG and TRAINING_BYTE_ERROR_FLAG bits

REG0x98 ~ REG0xD7: RX_BUFFER Registers [reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION	RESET BY
REG0x98[7:0]	RX_BUFFER_0[7:0]	0000 0000	RC	RX_BUFFER is a 64-byte received buffer. It includes all bytes in the received data packet except the training byte. All of the 64-byte data are automatically reset to 0000 0000 when it is read.	REG_RST or WDT or EN_PROTOCOL = 00 or one of the rising edges of BAUD_RATE_ERROR_FLAG, CRC_ERRO_FLAG, RX_BUFFER_OVERFLOW_FLAG and TRAINING_BYTE_ERROR_FLAG bits
REG0x99[7:0]	RX_BUFFER_1[7:0]	0000 0000	RC		
……	……	……	……		
REG0xD7[7:0]	RX_BUFFER_63[7:0]	0000 0000	RC		

DETAILED DESCRIPTION

The SGM41600T is an efficient 8A battery charger that operates in voltage divider mode (switched-capacitor charge pump) or in bypass mode. A two-channel switched-capacitor core is integrated in the device to minimize the ripples and improve efficiency in the voltage divider mode. A FET control output for protection, a reverse blocking NFET and all other necessary protection features for safe charging are included. A high speed 12-bit ADC converter is also included to provide bus voltage, bus current, battery voltage, battery current, output voltage and die temperature information for the charge management host via I²C serial interface.

Charge-Pump Voltage Divider Mode

The charge-pump voltage divider mode operates with a fixed 50% duty cycle. The basic principle of operation is shown in Figure 4. In period 1, Q1 and Q3 are tuned on and V_{PMID} charges the C_{FLY} and the battery (in series) such that:

$$V_{CFLY} = V_{PMID} - V_{BAT} \quad (1)$$

In period 2, Q2 and Q4 are turned on and C_{FLY} appears in parallel with the battery:

$$V_{CFLY} = V_{BAT} \quad (2)$$

Ignoring the small fluctuation of the capacitor and battery voltages in period 1 and 2 in steady state operation, Equation 1 and 2 can be combined to calculate capacitor voltage:

$$V_{CFLY} = V_{BAT} = V_{PMID}/2 \quad (3)$$

Ignoring small energy loss in each switching period, the input and output cycle-average powers are equal. Therefore,

$$V_{PMID} \times I_{BUS} = V_{BAT} \times I_{BAT} \quad (4)$$

or

$$I_{BUS} = I_{BAT}/2 \quad (5)$$

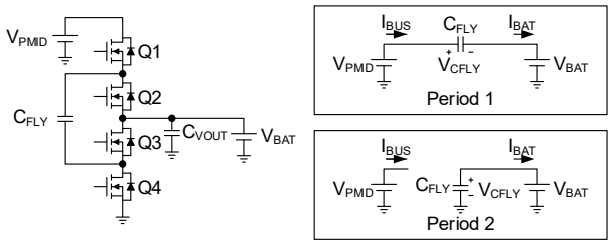


Figure 4. Voltage Divider Charger Operating Principle

Assuming no charge leakage path and considering R_{EFF} as the effective input to output resistance (due to the switch on-resistances and C_{FLY} losses), the divider can be modeled as shown in Figure 5. Using this model, the output voltage is half of the input voltage under no load conditions as explained before. The SGM41600T has two channels of such architecture operating at f_{SW} frequency with 180° phase difference. Each channel provides $I_{VOUT}/2$ at the VOUT node, so:

$$V_{VOUT} = ½V_{PMID} - ½R_{EFF} \times I_{VOUT} \quad (6)$$

At low switching frequencies, the capacitor charge sharing losses are dominant and $R_{EFF} \approx 1/(4f_{SW}C_{FLY})$. As frequency increases, R_{EFF} finally approaches (R_{DS_QCH} + R_{DS_QDH} + R_{DS_QCL} + R_{DS_QDL})/2.

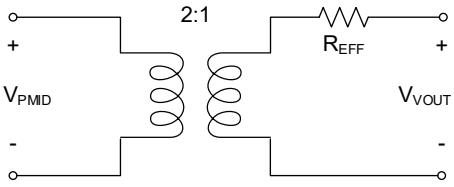


Figure 5. Model of Voltage Divider

The two-channel interleaved operation ensures a smooth input current and simplifies the noise filtering. The VOUT ripple can be estimated by the first order approximation of C_{FLY} voltage drop due to the discharge in the half period, plus the discharge drop during the short dead time (15ns, TYP).

Selecting high quality C_{FLY} capacitors and proper switching frequency are the key factors for a well performing capacitor voltage divider. Switching frequency selection is a trade-off between efficiency and capacitor size. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}). An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

Bypass Mode

The SGM41600T is designed to operate in bypass mode when V_{VBUS} is close to the V_{VOUT}. When such valid voltage is present on VBUS, the device enters bypass mode and all switches between VBUS and VOUT are fully turned on while the other switches are kept off. When V_{VBUS} is near V_{VOUT}, the bypass mode offers the best efficiency and the device is capable of sourcing up to 5.6A.

The output voltage is close to the V_{VBUS} minus a voltage drop caused by the on-resistances of the RBFET plus the two high-side switches of the two channels in parallel:

$$R_{EFF}(\text{Bypass mode}) \approx R_{DS\_QRB} + (R_{DS\_QCH1} + R_{DS\_QDH1}) \| (R_{DS\_QCH2} + R_{DS\_QDH2}) \quad (7)$$

where R_{DS_QXX} is the on-resistance of the switch Q_{XX}.

DETAILED DESCRIPTION (continued)

Charge System

The SGM41600T is a slave charger device and needs a host. The host must set up all protection functions and disable the main charger before enabling the SGM41600T. The host must monitor the nINT interrupts especially during high current charging. It must also communicate with the wall adapter to control the charge current.

Figure 6 shows the block diagram of a charge system using the SGM41600T along with other devices. In this system, the SGM41600T can be used to detect the adapter by USB BC1.2 or UFCS (Universal Fast Charging Specification), and the PD controller is used to communicate with adapter by PD protocol. When the smart wall adapter is detected, the AP unit controls the switching charger (SGM41516) that powers the load system and the switched capacitor charger (SGM41600T) that provides high current charging. The communication between those devices is through I²C interface.

A typical charge profile for a high-capacity battery using switching charger and switched capacitor charger together is shown in Figure 7. During the trickle charge and pre-charge, the charging is controlled by the switching charger. Once the battery voltage reaches 3V, the adapter can negotiate for a higher bus voltage and enable the SGM41600T for charging (bypass or voltage divider mode). Once the battery voltage reaches the V_{BAT_REG} point, the SGM41600T provides feedback to the adapter to reduce the current. This will eventually reduce and ramp down the bus current below $I_{BUS\_UCP\_F}$.

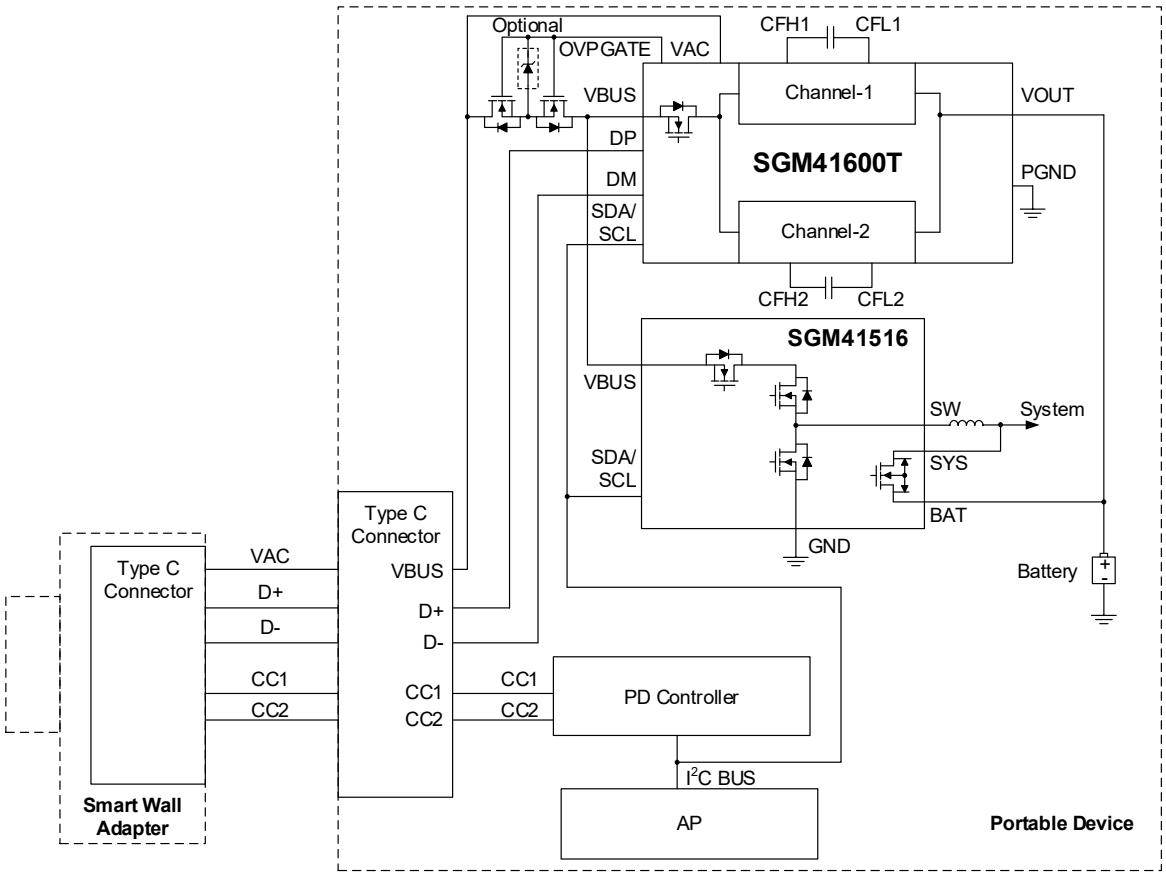


Figure 6. Simplified Charge System

DETAILED DESCRIPTION (continued)

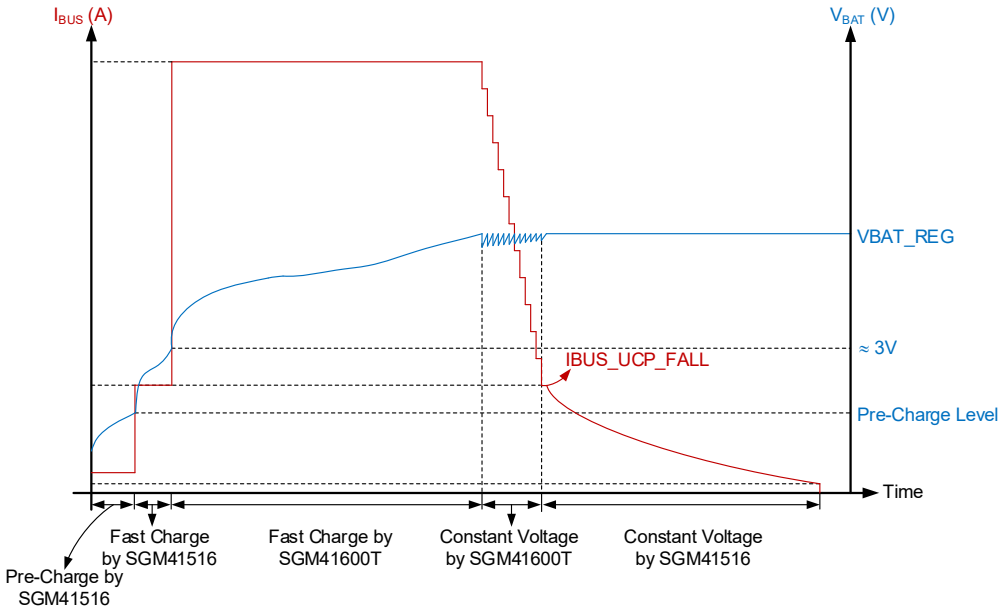


Figure 7. SGM41600T System Charging Profile

Startup Sequence

The SGM41600T is powered from the greater of VAC or VOUT (VAC is used as sense input for adapter voltage as well). The internal watchdog timer is enabled by default and if no I²C read or write occurs before its expiry, the ADC_EN and CHG_MODE[2:0] bits are reset to their default values and after an initial 8ms power-up time, a nINT pulse is triggered to show watchdog timeout. The host should not attempt to read or write before this initial nINT signal.

The device does not start charging after powered up, because by default the charger is disabled but the ADC can be enabled and the host can read the system parameters before enabling charge. The charge can be enabled only if V_{VBUS} > $V_{BUS\_PRESENT\_R}$ and V_{VOUT} > $V_{OUT\_PRESENT\_R}$.

Device Power-Up from Battery without Input Source

To reduce the quiescent current and maximize the battery run time when it is the only available source, the REGN LDO and most of the sensing circuits are turned off, except VAC_PRESENT, BUS_INSERT and VOUT_INSERT functions. When the BUS_PDN_EN bit is set, the external OVPFET is turned off, and VBUS pull-down R_{PDN_VBUS} is activated to help discharging VBUS after a hot-plug event. This will keep the device in low quiescent current mode even after an input source is plugged in.

Device Power-Up from Input Source

When an input source is plugged-in and the V_{VBUS} > $V_{BUS\_PRESENT\_R}$ condition is valid, the host must initialize all protections to the desired thresholds before enabling charge. The protection thresholds that need to be set are VAC_OVP, VBUS_LO, VBUS_HI, VBUS_OVP, IBUS_OCP, IBUS_UCP, VBAT_OVP, IBAT_OCP, VBAT_REG, IBAT_REG, and VDRP_OVP. If one of the protection trigger conditions is met, the charger stops switching. It will also be turned off the external OVPFET when VAC_OVP or VBUS_SC event occurs.

After setting protections, the VBUS voltage is checked to be between 2 × V_{BUS_LO} × V_{VOUT} and 2 × V_{BUS_HI} × V_{VOUT} to allow voltage divider mode operation, or between V_{BUS_LO} × V_{VOUT} and V_{BUS_HI} × V_{VOUT} for bypass mode operation. Charging is enabled and current flows into the battery when the host sets bypass or voltage divider mode by writing 001 or 010 in the CHG_MODE[2:0] bits respectively. Then raising the VBUS voltage will increase the battery charge current. When the converter is on, any command to change the charge mode is ignored. To do so, the charging must be disabled first, and then the charge mode can be changed by I²C serial interface.

DETAILED DESCRIPTION (continued)

ADC

The SGM41600T integrates a fast 6-channel, 12-bit ADC converter to monitor input/output currents and voltages and the temperature of the device. The ADC is controlled by the ADC_CTRL register. Setting the ADC_EN bit to 1 enables the ADC. This bit can be used to turn off the ADC and save power when it is not needed. The ADC_RATE bit allows choosing continuous conversion or 1-shot conversion mode. The ADC operates independent of the faults, unless the host sets the ADC_EN bit to 0.

The ADC can operate if V_{VAC} > $V_{VAC\_PRESENT\_R}$ or V_{VBUS} > $V_{BUS\_PRESENT\_R}$ or V_{VOUT} > 2.8V condition is valid. Otherwise, the ADC conversion is postponed until one of them is satisfied. The ADC readings are valid only for DC values and not for transients.

By default, all ADC channels are converted in continuous conversion mode except the channels disabled by the ADC_CTRL register. If the 1-shot conversion mode is selected, the ADC_DONE_FLAG bit is set to 1 when all channels are converted, then the ADC_EN bit is reset to 0. In the continuous conversion mode, the ADC_DONE_FLAG bit is set to 0.

nINT Pin, Flag and Mask Bits

The nINT pin is an open-drain output and must be pulled up to a logic high rail. It is pulled low with a duration of t_{INT} to notify the host when it is triggered by an event. See the register map for all event flag and control bits.

When an event occurs, a nINT signal is sent to the host and the corresponding flag bit is set to 1. The flag bit can be read and reset only after the fault is cleared. The nINT signal is not re-sent if an event is still present after the flag bit is read, unless another kind of event occurs. If an event mask bit is set, that event will not send nINT signal, but the flag bit is still updated independent of the mask bit.

The nINT pulse generation behavior examples are shown in Figure 8.

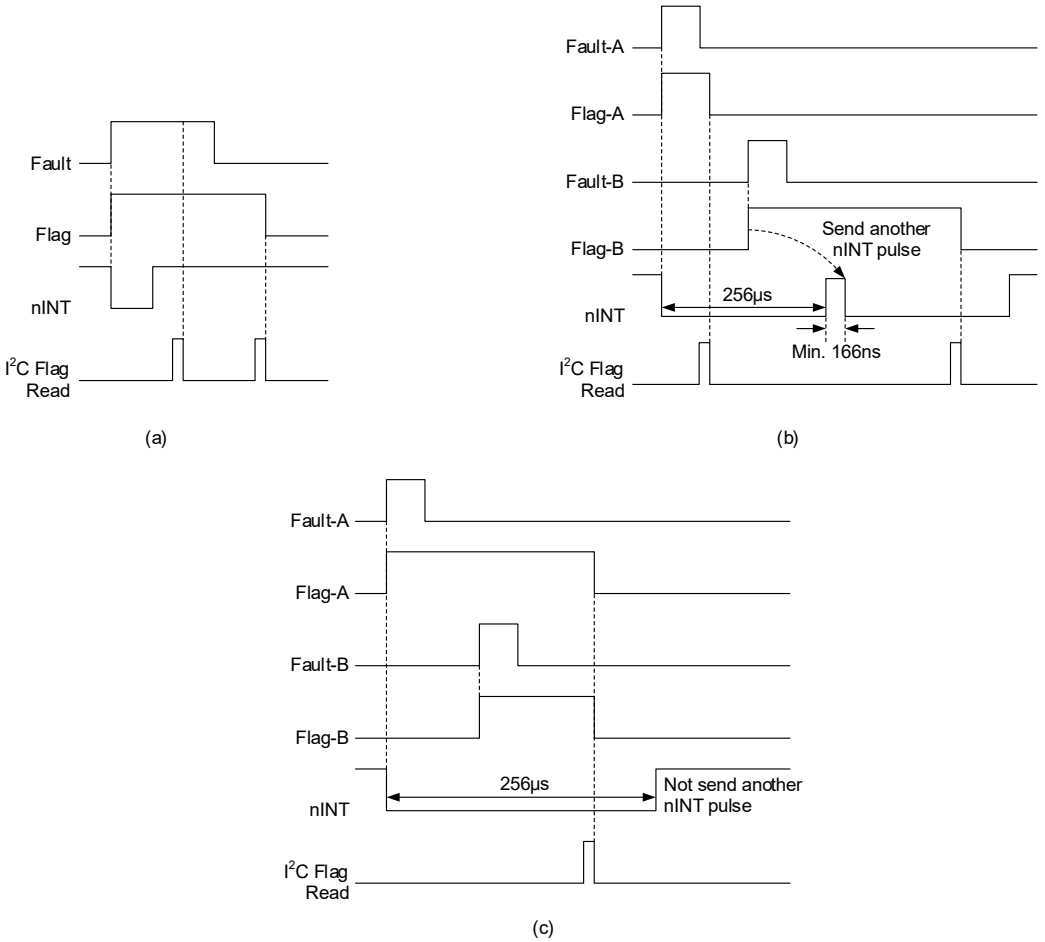


Figure 8. nINT Pulse Generation Behavior Examples

DETAILED DESCRIPTION (continued)

VAC Over-Voltage Protection (VAC_OVP)

The SGM41600T monitors the adapter voltage on the VAC pin to control the external OVPFET using OVPGATE output. The VAC over-voltage protection circuit is powered by VAC and is enabled if V_{VAC} rises above $V_{VAC\_PRESENT\_R}$. If V_{VAC} is above $V_{VAC\_PRESENT\_R}$ for at least $t_{VAC\_IN\_DEG}$ time, a 4.8V gate voltage is sent to the OVPGATE output to turn on the external OVPFET. If the V_{VAC} reaches the V_{VAC_OVP} threshold, the gate voltage starts to drop and eventually the OVPFET is fully turned off. Figure 9 shows the VAC_OVP and OVPGATE operation timings. The V_{VAC_OVP} threshold can be set by I²C serial interface. The adapter voltage must never exceed the absolute maximum rating of the VAC pin and the external OVPFET.

Input Short-Circuit Protection (VBUS_SC)

The VBUS_SC function monitors the VBUS pin for short-circuit. This function is enabled if the external OVPFET is turned on or if V_{VBUS} rises above $V_{BUS\_PRESENT\_R}$. If the V_{VBUS} falls below 2.7V, the OVPFET is turned off, and charging is stopped. CHG_MODE[2:0] bits are reset to 000 (disable). Also, BUS_ABSENT_FLAG bit is set to 1, and a nINT pulse is asserted. The device will wait for 512ms before automatically re-enabling and initiating startup sequence.

During charging, if V_{VBUS} is less than 1.9 × V_{VOUT} in divider mode or 0.95 × V_{VOUT} in bypass mode, or if the Q_{RB} reverse current rises above 0.5A, the Q_{RB} and OVPFET are turned off, and charging is stopped. CHG_MODE[2:0] bits are reset to 000 (disable). Also, VBUS_ABSENT_FLAG bit is set to 1, and a nINT pulse is asserted.

VBUS Charge Voltage Range (VBUS_LO & VBUS_HI)

The VBUS_LO and VBUS_HI functions are included to avoid problems due to wrong VBUS setting for charging. If V_{VBUS} is less than (V_{VOUT} × V_{BUS_LO} × 2) or above (V_{VOUT} × V_{BUS_HI} × 2), the device remains in charge initiation operation if the voltage divider mode is selected. If the bypass mode is selected, the range is from (V_{VOUT} × V_{BUS_LO}) to (V_{VOUT} × V_{BUS_HI}). Charging will start once V_{VBUS} is within the charge range. VBUS_LO and VBUS_HI functions are kept enabled after soft-start timer timeout. The VBUS_LO and VBUS_HI thresholds can be set by I²C serial interface.

Input, OUTPUT and Battery Over-Voltage Protection (VBUS_OVP, VBUS_OVP_PK, VOUT_OVP and VBAT_OVP)

The VBUS_OVP, VBUS_OVP_PK, VOUT_OVP and VBAT_OVP functions detect input and output charge voltage conditions. If either input or output voltage is higher than the protection threshold, the charger is turned off and CHG_MODE[2:0] bits are reset to 000 (disable). The VBUS_OVP and VBUS_OVP_PK functions monitor VBUS pin voltage. The VOUT_OVP function monitors VOUT pin voltage. The VBAT_OVP uses BATP and BATN/SRP remote sense pins to monitor differential voltage between the battery terminals. To minimize the risk of battery terminal short in the manufacturing process, a series 100Ω resistor on the BATP pin is required. The VBUS_OVP, VOUT_OVP and VBAT_OVP thresholds can be set by I²C serial interface.

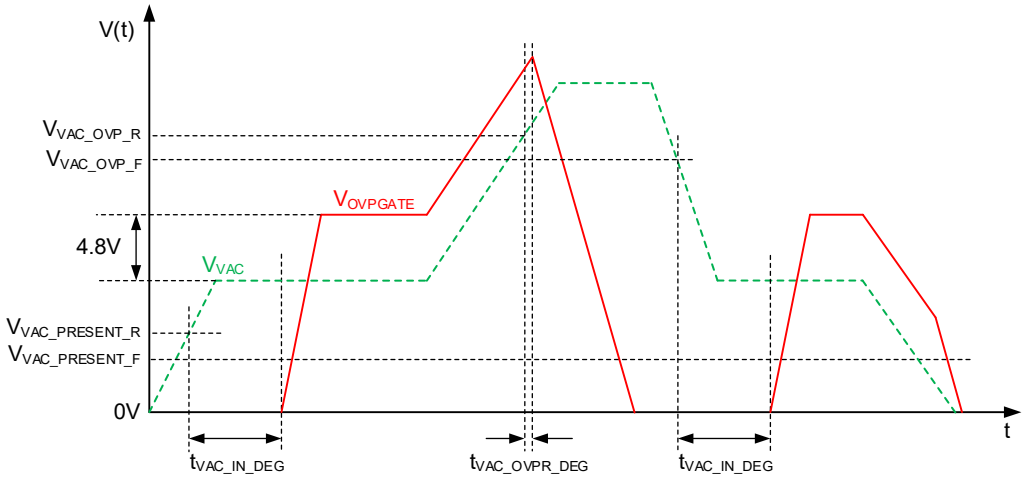


Figure 9. OVPGATE Operation Timing

DETAILED DESCRIPTION (continued)

Input and Battery Over-Current Protection (IBUS_OCP and IBAT_OCP)

The IBUS_OCP function monitors the input current via Q_{RB}. If CHG_MODE[2:0] bits are set to enable charge, the Q_{RB} is turned on and the IBUS_OCP function starts detecting the input current. If the I_{BUS} reaches I_{BUS_OCP} threshold, the device stops charging and resets CHG_MODE[2:0] bits to 000 (disable). The battery current is monitored by the voltage across an external series shunt resistor. This differential voltage is measured between BATN/SRP and SRN pins. If I_{BAT_OCP} threshold is reached, the device stops charging and resets CHG_MODE[2:0] bits to 000 (disable). The IBUS_OCP and IBAT_OCP thresholds can be set by I²C serial interface.

Input Under-Current Protection (IBUS_UCP)

The IBUS_UCP function detects the input current via Q_{RB} during forward charging. After charging is started, the $t_{IBUS\_UCP\_BLK}$ timer is enabled and I_{BUS} current is compared with $I_{BUS\_UCP\_R}$. If I_{BUS} cannot exceed $I_{BUS\_UCP\_R}$ within $t_{IBUS\_UCP\_BLK}$, the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). If I_{BUS} exceeds $I_{BUS\_UCP\_R}$ when $t_{IBUS\_UCP\_BLK}$ times out, from then on, if I_{BUS} falls below the $I_{BUS\_UCP\_F}$ threshold, the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The $t_{IBUS\_UCP\_BLK}$ timer can be set by I²C serial interface.

VOUT Short-Circuit Protection (VOUT_SC)

The VOUT_SC function monitors the VOUT pin for short-circuit. This function is enabled during charging. If V_{VOUT} falls below 2.7V when the voltage divider mode is selected, the charger is turned off and CHG_MODE[2:0] bits are reset to 000 (disable). Also, the PIN_DIAG_FLAG bit is set to 1, and a nINT pulse is generated.

CFLY Short-Circuit Protection (CFLY_SC)

The CFLY_SC function identifies the health of flying capacitors before and during voltage divider switching (charging). The device initialization process is started after CHG_MODE[2:0] bits are set to 010. When V_{VBUS} is in the charge range, the flying capacitors (C_{FLY}) in both channels are pre-charged. A CFLY short-circuit is detected if they cannot be charged, and the voltage between V_{CFHx} and V_{CFLx} remains below (V_{VOUT} - 1.2V). If so, the initialization process is stopped and CHG_MODE[2:0] bits are reset to 000 (disable). Even if C_{FLY} capacitors pass the short-circuit test in the initialization process, the CFLY_SC function remains active and whenever a V_{CFLY} voltage falls below (V_{VOUT} - 1.2V), the charger is turned off and CHG_MODE[2:0] bits are reset to 000 (disable). The PIN_DIAG_FLAG bit is set to 1 and a nINT pulse is generated as well. During a CFLY_SC event, other protection events such as IBUS_OCP, VBAT_OVP or PEAK_OCP may occur.

A CFLY discharge circuit is activated before the internal RBFET (Q_{RB}) is turned on if $V_{VBUS} > V_{BUS\_PRESENT\_R}$ to prevent over-current stress at the start of charging.

Converter Peak Over-Current Protection (PEAK_OCP)

The PEAK_OCP function monitors the converter switch operating currents. If the Q_{CHx} or Q_{DLx} current reaches switch OCP threshold during charging, the PEAK_OCP_FLAG bit is set to 1 and a nINT pulse is generated, the charging is stopped and CHG_MODE[2:0] bits are reset to 000 (disable).

Regulation Feature

The SGM41600T has VBAT_REG and IBAT_REG regulation functions to regulate the battery voltage and current for a short period before the system can re-adjust the conditions such that these functions can be disabled. The regulation thresholds can be set by I²C serial interface.

The VBAT_REG function monitors the differential voltage between BATP and BATN/SRP pins and if the battery voltage is above the V_{BAT_REG} threshold, the OVPGATE voltage is controlled to regulate the battery voltage.

The VBAT_REG_FLAG bit is also set to 1, and a nINT pulse is generated. Then the host can negotiate with the adapter to reduce the current. This will gradually reduce the current until the bus current falls to the $I_{BUS\_UCP\_F}$ and charging will end.

Similarly, the IBAT_REG function monitors the differential voltage between BATN/SRP and SRN pins to find the battery current and if the I_{BAT_REG} threshold is exceeded, the OVPGATE voltage is controlled (reduced) to regulate the charge current.

If one of the regulation functions is triggered and persist for 650ms when REG_TIMEOUT_DIS bit is set to 0, the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The system should adjust the charging conditions to prevent the battery voltage and current regulation for more than 650ms (or prevent triggering of the VDRP_OVP).

DETAILED DESCRIPTION (continued)

Dropout Over-Voltage Protection (VDRP_OVP)

When VBAT_REG or IBAT_REG is active, a large voltage drop may appear on the external OVPFET and cause excessive power loss and heat. To avoid that, the VDRP_OVP function monitors the voltage drop between VAC and VBUS pins. If it is higher than V_{DRP_OVP} threshold with $t_{DRP\_OVP\_DEG}$ deglitch time (set by VDRP_OVP_DEG bit in REG0x05), the charging will be stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The V_{DRP_OVP} threshold and $t_{DRP\_OVP\_DEG}$ deglitch time can be programmed by I^2C serial interface.

TDIE Over-Temperature Protection (TDIE_OTP)

The TDIE_OTP function prevents charging in over-temperature condition. The die temperature is monitored and if the +150℃ threshold is reached, the charging is stopped and CHG_MODE[2:0] bits are reset to 000 (disable). The startup sequence cannot be initiated again until the die temperature falls down to +130℃.

APPLICATION INFORMATION

Input Capacitors (C_{VAC}, C_{VBUS} and C_{PMID})

Input capacitors are selected by considering two main factors:

1. Adequate voltage margin above maximum surge voltage;
2. Not too large voltage margin in order to limit the peak currents drawn from the source and reduce the input noise.

For C_{VAC}, use at least a 1μF low ESR bypass ceramic capacitor placed close to the VAC and PGND pins. The C_{VBUS} and C_{PMID} are determined by the minimum capacitance needed for stable operation and the required ESR to minimize the voltage ripple and load step transients. Typically, 10μF or larger X5R ceramic capacitors are sufficient for C_{VBUS} and C_{PMID}. Consider the DC bias derating of the ceramic capacitors. The X5R and X7R capacitors are relatively stable against DC bias and high temperature. Note that the bias effect is more severe with smaller package sizes, so choose the largest affordable package size. Also consider a large margin for the voltage rating for the worst-case transient input voltages.

External OVPFET (Q_{OVP})

The maximum recommended V_{VBUS} input range is 11.5V. If the supplied VAC voltage is above 11.5V, or if regulation functions are needed during load or wall adapter transients, an external OVPFET is recommended between the USB connector and the SGM41600T. Choose a low R_{DSON} MOSFET for the OVPFET to minimize power losses.

Flying Capacitors (C_{FLY})

For selection of the C_{FLY} capacitors, the current rating, ESR and the bias voltage derating are critical parameters. The C_{FLY} capacitors are biased to half of the input voltage. For a trade-off between efficiency and power density, set the C_{FLY} voltage ripple to the 2% of the V_{VOUT} as a good starting point. The C_{FLY} for each channel can be calculated by Equation 8:

$$C_{FLY} = \frac{I_{BAT}}{4 f_{SW} V_{CFLY\_RPP}} = \frac{I_{BAT}}{8\% f_{SW} V_{VOUT}} \quad (8)$$

where I_{BAT} is the charging current and V_{CFLY_RPP} is the peak-to-peak voltage ripple of the C_{FLY}.

Choosing a too small capacitor for C_{FLY} results in lower efficiency and high output voltage/current ripples. However, choosing a too large C_{FLY} only provides minor efficiency and output ripple improvements.

The default switching frequency is f_{SW} = 500kHz. It can be adjusted by FSW_SET[2:0] bits in REG0x01. Lower frequency increases efficiency by reducing switching losses but requires larger capacitance to maintain low output ripple and low output impedance (R_{EFF}). An optimum switching frequency can be found for any selected C_{FLY} capacitor to minimize losses.

Output Capacitor (C_{VOUT})

C_{VOUT} selection criteria are similar to the C_{FLY} capacitor. Larger C_{VOUT} value results in less output voltage ripple, but due to the dual-channel operation, the C_{VOUT} RMS current is much smaller than C_{FLY}, so smaller capacitance value can be chosen for C_{VOUT} as given in Equation 9:

$$C_{VOUT} = \frac{I_{BAT} \times t_{DEAD}}{0.5 \times V_{VOUT\_RPP}} \quad (9)$$

where t_{DEAD} is the dead time between the two channels and V_{VOUT_RPP} is the peak-to-peak output voltage ripple and is typically set to the 2% of V_{OUT}.

C_{VOUT} is biased to the battery voltage and its nominal value should be derated for battery voltage DC bias. Typically two 10μF, X5R or better grade ceramic capacitors placed close to the VOUT and PGND pins provide stable performance.

External Bootstrap Capacitor (C_{BST})

The bootstrap capacitors provide the gate driver supply voltage for the internal high-side switches (Q_{CH1} and Q_{CH2}). Place a 100nF low ESR ceramic capacitor between BST1 and CFH1 pins and another one between BST2 and CFH2 pins.

PCB Layout Guidelines

A good PCB layout is critical for stable operation of the SGM41600T. Follow these guidelines for the best results:

1. Use short and wide traces for VBUS as it carries high current.
2. Minimize connectors wherever possible. Connector losses are significant especially at high currents.
3. Use solid thermal vias for better thermal relief.
4. Bypass VBUS, PMID and VOUT pins to PGND with ceramic capacitors as close to the device pins as possible.
5. Place C_{FLY} capacitors as close as possible to the device with small pad areas to reduce switching noise and EMI.
6. Connect or reference all quiet signals to the AGND pin.
7. Connect and reference all power signals to the PGND pins (preferably the nearest ones).
8. Try not to interrupt or break the power planes by signal traces.
9. Connecting an external resistor to VAC can effectively reduce the impact of surge on VAC.

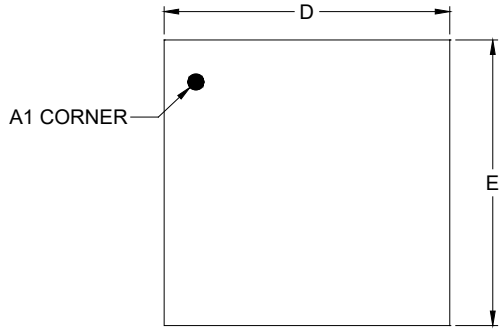
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

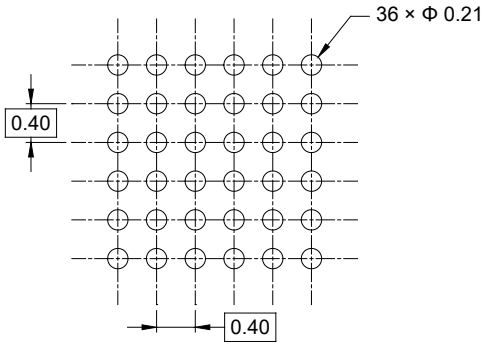
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

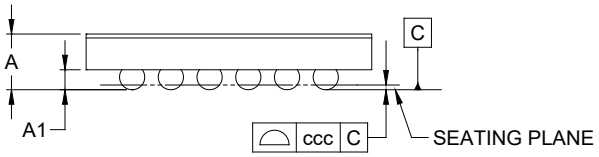
WLCSP-2.95×2.95-36B



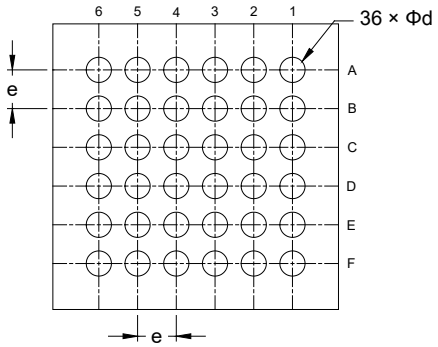
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



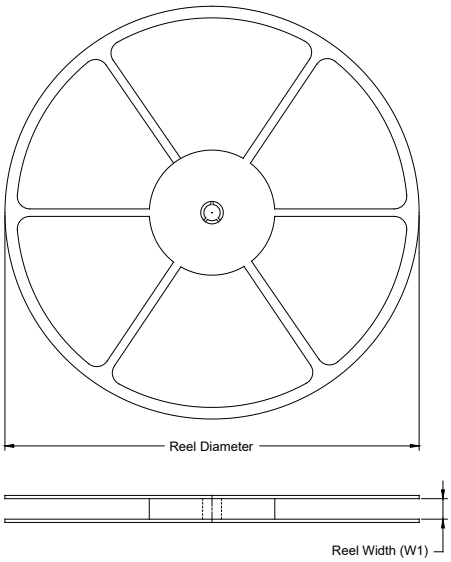
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.613
A1	0.186	-	0.226
D	2.920	-	2.980
E	2.920	-	2.980
d	0.230	-	0.290
e	0.400 BSC		
ccc	0.050		

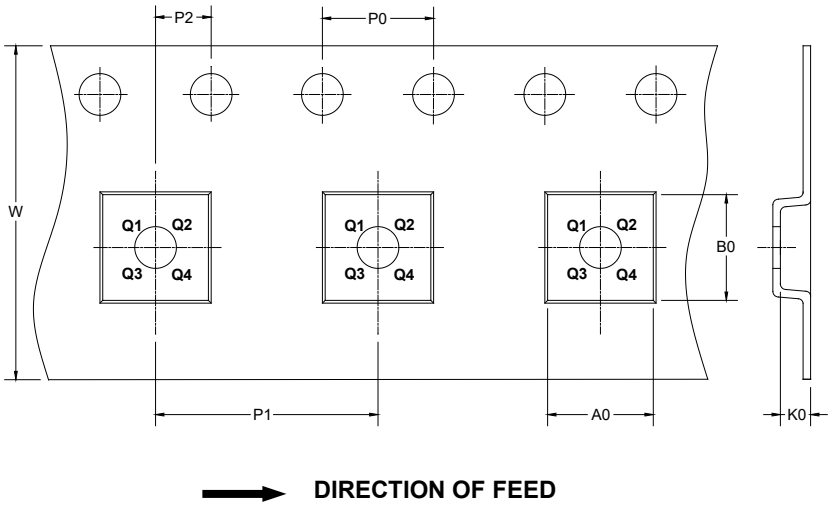
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



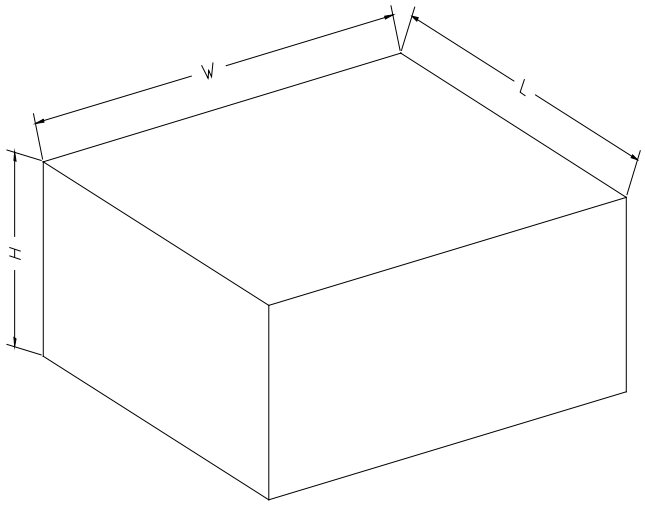
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-2.95×2.95-36B	7"	9.0	3.30	3.30	0.75	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002