SGM61006
600mA, 1.8V to 5.5V Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61006 is a high efficiency and miniature size synchronous Buck converter for low input voltage applications. This high frequency device does not need external compensation and is a perfect solution for compact designs. The 1.8V to 5.5V input voltage range is suitable for kinds of battery applications. The minimum input voltage can be as low as 1.6V after startup. It operates in PWM mode at heavy loads and automatically enters power-save mode (PSM) at light loads to maintain its high efficiency.

With its adaptive hysteresis and pseudo-constant on-time control (AHP-COT) architecture, the load transient performance is excellent and the output voltage regulation accuracy is achieved. The device is available in a Green WLCSP-0.9×1.3-6B-A package.

FEATURES

- **1.8V to 5.5V Input Voltage Range**
- **0.5V to V_{IN} Adjustable Output Voltage**
- **AHP-COT Architecture for Fast Transient Regulation**
- **3.5MHz Switching Frequency**
- **Up to 90% Efficiency**
- **Low R_{DSON} MOSFET Switches (100mΩ/95mΩ)**
- **26μA (TYP) Operating Quiescent Current**
- **Power-Save Mode for Light Load Efficiency**
- **100% Duty Cycle for Lowest Dropout**
- **Output Discharge Function**
- **Power Good Output**
- **Thermal Shutdown Protection**
- **Available in a Green WLCSP-0.9×1.3-6B-A Package**

APPLICATIONS

Battery-Powered Application
Point-of-Load
Processor Supply
OLED/LCD Module Power Supply

TYPICAL APPLICATION

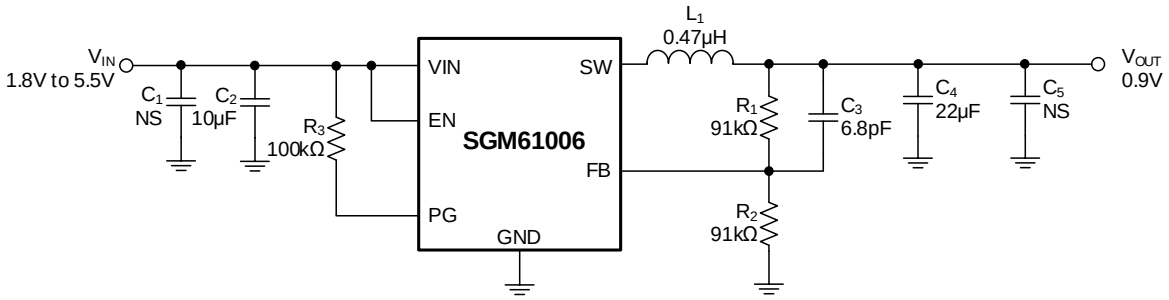


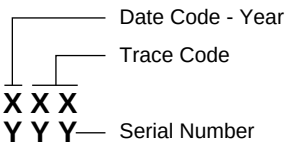
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61006	WLCSP-0.9×1.3-6B-A	-40℃ to +125℃	SGM61006XG/TR	XXX MBX	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltages Referred to GND
VIN, FB, EN, PG ..... -0.3V to 6V
SW (DC) .....-0.3V to V_{IN} + 0.3V
SW (AC, less than 10ns) while Switching ..... -2V to 8V
Package Thermal Resistance
WLCSP-0.9×1.3-6B-A, θ_{JA} ..... 158℃/W
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃
ESD Susceptibility
HBM.....2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range, V_{IN} .....1.8V to 5.5V
Output Voltage Range, V_{OUT} ..... 0.5V to V_{IN}
Sink Current at PG Pin, I_{SINK_PG} 1mA
Pull-Up Resistor Voltage, V_{PG} 5.5V
Operating Junction Temperature .....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

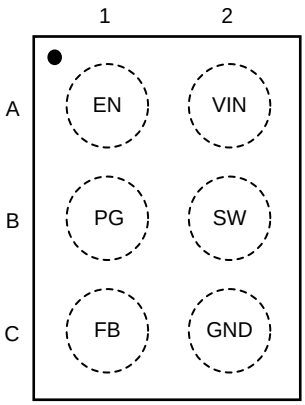
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-0.9×1.3-6B-A

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
A1	EN	I	Active High Device Enable Input Pin. Pull this pin to logic high to enable the device and pull it low to disable it. An internal 450kΩ (TYP) pull-down resistor disables the device by default. This resistor is removed when the device is enabled.
A2	VIN	P	Input Voltage Pin.
B1	PG	O	Open-Drain Power Good Output Pin. This output is released to go high if the device is in power good status. Pull up this pin to a 5.5V or less voltage rail. It can be left open if not used.
B2	SW	P	Switch Node of the Power Converter. Connect it to the output inductor.
C1	FB	I	Feedback Pin. Connect a resistor divider between the output voltage sense point and ground and tap it to the FB pin to set the output voltage.
C2	GND	G	Ground Pin.

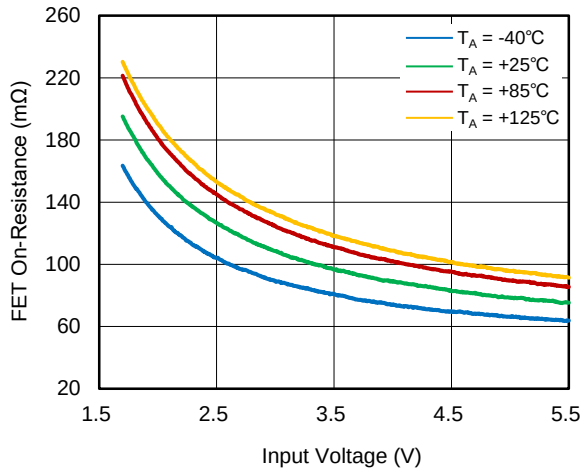
ELECTRICAL CHARACTERISTICS

(V_{IN} = 3.3V, T_J = -40℃ to +125℃, and all typical values are at T_J = +25℃, unless otherwise noted.)

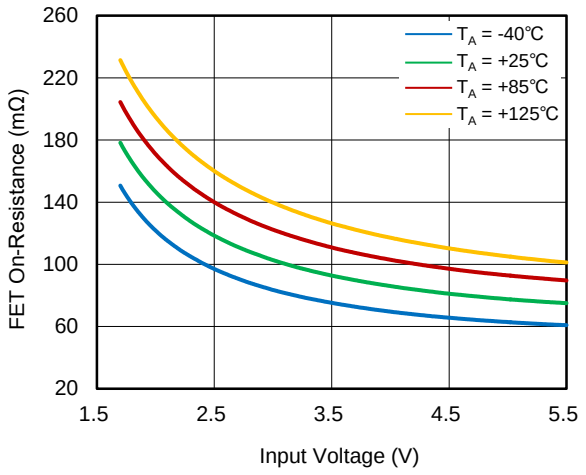
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply						
Quiescent Current into VIN Pin	I_Q	V_{IN} = 1.8V to 5.5V, not switching		26	40	μA
Shutdown Current into VIN Pin	I_{SD}	V_{IN} = 1.8V to 5.5V, EN = Low		0.1	3	μA
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	1.47	1.57	1.65	V
		Hysteresis		70		mV
Thermal Shutdown	T_{JSD}	Junction temperature rising		150		℃
		Junction temperature falling		135		℃
Logic Interface						
High-Level Threshold at EN Pin	V_{IH}	V_{IN} = 1.8V to 5.5V	1			V
Low-Level Threshold at EN Pin	V_{IL}	V_{IN} = 1.8V to 5.5V			0.4	V
Pull-Down Resistance at EN Pin	R_{PD}	EN = Low	250	450	620	kΩ
EN Input Leakage Current	I_{ENLKG}	V_{EN} = V_{IN} = 5.5V		0.01	1	μA
Power Good						
Power Good Threshold	V_{PG}	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		96		%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		91		
V_{OUT} Over-Voltage Threshold	V_{OVP}	V_{PG} rising, V_{FB} referenced to V_{FB} nominal		110		%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal		105		
Power Good Low-Level Output Voltage	V_{PG_OL}	I_{SINK} = 1mA			0.15	V
Input Leakage Current into PG Pin	I_{PG_LKG}	V_{PG} = 5.0V		0.01	0.1	μA
Output						
Feedback Regulation Voltage	V_{FB}	PWM mode	0.443	0.450	0.457	V
Feedback Input Leakage Current	I_{FB}	V_{FB} = 0.45V		0.001	0.01	μA
Output Discharge Resistor	R_{DIS}	EN = Low, V_{OUT} = 1.8V	750	1100	1450	Ω
Power Switch						
High-side FET On-Resistance	R_{DSON}	V_{IN} = 1.8V, I_{SW} = 500mA		180		mΩ
		V_{IN} = 3.3V, I_{SW} = 500mA		100		
Low-side FET On-Resistance		V_{IN} = 1.8V, I_{SW} = 500mA		170		mΩ
		V_{IN} = 3.3V, I_{SW} = 500mA		95		
High-side FET Current Limit	I_{LIM}	Rising inductor current	1.0	1.2	1.5	A
Switching Frequency	f_{SW}	V_{OUT} = 1.2V		3.5		MHz

TYPICAL PERFORMANCE CHARACTERISTICS

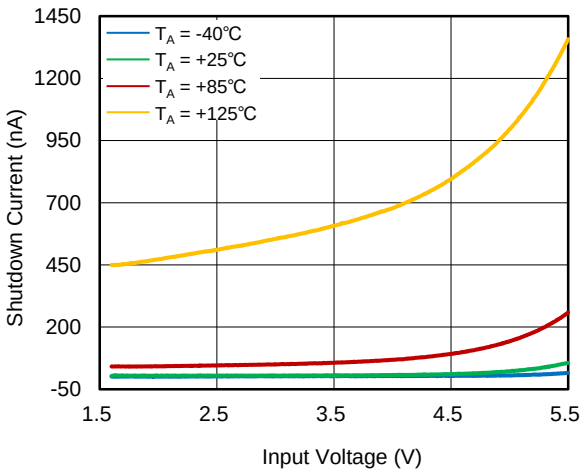
High-side FET On-Resistance vs. Input Voltage



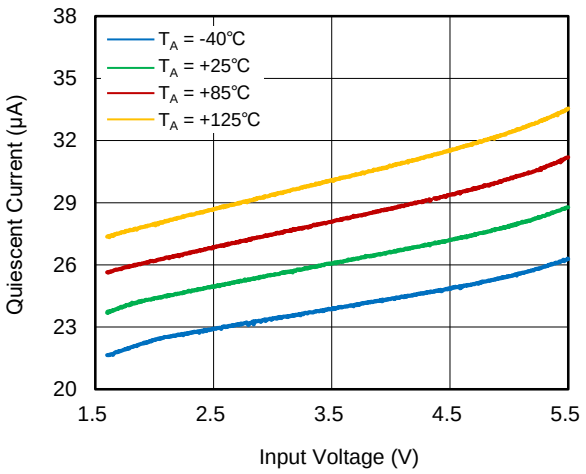
Low-side FET On-Resistance vs. Input Voltage



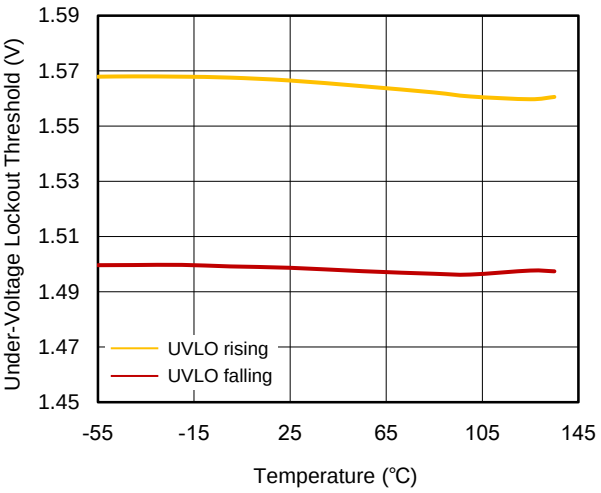
Shutdown Current vs. Input Voltage



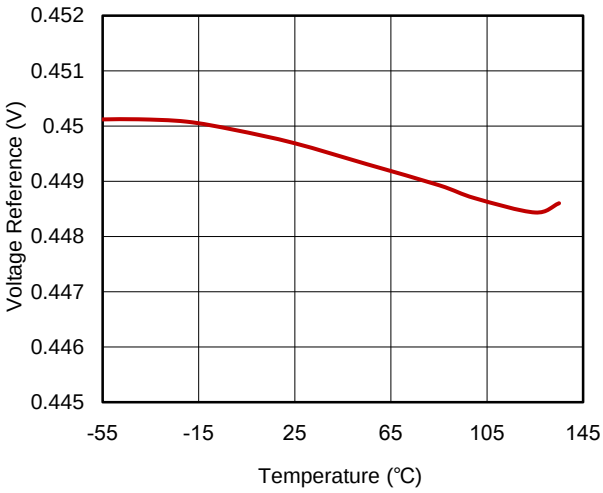
Quiescent Current vs. Input Voltage



Under-Voltage Lockout Threshold vs. Temperature



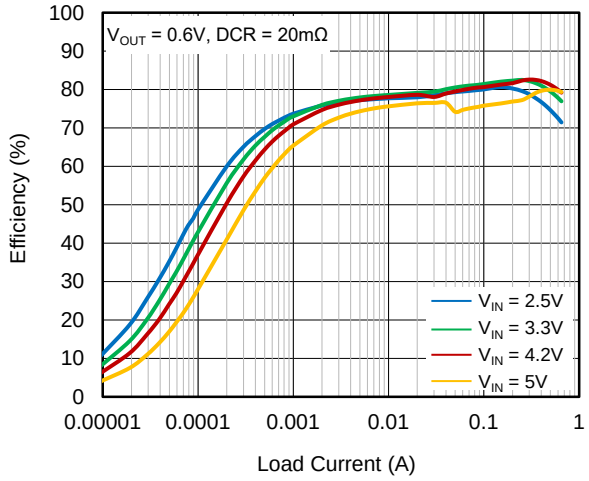
Regulated FB Voltage vs. Temperature



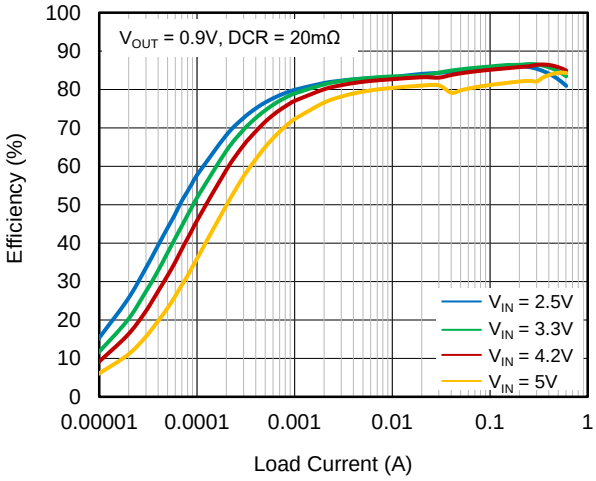
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 1.8V, V_{OUT} = 0.9V, C_{OUT} = 22μF and L = 0.47μH, unless otherwise noted.

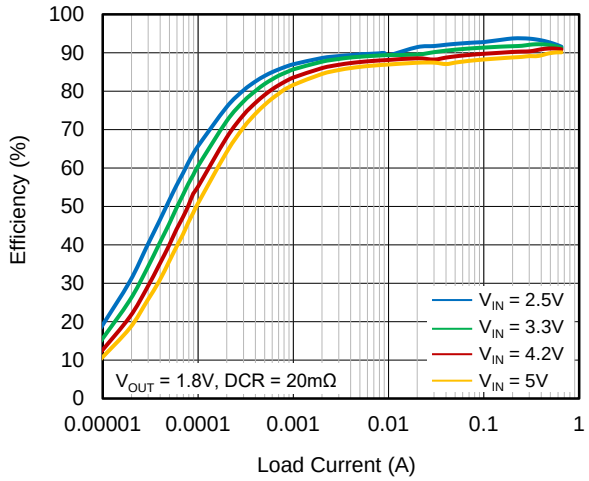
Efficiency vs. Load Current



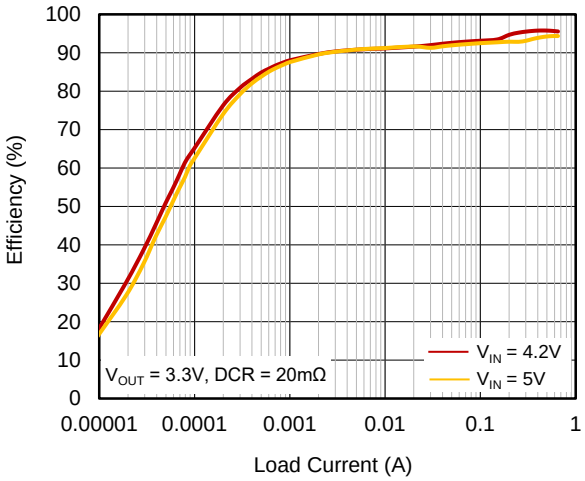
Efficiency vs. Load Current



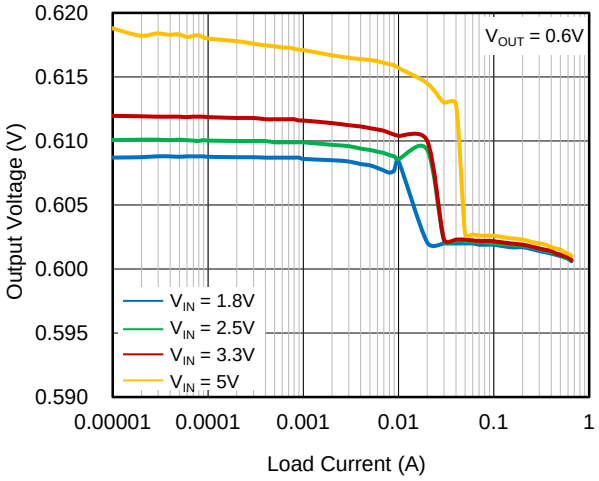
Efficiency vs. Load Current



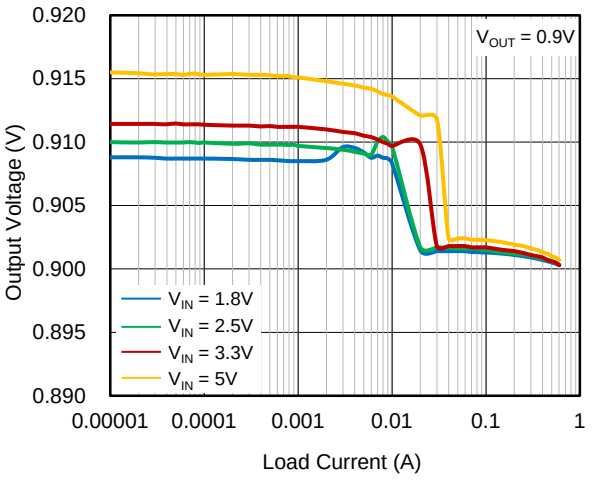
Efficiency vs. Load Current



Load Regulation vs. Load Current



Load Regulation vs. Load Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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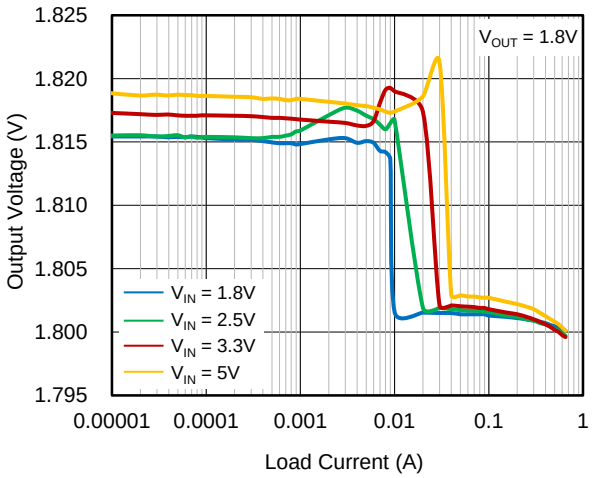
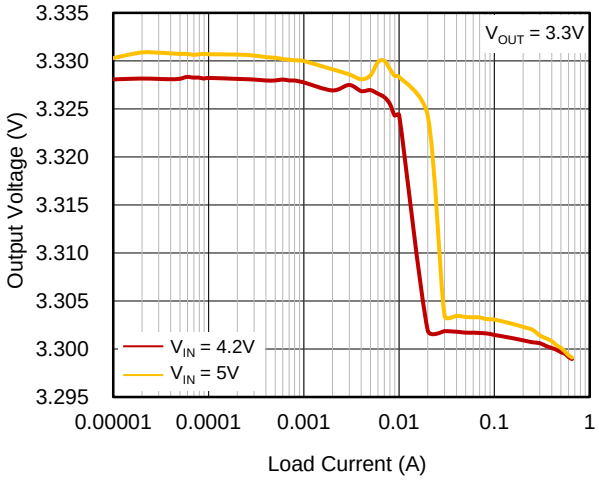
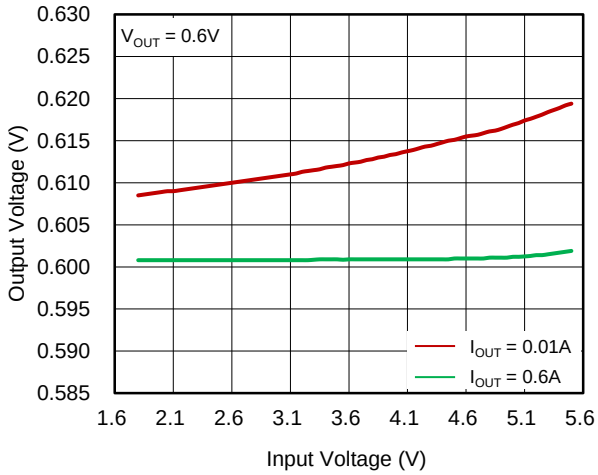
Load Regulation vs. Load Current



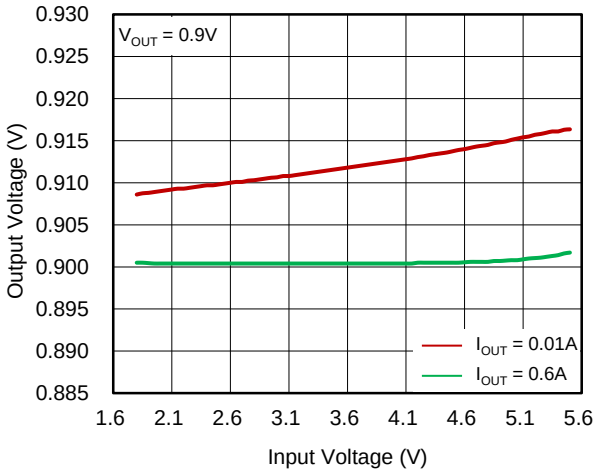
Load Regulation vs. Load Current



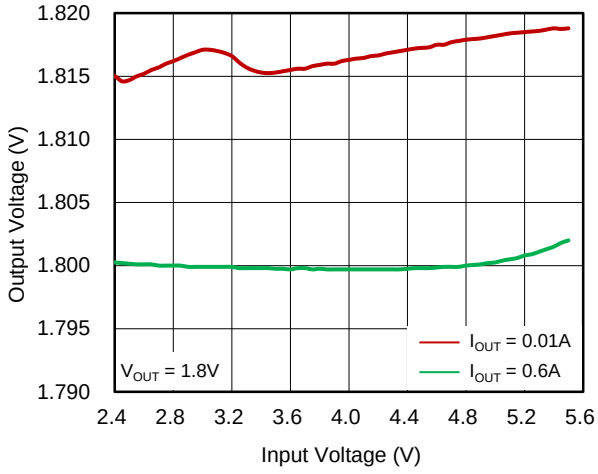
Line Regulation vs. Input Voltage



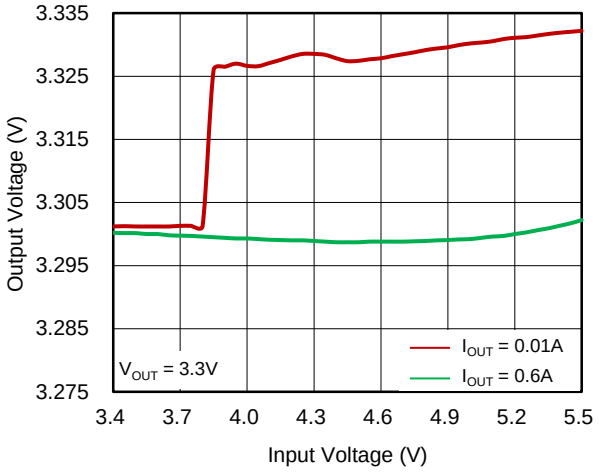
Line Regulation vs. Input Voltage



Line Regulation vs. Input Voltage



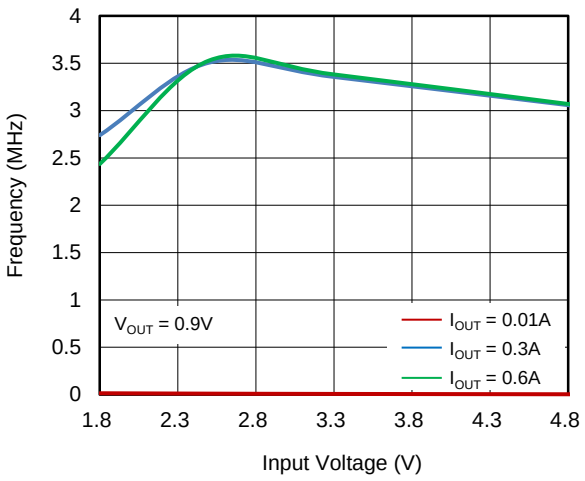
Line Regulation vs. Input Voltage



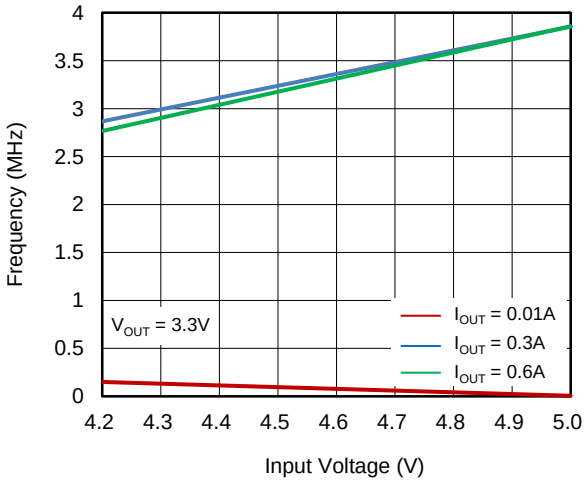
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 1.8V, V_{OUT} = 0.9V, C_{OUT} = 22μF and L = 0.47μH, unless otherwise noted.

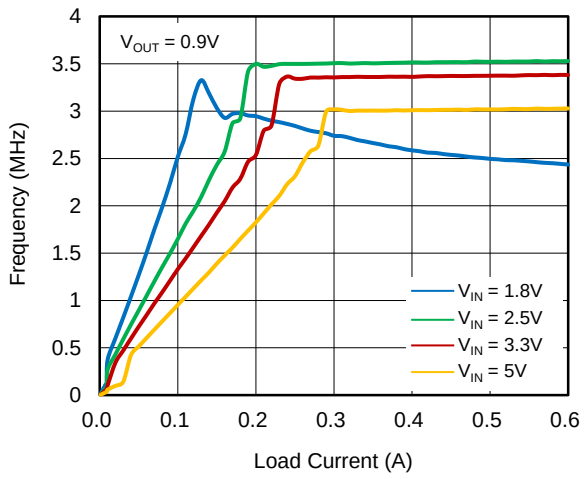
Frequency vs. Input Voltage



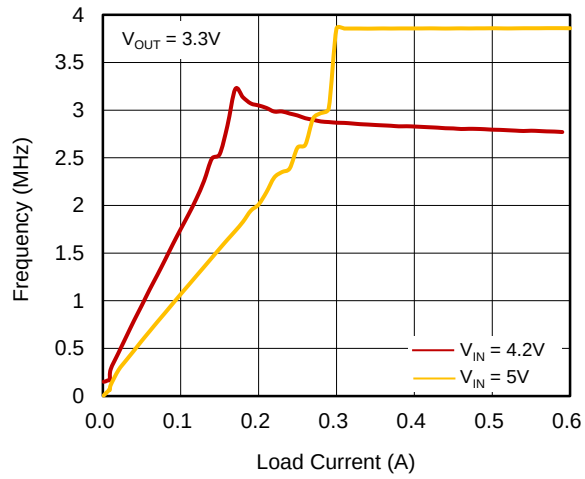
Frequency vs. Input Voltage



Frequency vs. Load Current



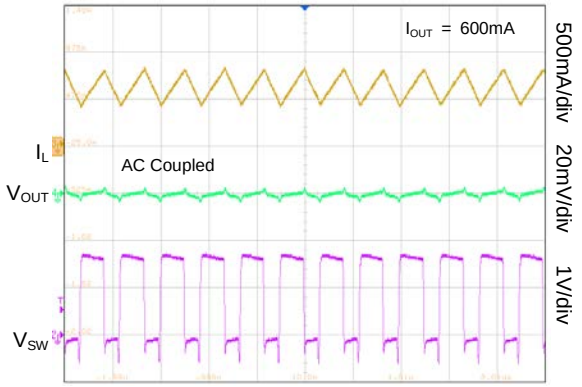
Frequency vs. Load Current



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

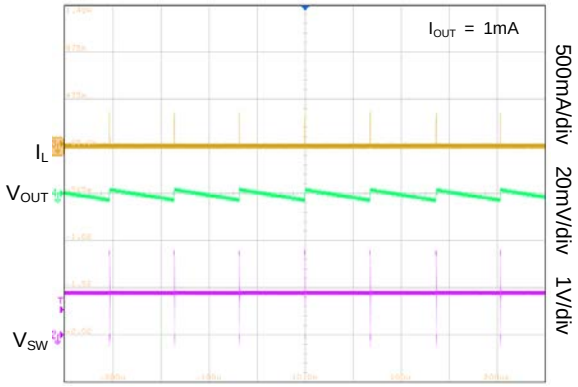
T_A = +25℃, V_{IN} = 1.8V, V_{OUT} = 0.9V, C_{OUT} = 22μF and L = 0.47μH, unless otherwise noted.

PWM Operation



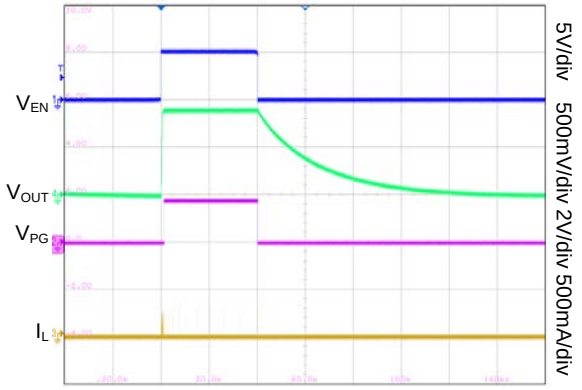
Time (500ns/div)

PSM Operation



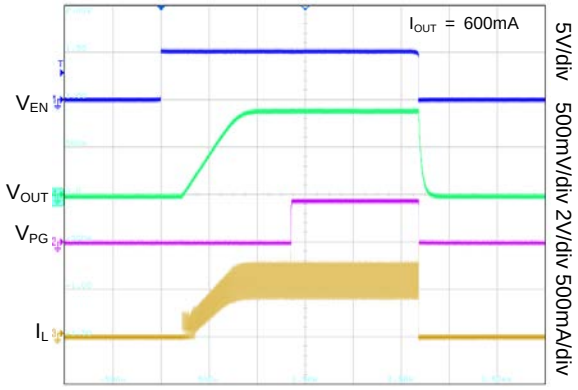
Time (50μs/div)

Startup and Shutdown without Load



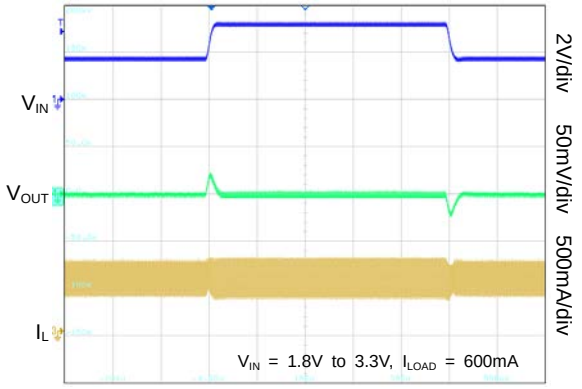
Time (20ms/div)

Startup and Shutdown with Load



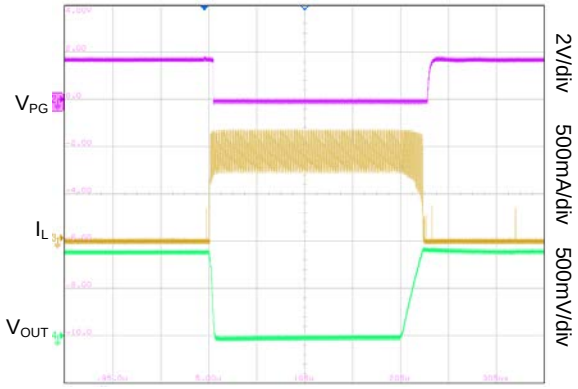
Time (500μs/div)

Line Transient



Time (100μs/div)

Short Circuit Entry & Exit

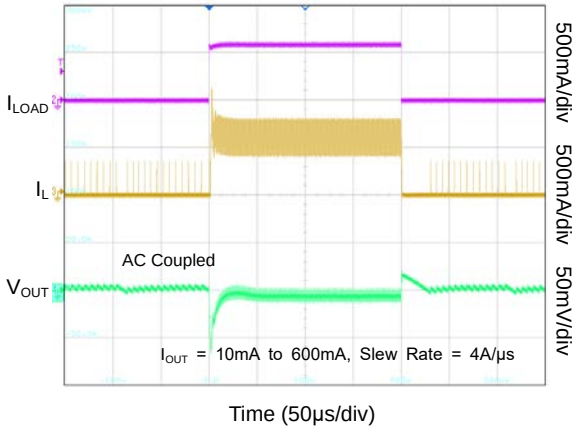


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

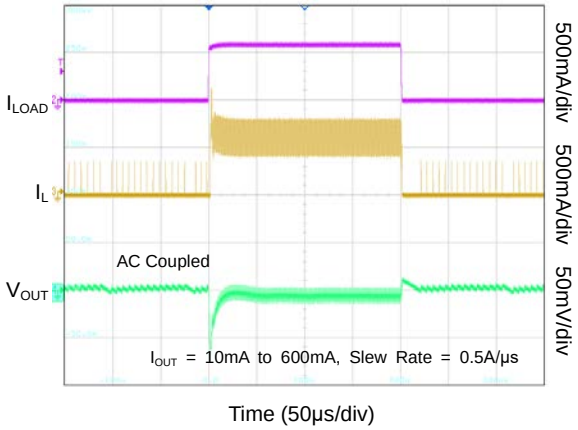
T_A = +25℃, V_{IN} = 1.8V, V_{OUT} = 0.9V, C_{OUT} = 22μF and L = 0.47μH, unless otherwise noted.

Load Transient



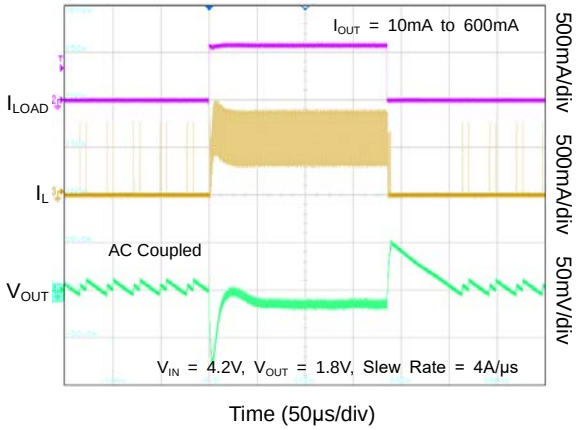
Time (50μs/div)

Load Transient



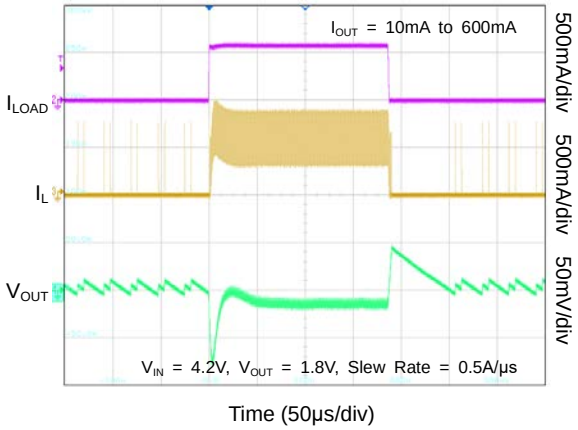
Time (50μs/div)

Load Transient



Time (50μs/div)

Load Transient



Time (50μs/div)

FUNCTIONAL BLOCK DIAGRAM

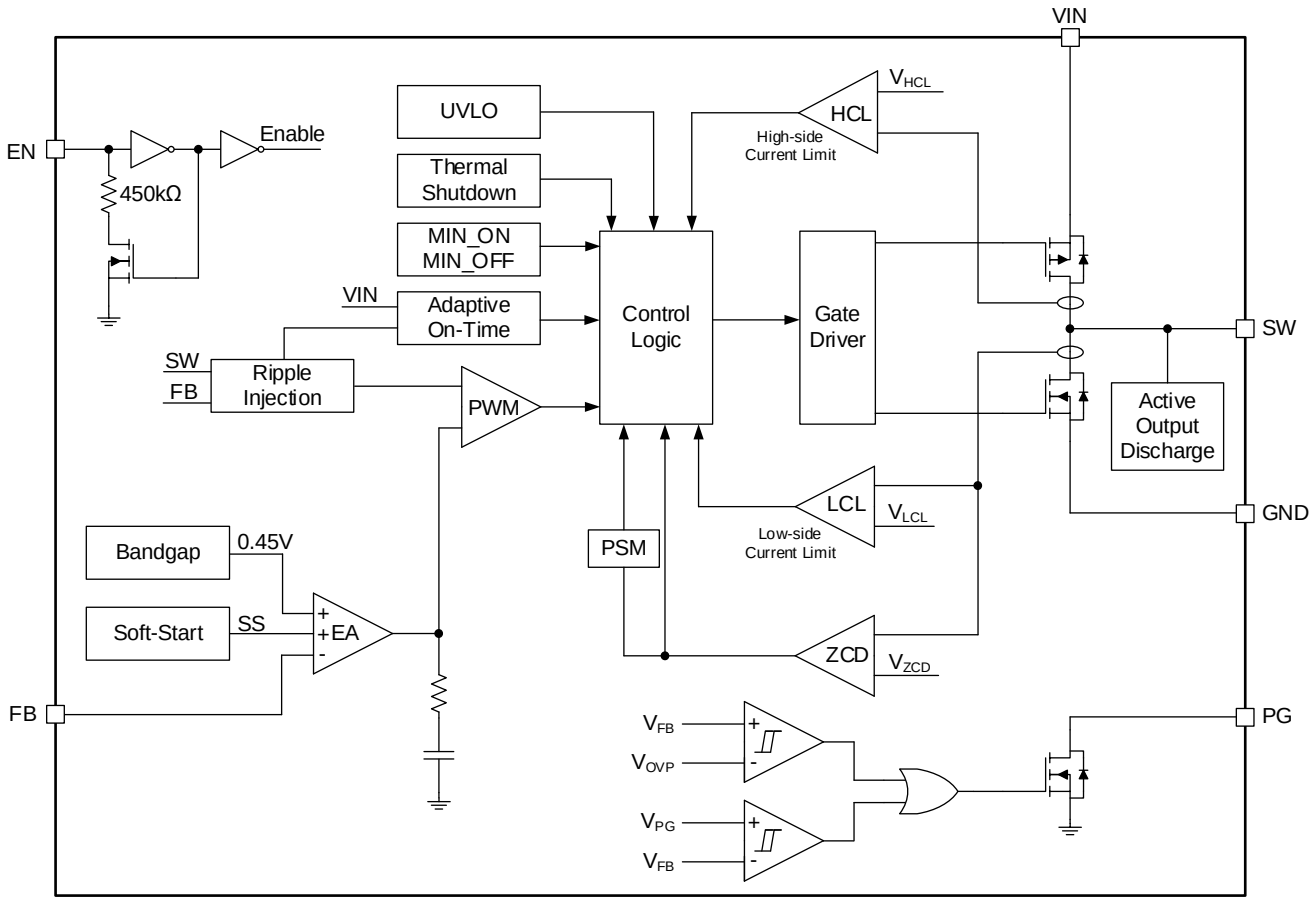


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61006 is a high efficiency Buck converter with AHP-COT architecture and advanced regulation topology.

At medium to heavy loads, the device works in pulse width modulation (PWM) mode. At light loads, it automatically switches to power-save mode (PSM). In PWM mode, the device works with a nominal switching frequency of 3.5MHz. When the load current falls, the device goes into PSM to achieve high efficiency with reducing switching frequency and minimizing quiescent current. PSM mode can reduce the standby energy consumption of system. During shutdown mode, the energy consumption falls below 3μA.

Under-Voltage Lockout (UVLO)

The device implements the under-voltage lockout (UVLO) with a 70mV (TYP) hysteresis. When the input voltage falls below the V_{UVLO}, it shuts down the device.

Enable and Disable

A logic high input to EN activates the device, and a logic low disables the device. An internal 450kΩ (TYP) pull-down resistor disables the device by default. This resistor is removed when the device is enabled.

Soft-Start

When EN is set to logic high and after about 260μs delay, the device starts switching and V_{OUT} increases with 600μs (typical timing is from the first pulse to 95% regulated voltage) internal soft-start circuit.

Power Good (PG)

The power good output of SGM61006 will be low in the condition that the output voltage is less than its nominal value. If the output is between 96% and 105% of the regulated voltage, the power good is in high-impedance state. If the output voltage is less than 91% or greater than 110% of the regulated voltage, the power good is driven to low.

The PG pin is an open-drain output with a maximum sink current of 1mA. A pull-up resistor connecting to power good output is required. When the device is disabled or under-voltage lockout, the PG pin is driven to low (see Table 1). The PG signal connected to the EN pin of other converters can be used for multiple rails sequences. Leave the PG pin floating when not in use.

Table 1. Logic Table of PG Pin

Device Information		Logic Status	
		High Z	Low
Enable (EN = High)	EN = High, V_{FB} Rising ≥ 0.432V	√	
	EN = High, V_{FB} Falling ≤ 0.410V		√
	EN = High, V_{FB} Rising ≥ 0.495V		√
	EN = High, V_{FB} Falling ≤ 0.473V	√	
Shutdown (EN = Low)			√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 0.7V$	undefined	

100% Duty Cycle

The device provides low input-to-output voltage drop by going into 100% duty cycle mode. In this mode, the high-side MOSFET is constantly turned on and the low-side MOSFET is turned off. This function can increase the operation time to the utmost extent for battery powered applications. To maintain an appropriate output voltage, the minimum input voltage is calculated by:

$$V_{IN\_MIN} = V_{OUT} + I_{OUT\_MAX} \times (R_{DSON} + R_L) \quad (1)$$

where:

- V_{IN_MIN} is the minimum input voltage.
- I_{OUT_MAX} is the maximum output current.
- R_{DSON} is the high-side MOSFET on-resistance.
- R_L is the inductor ohmic resistance.

Output Discharge

Whenever the device is disabled by enable, thermal shutdown or under-voltage lockout, the output is discharged by the SW pin through a typical discharge resistor of R_{DIS}.

Power-Save Mode (PSM)

Once the load current decreases, the SGM61006 will enter power-save mode. Then, the device has a reduced switching frequency and works with the minimum quiescent current to keep high efficiency. In power-save mode, the inductor current is discontinuous. Then a fixed on-time architecture is activated and the typical on-time is t_{ON} = 286ns × (V_{OUT}/V_{IN}).

DETAILED DESCRIPTION (continued)

Inductor Current Limit

The device implements an inductor current limit if over-current or short-circuit exists. Both the peak current of high-side and valley current of low-side power MOSFETs are limited to protect the device. The high-side MOSFET is turned off and the low-side MOSFET is turned on to reduce the inductor current when the high-side switch current limit is triggered. The low-side MOSFET is turned off and the high-side switch is turned on again when the inductor current drops to the low-side switch current limit. It repeats until the inductor current falls below the high-side switch current limit. The actual current limit value may be larger than the static current limit due to internal propagation delays.

Thermal Shutdown

To protect the device from overheating damage, thermal protection is included in the device. If the junction temperature exceeds the typical T_{JSD} (+150℃ TYP), the switching will stop. When the device temperature drops below the threshold minus hysteresis, the switching will resume automatically.

APPLICATION INFORMATION

The SGM61006 is a synchronous Buck converter with output voltage adjusted by feedback dividers. Taking SGM61006 typical application as a reference, the following sections discuss the design of external components and how to achieve the application.

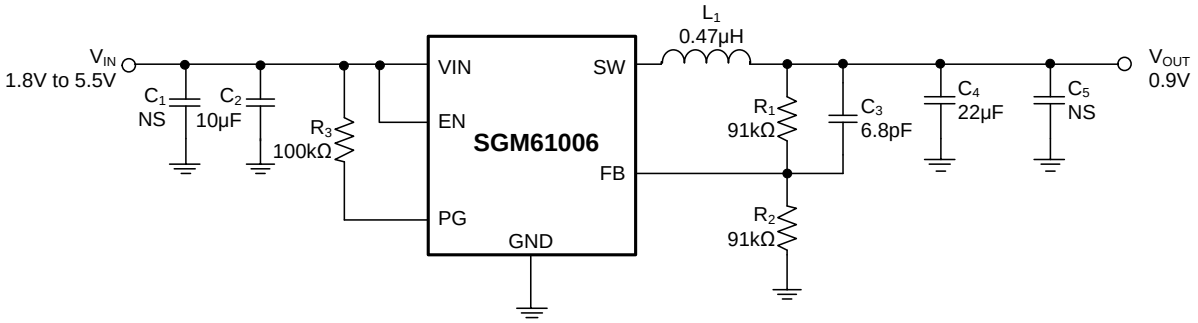


Figure 3. SGM61006 Typical Application Circuit

Requirements

The design parameters given in Table 2 are used for this design example.

Table 2. Design Parameters

Design Parameter	Example Value
Input Voltage	1.8V to 5.5V
Output Voltage	0.9V
Output Ripple Voltage	< 20mV
Output Current (MAX)	600mA

Design Details

Table 3 shows the components included in this example.

Table 3. Components List

Reference	Description	Manufacturer
L_1	0.47μH, Power Inductor, DCR = 45mΩ, I_{SAT} = 3.3A, I_{RMS} = 2.6A DFE18SANR47MG0L	Murata
C_2	10μF, Ceramic Capacitor, 10V, X5R, Size 0603	Standard
C_3	6.8pF, Ceramic Capacitor, 50V, C0G, Size 0603	Standard
C_4	22μF, Ceramic Capacitor, 10V, X5R, Size 0603	Standard
R_1	91kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_2	91kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard
R_3	100kΩ, Chip Resistor, 1/16W, 1%, Size 0603	Standard

Adjustable Output Voltage

An external resistor divider connected to FB pin is used for setting the output voltage. Through adjusting R_1 and R_2, the output voltage can be programmed to the desired value. Calculate R_1 and R_2 with Equation 2.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.45V \times \left(1 + \frac{R_1}{R_2}\right) \quad (2)$$

A lower value of R_2 increases the robustness against noise injection, and a higher value reduces the current consumption of the voltage divider, thereby improving the efficiency of light load.

A feed-forward capacitor is recommended to improve the performance of smooth transition into power-save mode and reduce undershoot during load transient. 5pF to 10pF is enough for typical applications.

Inductor Design

Equation 3 is conventionally used to calculating the output inductance of a Buck converter. The inductor should be selected by its value and the saturation current. The saturation current of inductor should be higher than I_{L_MAX} in Equation 3, and sufficient margin should be reserved. Typically, the current above high-side current limit is enough, and a 20% to 40% ripple current is selected to calculate the inductance. Larger inductor can reduce the ripple current, but with an increasing response time.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (3)$$

where:

- I_{OUT_MAX} is the maximum output current.
- ΔI_L is the inductor current ripple.
- f_{SW} is the switching frequency.
- L is the inductor value.

APPLICATION INFORMATION (continued)

Capacitor Design

For input capacitor design, an X5R/X7R dielectric ceramic capacitor should be selected for its low ESR and high-frequency performance. 10μF is enough for most applications. The voltage rating of input capacitor must be considered for its significant bias effect. The input ripple voltage can be calculated from Equation 4.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{C_{IN} \times f_{SW}} \quad (4)$$

The ripple current rating of input capacitor should be greater than I_{CIN_RMS} in Equation 5 and the maximum value occurs at 50% duty cycle. A bulk capacitor is suggested to add if the input wire long.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{IN}-V_{OUT})}{V_{IN} \times V_{IN}}} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (5)$$

For output capacitor design, output ripple, transient response and loop stability should be considered. Minimum capacitance of output ripple criteria can be calculated from Equation 6.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT\_RIPPLE}} \quad (6)$$

Both the input and output capacitors should be placed as close to VIN and GND pins as possible to reduce noise caused by PCB parasitic parameters.

Layout Considerations

Good PCB layout is the key factor for high performance operation of a device regarding the stability, regulation, efficiency and other performance measures.

A list of guidelines for designing the PCB layout of SGM61006 is provided below:

- Place the power components close together and connect them with short and wide routes. The low-side of the capacitors must be connected to GND properly to avoid potential shift.
- FB pin is noise sensitive and must be placed away from SW. Connect the inductor with a short trace to minimize noise.

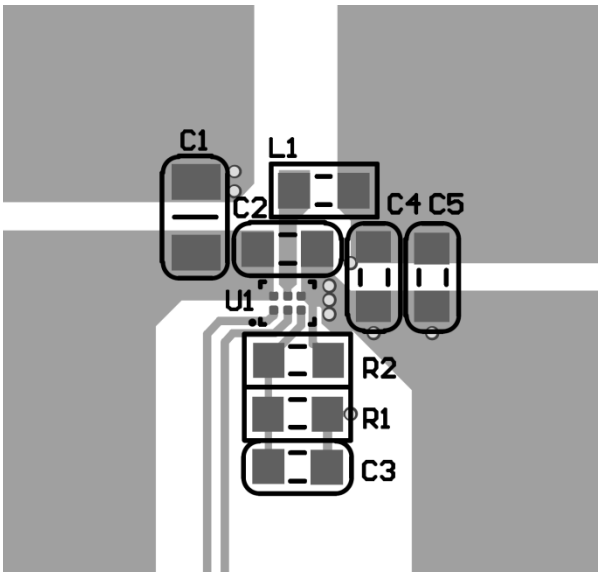


Figure 4. Top Layer

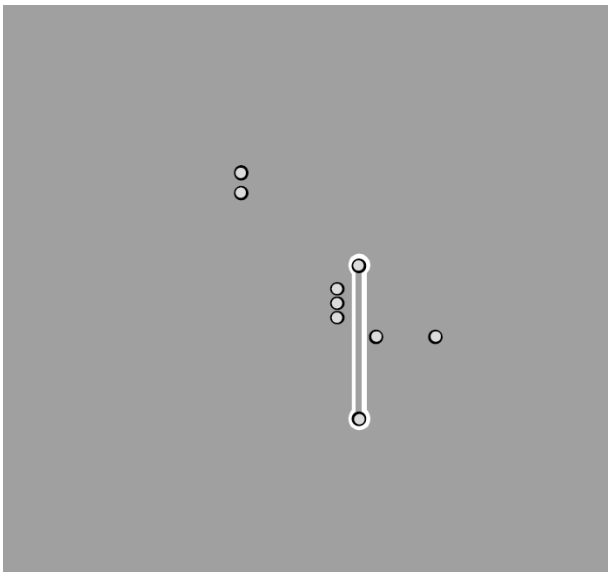


Figure 5. Bottom Layer

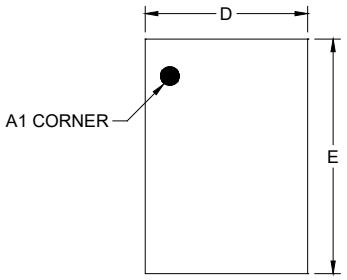
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

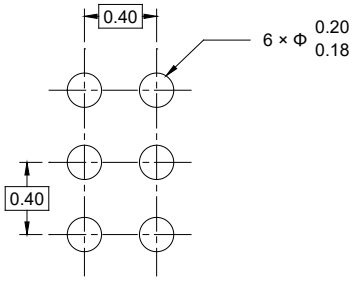
Changes from Original (MARCH 2023) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

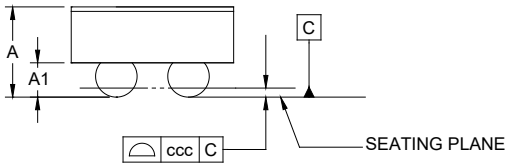
WLCSP-0.9×1.3-6B-A



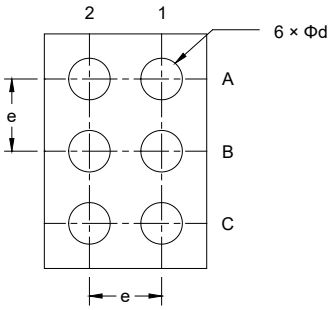
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



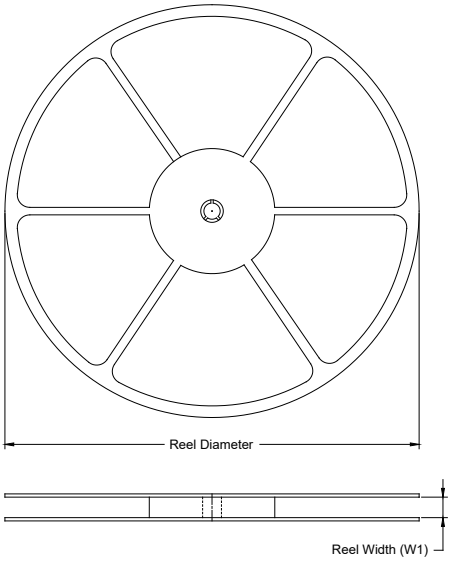
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.545
A1	0.170	-	0.210
D	0.870	-	0.930
E	1.270	-	1.330
d	0.200	-	0.260
e	0.400 BSC		
ccc	0.050		

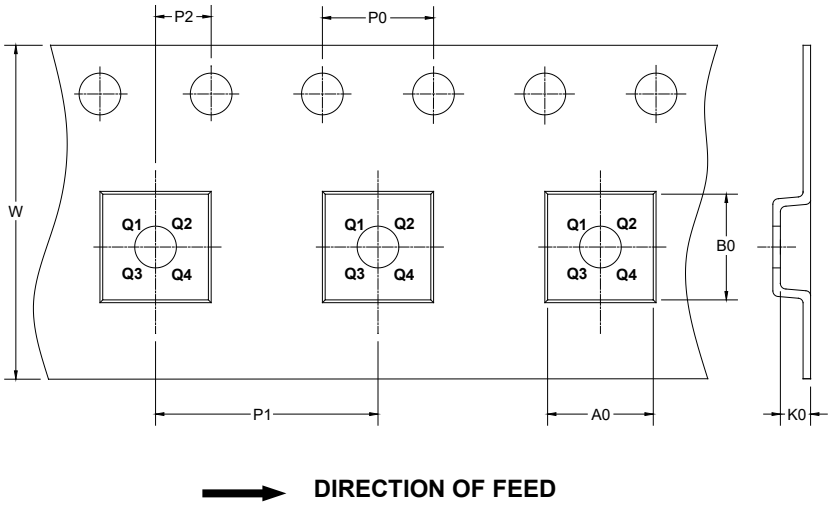
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



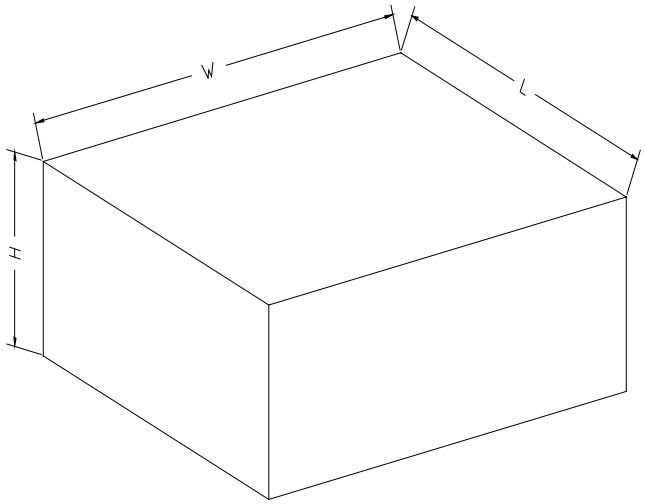
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.9×1.3-6B-A	7″	9.5	1.00	1.40	0.62	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002