SGM8473
Rail-to-Rail Output, High Input Impedance, Low Power, Low Noise Difference Amplifier

GENERAL DESCRIPTION

The SGM8473 series is a high accuracy, high voltage, low power, low noise and high input impedance difference amplifier, which is designed to offer fixed gain options of 0.2V/V and 0.6V/V by using integrated resistors. The device works well in battery-powered applications due to the low power consumption of 1.3mA typical quiescent current.

The SGM8473 provides 70ppm (MAX) non-linearity. SGM8473A1 offers 1.5mV (MAX) low input offset voltage and SGM8473A3 offers 1.2mV (MAX) low input offset voltage. The device also features low noise, low bias current and low power. The combination of these characteristics makes it a good choice for applications requiring excellent DC performance.

The SGM8473A1 offers 120nV/$\sqrt{Hz}$ low input voltage noise, 300fA/$\sqrt{Hz}$ input current noise at 1kHz, and 9μV_{P-P} in the 0.1Hz to 10Hz band. The SGM8473A3 offers 80nV/$\sqrt{Hz}$ low input voltage noise, 300fA/$\sqrt{Hz}$ input current noise at 1kHz, and 6μV_{P-P} in the 0.1Hz to 10Hz band. They are suitable for pre-amplifier applications. The 10μs settling time to 0.1% makes SGM8473 appropriate for multiplexed applications.

The SGM8473 series is available in a Green SOIC-8 package. It is specified over the extended -40℃ to +125℃ temperature range.

FEATURES

- **Gain Options:**
  - **SGM8473A1 Gain: 0.2V/V**
  - **SGM8473A3 Gain: 0.6V/V**
- **Integrated Resistors**
- **High Input Impedance**
- **Input Offset Voltage:**
  - **SGM8473A1: 1.5mV (MAX)**
  - **SGM8473A3: 1.2mV (MAX)**
- **Input Bias Current: 15nA (TYP)**
- **Common Mode Rejection Ratio: 72dB (TYP)**
- **Input Voltage Noise:**
  - **SGM8473A1: 120nV/$\sqrt{Hz}$ at 1kHz**
  - **SGM8473A3: 80nV/$\sqrt{Hz}$ at 1kHz**
- **0.1Hz to 10Hz Voltage Noise:**
  - **SGM8473A1: 9μV_{P-P}**
  - **SGM8473A3: 6μV_{P-P}**
- **Bandwidth: 1.3MHz**
- **Settling Time to 0.1%: 10μs**
- **Rail-to-Rail Output**
- **Support Single or Dual Power Supplies: 4.6V to 36V or ±2.3V to ±18V**
- **Low Power Supply Current: 1.3mA (TYP)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green SOIC-8 Package**

APPLICATIONS

Industrial System
PLC

TYPICAL APPLICATION

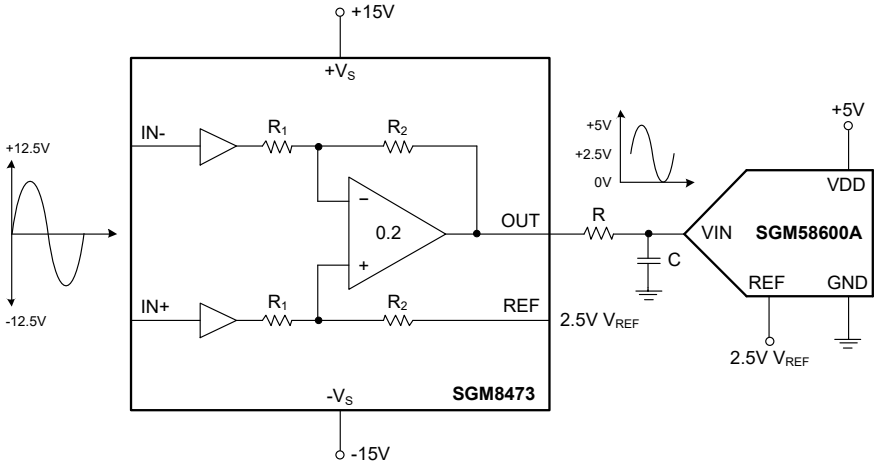


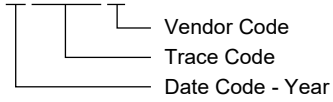
Figure 1. Focus Application – ADC Driver

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8473A1 (Gain = 0.2V/V)	SOIC-8	-40℃ to +125℃	SGM8473A1XS8G/TR	SGM 8473A1XS8 XXXXX	Tape and Reel, 4000
SGM8473A3 (Gain = 0.6V/V)	SOIC-8	-40℃ to +125℃	SGM8473A3XS8G/TR	SGM 8473A3XS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $+V_S$ to $-V_S$ 40V
Input Common Mode Voltage ..... $\pm V_S$
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±7000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.
2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

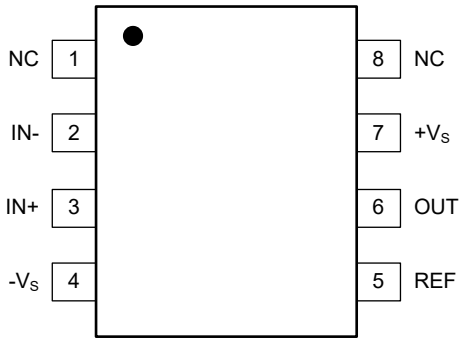
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

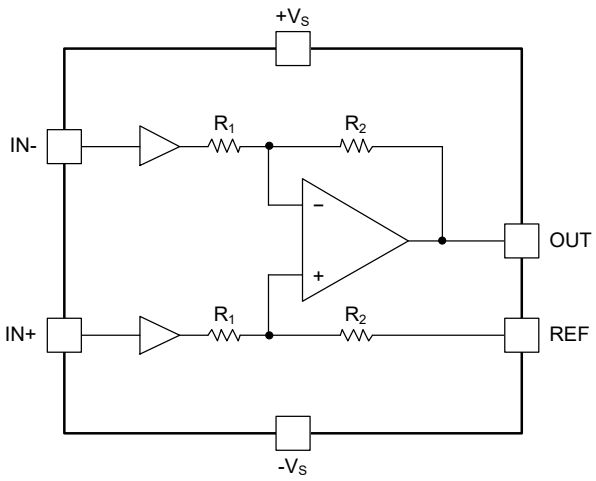
PIN CONFIGURATION

(TOP VIEW)



SOIC-8

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 8	NC	Not Connected.
2	IN-	High Impedance Inverting Input.
3	IN+	High Impedance Non-Inverting Input.
4	$-V_S$	Negative Power Supply.
5	REF	Voltage Reference Pin. A voltage source with low impedance can be placed to supply this terminal in order to shift the output level.
6	OUT	Output.
7	$+V_S$	Positive Power Supply.

ELECTRICAL CHARACTERISTICS

(V_S = ±15V, R_L = 2kΩ, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Gain									
Gain		G	SGM8473A1				0.2		V/V
			SGM8473A3				0.6		
Gain Error		GE	V_{IN} = -10V to +10V	G = 0.2, 0.6	+25℃		0.01	0.075	%
					Full			0.1	
Gain Temperature Coefficient				G = 0.2, 0.6	Full		3		ppm/℃
Non-Linearity			V_{IN} = -10V to +10V	G = 0.2, 0.6	+25℃		10	70	ppm
					Full			100	
Voltage Offset (Total RTI Error = V_{OSO}/G)									
Input Offset Voltage		V_{OSI}	V_S = ±5V to ±15V	G = 0.2	+25℃		400	1500	μV
					Full			2000	
				G = 0.6	+25℃		200	1200	
					Full			1600	
Input Offset Voltage Drift		$\Delta V_{OSI}/\Delta T$			Full		0.2		μV/℃
Offset Referred to the Input vs. Supply		PSRR	V_S = ±2.3V to ±18V	G = 0.2, 0.6	+25℃	108	120		dB
					Full	105			
Input Current									
Input Bias Current		I_B			+25℃		15	28	nA
					Full			45	
Average Temperature Coefficient of Input Bias Current		$\Delta I_B/\Delta T$			Full		0.15		nA/℃
Input Offset Current		I_{OS}			+25℃		5	15	nA
					Full			20	
Average Temperature Coefficient of Input Offset Current		$\Delta I_{OS}/\Delta T$			Full		0.05		nA/℃
Input									
Input Impedance	Differential	Z_{DIFF}			+25℃		10 || 4		GΩ || pF
	Common Mode	Z_{CM}			+25℃		10 || 4		
Input Voltage Range			V_S = ±2.3V to ±18V		Full	$(-V_S)$ + 1.9		$(+V_S)$ - 1.2	V
Common Mode Rejection Ratio with 1kΩ Source Imbalance		CMRR	V_{CM} = $(-V_S)$ + 1.9V to $(+V_S)$ - 1.2V	G = 0.2, 0.6	+25℃	60	72		dB
					Full	57			
Reference Input									
Reference Input Resistance		R_{REF}			+25℃		18		kΩ
Reference Input Current		I_{REF}	V_{IN+} = V_{IN-} = 0V, V_{REF} = 0V		+25℃		40	60	μA
					Full			70	

ELECTRICAL CHARACTERISTICS (continued)

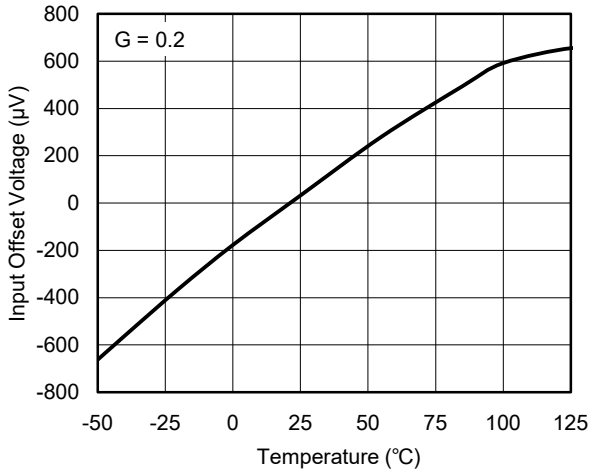
(V_S = ±15V, R_L = 2kΩ, Full = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Output Characteristics								
Output Voltage Swing	V_{OH}	V_S = ±18V		+25℃		310	450	mV
				Full			600	
	V_{OL}	V_S = ±18V		+25℃		150	220	
				Full			300	
Short-Circuit Current	I_{SC}	V_S = ±2.3V to ±18V, R_L = 50Ω to V_S/2		+25℃	19	24		mA
				Full	14			
Power Supply								
Quiescent Current	I_Q	V_S = ±2.3V to ±18V, I_{OUT} = 0A		+25℃		1.3	1.7	mA
				Full			2.2	
Dynamic Response								
Small-Signal -3dB Bandwidth	BW		G = 0.2, 0.6	+25℃		1300		kHz
Slew Rate	SR	V_{OUT} = 1V_{P-P} Step	G = 0.2	+25℃		0.3		V/μs
			G = 0.6	+25℃		0.7		
Settling Time to 0.1%	t_S	V_{OUT} = 2V_{P-P} Step	G = 0.2, 0.6	+25℃		10		μs
Noise								
Input Voltage Noise Density	e_n	f = 1kHz	G = 0.2	+25℃		120		nV/√Hz
			G = 0.6	+25℃		80		
0.1Hz to 10Hz Voltage Noise, RTI		f = 0.1Hz to 10Hz	G = 0.2	+25℃		9		μV_{P-P}
			G = 0.6	+25℃		6		
Input Current Noise Density, RTI	i_n	f = 1kHz		+25℃		300		fA/√Hz
0.1Hz to 10Hz Current Noise, RTI		f = 0.1Hz to 10Hz		+25℃		15		pA_{P-P}

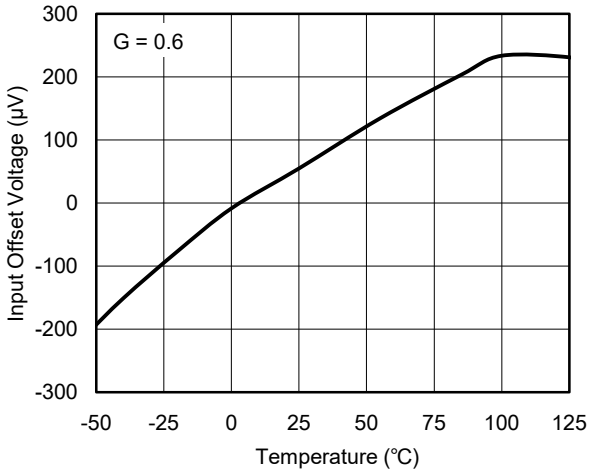
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, V_S = ±15V, unless otherwise noted.

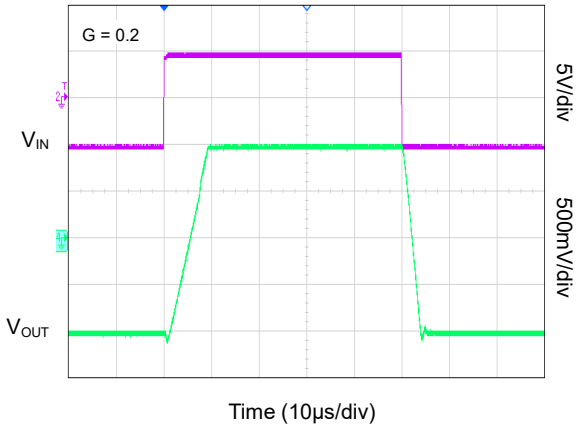
Input Offset Voltage vs. Temperature



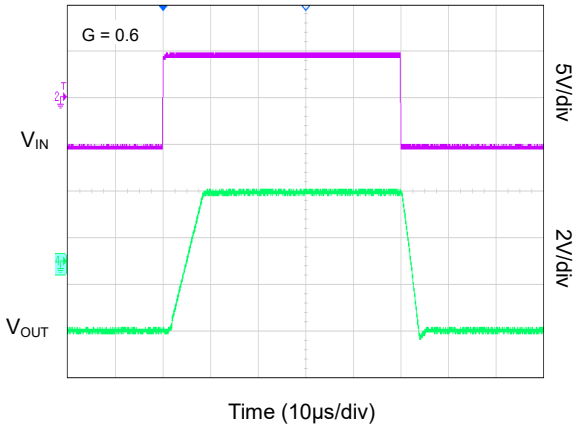
Input Offset Voltage vs. Temperature



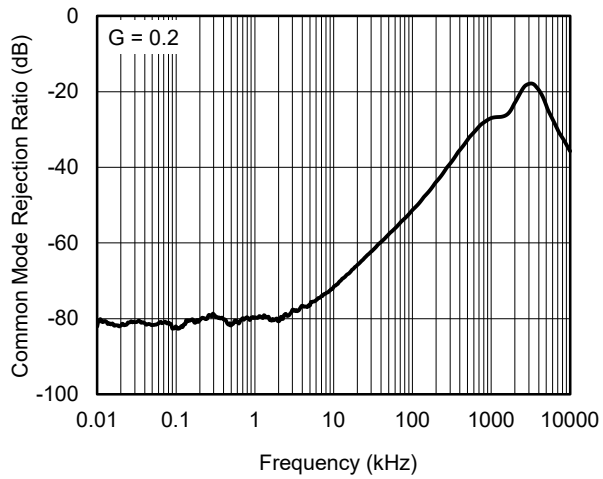
Large-Signal Step Response



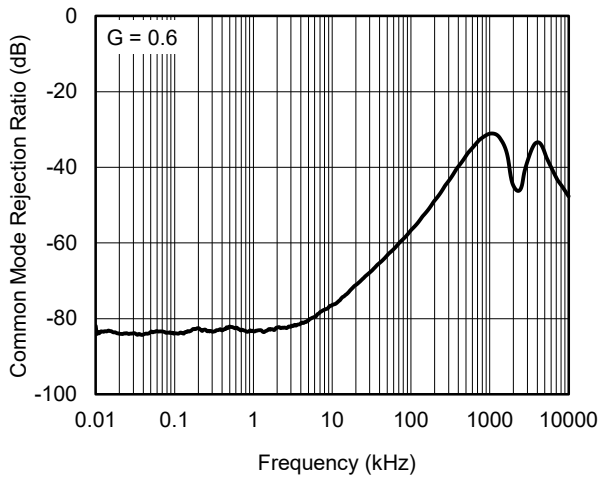
Large-Signal Step Response



CMRR vs. Frequency (Referred-to-Input)



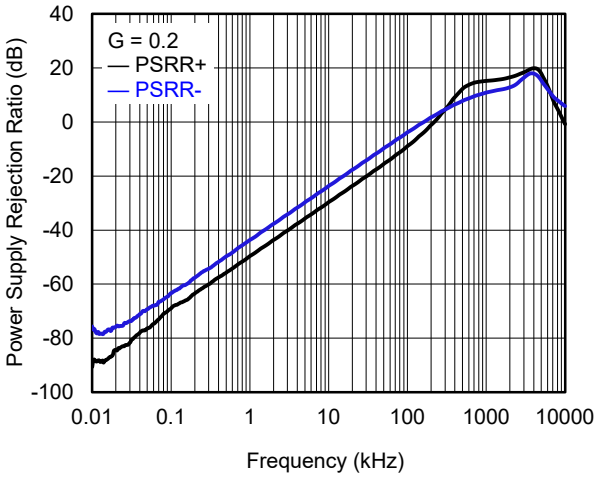
CMRR vs. Frequency (Referred-to-Input)



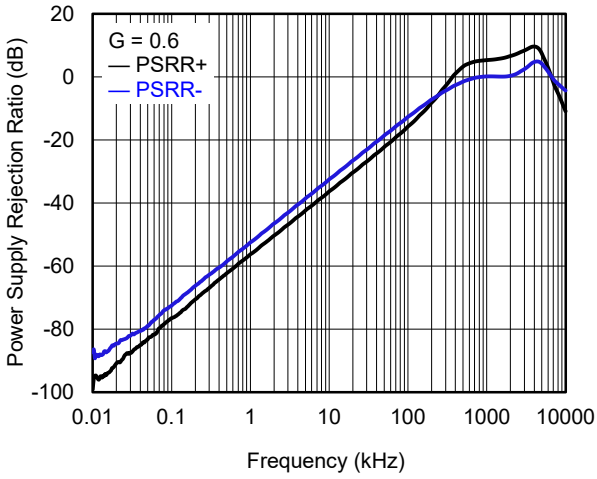
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V, unless otherwise noted.

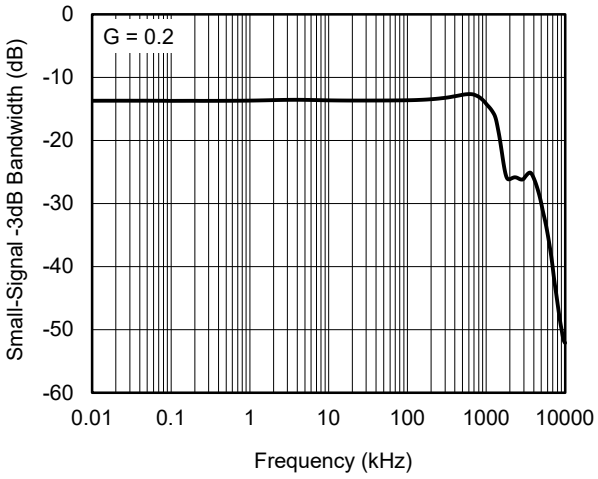
PSRR vs. Frequency (Referred-to-Input)



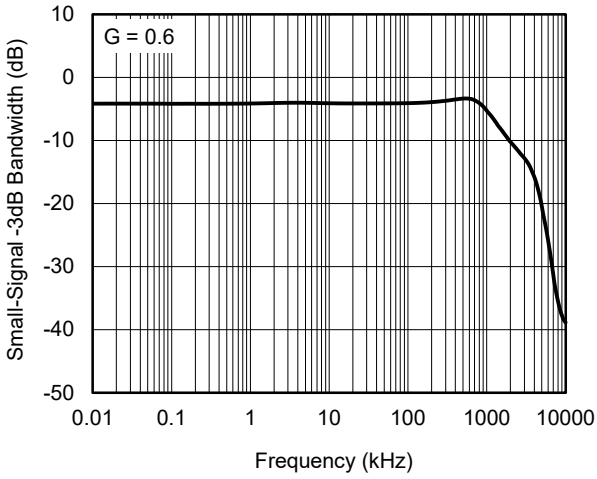
PSRR vs. Frequency (Referred-to-Input)



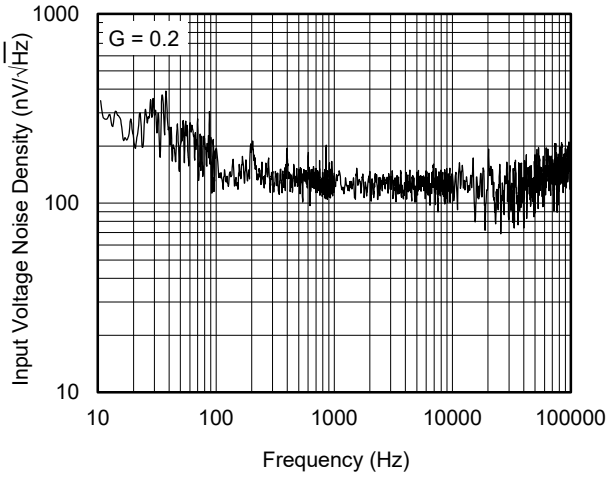
Small-Signal -3dB Bandwidth vs. Frequency



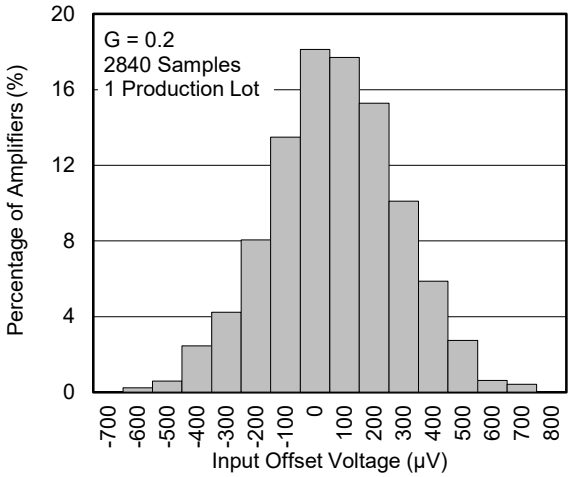
Small-Signal -3dB Bandwidth vs. Frequency



Input Voltage Noise Density vs. Frequency

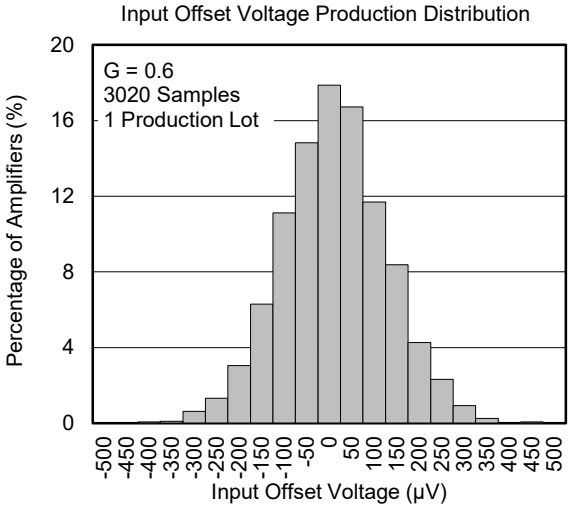


Input Offset Voltage Production Distribution



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, V_S = ±15V, unless otherwise noted.



APPLICATION INFORMATION

Typical Circuit

The typical application circuit of SGM8473 is shown in Figure 2:

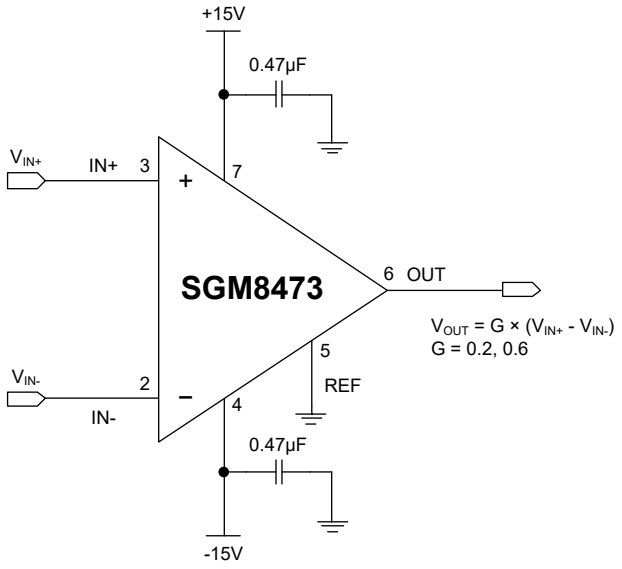


Figure 2. Typical Application Circuit

RF Interference

One of the characteristics of difference amplifier is rectifying the small signal which is out of the band. This kind of disturbance can be described as the small biased voltage. All the high frequency components can be filtered by the R-C network, which is placed in the input position of SGM8473, as shown in Figure 3. The following equation shows the equation of filtering frequency for the differential and common mode part of the input signal.

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

$C_D \geq 10C_C$ is required in the above equation.

The capacitor C_D influences the quality of the differential signal, while C_C influences the quality of the common mode signal. The common mode rejection ratio would be reduced if the R × C_C is mismatched. To reduce this negative influence and obtain a good CMRR, it is recommended that the capacitance of C_D should be 10 times larger than C_C. To conclude, the larger the ratio of C_D:C_C is, the less negative influence on the circuit.

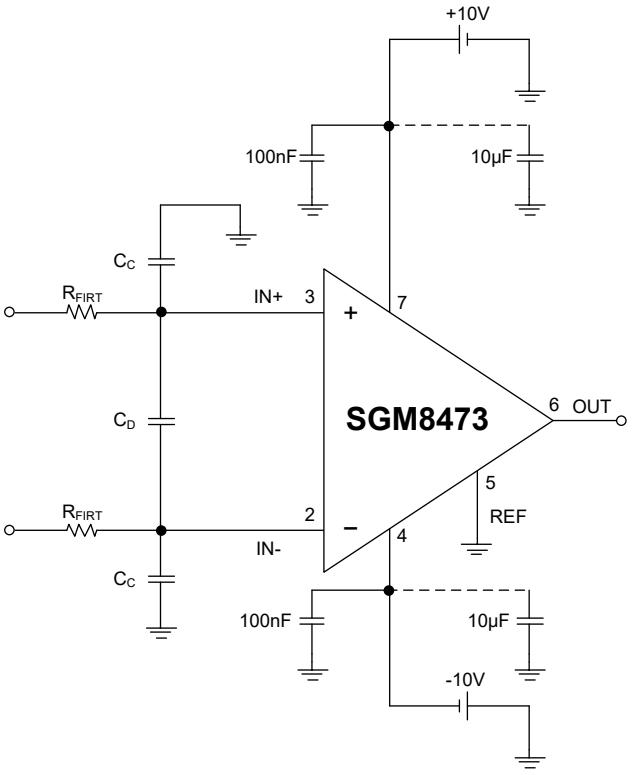


Figure 3. Using Input Low-Pass Filter to Reduce the Interference of RF

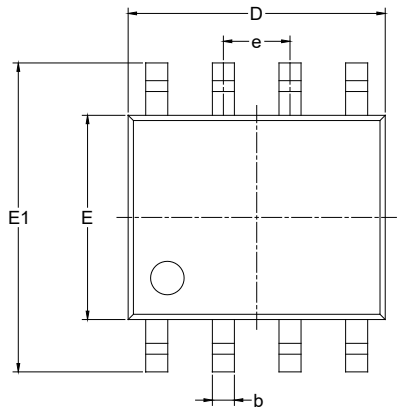
REVISION HISTORY

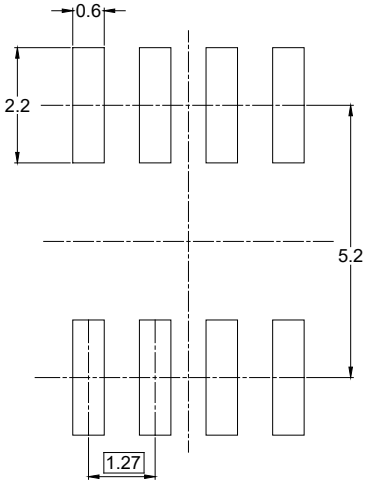
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (FEBRUARY 2025) to REV.A	Page
Changed from product preview to production data	All

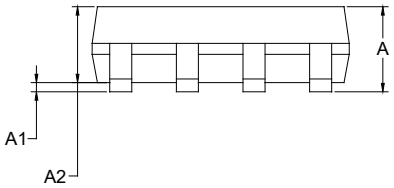
PACKAGE OUTLINE DIMENSIONS

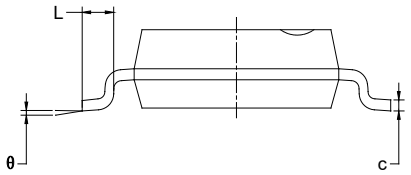
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)



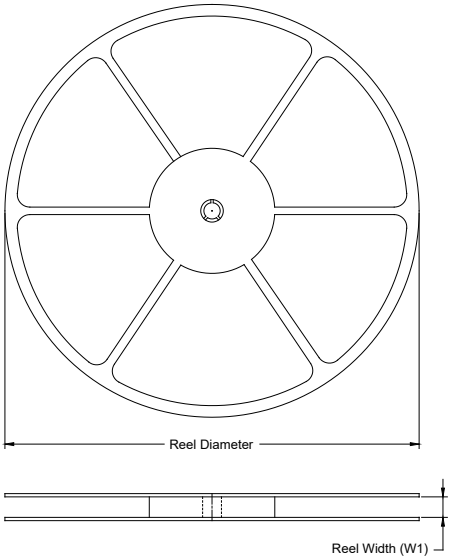


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

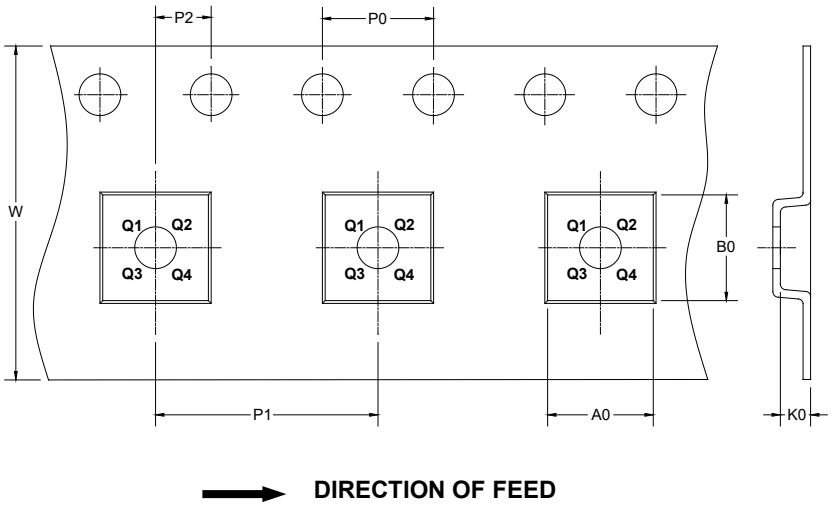
NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



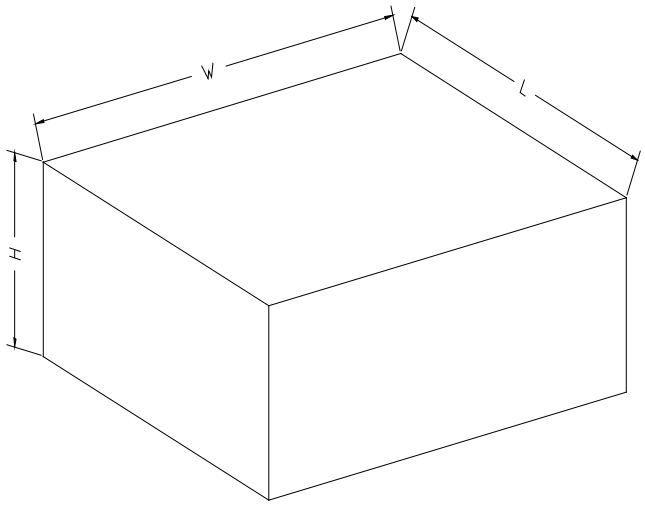
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002