SGM90509
8-Channel, 12-Bit, Configurable ADC/DAC with On-Chip Reference, SPI Interface

GENERAL DESCRIPTION

The SGM90509 features 8 input/output (I/O) pins, which can be independently configured as voltage digital-to-analog converter (DAC) outputs, analog-to-digital converter (ADC) inputs, digital outputs, or digital inputs. When an I/O pin is configured as a DAC output, it is from a 12-bit DAC output. The output range of the DAC can be configured to 0V to V_{REF} or 0V to 2 × V_{REF} by software. When an I/O pin is configured as an ADC input, its input goes to a 12-bit ADC through the multiplexer. The ADC input range can be configured to V_{REF} or 2 × V_{REF} by software. The I/O pins can also be configured as digital general-purpose input or output (GPIO) pins.

The SGM90509 is operated by a serial peripheral interface (SPI).

The SGM90509 contains an integrated 2.5V, 10ppm/℃ (TYP) reference, and an on-chip temperature sensor, which gives an estimation of the die temperature.

The SGM90509 is available in Green TSSOP-16, TQFN-3×3-16BL and WLCSP-2.05×2.05-16B packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Configurable 8 I/O Pins**
  - **8 Channels, 12-Bit DAC**
  - **8 Channels, 12-Bit ADC**
  - **8 Channels, GPIO**
- **On-Chip Temperature Sensor**
- **Supply Monitor**
- **SPI Interface**
- **Available in Green TSSOP-16, TQFN-3×3-16BL and WLCSP-2.05×2.05-16B Packages**

APPLICATIONS

Optical Module
Industrial Automation
General-Purpose Analog and Digital I/O

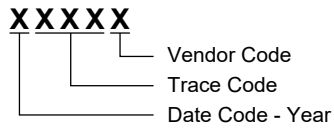
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM90509	TSSOP-16	-40℃ to +125℃	SGM90509XTS16G/TR	SGM90509 XTS16 XXXXX	Tape and Reel, 4000
	TQFN-3×3-16BL	-40℃ to +125℃	SGM90509XTSK16G/TR	00WSK XXXXX	Tape and Reel, 4000
	WLCSP-2.05×2.05-16B	-40℃ to +125℃	SGM90509XG/TR	90509 XXXXX XX#XX	Tape and Reel, 3000

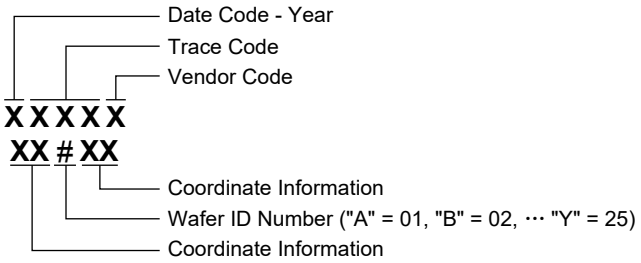
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.

TSSOP-16/TQFN-3×3-16BL



WLCSP-2.05×2.05-16B



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

V_{DD} (1) ..... -0.3V to 6V

V_{LOGIC} (1) ..... -0.3V to 6V

Analog Input Voltage ..... -0.3V to V_{DD} + 0.3V

Digital Input Voltage ..... -0.3V to V_{LOGIC} + 0.3V

Digital Output Voltage ..... -0.3V to V_{LOGIC} + 0.3V

V_{REF} ..... -0.3V to V_{DD} + 0.3V

Package Thermal Resistance

TSSOP-16, θ_{JA} ..... 88℃/W

TQFN-3×3-16BL, θ_{JA} ..... 91℃/W

WLCSP-2.05×2.05-16B, θ_{JA} ..... 97℃/W

Junction Temperature ..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s) ..... +260℃

ESD Susceptibility

HBM 1500V

CDM 500V

NOTE:

1. V_{DD} is powered up first, and the V_{DD} voltage must be higher than or equal to the V_{LOGIC} voltage.

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

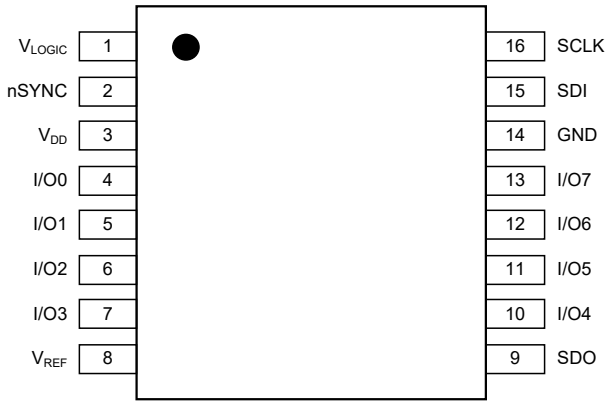
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

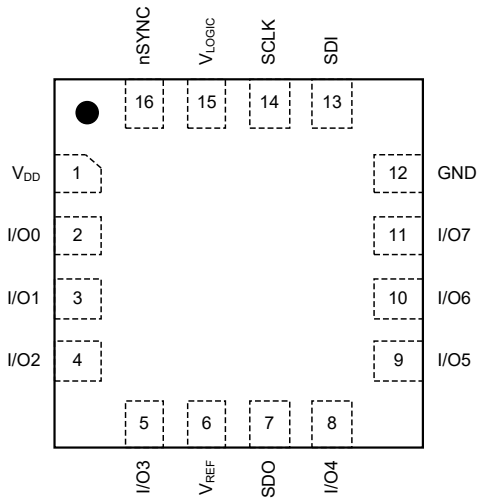
PIN CONFIGURATIONS

(TOP VIEW)



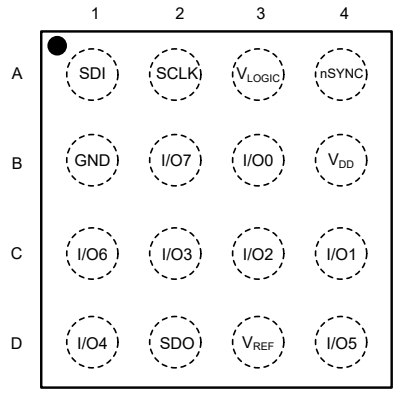
TSSOP-16

(TOP VIEW)



TQFN-3×3-16BL

(TOP VIEW)



WLCSP-2.05×2.05-16B

PIN DESCRIPTION

PIN			NAME	FUNCTION
TSSOP-16	TQFN-3×3-16BL	WLCSP-2.05×2.05-16B		
1	15	A3	V_{LOGIC}	Interface Power Supply Pin. The voltage range is from 1.7V to 5.5V.
2	16	A4	nSYNC	Frame Synchronization Input Pin. Active low. When this pin goes low, the data frame is shifted on the falling edges of the next 16 clocks.
3	1	B4	V_{DD}	Power Supply Pin. It can be operated from 2.7V to 5.5V. It needs a 0.1μF decoupled capacitor to GND.
4, 5, 6, 7, 10, 11, 12, 13	2, 3, 4, 5, 8, 9, 10, 11	B3, C4, C3, C2, D1, D4, C1, B2	I/O0 to I/O7	Input0/Output0 through Input7/Output7. These pins can be independently configured as DACs, ADCs, or GPIOs.
8	6	D3	V_{REF}	Reference Input/Output Pin.
9	7	D2	SDO	Data Output Pin. Logic output.
14	12	B1	GND	Ground.
15	13	A1	SDI	Data Input Pin. Logic input.
16	14	A2	SCLK	Serial Clock Input Pin.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), R_L = 2kΩ to GND, C_L = 200pF to GND, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Performance (f_{IN} = 1kHz Sine Wave)						
Resolution				12		Bits
Input Range		When using the internal ADC buffer, there is a dead band of 0mV to 5mV	0		V_{REF}	V
			0		2 × V_{REF}	
Integral Nonlinearity	INL		-1.74		1.97	LSB
Differential Nonlinearity	DNL		-1		1	LSB
Offset Error	E_O		-14		14	mV
Gain Error	E_G		-0.26		0.38	% FSR
Throughput Rate (1)					250	kSPS
Track Time (1)	t_{TRACK}		500			ns
Conversion Time (1)	t_{CONV}				2	μs
Signal-to-Noise Ratio	SNR	V_{DD} = 2.7V, input range = 0V to V_{REF}		69		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		67		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		66		
Signal-to-Noise + Distortion	SINAD	V_{DD} = 2.7V, input range = 0V to V_{REF}		69		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		67		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		66		
Total Harmonic Distortion	THD	V_{DD} = 2.7V, input range = 0V to V_{REF}		-93		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		-93		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		-76		
Spurious Free Dynamic Range	SFDR	V_{DD} = 2.7V, input range = 0V to V_{REF}		93		dB
		V_{DD} = 3.3V, input range = 0V to V_{REF}		93		
		V_{DD} = 5.5V, input range = 0V to 2 × V_{REF}		76		
Channel-to-Channel Isolation		f_{IN} = 1kHz		-95		dB
Input Capacitance (2)				25		pF
Full Power Bandwidth		At -3dB		22		MHz
		At -0.1dB		3		
DAC Performance (3)						
Resolution				12		Bits
Output Range			0		V_{REF}	V
			0		2 × V_{REF}	
Integral Nonlinearity	INL		-4.5		3.5	LSB
Differential Nonlinearity	DNL		-0.99		1	LSB
Offset Error	E_O		-21		22	mV
Offset Error Drift (1)				9		μV/℃
Gain Error	E_G	Output range = 0V to V_{REF}	-0.7		0.92	% FSR
		Output range = 0V to 2 × V_{REF}	-0.87		0.6	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), R_L = 2kΩ to GND, C_L = 200pF to GND, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero-Code Error				1.4	12	mV
Total Unadjusted Error	TUE	Output range = 0V to V_{REF}		±0.05	±1.14	% FSR
		Output range = 0V to 2 × V_{REF}		±0.18	±1	
Capacitive Load Stability (1)		R_{LOAD} = ∞			2	nF
		R_{LOAD} = 1kΩ			10	
Resistive Load (2)			1			kΩ
Short-Circuit Current				25		mA
DC Crosstalk (1)		Due to single channel, full-scale output change	-4		4	μV
DC Output Impedance				0.2		Ω
DC Power Supply Rejection Ratio (1)	PSRR	DAC code = mid-scale, V_{DD} = 3V ± 10% or 5V ± 10%		0.02		mV/V
Load Impedance at Rails (4)				57		Ω
Load Regulation		V_{DD} = 5V ± 10%, DAC code = mid-scale, -10mA ≤ I_{OUT} ≤ 10mA		180		μV/mA
		V_{DD} = 3V ± 10%, DAC code = mid-scale, -10mA ≤ I_{OUT} ≤ 10mA		150		
Power-Up Time		Exiting power-down mode, V_{DD} = 5V		5		μs
AC Specifications						
Slew Rate		Measured from 10% to 90% of full-scale		0.5		V/μs
Settling Time		¼ scale to ¾ scale settling to 1LSB		3.6		μs
DAC Glitch Impulse				4		nV-sec
DAC to DAC Crosstalk				1.3		nV-sec
Digital Crosstalk				0.1		nV-sec
Analog Crosstalk				1		nV-sec
Digital Feedthrough				0.1		nV-sec
Multiplying Bandwidth		DAC code = full-scale, output range = 0V to V_{REF}		240		kHz
Output Voltage Noise Spectral Density		DAC code = mid-scale, output range = 0V to 2 × V_{REF}, measured at 10kHz		210		nV/√Hz
Signal-to-Noise Ratio	SNR			79		dB
Spurious Free Dynamic Range	SFDR			81		dB
Signal-to-Noise + Distortion	SINAD			75		dB
Total Harmonic Distortion	THD			-77		dB
Reference Input						
V_{REF} Input Voltage			2		V_{DD}	V
Reference Input Impedance		DAC output range = 0V to 2 × V_{REF}		15		kΩ
		DAC output range = 0V to V_{REF}		20		
Reference Output						
V_{REF} Output Voltage		At ambient	2.484	2.5	2.516	V
		Factory precision	2.498	2.5	2.502	
V_{REF} Temperature Coefficient				10		ppm/℃

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), R_L = 2kΩ to GND, C_L = 200pF to GND, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Output							
Capacitive Load Stability		R_L = 2kΩ			5		μF
Output Impedance (1)		V_{DD} = 2.7V			0.15		Ω
		V_{DD} = 5V			0.25		
Output Voltage Noise		0.1Hz to 10Hz			25		μVp-p
Output Voltage Noise Density		At ambient, f = 1kHz, C_L = 1μF			210		nV/√Hz
Output Current Load Capability		V_{DD} ≥ 3V			±5		mA
GPIO Input							
High Input Voltage	V_{IH}			0.7 × V_{DD}			V
Low Input Voltage	V_{IL}					0.3 × V_{DD}	V
Input Capacitance (1)					20		pF
Hysteresis					0.5		V
Input Current					±1		μA
GPIO Output							
High Output Voltage	V_{OH}	I_{SOURCE} = 1mA	V_{DD} = 2.7V	2.3			V
			V_{DD} = 5.5V	5.2			
Low Output Voltage	V_{OL}	I_{SINK} = 1mA	V_{DD} = 2.7V			0.4	V
			V_{DD} = 5.5V			0.4	
Logic Input							
High Input Voltage	V_{INH}			0.7 × V_{LOGIC}			V
Low Input Voltage	V_{INL}					0.3 × V_{LOGIC}	V
Input Current	I_{IN}				±1		μA
Input Capacitance (1)	C_{IN}				10		pF
Logic Output (SDO)							
High Output Voltage	V_{OH}	I_{SOURCE} = 200μA	V_{DD} = 2.7V, V_{LOGIC} = 1.7V	1.5			V
			V_{DD} = 5.5V, V_{LOGIC} = 5.5V	5.3			
Low Output Voltage	V_{OL}	I_{SINK} = 200μA	V_{DD} = 2.7V, V_{LOGIC} = 1.7V			0.4	V
			V_{DD} = 5.5V, V_{LOGIC} = 5.5V			0.4	
Floating-State Output Capacitance (1)					10		pF
Temperature Sensor (1)							
Resolution					12		Bits
Operating Temperature Range				-40		125	℃
Accuracy					±3		℃
Track Time (1)	t_{TRACK}	ADC buffer enabled			2		μs
		ADC buffer disabled			2		
Supply Monitor Accuracy					0.5		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 5.5V, V_{REF} = 2.5V (internal), R_L = 2kΩ to GND, C_L = 200pF to GND, T_A = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Requirements							
Analog Supply Voltage	V_{DD}			2.7		5.5	V
Analog Supply Current	I_{DD}	Digital inputs = 0V or V_{DD}, I/O0 to I/O7 configured as DACs and ADCs, internal reference on, ADC buffer on, DAC code = 0xFFF, range is 0V to 2 × V_{REF} for DACs and ADCs				5	mA
		Power-down mode				350	μA
		Normal mode, V_{DD} = 5V	I/O0 to I/O7 are DACs, internal reference, gain = 2		1.15		mA
			I/O0 to I/O7 are DACs, external reference, gain = 2		0.9		
			I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 2		2.4		
			I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 2		2.17		
			I/O0 to I/O7 are ADCs, internal reference, gain = 2		1.94		
			I/O0 to I/O7 are ADCs, external reference, gain = 2		1.7		
			I/O0 to I/O7 are general-purpose outputs		0.66		
			I/O0 to I/O7 are general-purpose inputs		0.66		
			I/O0 to I/O3 are general-purpose outputs, I/O4 to I/O7 are general-purpose inputs		0.66		
		Normal mode, V_{DD} = 3V	I/O0 to I/O7 are DACs, internal reference, gain = 1		0.92		mA
			I/O0 to I/O7 are DACs, external reference, gain = 1		0.73		
			I/O0 to I/O7 are DACs and sampled by the ADC, internal reference, gain = 1		2.15		
			I/O0 to I/O7 are DACs and sampled by the ADC, external reference, gain = 1		1.96		
			I/O0 to I/O7 are ADCs, internal reference, gain = 1		1.75		
			I/O0 to I/O7 are ADCs, external reference, gain = 1		1.56		
			I/O0 to I/O7 are general-purpose outputs		0.5		
			I/O0 to I/O7 are general-purpose inputs		0.5		
Digital I/O Supply Voltage	V_{LOGIC}			1.7		V_{DD}	V
Digital I/O Supply Current	I_{LOGIC}					15	μA

NOTES:

1. Guaranteed by design and characterization. Not production tested.
2. All specifications are tested with an input signal at 0.5dB below full-scale, unless otherwise noted. All available input ranges are described in full-scale input range (FSR), but not performance guaranteed.
3. DC specifications are tested when the output is floating, unless otherwise noted. The linearity is calculated with the code range of 64 to 4032.
4. When drawing a load current at either power rail, there will be a voltage dropping respect to the power rail as there is a 57Ω typical output impedance of the chip output channel. For example, when sourcing 1mA, the minimum output voltage dropping = 57Ω × 1mA = 57mV.

TIMING CHARACTERISTICS

(All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$, T_A = -40℃ to +125℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SCLK Cycle Time	t_1	Write operation	$1.7V \le V_{LOGIC} < 3V$	33			ns
			$3V \le V_{LOGIC} \le 5.5V$	20			
		Read operation	$1.7V \le V_{LOGIC} < 3V$	65			
			$3V \le V_{LOGIC} \le 5.5V$	50			
SCLK High Time	t_2	$1.7V \le V_{LOGIC} < 3V$		16			ns
		$3V \le V_{LOGIC} \le 5.5V$		10			
SCLK Low Time	t_3	$1.7V \le V_{LOGIC} < 3V$		16			ns
		$3V \le V_{LOGIC} \le 5.5V$		10			
nSYNC Falling Edge to SCLK Falling Edge Setup Time (2)	t_4	$1.7V \le V_{LOGIC} < 3V$		1.7			μs
		$3V \le V_{LOGIC} \le 5.5V$		1.7			
Data Setup Time	t_5	$1.7V \le V_{LOGIC} < 3V$		7			ns
		$3V \le V_{LOGIC} \le 5.5V$		7			
Data Hold Time	t_6	$1.7V \le V_{LOGIC} < 3V$		5			ns
		$3V \le V_{LOGIC} \le 5.5V$		5			
SCLK Falling Edge to nSYNC Rising Edge	t_7	$1.7V \le V_{LOGIC} < 3V$		15			ns
		$3V \le V_{LOGIC} \le 5.5V$		10			
Minimum nSYNC High Time for Register Write Operation	t_8	$1.7V \le V_{LOGIC} < 3V$		30			ns
		$3V \le V_{LOGIC} \le 5.5V$		30			
Minimum nSYNC High Time for Register Read Operation		$1.7V \le V_{LOGIC} < 3V$		60			ns
		$3V \le V_{LOGIC} \le 5.5V$		60			
SCLK Rising Edge to SDO Valid	t_9	$1.7V \le V_{LOGIC} < 3V$				56	ns
		$3V \le V_{LOGIC} \le 5.5V$				25	

NOTES:

1. Guaranteed by design and characterization. Not production tested.

2. For high-speed applications, the SGM90509 supports the minimum t_4 value of 30ns. In this case, the ADC maximum throughput rate can be up to 400kSPS, and the typical SNR is 60dB. The 400kSPS throughput rate and 60dB SNR are guaranteed only by the characteristic test results with limited samples. For the best ADC performance, t_4 > 1.7μs and t_8 > 500ns are required. Otherwise, t_4 > 30ns and t_8 > 500ns are required for reading ADC, t_4 > 30ns and t_8 > 60ns are required for reading registers, and t_4 > 30ns and t_8 > 30ns are required for writing registers.

TIMING DIAGRAM

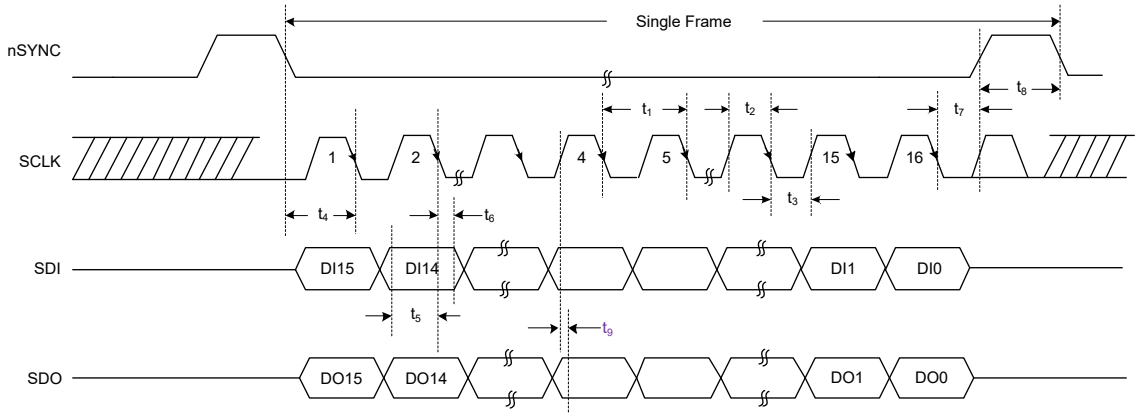
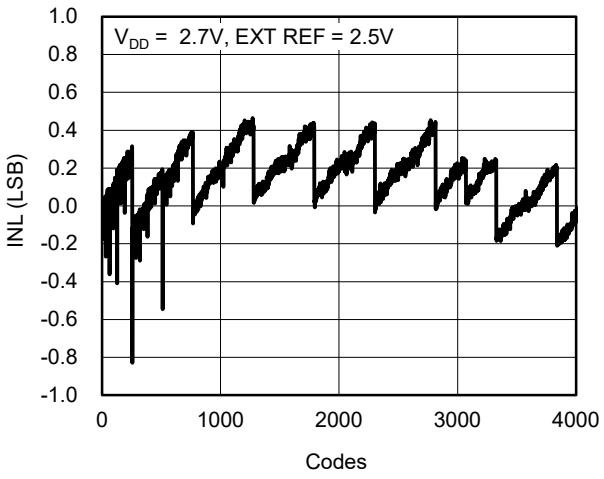


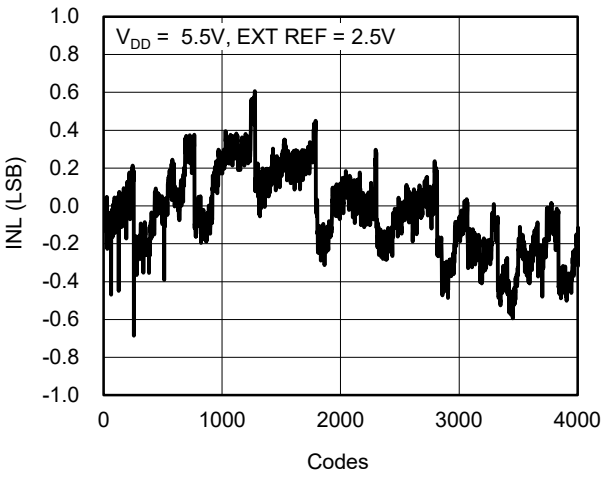
Figure 1. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

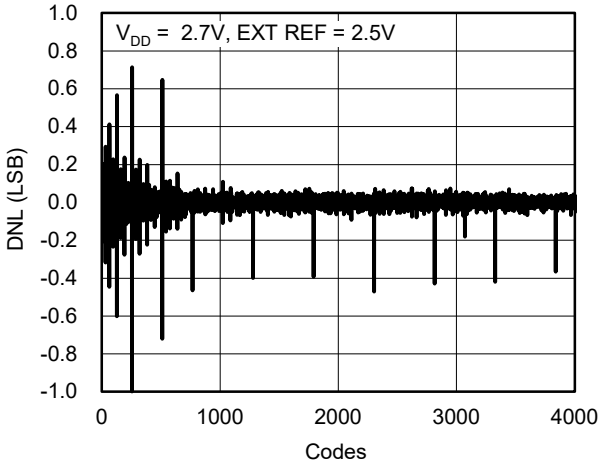
ADC INL (V_{DD} = 2.7V)



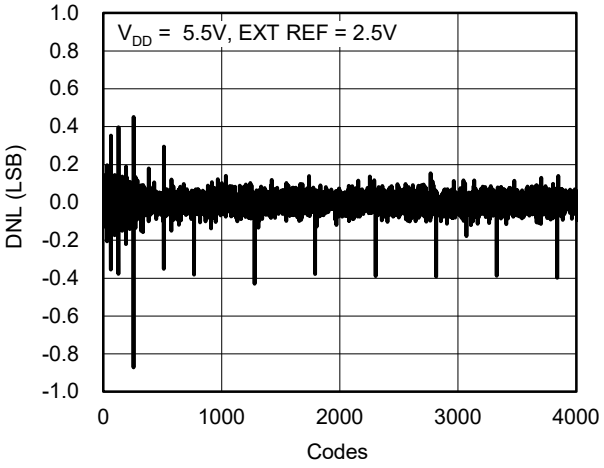
ADC INL (V_{DD} = 5.5V)



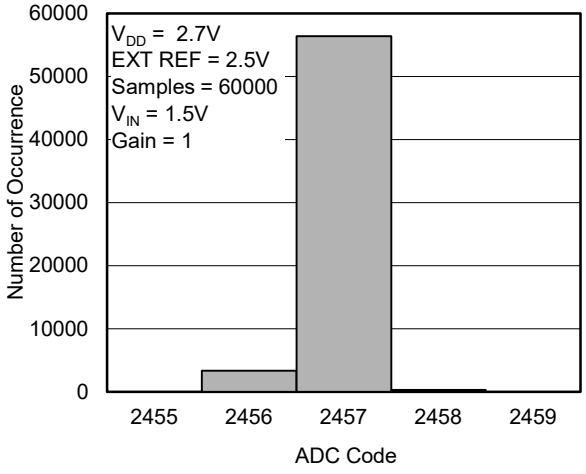
ADC DNL (V_{DD} = 2.7V)



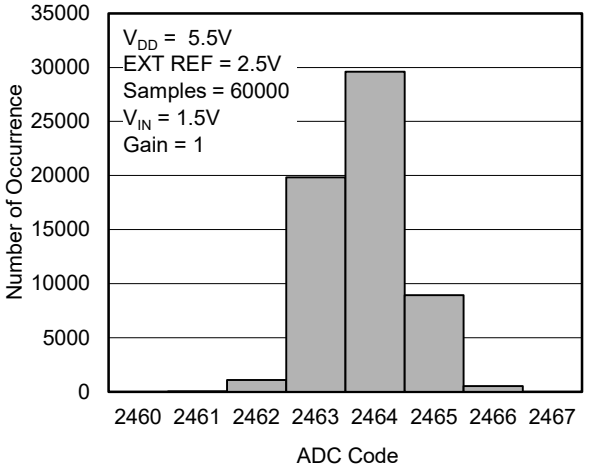
ADC DNL (V_{DD} = 5.5V)



Histogram of ADC Codes (V_{DD} = 2.7V)

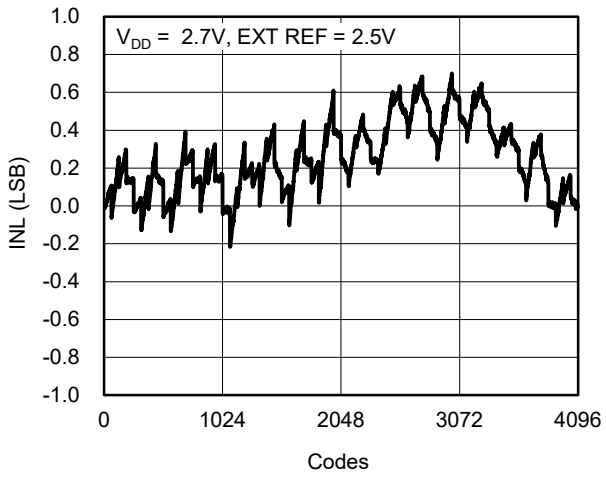


Histogram of ADC Codes (V_{DD} = 5.5V)

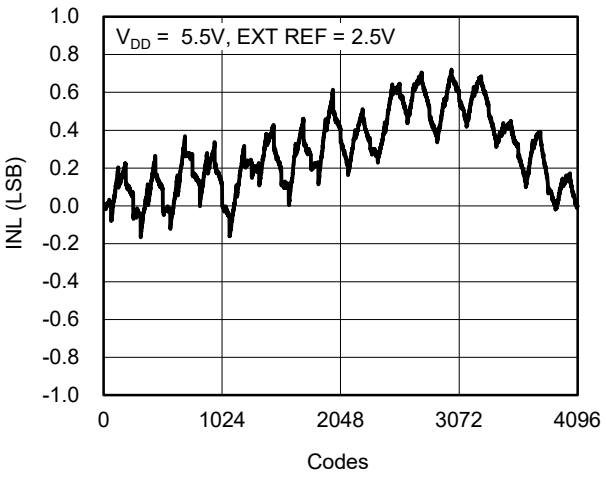


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

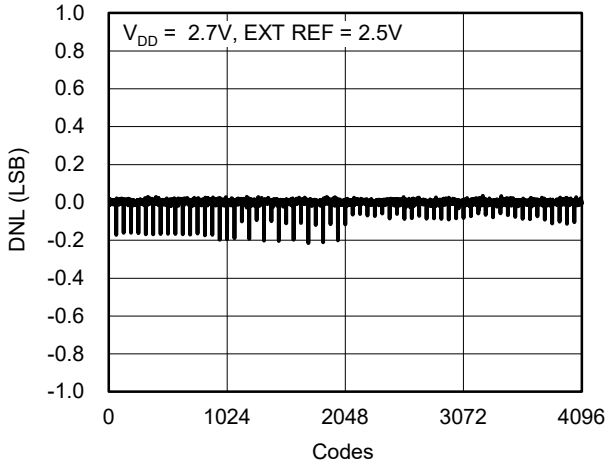
DAC INL (V_{DD} = 2.7V)



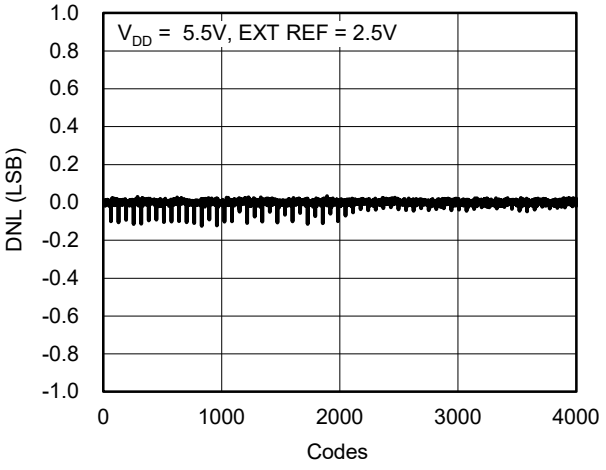
DAC INL (V_{DD} = 5.5V)



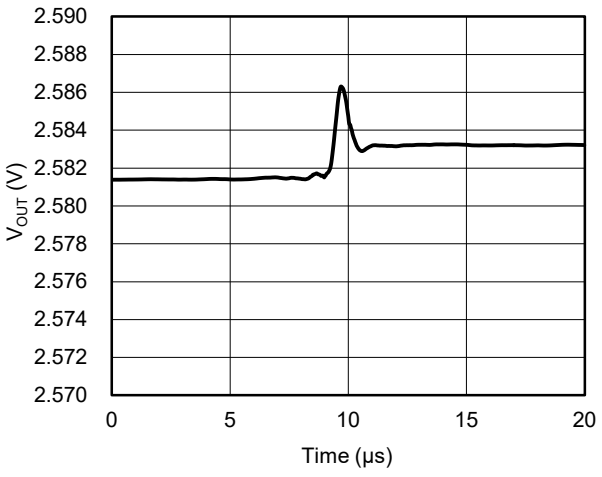
DAC DNL (V_{DD} = 2.7V)



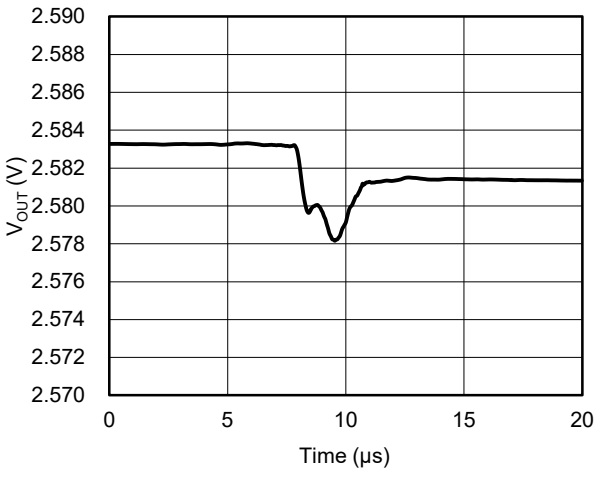
DAC DNL (V_{DD} = 5.5V)



DAC Digital-to-Analog Glitch (Rising)

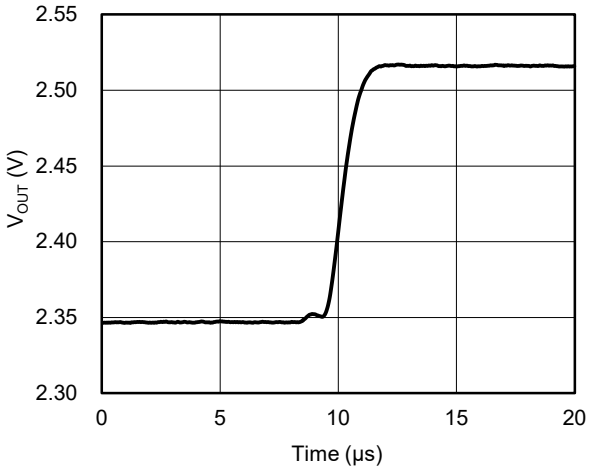


DAC Digital-to-Analog Glitch (Falling)

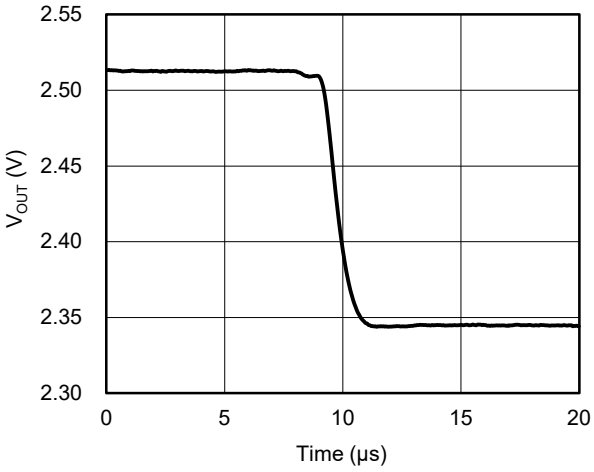


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

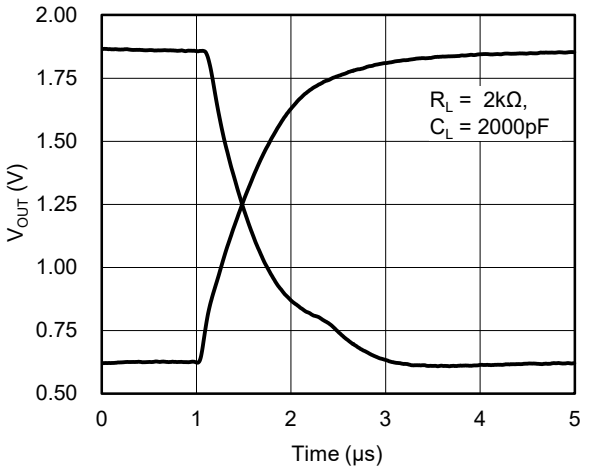
DAC Settling Time (100 Code Change Rising Edge)



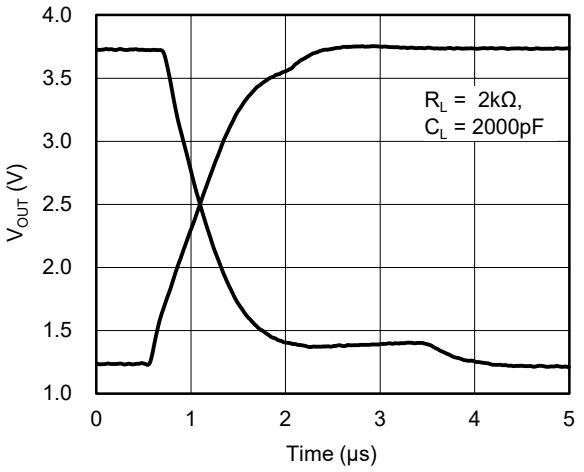
DAC Settling Time (100 Code Change Falling Edge)



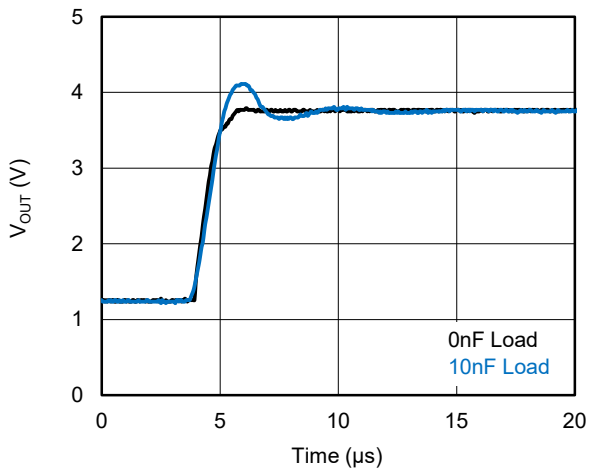
DAC Settling Time (Output Range = 0V to V_{REF})



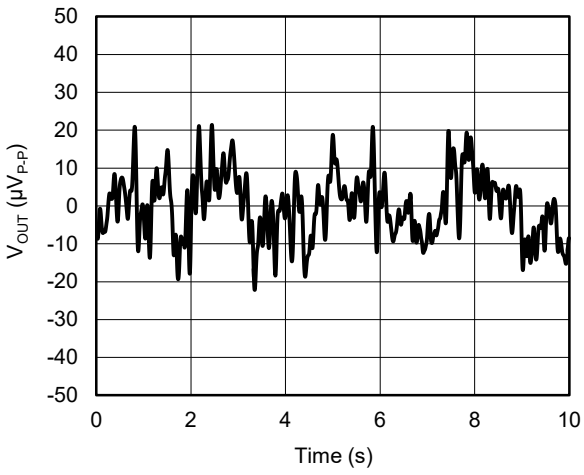
DAC Settling Time (Output Range = 0V to 2 × V_{REF})



DAC Settling Time vs. Capacitive Load

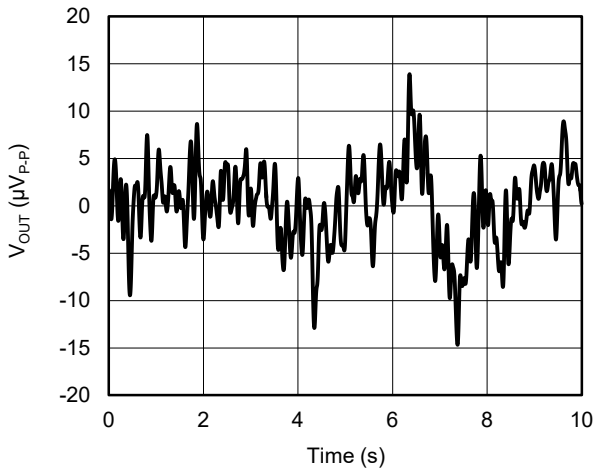


Internal Reference 1/f Noise

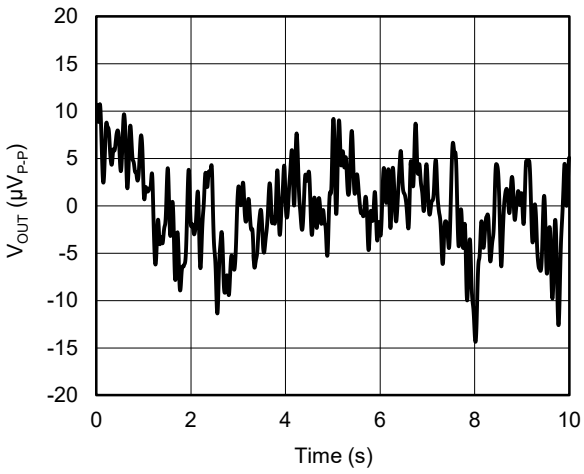


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

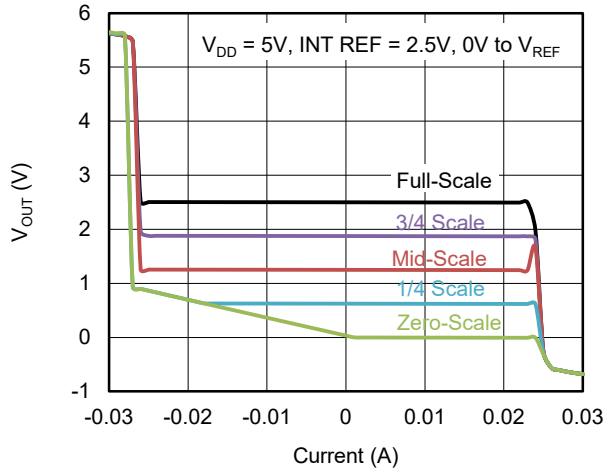
DAC 1/f Noise with External Reference



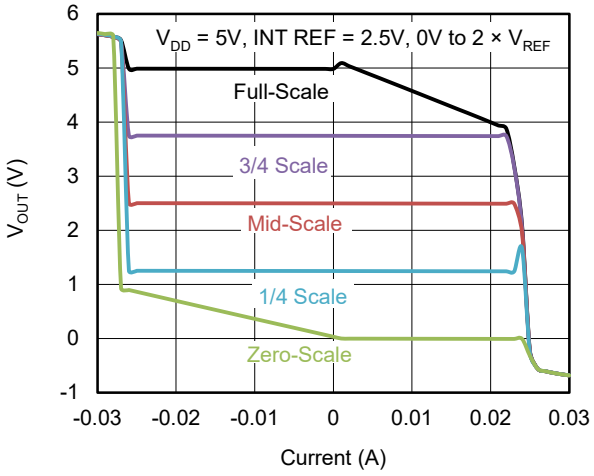
DAC 1/f Noise with Internal Reference



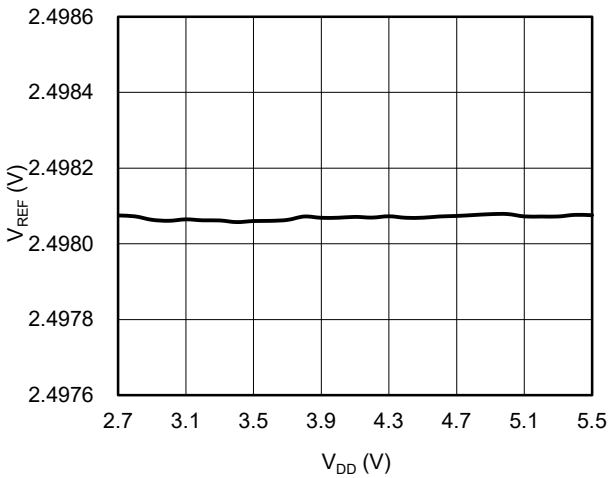
DAC Output Sink and Source Capability



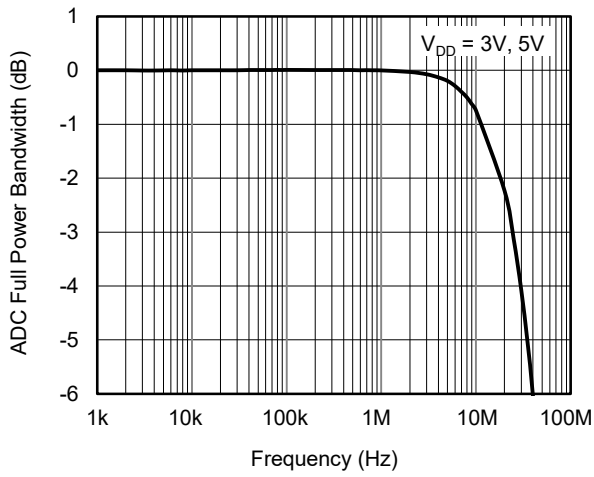
DAC Output Sink and Source Capability



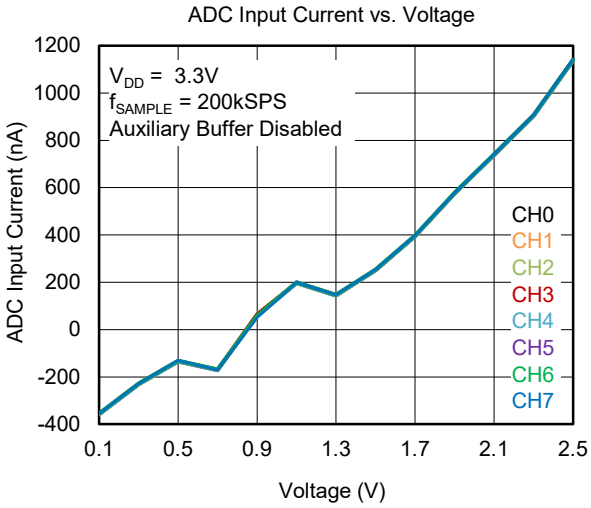
Reference Line Regulation

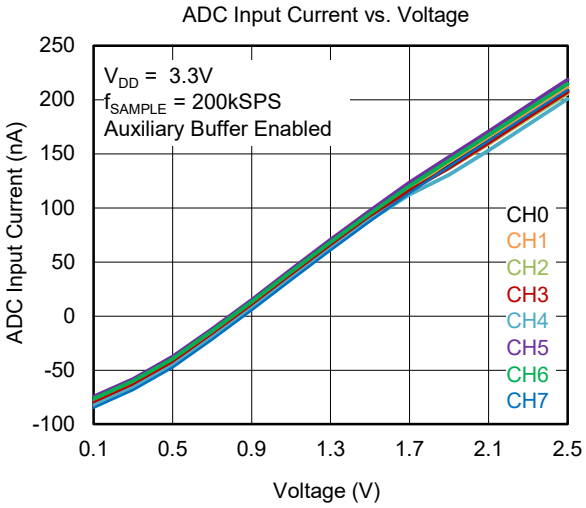


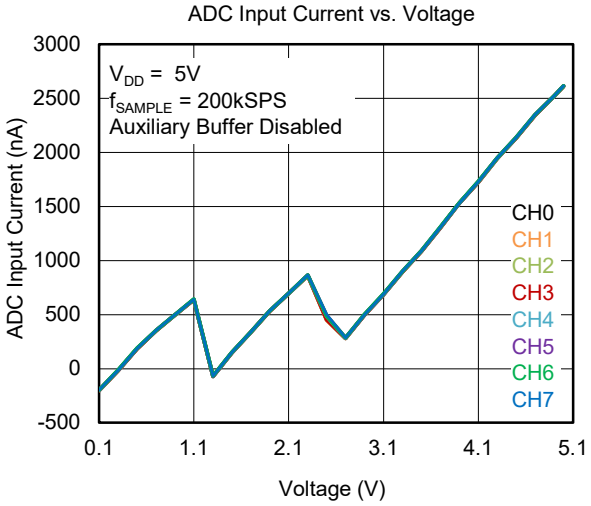
ADC Full Power Bandwidth vs. Frequency

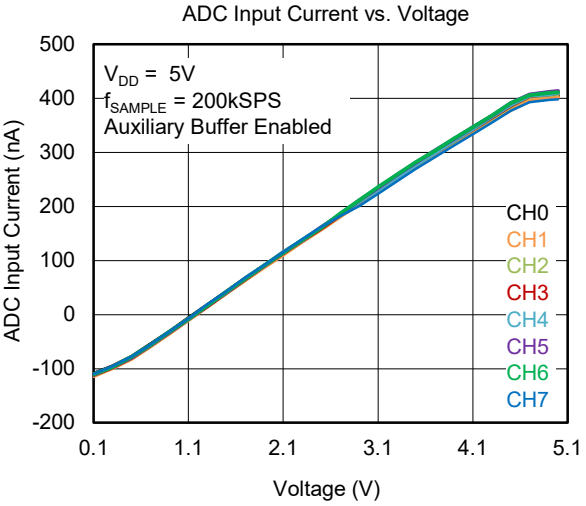


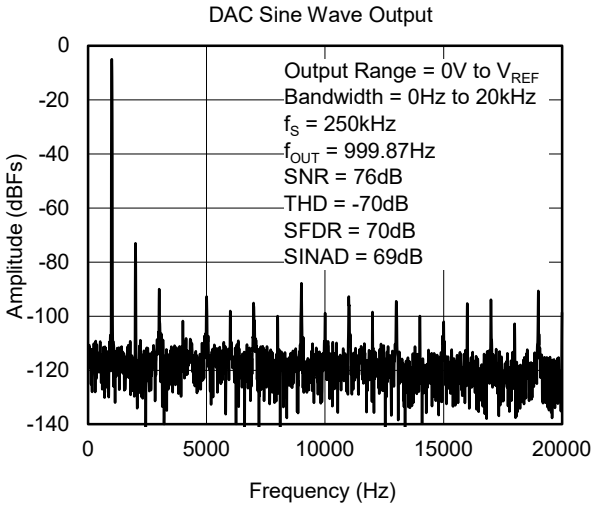
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

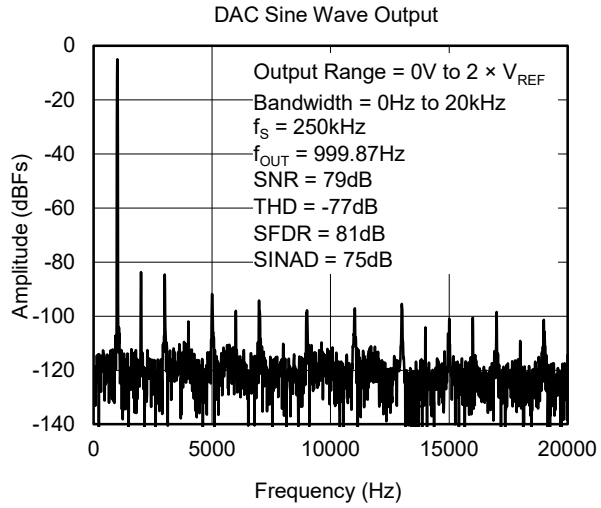






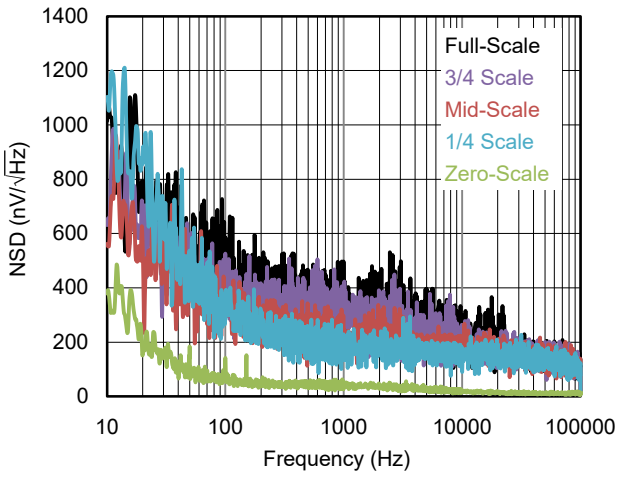




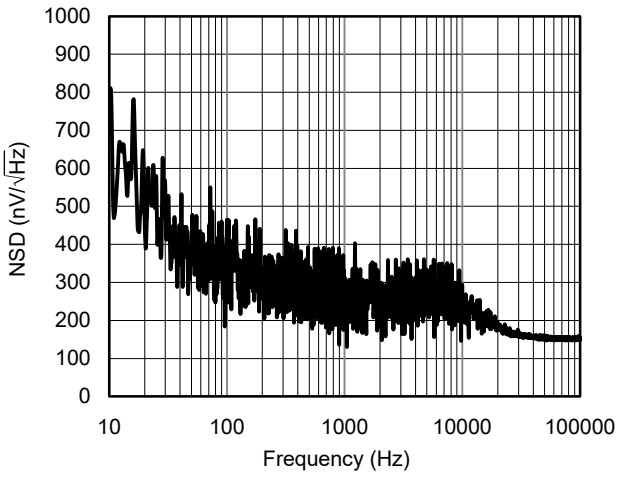


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

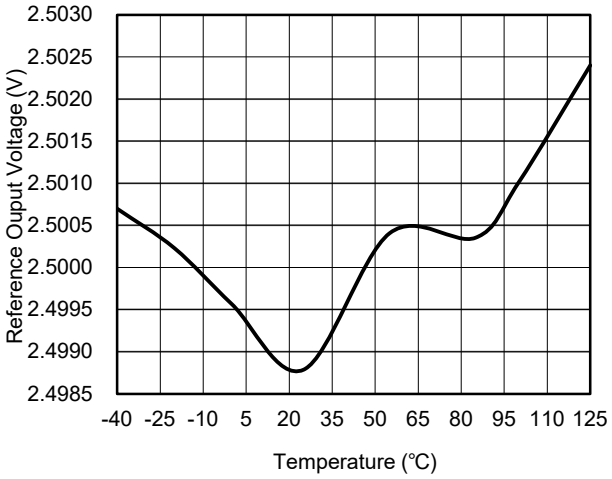
DAC Output Noise Spectral Density (NSD)



Reference Noise Spectral Density (NSD)



Reference Output Voltage vs. Temperature



FUNCTIONAL BLOCK DIAGRAM

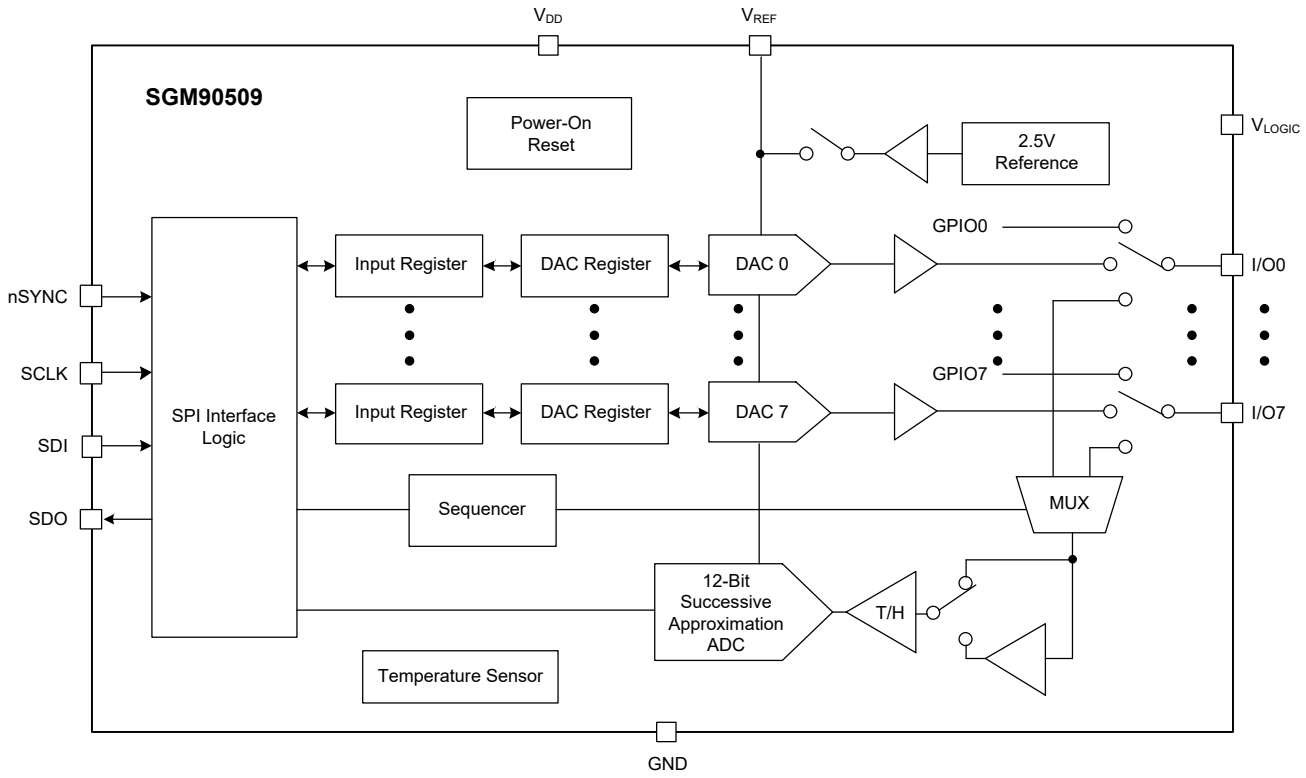


Figure 2. Block Diagram

DETAILED DESCRIPTION

DAC Section

The SGM90509 has eight 12-bit DACs. The DAC output range can be set to 0V to V_{REF} or 0V to 2 × V_{REF}. And the output range configuration is shared by all channels. The input code to the DAC is straight binary, so the ideal output voltage can be calculated based on the following equation:

$$V_{OUT} = G \times V_{REF} \times \left(\frac{D_{IN}}{2^N} \right) \quad (1)$$

Where:

G = 1 for an output range of 0V to V_{REF} or G = 2 for an output range of 0V to 2 × V_{REF}.

V_{REF} = Voltage on the V_{REF} pin.

D_{IN} = Decimal equivalent of the binary code, which is loaded to the DAC register. It can range from 0 to 4095.

N = 12.

ADC Section

The ADC is a fast, 12-bit, single-supply ADC. Each conversion takes 2μs. The ADC input range can be configured as 0V to V_{REF} or 0V to 2 × V_{REF}. All ADC channels share the same input range. The ADC output code is straight binary format. It is possible to set an I/Ox pin as both a DAC and an ADC. In this case, the I/O is a DAC output, and at the same time, the DAC voltage can be read back by an ADC conversion and read sequence. The ADC conversion result is in 16-bit format, please refer to Table 1.

GPIO Section

Each I/Ox pins can be used as a GPIO pin. An output can be set by write data register. An input can be read by configuration register. When an I/Ox pin is set as an output, it is possible to read its status by also setting it as an input pin at the same time.

Internal Reference

The SGM90509 has an on-chip 2.5V reference. The internal reference is powered off by default. To enable the internal reference, the bit D9 is set in the power-down and reference control register (refer to Table 18).

Temperature Sensor

The SGM90509 has an integrated temperature sensor that can be used to estimate the temperature of die. The temperature conversion time is 3μs, whether the ADC buffer is enabled or not. To enable the temperature sampling, set the bit D8 in the ADC sequence register (refer to Table 10).

Calculation of the temperature is shown below:

When ADC gain = 1:

$$\text{Temperature}(℃) = 25 + \frac{(\text{ADC Code} - (0.56/V_{REF}) \times 4095)}{(3.015 \times (2.5/V_{REF}))} \quad (2)$$

When ADC gain = 2:

$$\text{Temperature}(℃) = 25 + \frac{(\text{ADC Code} - (0.56/(2 \times V_{REF})) \times 4095)}{(1.508 \times (2.5/V_{REF}))} \quad (3)$$

The codes range returned by the ADC is approximately 721 to 1219, and its temperature range is from -40℃ to +125℃.

Serial Interface

The SGM90509 has an SPI-compatible interface. Please refer to Table 2 for the input shift register in 16-bit format. The control register maps are shown in Table 3.

Table 1. ADC Conversion Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ADC Address			12-Bit ADC Data											

Table 2. Input Shift Register Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Control Register Address				0	0	Control Register Data								
1	DAC Address			12-Bit DAC Data											

DETAILED DESCRIPTION (continued)

Table 3. Control Register Maps

MSB (D15)	Address (D[14:11])	Register Name	Description	Default Value
0	0000	NOP	No operation	0x000
0	0001	DAC Readback	Select and enable DAC readback	0x000
0	0010	ADC Sequence Register	Select ADC channels for conversion	0x000
0	0011	General-Purpose Control Register	DAC and ADC control register	0x000
0	0100	ADC Pin Configuration Register	Configure pins working as ADC inputs	0x000
0	0101	DAC Pin Configuration Register	Configure pins working as DAC outputs	0x000
0	0110	Pull-Down Configuration Register	Configure pins with a 85kΩ pull-down resistor to GND	0x0FF
0	0111	Readback and LDAC Mode Register	Configure the operation of the load DAC (LDAC) function and/or which configuration register is read back	0x000
0	1000	GPIO Write Configuration Register (1)	Configure pins working as general-purpose outputs	0x000
0	1001	GPIO Write Data Register	Write data to the general-purpose outputs	0x000
0	1010	GPIO Read Configuration Register	Configure pins working as general-purpose inputs	0x000
0	1011	Power-Down and Reference Control Register	Power down selected DAC channels and the internal reference	0x000
0	1100	GPIO Open-Drain Configuration Register	Configure open-drain or push/pull for general-purpose outputs	0x000
0	1101	Three-State Configuration	Configure which I/O pins are three-state	0x000
0	1110	Reserved	Reserved	
0	1111	Software Reset Register	Reset the SGM90509	0x000
1	XXXX (2)	DAC Write	Write to addressed DAC register	0x000

NOTES:
1. This register is also used to set I/O7 as an nBUSY output.
2. D[14:12] is the DAC register address (see Table 2).

Power-Up Time

When the system is power-on or there is a reset operation, it will take SGM90509 250μs to power up, it is not suggested to do any operation during this time.

Write Mode

Figure 1 shows the read and write timing for the SGM90509. A falling edge of nSYNC starts a write frame. Data is locked on the falling edge of SCLK. After 16 falling edges of SCLK, all 16-bit data is shifted in. Then nSYNC can be pulled high.

Read Mode

The SGM90509 supports data readback from the ADCs and control registers. ADC conversion result will be shifted out automatically when there is an operation on the chip. To read out a register, it is necessary to issue a write to the Readback and LDAC Mode register firstly to select which register to read back. Then the selected register content will be read out on the next nSYNC frame with 16 clocks falling edge.

DETAILED DESCRIPTION (continued)

Configuring the SGM90509

In order for the SGM90509 to work in the target state, a series of configuration registers need to be set. After power-up, the SGM90509 I/O pins are configured as 85kΩ resistors connected to GND by default. The I/O pins can be software re-configured as DAC outputs, ADC inputs, digital outputs, digital inputs, three-state, or connected to GND with 85kΩ pull-down resistors. The configuration operating can be issued at any time, when there is no any ADC conversion is on-going or a register is being read back. The lock configuration bit must also be 0 before a configuration is issued.

Table 4. I/Ox Pin Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Selects which pin configuration register is addressed. 0100 = ADC pin configuration 0101 = DAC pin configuration 0110 = Pull-down configuration (default condition at power-up) 1000 = GPIO write configuration 1010 = GPIO read configuration 1100 = GPIO open-drain configuration 1101 = Three-state configuration	0110
D[10:8]	Reserved	Reserved. Set these bits to 0.	000
D[7:0]	IO[7:0]	Enable register function on selected I/Ox pin. 0 = No function selected (default) 1 = Set the selected I/Ox pin to the register function	0000 0000

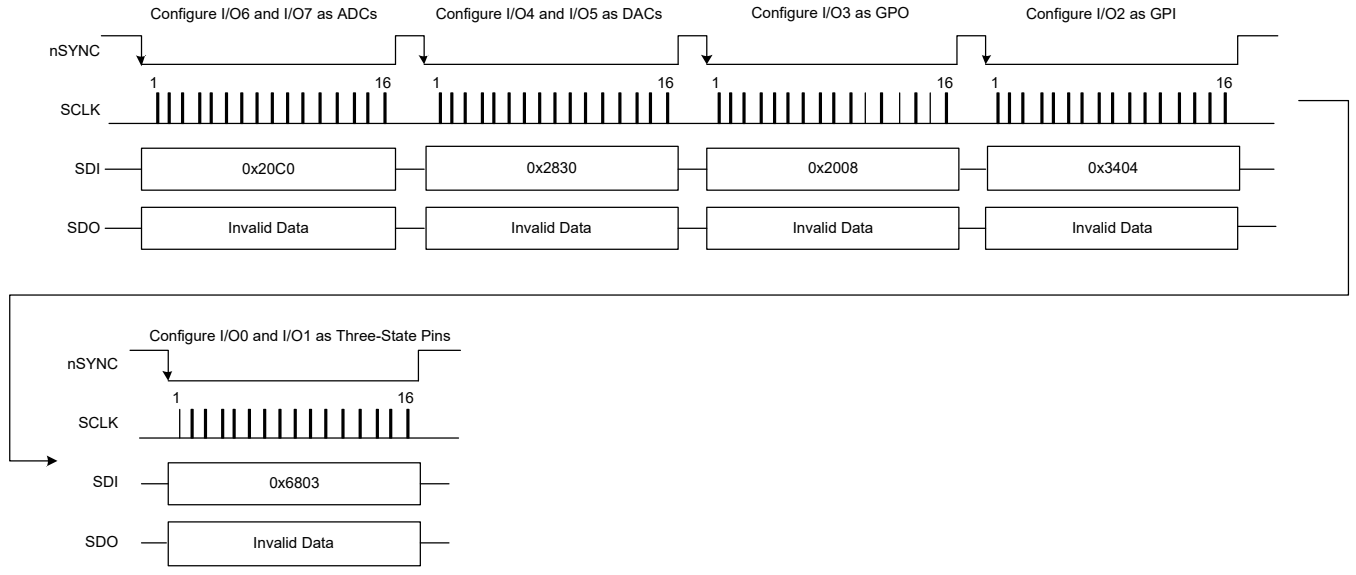


Figure 3. Typical Configuration Example

DETAILED DESCRIPTION (continued)

General-Purpose Control Register

Table 5. General-Purpose Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Must be set to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0011.	0011
D[10]	Reserved	Reserved. Must be set to 0.	0
D[9]	ADC Auxiliary Buffer Configuration	0 = ADC auxiliary buffer disabled (default) 1 = ADC auxiliary buffer enabled	0
D[8]	Reserved	Reserved. Must be set to 0.	0
D[7]	Lock	Lock Configuration 0 = The contents of the I/Ox pin configuration registers can be changed (default) 1 = The contents of the I/Ox pin configuration registers are locked	0
D[6]	Write All DACs	Writing All DACs Enable 0 = For the coming DAC writes, the DAC address bits determine which DAC channel is written to (default) 1 = For the coming DAC writes, the DAC address bits are ignored and all DAC channels configured as DACs are updated with the same data	0
D[5]	ADC Range	ADC Input Range Setting 0 = Set the ADC range 0V to V_{REF} (default) 1 = Set the ADC range 0V to 2 × V_{REF}	0
D[4]	DAC Range	DAC Output Range Setting 0 = Set the DAC range 0V to V_{REF} (default) 1 = Set the DAC range 0V to 2 × V_{REF}	0
D[3:0]	Reserved	Reserved. Must set these bits to 0.	0000

DAC Write Operation

The data is written to a DAC when the pointer byte is 0b0101 (see Table 6). Bits D[7:0] determine which DAC is addressed.

LDAC Mode Operation

LDAC function details please see Table 20.

Table 6. DAC Pin Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0101.	0101
D[10:8]	Reserved	Reserved. Set these bits to 0.	000
D[7:0]	DAC[7:0]	Select I/Ox Pins as DAC Outputs 0 = I/Ox function is determined by the pin configuration registers (default) 1 = I/Ox is a DAC output	0000 0000

Table 7. DAC Write Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 1.	1
D[14:12]	DAC Address[2:0]	Bits D[14:12] select the DAC register to which the data in D[11:0] bits is loaded. 000 = DAC0 001 = DAC1 010 = DAC2 011 = DAC3 100 = DAC4 101 = DAC5 110 = DAC6 111 = DAC7	000
D[11:0]	12-Bit DAC Data[11:0]	12-Bit DAC Data.	0000 0000 0000

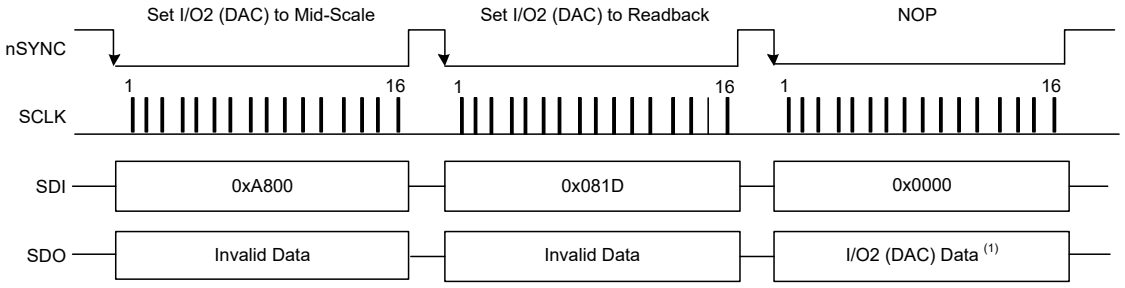
DETAILED DESCRIPTION (continued)

DAC Readback

The input register of each DAC can be read back via the SPI interface. The data can be read back from a DAC only when there is not an ADC conversion sequence taking place.

Table 8. DAC Readback Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0001.	0001
D[10:5]	Reserved	Reserved. Set these bits to 0.	00 0000
D[4:3]	Enable DAC Readback[1:0]	Enable Readback of the DAC Input Register 00 = Readback disabled (default) 11 = Readback enabled	00
D[2:0]	DAC Channel[2:0]	Select DAC Channel 000 = DAC0 (default) 001 = DAC1 010 = DAC2 011 = DAC3 100 = DAC4 101 = DAC5 110 = DAC6 111 = DAC7	000



NOTE:
1. D15 = 1, D[14:12] = DAC Address, D[11:0] = DAC Data.

Figure 4. DAC Readback Operation

DETAILED DESCRIPTION (continued)

ADC Operation

The SGM90509 is operated as same as usual multiplexer plus one core ADC architecture chip, where the current data reading selects the next channel for conversion.

Figure 5 to Figure 9 show how to configure the SGM90509 for ADC conversions.

Table 9. ADC Pin Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0100.	0100
D[10:8]	Reserved	Reserved. Set these bits to 0.	000
D[7:0]	ADC[7:0]	Select I/Ox Pins as ADC Inputs 0 = I/Ox function is determined by the pin configuration registers (default) 1 = I/Ox is an ADC input	0000 0000

Table 10. ADC Sequence Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0010.	0010
D[10]	V_{DD} Monitor Enable	V_{DD} Monitor Enable 0 = V_{DD} monitor disable (default) 1 = V_{DD} monitor enable, V_{DD}/4 will be converted by ADC, the result can be read by ADC data register, more details refer to Table 11.	0
D[9]	REP	ADC Sequence Repetition 0 = Sequence repetition disabled (default) 1 = Sequence repetition enabled	0
D[8]	TEMP	Include Temperature Sensor Sampling in ADC Sequence 0 = Disable temperature sensor readback (default) 1 = Enable temperature sensor readback	0
D[7:0]	ADC[7:0]	Select Corresponding ADC Channels in Conversion Sequence 0 = The selected ADC channel is not enabled in the conversion sequence (default) 1 = The selected ADC channel is enabled in the conversion sequence	0000 0000

Table 11. ADC Data Register Format

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	ADC Address (1)			12-Bit ADC Data											
1	000 (2)			12-Bit Temperature Sensor Channel Data											
1	001 (3)			12-Bit V_{DD}/4 Channel Data											

NOTES:
1. When D[15] = 0, the ADC addresses are as follows: 000 = ADC0, …, 111 = ADC7.
2. When D[15:12] = 1000, ADC result is internal temperature sensor sampling data.
3. When D[15:12] = 1001, ADC result is V_{DD}/4 sampling data.

DETAILED DESCRIPTION (continued)

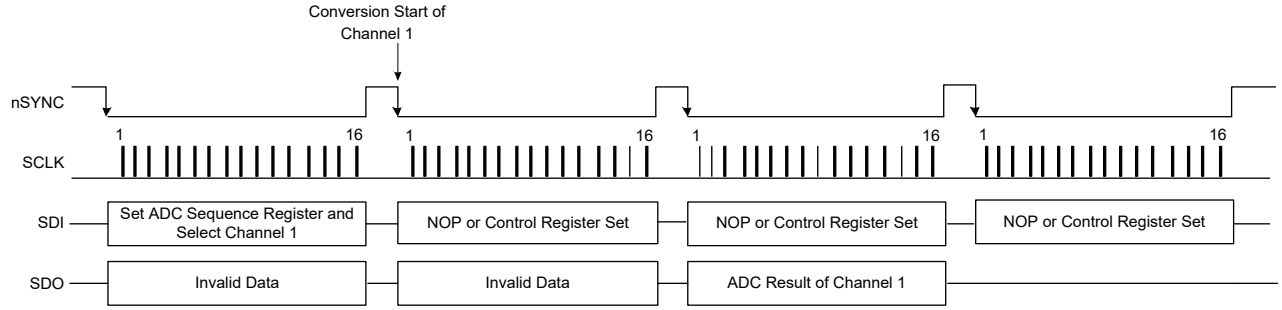


Figure 5. Single-Channel, No Repeat, ADC Conversion Sequence

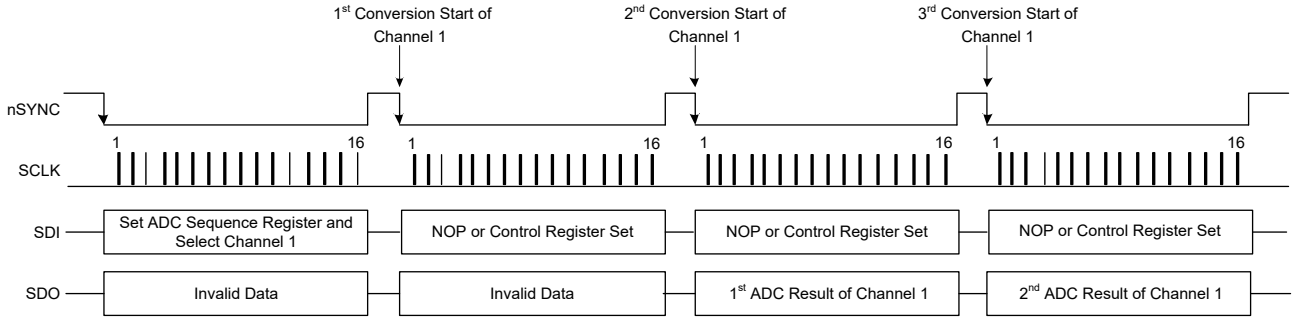


Figure 6. Single-Channel, Repeating, ADC Conversion Sequence

DETAILED DESCRIPTION (continued)

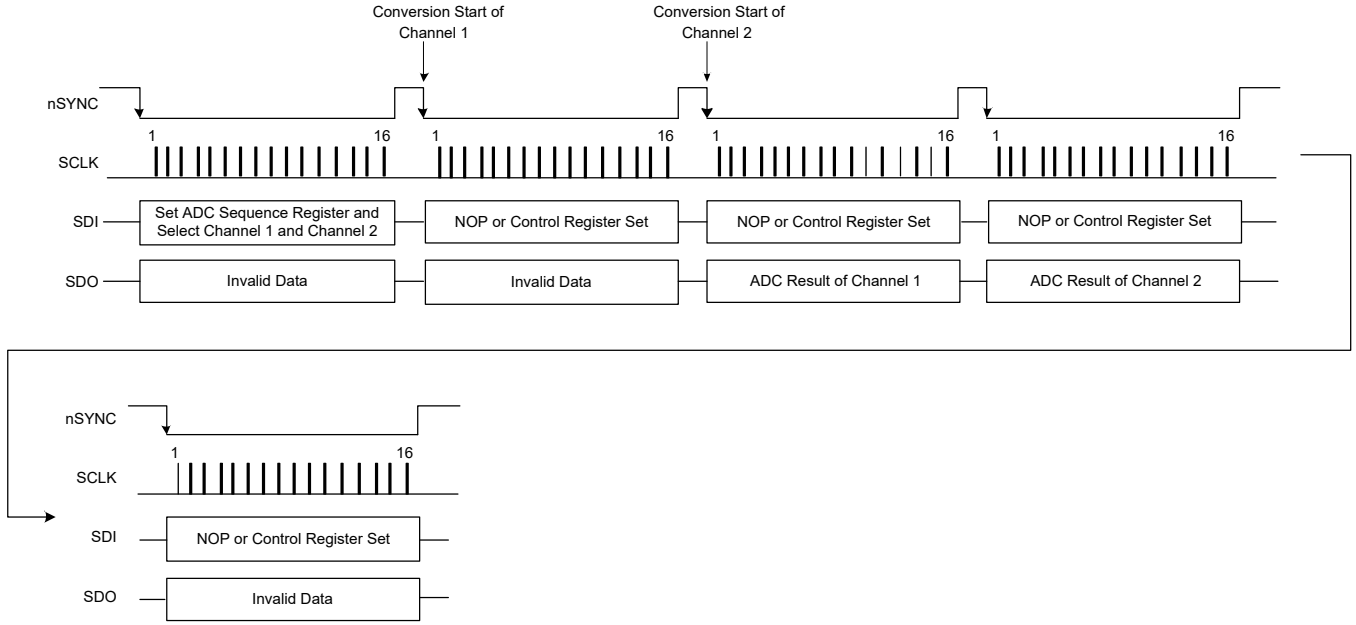


Figure 7. Multi-Channel, No Repeat, ADC Conversion Sequence

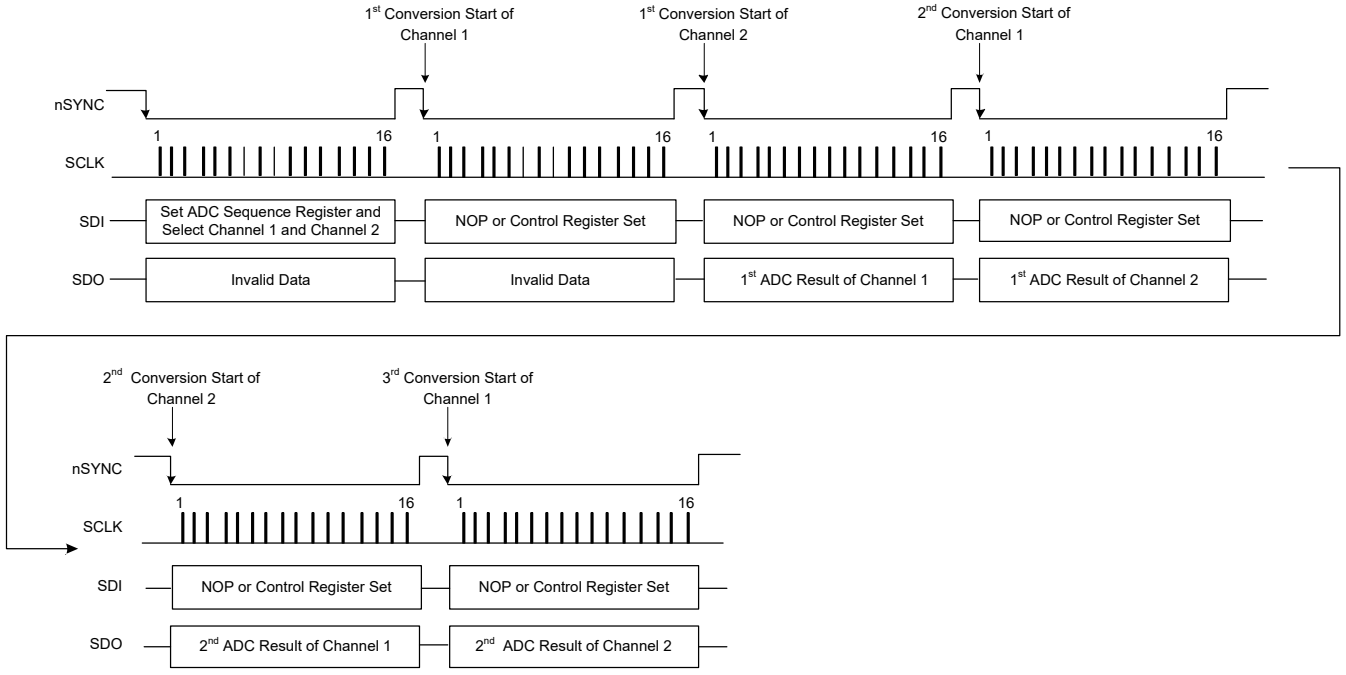


Figure 8. Multi-Channel, Repeating, ADC Conversion Sequence

DETAILED DESCRIPTION (continued)

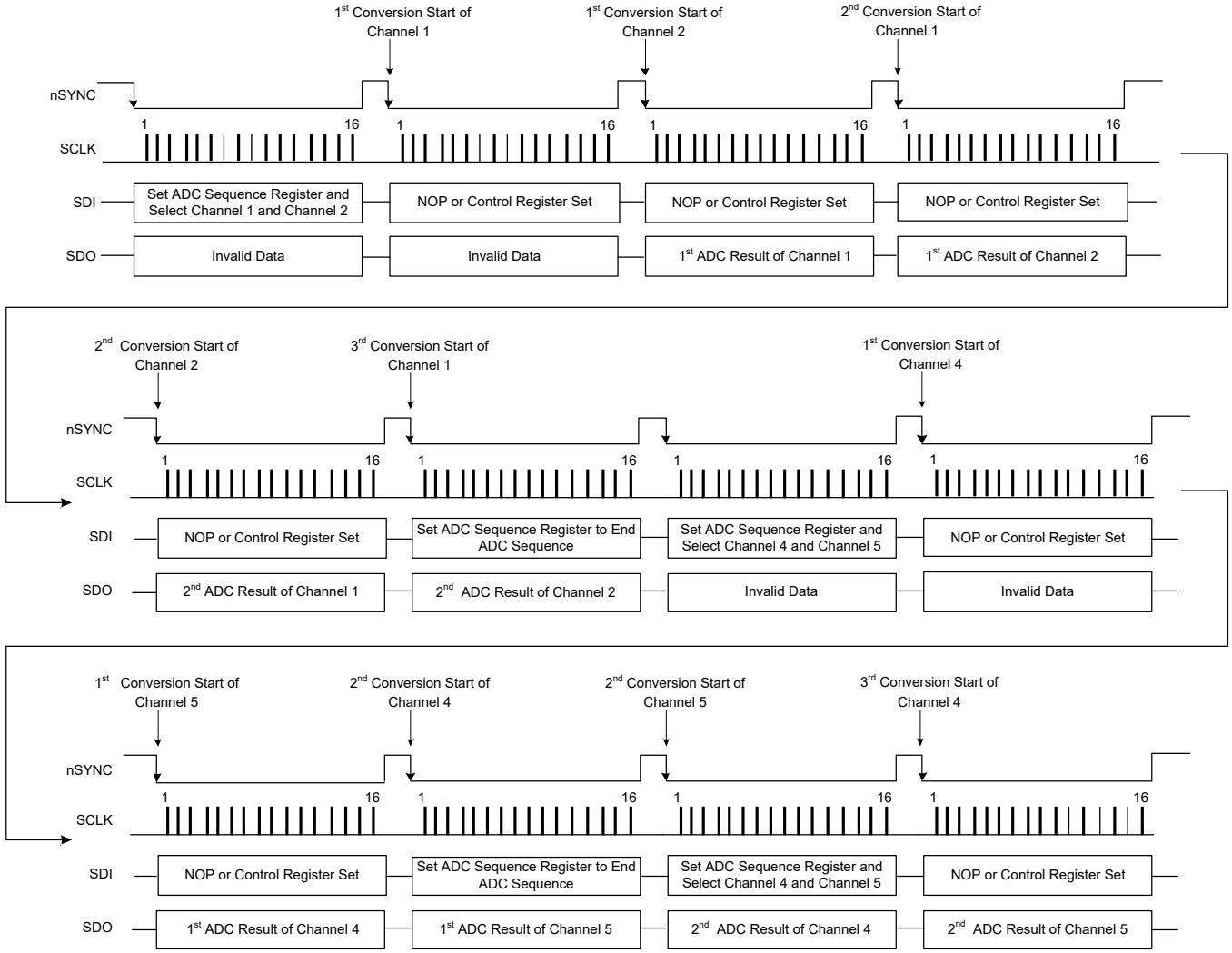


Figure 9. Changing a Multi-Channel, Repeating, ADC Conversion Sequence

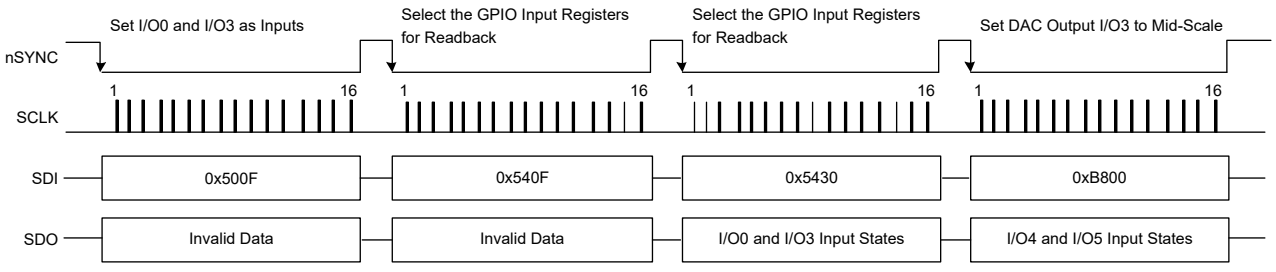


Figure 10. Configuring and Reading General-Purpose Input Pins

DETAILED DESCRIPTION (continued)

GPIO Operation

Each of I/Ox pins of the SGM90509 can be configured as a general-purpose digital input or output pin.

Setting Pins as Outputs

Table 12. GPIO Write Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 1000.	1000
D[10:9]	Reserved	Reserved. Set these bits to 0.	00
D[8]	Enable nBUSY	Enable the I/O7 Pin as nBUSY 0 = Pin I/O7 is not configured as nBUSY 1 = Pin I/O7 is configured as nBUSY. D7 must also be set to 1 to enable the I/O7 pin as an output	0
D[7:0]	GPIO7 to GPIO0	Select I/Ox Pins as GPIO Outputs 0 = I/Ox function depends on the pin configuration registers (default) 1 = I/Ox is a general-purpose output pin	0000 0000

Table 13. GPIO Open-Drain Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 1100.	1100
D[10:8]	Reserved	Reserved. Set these bits to 0.	000
D[7:0]	Open-Drain 7 to Open-Drain 0	Set Output Pins as Open-Drain The pins must also be set as digital output pins. See Table 12. 0 = I/Ox is a push/pull output pin (default) 1 = I/Ox is an open-drain output pin	0000 0000

Table 14. GPIO Write Data Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 1001.	1001
D[10:8]	Reserved	Reserved. Set these bits to 0.	000
D[7:0]	GPIO7 to GPIO0	Set the State of Output Pins 0 = I/Ox is a logic 0 (default) 1 = I/Ox is a logic 1	0000 0000

Setting Pins as Inputs

To set an I/Ox pin as a general-purpose input, set the according bit in the GPIO read configuration register to 1.

Table 15. GPIO Read Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 1010.	1010
D[10]	Enable Readback	Enable GPIO Readback 0 = Bit D7 to Bit D0 determine which pins are set as general-purpose inputs (default) 1 = The next SPI operation clocks out the state of the GPIO pins	0
D[9:8]	Reserved	Reserved. Set these bits to 0.	00
D[7:0]	GPIO7 to GPIO0	Set I/Ox Pins as GPIO Inputs 0 = I/Ox function depends on the pin configuration registers (default) 1 = I/Ox is a general-purpose input pin	0000 0000

DETAILED DESCRIPTION (continued)

Three-State Pins

The I/Ox pins can be set to three-state by writing to the three-state configuration register, as shown in Table 16.

Table 16. Three-State Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 1101.	1101
D[10:8]	Reserved	Reserved. These bits must be set to 0.	000
D[7:0]	TSO[7:0]	Set Pins as Three-State Outputs 0 = I/Ox function depends on the pin configuration registers (default) 1 = I/Ox is a three-state output pin	0000 0000

85kΩ Pull-Down Resistor Pins

Table 17. Pull-Down Configuration Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0110.	0110
D[10:8]	Reserved	Reserved. These bits must be set to 0.	000
D[7:0]	Pull_Down[7:0]	Set Pins as Weak Pull-Down Outputs 0 = I/Ox function depends on the pin configuration registers 1 = I/Ox is connected to GND through an 85kΩ pull-down resistor (default)	1111 1111

Power-Down and Reference Control

The SGM90509 has a power-down and reference control register, and it can power down the internal reference and DACs (see Table 18). There is no dedicated power-down function for the ADC, but the ADC is automatically powered down if there is no an ADC operation.

Table 18. Power-Down and Reference Control Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 1011.	1011
D[10]	PD_ALL	Power-Down DACs and Internal Reference 0 = The reference and DACs power-down states depend on D9 and D[7:0] bits (default) 1 = The reference, DACs and ADC are powered down	0
D[9]	EN_REF	Enable Internal Reference 0 = The reference and its buffer are powered down. Set this bit if an external reference is used (default) 1 = The reference and its buffer are powered up. The reference is available on the V_{REF} pin	0
D[8]	Reserved	Reserved. Must be set to 0.	0
D[7:0]	PD[7:0]	Power-Down DACs 0 = The channel is in normal operating mode (default) 1 = The channel is powered down if it is configured as a DAC	0000 0000

DETAILED DESCRIPTION (continued)

Reset Function

The SGM90509 can be reset by setting the reset register (pointer byte = 0b00001111). This operation resets all registers to their default values.

Table 19. Software Reset Register

MSB LSB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	1	0	1	1	0	1	0	1	1	0	0
Control Register Write	Write to Reset Register				Reset the SGM90509										

Readback and LDAC Mode Register

The input register of each DAC can be read back via the SPI interface. The data can be read back from a DAC only when there is no ADC conversion sequence.

Table 20. Readback and LDAC Mode Register Details

BITS	BIT NAME	DESCRIPTION	DEFAULT VALUE
D[15]	MSB	Set this bit to 0.	0
D[14:11]	Register Address[3:0]	Set these bits to 0111.	0111
D[10:7]	Reserved	Reserved. Set these bits to 0.	0000
D[6]	EN	Enable Readback Note that the LDAC mode bits are always used regardless of the EN bit. 0 = No readback is initiated (default) 1 = Bits D[5:2] select which register is read back. Bit D6 automatically clears when the read is completed	0
D[5:2]	REG_READBACK[3:0]	If bit D6 is 1, the bits D[5:2] determine which register is to be read back. 0000 = NOP (default) 0001 = DAC readback 0010 = ADC sequence 0011 = General-purpose configuration 0100 = ADC pin configuration 0101 = DAC pin configuration 0110 = Pull-down configuration 0111 = LDAC configuration 1000 = GPIO write configuration 1001 = GPIO write data 1010 = GPIO read configuration 1011 = Power-down and reference control 1100 = Open-drain configuration 1101 = Three-state pin configuration 1110 = Reserved 1111 = Software reset	0000
D[1:0]	LDAC Mode[1:0]	Determines how data written to an input register of a DAC is handled. 00 = Data written to an input register is immediately copied to a DAC register, and the DAC output updates (default) 01 = Data written to an input register is not copied to a DAC register. The DAC output is not updated 10 = Data in the input registers is copied to the corresponding DAC registers. When the data has been transferred, the DAC outputs are updated simultaneously 11 = Reserved	00

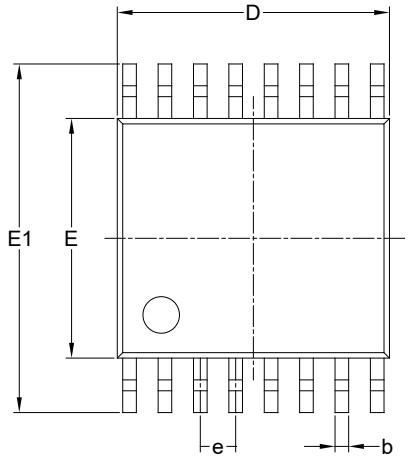
REVISION HISTORY

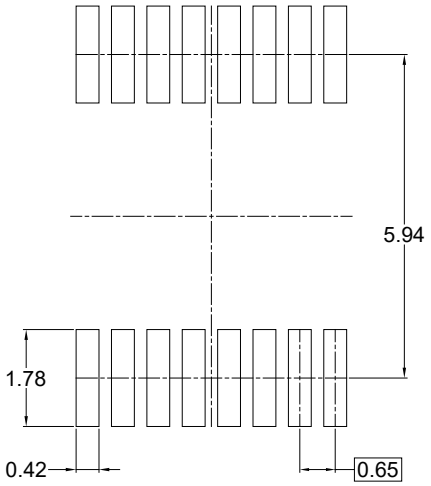
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2023) to REV.A	Page
Changed from product preview to production data	All

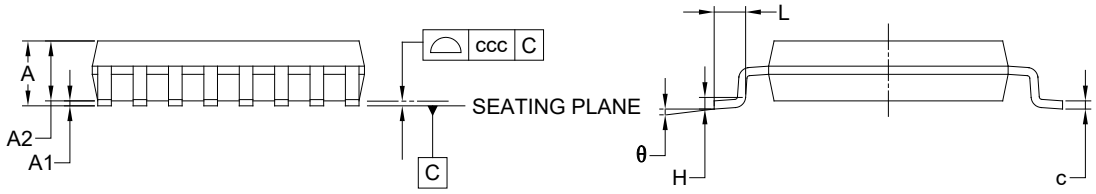
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

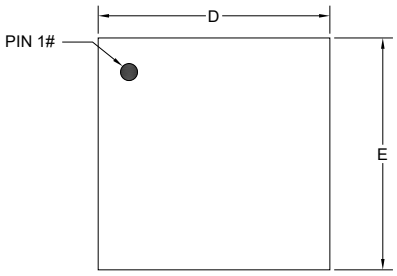


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

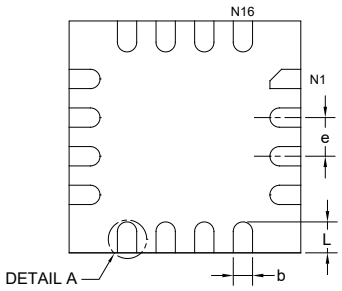
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

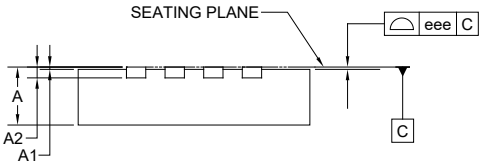
TQFN-3×3-16BL



TOP VIEW

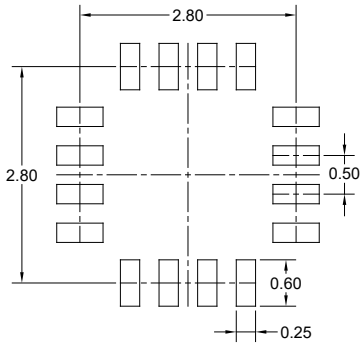


BOTTOM VIEW



SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



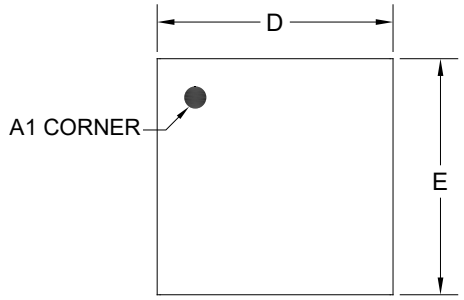
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	0.700	-	0.800
A1	-0.004	-	0.050
A2	0.110 REF		
b	0.200	-	0.300
D	2.900	-	3.100
E	2.900	-	3.100
e	0.500 BSC		
L	0.300	-	0.500
eee	0.080		

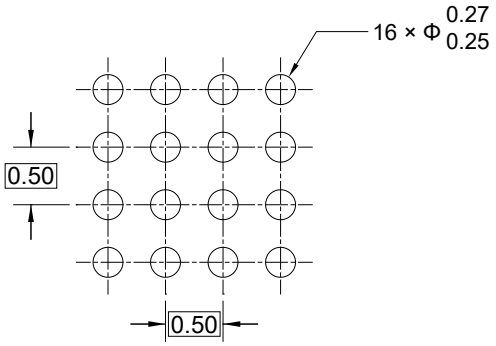
NOTE: This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

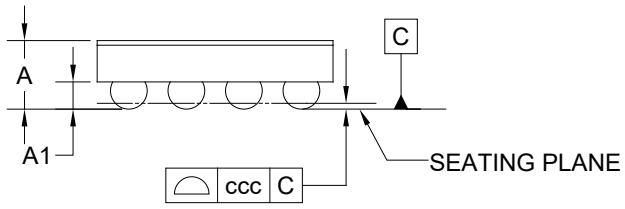
WLCSP-2.05×2.05-16B



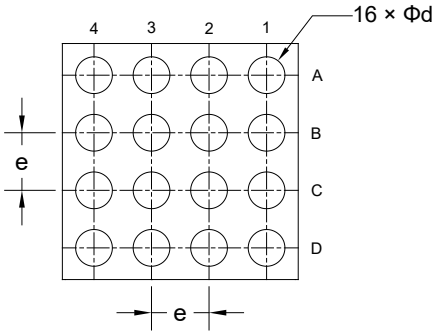
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



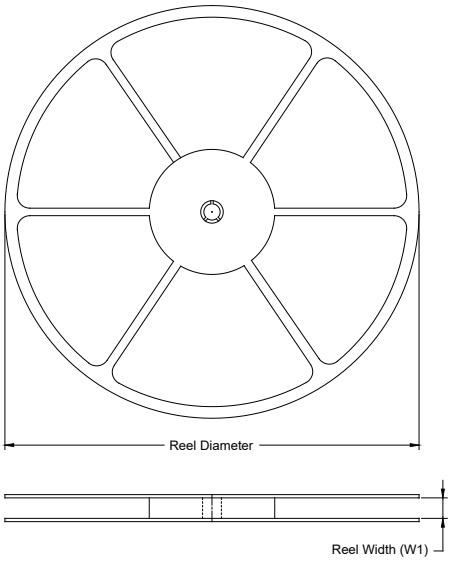
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	0.633
A1	0.216	-	0.256
D	2.020	-	2.080
E	2.020	-	2.080
d	0.289	-	0.349
e	0.500 BSC		
ccc	0.050		

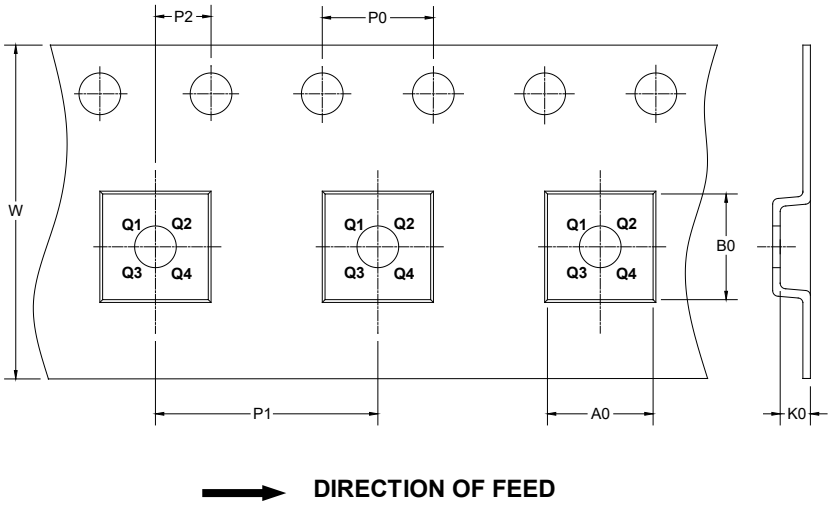
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



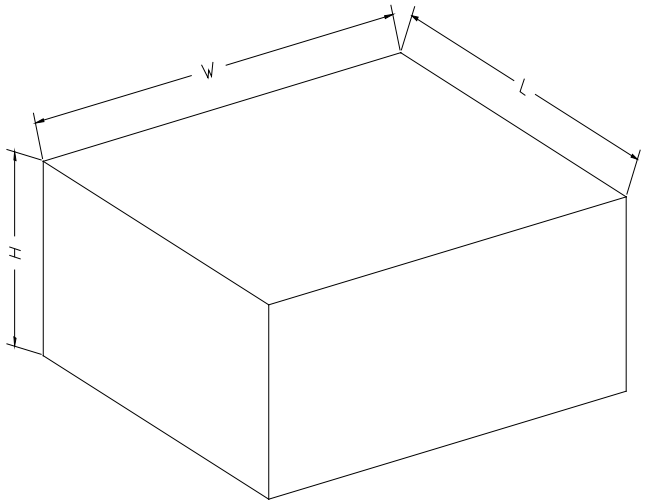
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-3×3-16BL	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2
WLCSP-2.05×2.05-16B	7″	9.5	2.24	2.24	0.75	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002