

SGM721Q Automotive, 11MHz, Rail-to-Rail I/O CMOS Operational Amplifier

GENERAL DESCRIPTION

The SGM721Q is a single, low voltage, low noise and low power operational amplifier for automotive applications. This device can operate from 2.1V to 5.5V single supply, and consumes low quiescent current.

The SGM721Q features a ± 6.5 mV maximum input offset voltage. The minimum input common mode voltage is within 0.1V below the negative rail, and the output swing is rail-to-rail with heavy loads. It exhibits a high gain-bandwidth product of 11MHz and a slew rate of 7V/ μ s. These specifications make the operational amplifier appropriate for various applications.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM721Q is available in a Green SOT-23-5 package. It operates over an ambient temperature range of -40°C to +125°C.

FEATURES

AEC-Q100 Qualified for Automotive Applications
Device Temperature Grade 1

 $T_A = -40^{\circ}C$ to +125°C

• Input Offset Voltage: ±6.5mV (MAX)

• High Gain-Bandwidth Product: 11MHz

• High Slew Rate: 7V/µs

• Settling Time to 0.1% with 2V Step: 0.4µs

Overload Recovery Time: 0.5µs
Low Noise: 8.5nV/√Hz at 10kHz

• Rail-to-Rail Input and Output

Supply Voltage Range: 2.1V to 5.5V

Input Voltage Range: -0.1V to 5.6V with V_s = 5.5V

Low Quiescent Current: 1.2mA (TYP)
Available in a Green SOT-23-5 Package

APPLICATIONS

Automotive Application

Sensor

Automotive Inverter

Automotive Audio

Active Filter

Driver of A/D Converter

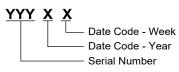
Photodiode Amplification

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION	
SGM721Q	SOT-23-5	-40°C to +125°C	SGM721QN5G/TR	0GQXX	Tape and Reel, 3000	

MARKING INFORMATION

NOTE: XX = Date Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V _S to -V _S	6V
Input Common Mode Voltage Ra	inge
	$(-V_S) - 0.3V$ to $(+V_S) + 0.3V$
Package Thermal Resistance	
SOT-23-5, θ _{JA}	163.5°C/W
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10	0s)+260°C
ESD Susceptibility	
HBM	8000V
CDM	1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range-40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

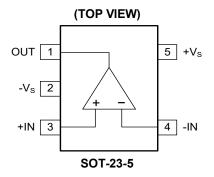
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

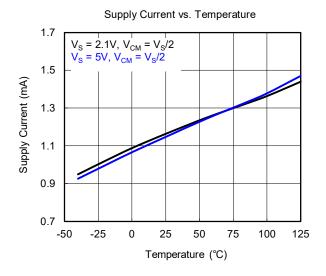


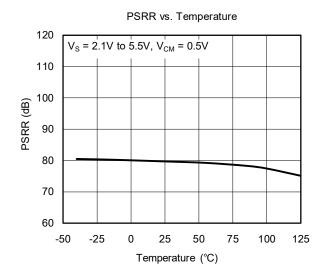
ELECTRICAL CHARACTERISTICS

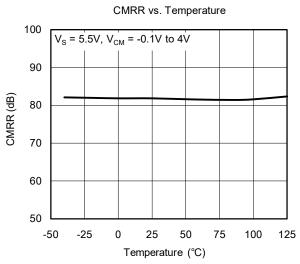
(At T_A = +25°C, V_S = 2.1V to 5V, V_{CM} = $V_S/2$ and R_L = 600 Ω , unless otherwise noted.)

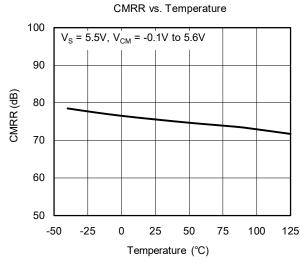
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C +25°C		-40℃ to +85℃	-40℃ to +125℃	UNITS	MIN/ MAX	
Input Characteristics								
Input Offset Voltage (Vos)		±2	±5.5	±6	±6.5	mV	MAX	
Input Bias Current (I _B)		0.01		1	6	nA	MAX	
Input Offset Current (Ios)		0.01		1	3	nA	MAX	
Input Common Mode Voltage Range (V _{CM})	V _S = 5.5V	-0.1 to 5.6				V	TYP	
	$V_S = 2.1V$, $V_{CM} = -0.1V$ to 2.2V	67	53	50	46	dB	MIN	
Common Mode Rejection Ratio (CMRR)	$V_S = 5.5V$, $V_{CM} = -0.1V$ to 4V	81	66	63	61	dB	MIN	
	V _S = 5.5V, V _{CM} = -0.1V to 5.6V	75	60	57	55	dB	MIN	
Open-Loop Voltage Gain (A _{OL})	$R_L = 600\Omega$, $V_{OUT} = 0.15V$ to $(+V_S) - 0.15V$	86	80	72	62	dB	MIN	
open zeep verage earn (vol.)	$R_L = 10k\Omega$, $V_{OUT} = 0.05V$ to $(+V_S) - 0.15V$	98	91	80	68	dB	MIN	
Input Offset Voltage Drift (ΔV _{OS} /ΔT)	(9, 1	5.5				μV/°C	TYP	
Output Characteristics				•	•	•	•	
Outside Valley of Outside France Paril	R _L = 600Ω	76	100	110	120	mV	MAX	
Output Voltage Swing from Rail	$R_L = 10k\Omega$	6	20	30	40	mV	MAX	
Outside Ourside (I)	V _S = 2.1V	±25	±19	±15	±13	mA	MIN	
Output Current (I _{OUT})	V _S = 5V	±58	±48	±38	±34	mA	MIN	
Closed-Loop Output Impedance	f = 1MHz, G = +1	9.5				Ω	TYP	
Power Supply								
On another Walters Banks					2.1	V	MIN	
Operating Voltage Range					5.5	V	MAX	
Power Supply Rejection Ratio (PSRR)	$V_S = 2.1V$ to 5.5V, $V_{CM} = (-V_S) + 0.5V$	79	67	64	62	dB	MIN	
Quiescent Current (I _Q)	I _{OUT} = 0A	1.2	1.5	1.7	1.85	mA	MAX	
Dynamic Performance								
Gain-Bandwidth Product (GBP)	C _L = 50pF	11				MHz	TYP	
Phase Margin (φ _O)	C _L = 50pF	60				٥	TYP	
Full-Power Bandwidth (BW _P)	< 1% distortion, V _{OUT} = 1V _{P-P}	200				kHz	TYP	
Slew Rate (SR)	G = +1	6				V/µs	TYP	
Settling Time to 0.1% (t _S)	G = +1	0.4				μs	TYP	
Overload Recovery Time	$V_{IN} \times G = V_{S}$	0.8				μs	TYP	
Noise Performance								
Input Valtage Naise Develop	f = 1kHz	12.5				nV/√ Hz	TYP	
Input Voltage Noise Density (e _n)	f = 10kHz	8.5				nV/√Hz	TYP	

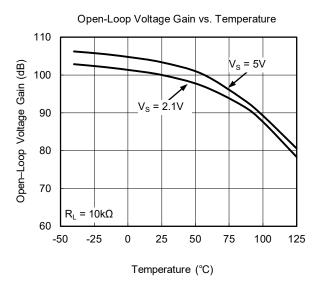
TYPICAL PERFORMANCE CHARACTERISTICS

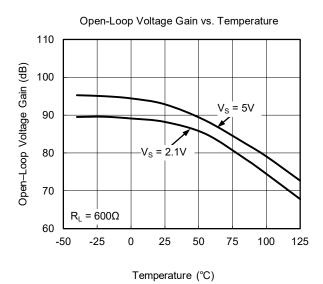


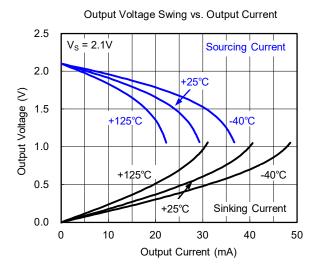


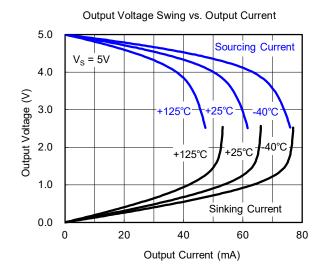


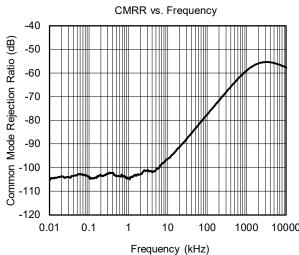


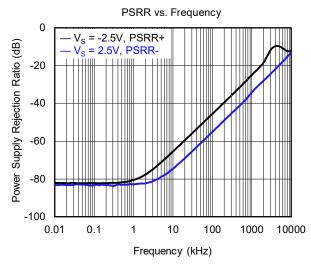


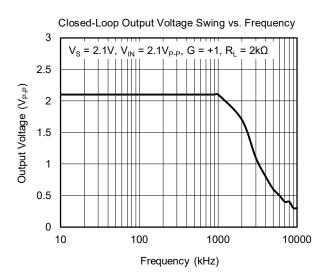


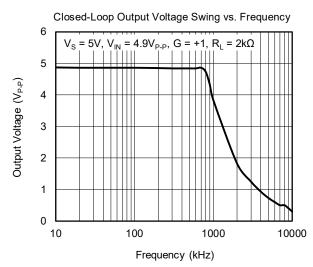


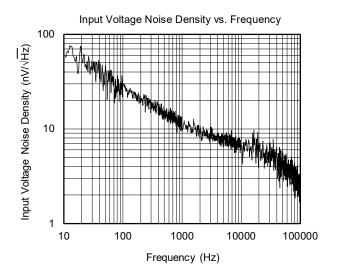


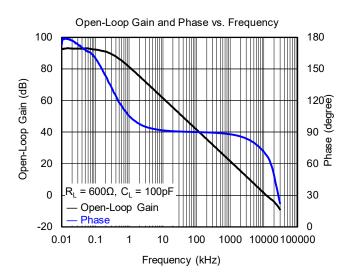


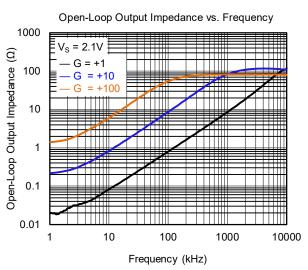


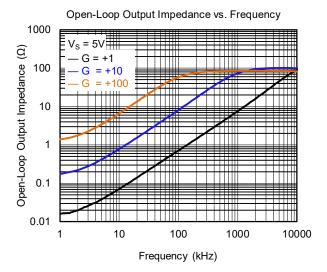


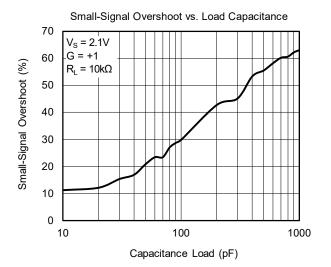


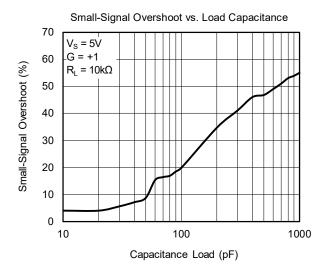


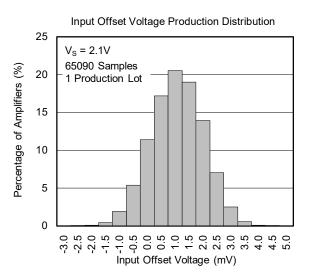


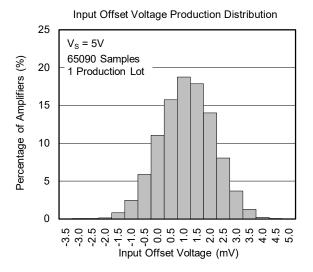


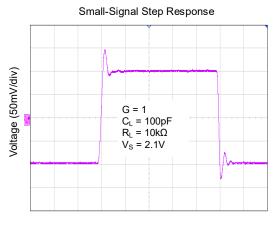




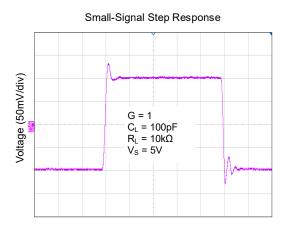




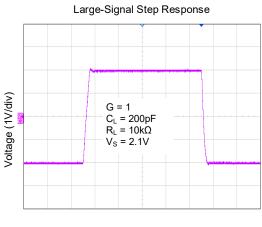




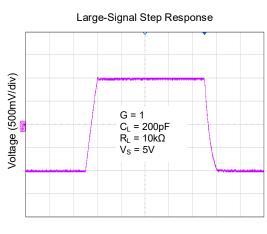




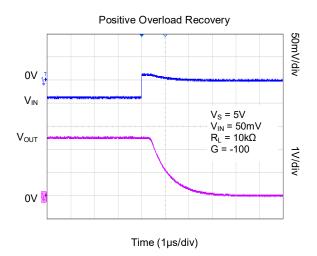
Time (200ns/div)

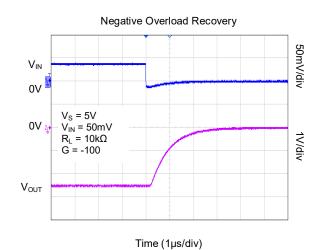


Time (1µs/div)



Time (1µs/div)





APPLICATION INFORMATION

Rail-to-Rail Input

When SGM721Q works at the power supply between 2.1V and 5.5V, the input common mode voltage range is from $(-V_S)$ - 0.1V to $(+V_S)$ + 0.1V. In Figure 1, the ESD diodes between the inputs and the power supply rails will clamp the input voltage not to exceed the rails.

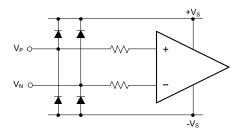


Figure 1. Input Equivalent Circuit

Input Current-Limit Protection

For ESD diode clamping protection, when the current flowing through ESD diode exceeds the maximum rating value, the ESD diode and amplifier will be damaged, so current-limit protection will be added in some applications. One resistor is selected to limit the current not to exceed the maximum rating value. In Figure 2, a series input resistor is used to limit the input current to less than 10mA, but the drawback of this current-limit resistor is that it contributes thermal noise at the amplifier input. If this resistor must be added, its value must be selected as small as possible.

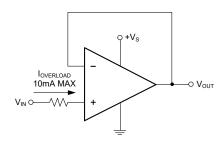


Figure 2. Input Current-Limit Protection

Rail-to-Rail Output

The SGM721Q supports rail-to-rail output operation. In single power supply application, for example, when $+V_S$ = 5V, $-V_S$ = GND, $10k\Omega$ load resistor is tied from OUT pin to ground, the typical output swing range is from 0.006V to 4.994V.

Driving Capacitive Loads

The SGM721Q is designed for driving the 4700pF capacitive load with unity-gain stable. If greater capacitive load must be driven in application, the circuit in Figure 3 can be used. In this circuit, the IR drop voltage generated by $R_{\rm ISO}$ is compensated by feedback loop.

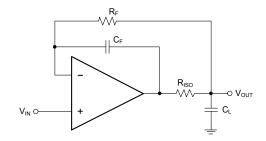


Figure 3. Circuit to Drive Heavy Capacitive Load

Power Supply Decoupling and Layout

A clean and low noise power supply is very important in amplifier circuit design. Besides of input signal noise, the power supply is one of important source of noise to the amplifier through +Vs and -Vs pins. Power supply bypassing is an effective method to clear up the noise at power supply, and the low impedance path to ground of decoupling capacitor will bypass the noise to GND. In application, $10\mu F$ ceramic capacitor paralleled with $0.1\mu F$ or $0.01\mu F$ ceramic capacitor is used in Figure 4. The ceramic capacitors should be placed as close as possible to +Vs and -Vs power supply pins.

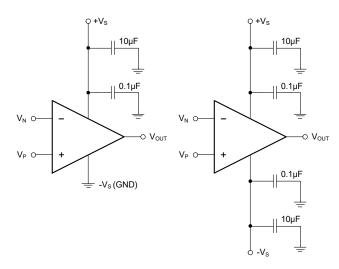


Figure 4. Amplifier Power Supply Bypassing

APPLICATION INFORMATION (continued)

Grounding

In low speed application, one node grounding technique is the simplest and most effective method to eliminate the noise generated by grounding. In high speed application, the general method to eliminate noise is to use a complete ground plane technique, and the whole ground plane will help distribute heat and reduce EMI noise pickup.

Reduce Input-to-Output Coupling

To reduce the input-to-output coupling, the input traces must be placed as far away from the power supply or output traces as possible. The sensitive trace must not be placed in parallel with the noisy trace in same layer. They must be placed perpendicularly in different layers to reduce the crosstalk. These PCB layout techniques will help to reduce unwanted positive feedback and noise.

Typical Application Circuits

Difference Amplifier

The circuit in Figure 5 is a design example of classical difference amplifier. If $R_4/R_3 = R_2/R_1$, then $V_{OUT} = (V_P - V_N) \times R_2/R_1 + V_{REF}$.

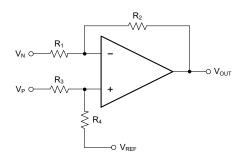


Figure 5. Difference Amplifier

High Input Impedance Difference Amplifier

The circuit in Figure 6 is a design example of high input impedance difference amplifier. The added amplifiers at

the input are used to increase the input impedance and eliminate drawback of low input impedance in Figure 5.

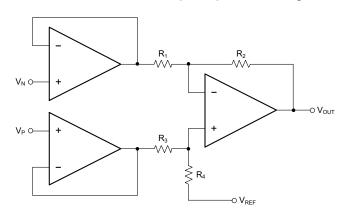


Figure 6. High Input Impedance Difference Amplifier

Active Low-Pass Filter

The circuit in Figure 7 is a design example of active low-pass filter, the DC gain is equal to $-R_2/R_1$ and the -3dB corner frequency is equal to $1/2\pi R_2C$. In this design, the filter bandwidth must be less than the bandwidth of the amplifier, and resistor values must be selected as low as possible to reduce ringing or oscillation generated by the parasitic parameters in PCB layout.

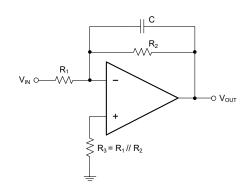


Figure 7. Active Low-Pass Filter

REVISION HISTORY

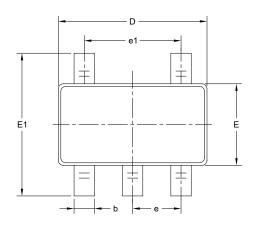
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

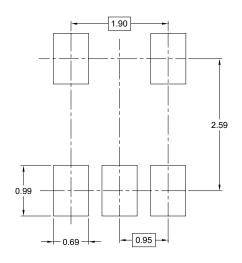
Changes from Original (APRIL 2024) to REV.A

Page

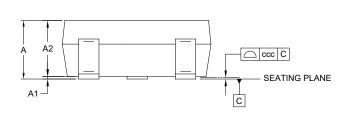


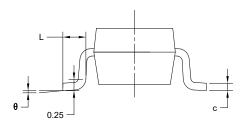
PACKAGE OUTLINE DIMENSIONS SOT-23-5





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters						
Symbol	MIN MOD		MAX				
Α	-	-	1.450				
A1	0.000	-	0.150				
A2	0.900	-	1.300				
b	0.300	-	0.500				
С	0.080	-	0.220				
D	2.750	-	3.050				
Е	1.450	-	1.750				
E1	2.600	- 3.000					
е	0.950 BSC						
e1	1.900 BSC						
L	0.300	-	0.600				
θ	0°	- 8°					
ccc	0.100						

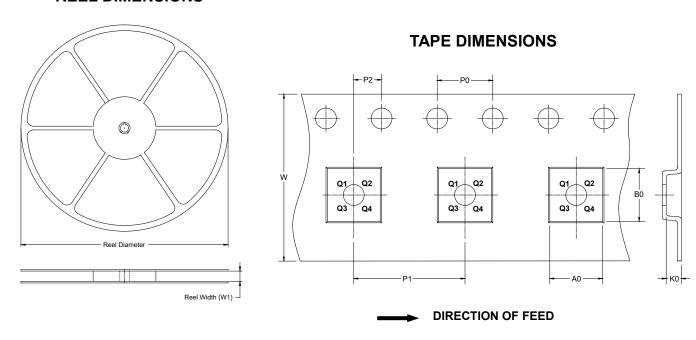
NOTES:

- 1. This drawing is subject to change without notice.
- 2. The dimensions do not include mold flashes, protrusions or gate burrs.
- 3. Reference JEDEC MO-178.



TAPE AND REEL INFORMATION

REEL DIMENSIONS

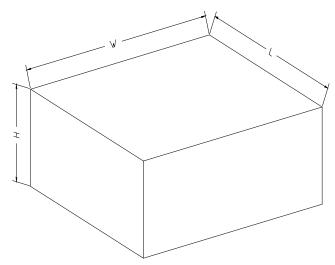


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18