# SGM8196
# High Voltage, High-Side Current-Sense Amplifier

## GENERAL DESCRIPTION

The SGM8196 is a high voltage, high-side current-sense amplifier that operates from 2.7V to 5.5V single supply. The device also features a wide common mode voltage range from 2.9V to 70V in single-supply operation or ($-V_S$) + 2.9V to ($-V_S$) + 70V in dual-supply operation. And the input common mode voltage is independent with the power supply voltage.

The SGM8196 is designed to convert the measured small differential voltage across the high-side shunt resistor to the output voltage referred to GND. There are four different gains for SGM8196: 20V/V, 25V/V, 50V/V or 100V/V. The current consumption of the device is only 320μA and almost no leakage current flows into the device in standby mode, which minimizes power consumption in applications.

The SGM8196 is available in Green SOIC-8 and TSSOP-8 packages. It is specified over the extended -40℃ to +125℃ temperature range.

## FEATURES

- **Independent Supply and Input Common Mode Voltages**
- **Wide Common Mode Voltage in Recommended Operating Conditions:**
  - **2.9V to 70V for Single-Supply Operation**
  - **($-V_S$) + 2.9V to ($-V_S$) + 70V for Dual-Supply Operation**
- **Wide Common Mode Voltage in Reversed Battery and Load-Dump Conditions: -75V to 75V**
- **Supply Voltage Range:**
  **2.7V to 5.5V Single Supply**
- **Low Supply Current: 320μA (TYP)**
- **Gain Options: 20V/V, 25V/V, 50V/V or 100V/V**
- **Output with Buffer**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green SOIC-8 and TSSOP-8 Packages**

## APPLICATIONS

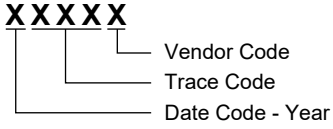
Current Monitoring
Application of Controlling DC Motor
Photo-Voltaic Application
Battery Charger
Precision Current Source
Current Monitoring of Laptops
Uninterruptible Power Supply
High-End Power Supply

# PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|---|---|---|---|---|---|
| SGM8196 | SOIC-8 | -40℃ to +125℃ | SGM8196XS8G/TR | SGM<br>8196XS8<br>XXXXX | Tape and Reel, 4000 |
| | TSSOP-8 | -40℃ to +125℃ | SGM8196XTS8G/TR | SGM8196<br>XTS8<br>XXXXX | Tape and Reel, 4000 |

## MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.




Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

## ABSOLUTE MAXIMUM RATINGS

Differential Voltage of Input Pins ($V_P$ - $V_M$), $V_{ID}$ ..... ±75V
Sensing Pins Input Voltages ($V_P$, $V_M$) (1), $V_{IN\_SENSE}$ ..... -75V to 75V
Voltages Level of Gain-Select Pins (SEL1, SEL2) (2), $V_{IN\_SEL}$ ..... -0.3V to ($+V_S$) + 0.3V
Positive Supply Voltage (2), $+V_S$ ..... -0.3V to 7V
DC Supply Voltage, ($+V_S$) - ($-V_S$) ..... 0V to 22V
DC Output Pin Voltage (2), $V_{OUT}$ ..... -0.3V to ($+V_S$) + 0.3V
Package Thermal Resistance
SOIC-8, $\theta_{JA}$ ..... 120℃/W
SOIC-8, $\theta_{JB}$ ..... 81℃/W
SOIC-8, $\theta_{JC}$ ..... 74.7℃/W
TSSOP-8, $\theta_{JA}$ ..... 160℃/W
TSSOP-8, $\theta_{JB}$ ..... 109.5℃/W
TSSOP-8, $\theta_{JC}$ ..... 55.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM ..... 4000V
CDM ..... 1000V

## RECOMMENDED OPERATING CONDITIONS

Supply Voltage for Single-Supply Operation ($-V_S$ Connected to GND = 0V), $+V_S$ ..... 2.7V to 5.5V
Negative Supply Voltage for Dual-Supply Operation
$+V_S$ = 5.5V (MAX) ..... -14.5V to 0V
$+V_S$ = 2.7V (MAX) ..... -17.3V to 0V
Common Mode Voltage Range Referred to $-V_S$ Pin ..... 2.9V to 70V
Operating Temperature Range ..... -40℃ to +125℃

NOTES:
1. These values of voltage are tested relative to the $-V_S$ pin.
2. These values of voltage are tested relative to the GND pin.

## OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

## ESD SENSITIVITY CAUTION

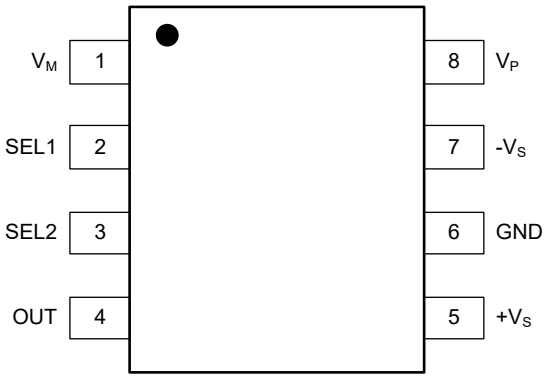
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

## DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

## PIN CONFIGURATION

(TOP VIEW)




SOIC-8/TSSOP-8

## PIN DESCRIPTION

| PIN | NAME | I/O | FUNCTION |
|---|---|---|---|
| 1 | $V_M$ | Analog Input | External Sense Resistor Connection. See Single-Supply Operation Schematic. |
| 2 | SEL1 | Digital Input | Gain-Select Pin. |
| 3 | SEL2 | Digital Input | Gain-Select Pin. |
| 4 | OUT | Analog Output | Output Pin. $V_{OUT}$ is proportional to $V_{SENSE} = V_P - V_M$. |
| 5 | $+V_S$ | — | Positive Power Supply Pin. |
| 6 | GND | — | Ground. |
| 7 | $-V_S$ | — | Negative Power Supply Pin. |
| 8 | $V_P$ | Analog Input | External Sense Resistor Connection. See Single-Supply Operation Schematic. |

## ELECTRICAL CHARACTERISTICS

(+$V_S$ = 5V, -$V_S$ connected to GND (single-supply operation), $V_M$ = 12V, $V_{SENSE}$ = $V_P$ - $V_M$ = 50mV, no load on OUT pin, all gain configurations, Full = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Input Characteristics** | | | | | | | |
| Input Offset Voltage (1) | $V_{OS}$ | | +25℃ | | ±15 | ±75 | μV |
| | | | Full | | | ±100 | |
| Input Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | G = 50V/V | Full | | ±0.05 | ±0.3 | μV/℃ |
| Input Leakage Current | $I_{LK}$ | $V_S$ = 0V | Full | | | 0.5 | μA |
| Input Bias Current | $I_B$ | $V_{SENSE}$ = 0V | Full | | 20 | 30 | μA |
| DC Common Mode Rejection Ratio, RTI (2) | DC CMRR | $V_M$ = 2.9V to 70V | Full | 110 | 145 | | dB |
| AC Common Mode Rejection Ratio, RTI (Peak-to-Peak Voltage Variation) | AC CMRR | G = 50V/V or G = 100V/V<br>$V_M$ = 2.9V to 30V, 1kHz sine wave | +25℃ | | 100 | | dB |
| Logic Low-Level Input Voltage (SEL1 and SEL2) | $V_{IL}$ | $V_S$ = 2.7V to 5.5V | Full | -0.3 | | 0.4 | V |
| Logic High-Level Input Voltage (SEL1 and SEL2) | $V_{IH}$ | $V_S$ = 2.7V to 5.5V | Full | 1.2 | | $V_S$ | V |
| Input Bias Current of Gain-Select Pins (SEL1 and SEL2) | $I_{SEL}$ | SEL pin connected to GND or $V_S$ | Full | | 20 | 150 | nA |
| **Output Characteristics** | | | | | | | |
| Gain | G | SEL1 = GND, SEL2 = GND | +25℃ | | 20 | | V/V |
| | | SEL1 = GND, SEL2 = +$V_S$ | +25℃ | | 25 | | |
| | | SEL1 = +$V_S$, SEL2 = GND | +25℃ | | 50 | | |
| | | SEL1 = +$V_S$, SEL2 = +$V_S$ | +25℃ | | 100 | | |
| Output Voltage Drift (3) | $\Delta V_{OUT}/\Delta T$ | G = 50V/V | Full | | ±10 | ±40 | ppm/℃ |
| Output Stage Load Regulation | $\Delta V_{OUT}/\Delta I_{OUT}$ | G = 50V/V, -10mA < $I_{OUT}$ < 10mA | +25℃ | | ±0.05 | ±0.8 | mV/mA |
| Total Output Voltage Accuracy (4) | $\Delta V_{OUT}$ | $V_{SENSE}$ = 50mV (5) | +25℃ | | | ±0.8 | % |
| | | | Full | | | ±3.0 | |
| | | $V_{SENSE}$ = 90mV (5) | +25℃ | | | ±0.8 | |
| | | | Full | | | ±3.0 | |
| | | $V_{SENSE}$ = 20mV | +25℃ | | | ±1 | |
| | | | Full | | | ±3.5 | |
| | | $V_{SENSE}$ = 10mV | +25℃ | | | ±1 | |
| | | | Full | | | ±3.5 | |
| | | $V_{SENSE}$ = 5mV | +25℃ | | | ±1 | |
| | | | Full | | | ±4.0 | |
| Output Short-Circuit Current | $I_{SC}$ | OUT connected to $V_S$ or GND | +25℃ | 30 | 35 | | mA |
| Output Stage High-State Saturation Voltage | $V_{OH}$ | $V_{OH}$ = $V_S$ - $V_{OUT}$, $V_{SENSE}$ = 1V,<br>$I_{OUT}$ = 1mA | +25℃ | | 50 | 60 | mV |
| Output Stage Low-State Saturation Voltage | $V_{OL}$ | $V_{SENSE}$ = -1V, $I_{OUT}$ = 1mA | +25℃ | | 40 | 55 | mV |

NOTES:

1. See Gain (G) and Input Offset Voltage ($V_{OS}$) section.
2. See Common Mode Rejection Ratio (CMRR) section.
3. See Output Voltage Drift section.
4. See Output Voltage Accuracy section.
5. Except for G = 100V/V.

## ELECTRICAL CHARACTERISTICS (continued)

(+$V_S$ = 5V, -$V_S$ connected to GND (single-supply operation), $V_M$ = 12V, $V_{SENSE}$ = $V_P$ - $V_M$ = 50mV, no load on OUT pin, all gain configurations, Full = -40℃ to +125℃, typical values are at $T_A$ = +25℃, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | TEMP | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | | | |
| Total Supply Current | $I_Q$ | $V_{SENSE}$ = 0V | | Full | | 320 | 420 | μA |
| | | G = 50V/V, $V_{SENSE}$ = 50mV | | Full | | 420 | 520 | |
| Power Supply Rejection Ratio (6) | PSRR | SEL1 = GND, SEL2 = GND, $V_S$ = 2.7V to 5.5V, $V_{SENSE}$ = 30mV | | Full | 95 | 130 | | dB |
| **Frequency Response** | | | | | | | | |
| 3dB Bandwidth | BW | G = 50V/V, $C_L$ = 47pF, $V_M$ = 12V, $V_{SENSE}$ = 50mV | | +25℃ | | 950 | | kHz |
| Slew Rate | SR | $V_{SENSE}$ = 10mV to 100mV | | +25℃ | | 1 | | V/μs |
| Response to Input Differential Voltage Change (Output Settling to 1% of Final Value) | $t_S$ | $V_{SENSE}$ square pulse applied to generate a variation of $V_{OUT}$ from 500mV to 3V, $C_L$ = 47pF | G = 20V/V | +25℃ | | 25 | | μs |
| | | | G = 25V/V | +25℃ | | 25 | | |
| | | | G = 50V/V | +25℃ | | 25 | | |
| | | | G = 100V/V | +25℃ | | 25 | | |
| Response to a Gain Change (Output Settling to 1% of Final Value) | $t_{SEL}$ | Any change of state of SEL1 or SEL2 pin | | +25℃ | | 15 | | μs |
| Response to Common Mode Voltage Change (Output Settling to 1% of Final Value) | $t_{REC}$ | +$V_S$ = 5V, -$V_S$ = -5V, $V_M$ step change from -2V to 30V or 30V to -2V | | +25℃ | | 35 | | μs |
| **Noise** | | | | | | | | |
| Equivalent Input Noise Voltage | $e_n$ | f = 1kHz | | +25℃ | | 50 | | nV/$\sqrt{Hz}$ |

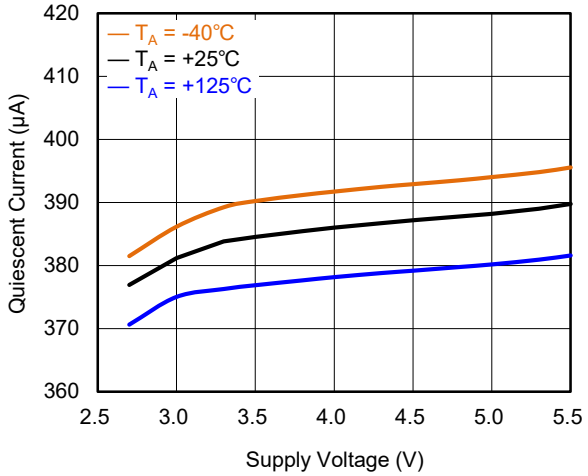
NOTE:

6. See Supply Voltage Rejection Ratio (PSRR) section.

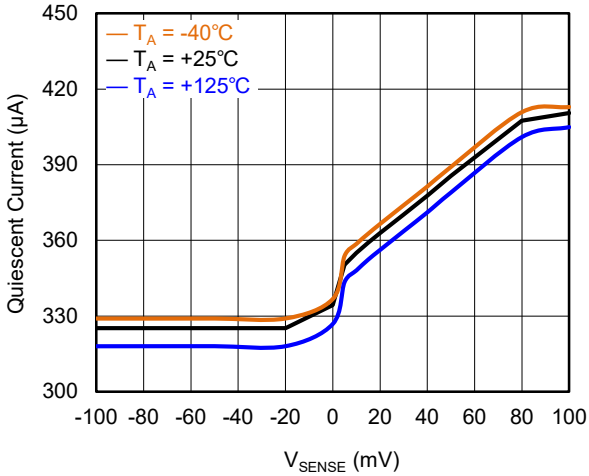
## TYPICAL PERFORMANCE CHARACTERISTICS

At $T_A$ = +25℃, $V_S$ = 5V, $V_{SENSE}$ = $V_P$ - $V_M$ = 50mV, $V_M$ = 12V, no load on OUT pin, unless otherwise noted.

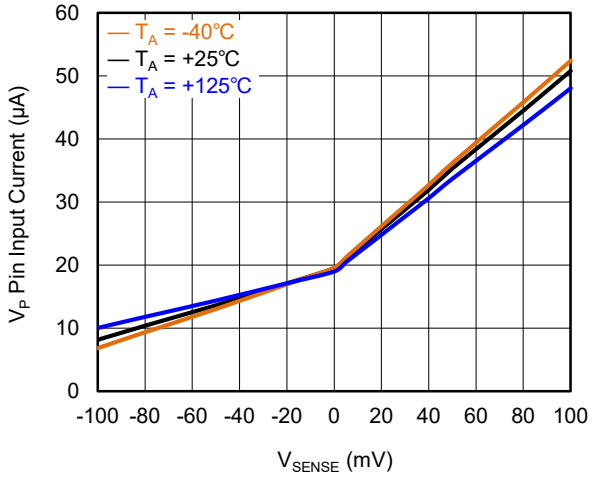
Quiescent Current vs. Supply Voltage



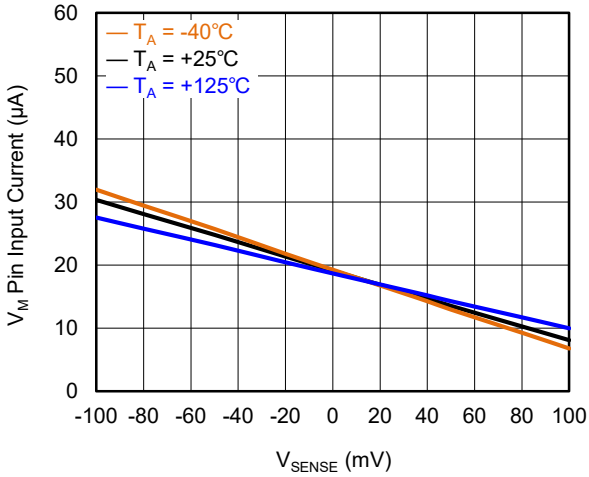

Quiescent Current vs. $V_{SENSE}$



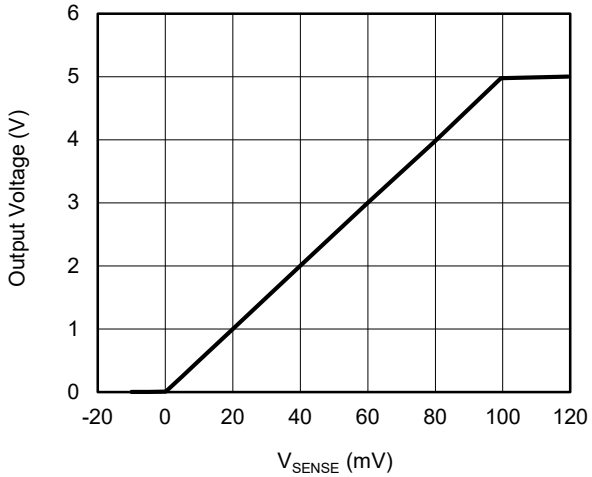

$V_P$ Pin Input Current vs. $V_{SENSE}$



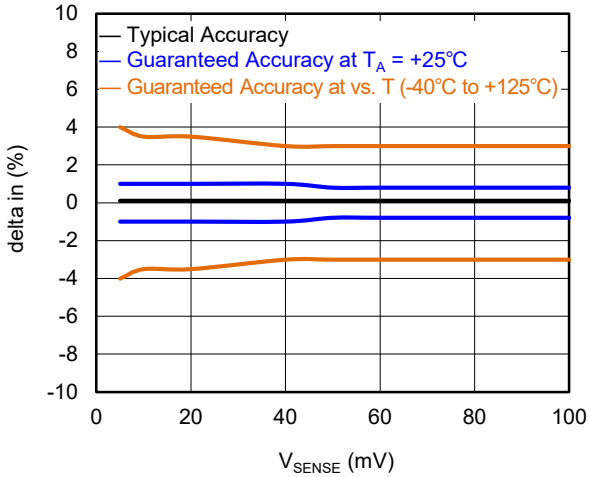

$V_M$ Pin Input Current vs. $V_{SENSE}$




Output Voltage vs. $V_{SENSE}$



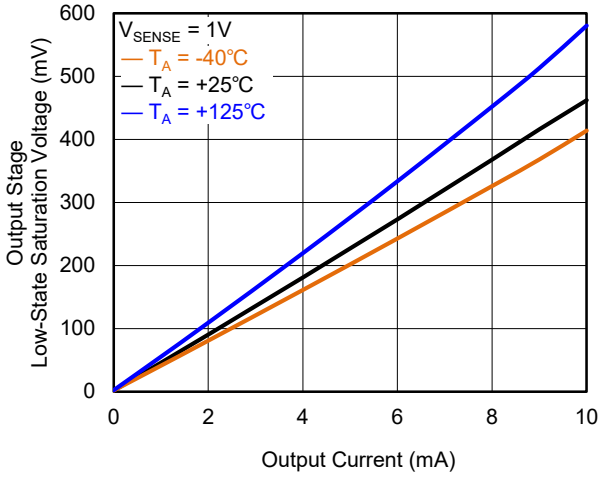

Output Voltage Accuracy vs. $V_{SENSE}$



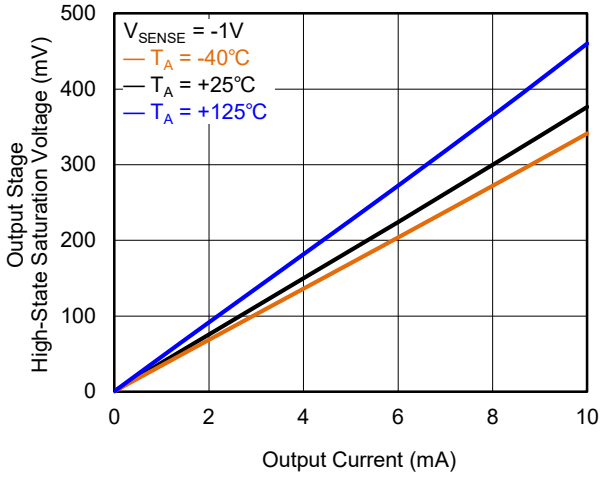
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_A$ = +25℃, $V_S$ = 5V, $V_{SENSE}$ = $V_P$ - $V_M$ = 50mV, $V_M$ = 12V, no load on OUT pin, unless otherwise noted.

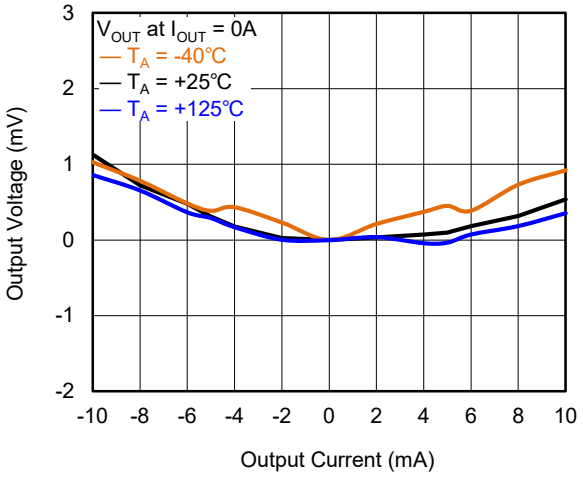
Output Stage Low-State Saturation Voltage vs. Output Current



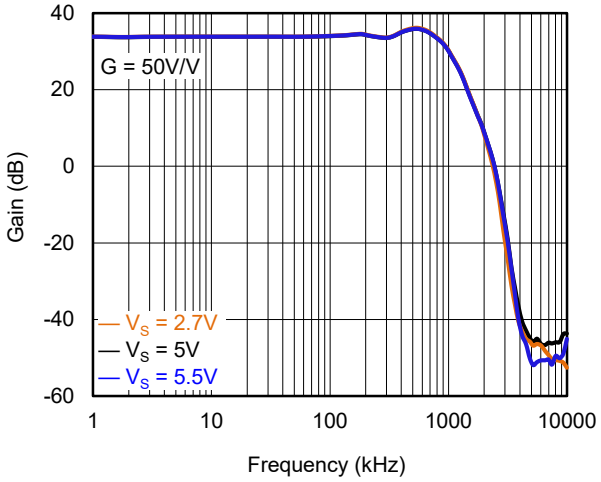

Output Stage High-State Saturation Voltage vs. Output Current



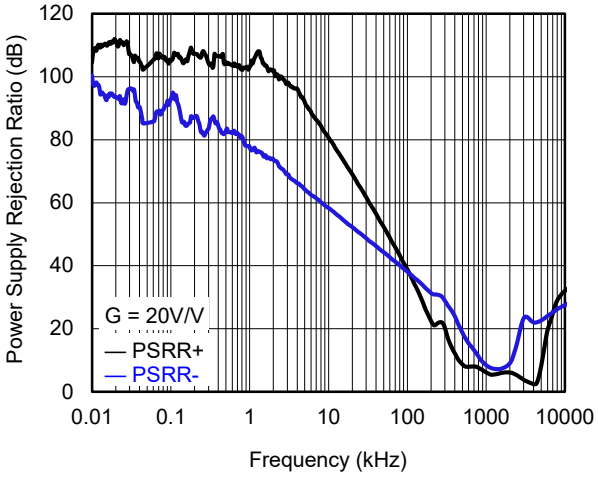

Output Stage Load Regulation



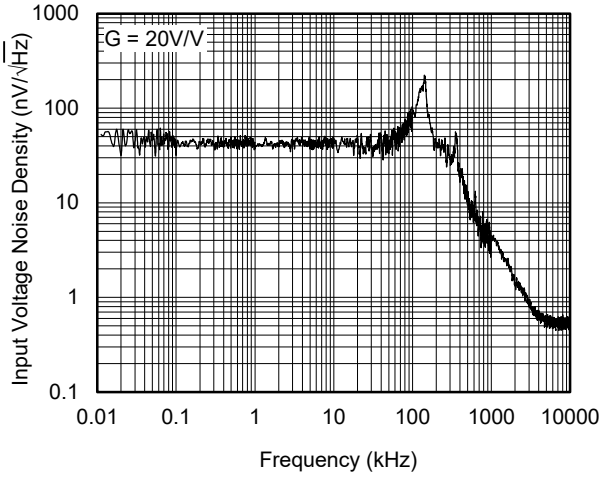

Gain vs. Frequency




PSRR vs. Frequency



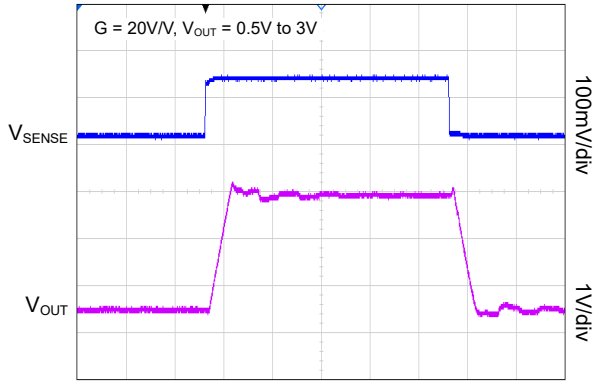

Input Voltage Noise Density vs. Frequency



## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

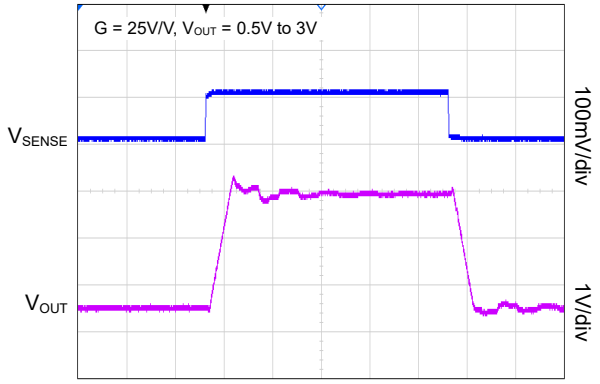
At $T_A$ = +25℃, $V_S$ = 5V, $V_{SENSE}$ = $V_P$ - $V_M$ = 50mV, $V_M$ = 12V, no load on OUT pin, unless otherwise noted.

Step Response



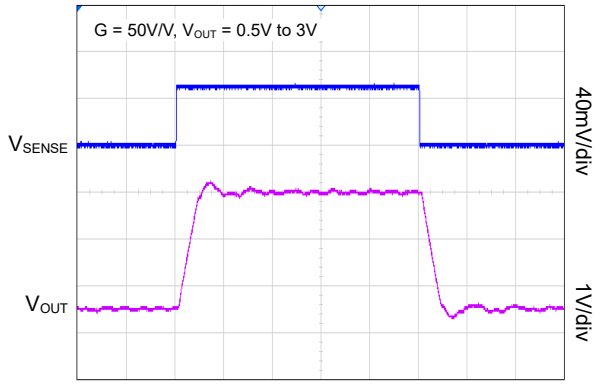

Time (5μs/div)

Step Response



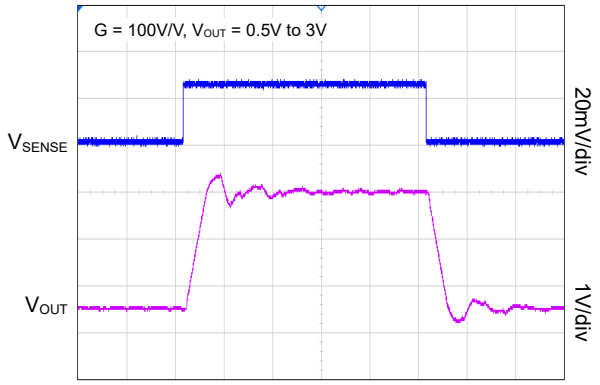

Time (5μs/div)

Step Response




Time (5μs/div)

Step Response




Time (5μs/div)

# DETAILED DESCRIPTION

## Common Mode Rejection Ratio (CMRR)

The CMRR measures the ability to reject any variation from input common mode voltage of the SGM8196. The CMRR equation in Equation 1 illustrates the effect on the differential input signal by changing the common mode voltage level:

$$CMRR = -20 \times \log\frac{\Delta V_{OUT}}{\Delta V_{CM} \times G} \quad (1)$$

## Power Supply Rejection Ratio (PSRR)

The PSRR measures the ability of the SGM8196 to reject any variation from the power supply. The PSRR equation in Equation 2 illustrates the effect on the differential input signal by changing the supply voltage level:

$$PSRR = -20 \times \log\frac{\Delta V_{OUT}}{\Delta V_{S} \times G} \quad (2)$$

## Gain (G) and Input Offset Voltage ($V_{OS}$)

The input offset voltage can be calculated within the linear region of the curve in Figure 1. If the corresponding sense voltage for $V_{OUT1}$ is $V_{SENSE1}$ and the corresponding sense voltage for $V_{OUT2}$ is $V_{SENSE2}$, the following equation can be used to calculate the offset voltage of SGM8196:

$$V_{OS} = V_{SENSE1} - \left(\frac{V_{SENSE1} - V_{SENSE2}}{V_{OUT1} - V_{OUT2}} \times V_{OUT1}\right) \quad (3)$$

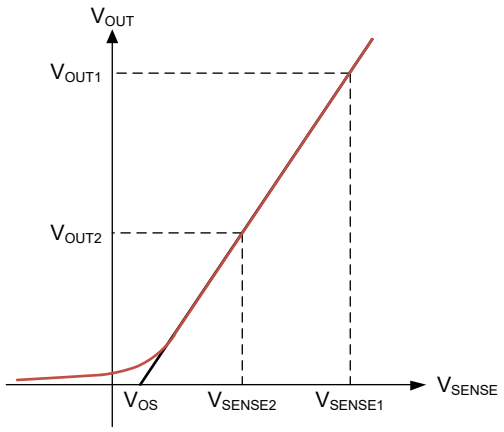



**Figure 1. $V_{OUT}$ vs. $V_{SENSE}$ Characteristics: Detail for Low $V_{SENSE}$ Values**

The values of $V_{SENSE1}$ and $V_{SENSE2}$ used for the input offset calculations are detailed in Table 1.

**Table 1. Test Conditions for $V_{OS}$ Voltage Calculation**

| Product | Gain (V/V) | $V_{SENSE1}$ (mV) | $V_{SENSE2}$ (mV) |
|---|---|---|---|
| SGM8196 | 20 | 50 | 5 |
| | 25 | 50 | 5 |
| | 50 | 50 | 5 |
| | 100 | 40 | 5 |

## Input Offset Voltage Drift

The offset voltage drift versus temperature is the absolute maximum variation of $V_{OS}$ relative to its value at +25℃ over the temperature range. It is calculated with Equation 5:

$$\frac{\Delta V_{OS}}{\Delta T} = MAX\frac{V_{OS}(T_A) - V_{OS}(+25℃)}{T_A - 25℃} \quad (5)$$

with $T_A$ = -40℃ to +125℃

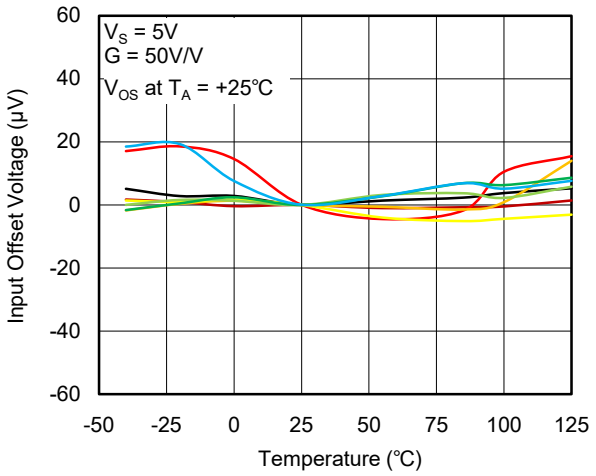



**Figure 2. Input Offset Voltage Drift vs. Temperature**

## Output Voltage Drift

The output voltage drift versus temperature is the absolute maximum variation of $V_{OUT}$ relative to its value at +25℃ over the temperature range. The following equation illustrates how to calculate the drift of the output voltage:

$$\frac{\Delta V_{OUT}}{\Delta T} = MAX\frac{V_{OUT}(T_A) - V_{OUT}(+25℃)}{T_A - 25℃} \quad (4)$$

with $T_A$ = -40℃ to +125℃

## DETAILED DESCRIPTION (continued)

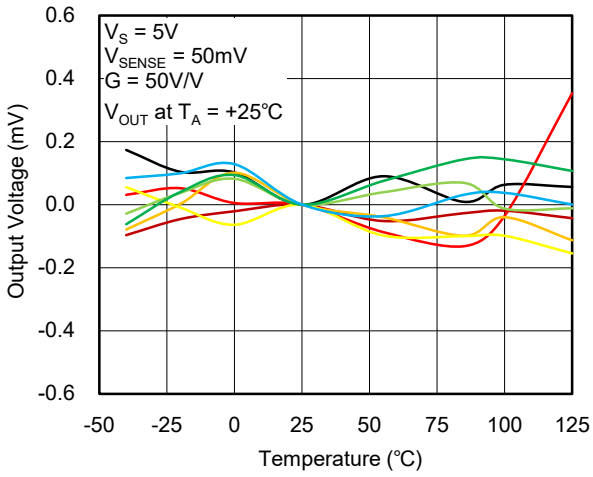



**Figure 3. Output Voltage Drift vs. Temperature**

### Output Voltage Accuracy

The accuracy of the output voltage is the gap between the actual $V_{OUT}$ and the ideal $V_{OUT}$. For the ideal $V_{OUT}$, it equals to the differential input voltage multiplied by the theoretical gain of the SGM8196, which is shown as Equation 6:

$$V_{OUT\text{-}TH} = G \times V_{SENSE} \quad (6)$$

The actual $V_{OUT}$ is different from the ideal one due to the following two features:

- the input offset voltage $V_{OS}$
- the non-linearity

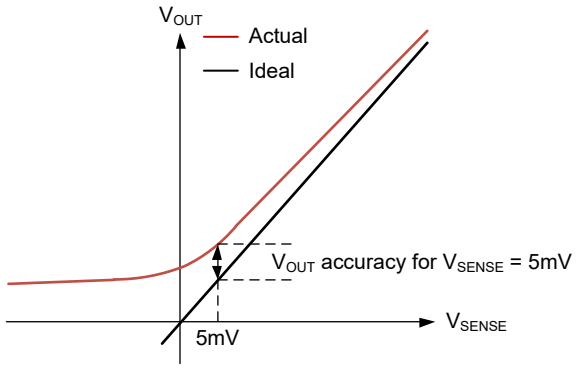



**Figure 4. $V_{OUT}$ vs. $V_{SENSE}$ Theoretical and Actual Characteristics**

The output voltage accuracy is a percentage value. The Equation 7 illustrates how to calculate the accuracy of the output voltage:

$$\Delta V_{OUT} = \frac{ABS\left(V_{OUT} - \left(G \times V_{SENSE}\right)\right)}{G \times V_{SENSE}} \quad (7)$$

with 20V/V, 25V/V, 50V/V or 100V/V which can be set by the gain-select pins (SEL1 and SEL2).

### Maximum Permissible Voltages on Pins

Both the single-supply and dual-supply operations can be applied to the SGM8196. For dual-supply mode, the customers need to connect the $-V_S$ pin to a negative supply voltage. In Figure 5, it shows that the potential voltage for the absolute maximum voltage of $V_P$ and $V_M$ is referred to the $-V_S$ pin, while the absolute voltage for SEL1, SEL2 and positive power supply is referred to the GND pin. Also, one thing should be mentioned that the maximum voltage difference between $+V_S$ and $-V_S$ is equal to 22V.

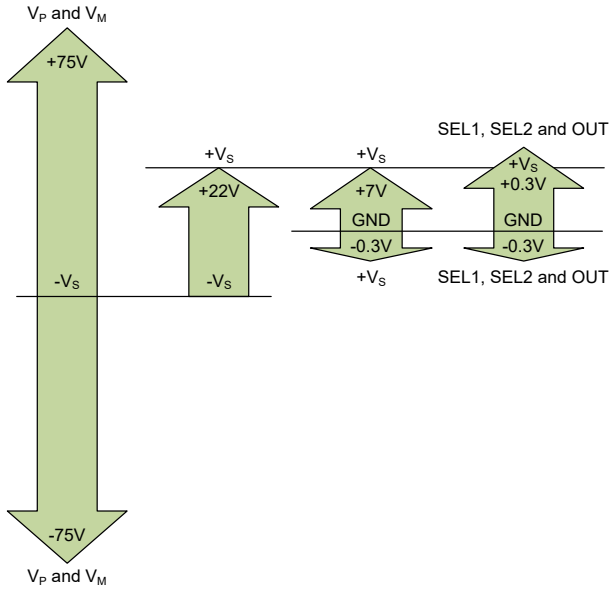



**Figure 5. Maximum Voltages on Pins**

# APPLICATION INFORMATION

The SGM8196 can operate in single-supply operation or dual-supply operation. If the users desire to apply a single-supply voltage to the SGM8196, the allowable input common mode voltage is not related to the power supply and the range is from 2.9V to 70V. If the users desire to apply a dual-supply voltage to the SGM8196, the allowable input common mode voltage will be shifted by the voltage level of $-V_S$. For example, if the $+V_S$ and $-V_S$ of the SGM8196 are equal to +5V and -5V respectively, the allowable input common mode voltage range is from -2.1V to 65V. Ramp time of SGM8196 within 1ms could keep from output jitter.

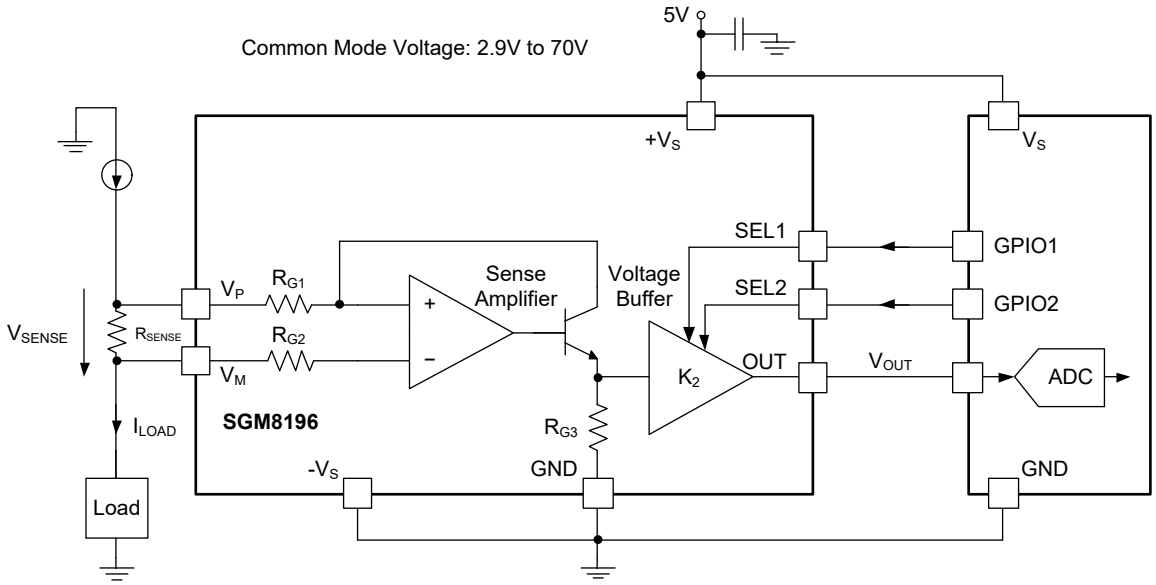



**Figure 6. Single-Supply Operation Schematic**

The SGM8196 can measure the current from the load and transfer the analog output voltage to the internal ADC of the MCU. The SEL1 and SEL2 pins are also controlled by the I/O pins of MCU to adjust the gain of the SGM8196.

The $V_{SENSE}$ is the voltage drop of $R_{SENSE}$ due to the current flowing through the shunt resistor. Because of the significant small input current of the sense amplifier, the inverting input voltage is equal to $V_M$. The open-loop gain of the amplifier is special large, so the non-inverting input of the amplifier is forced to be equal to the inverting input. Consequently, the $V_{SENSE}$ is matched with the voltage drop across $R_{G1}$.

The voltage drop at $R_{G1}$ is equal to:

$$V_{RG1} = V_{SENSE} = R_{SENSE} \times I_{LOAD} \quad (8)$$

$I_{RG1}$ is the amount of current that flows through the $R_{G1}$, so the calculation of $I_{RG1}$ is given as follows:

$$I_{RG1} = V_{SENSE}/R_{G1} \quad (9)$$

All of the $I_{RG1}$ flows into the resistor $R_{G3}$ (the input impedance of the buffer is significant large). As a result, the voltage drop across $R_{G3}$ can be calculated as below:

$$V_{RG3} = R_{G3} \times I_{RG1} = (R_{G3}/R_{G1}) \times V_{SENSE} = K_1 \times V_{SENSE}$$
$$\text{with } K_1 = R_{G3}/R_{G1} \quad (10)$$

The $V_{RG3}$ will be buffered by the second stage amplifier with a voltage gain of $K_2$ (can be adjusted by SEL1 and SEL2):

$$V_{OUT} = K_1 \times K_2 \times V_{SENSE} = G \times V_{SENSE}$$
$$\text{with } G = K_1 \times K_2 \quad (11)$$

$$\text{or: } V_{OUT} = G \times R_{SENSE} \times I_{LOAD} \quad (12)$$

The first gain $K_1$, which is equal to $R_{G3}/R_{G1}$, can be set to 20V/V. The second gain $K_2$ can be set to 1, 1.25, 2.5 or 5 by the voltage level of SEL1 and SEL2. The values of $R_{SENSE}$ and gain will determine the full-scale output voltage range of the SGM8196, so these values should be selected properly based on the application.

## APPLICATION INFORMATION (continued)

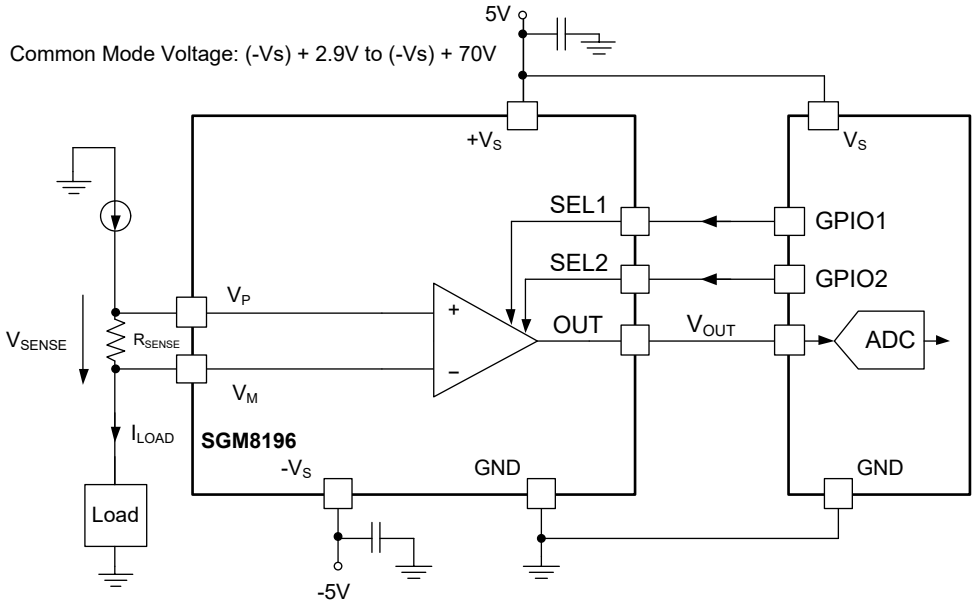



**Figure 7. Dual-Supply Operation Schematic**

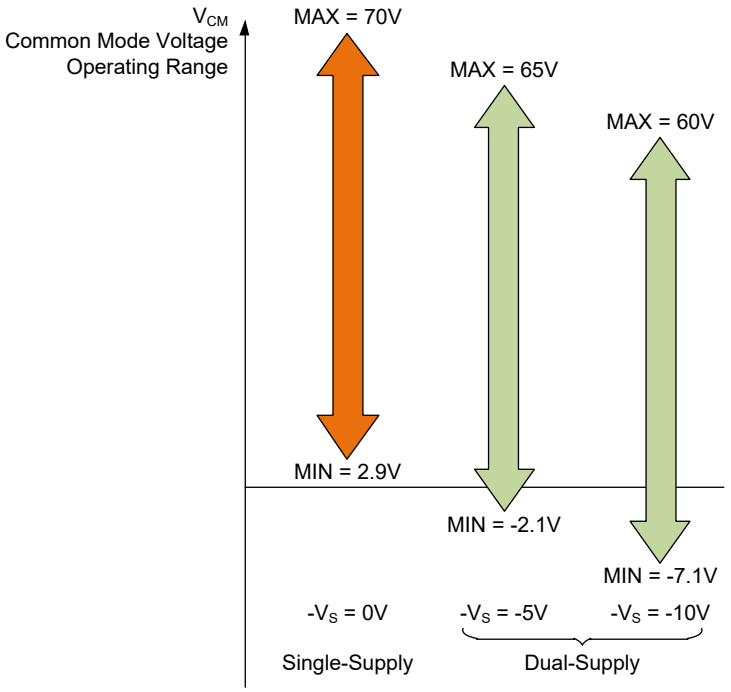



**Figure 8. Common Mode vs. Supply Voltage in Dual-Supply Operation**

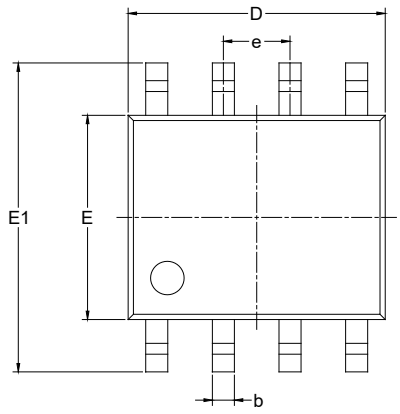
# REVISION HISTORY

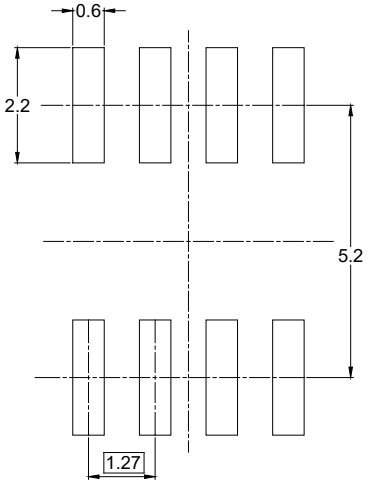
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (AUGUST 2024) to REV.A | Page |
|---|---|
| Changed from product preview to production data | All |

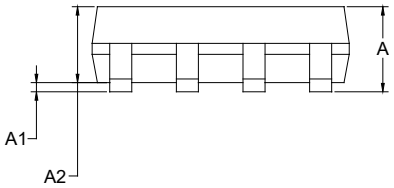
# PACKAGE OUTLINE DIMENSIONS

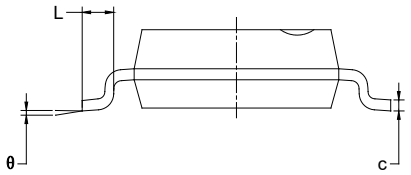
## SOIC-8




**RECOMMENDED LAND PATTERN** (Unit: mm)



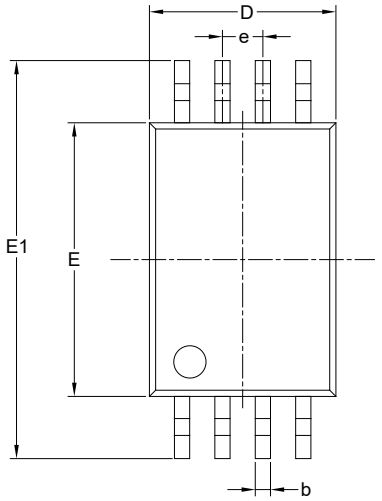



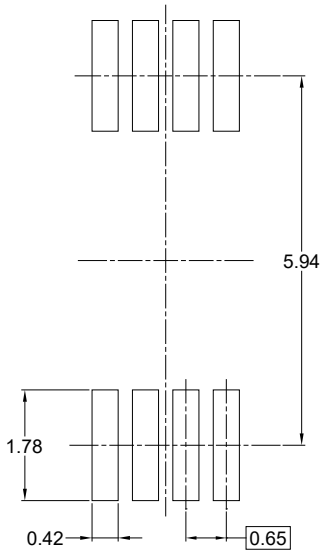

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

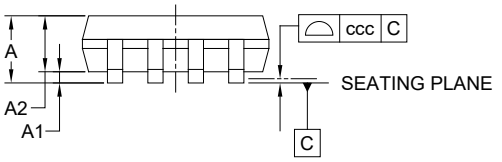
# PACKAGE OUTLINE DIMENSIONS

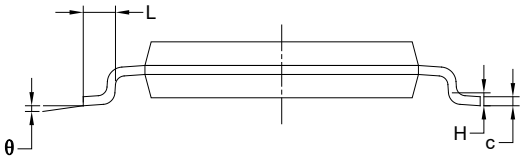
## TSSOP-8




**RECOMMENDED LAND PATTERN** (Unit: mm)



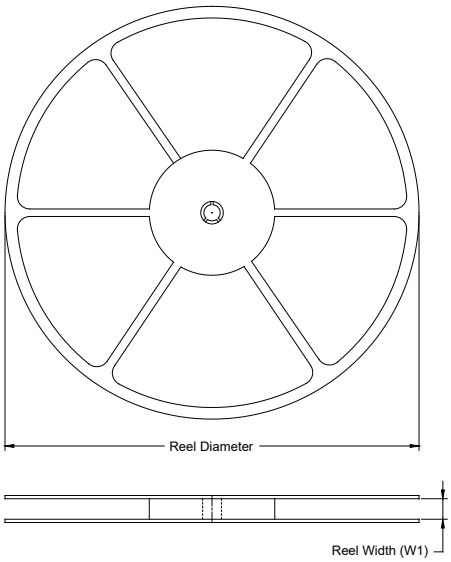




| Symbol | Dimensions In Millimeters | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.200 |
| A1 | 0.050 | - | 0.150 |
| A2 | 0.800 | - | 1.050 |
| b | 0.190 | - | 0.300 |
| c | 0.090 | - | 0.200 |
| D | 2.900 | - | 3.100 |
| E | 4.300 | - | 4.500 |
| E1 | 6.200 | - | 6.600 |
| e | 0.650 BSC | | |
| L | 0.450 | - | 0.750 |
| H | 0.250 TYP | | |
| θ | 0° | - | 8° |
| ccc | 0.100 | | |

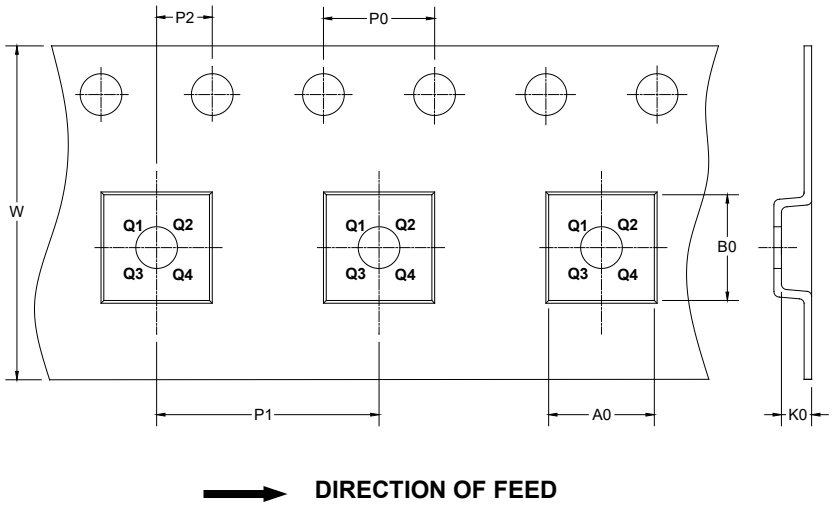
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

# TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



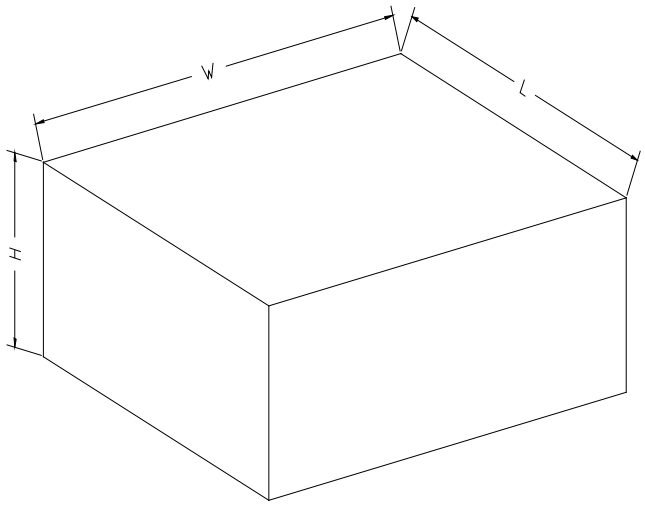

NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| SOIC-8 | 13″ | 12.4 | 6.40 | 5.40 | 2.10 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| TSSOP-8 | 13″ | 12.4 | 6.76 | 3.30 | 1.80 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

## CARTON BOX DIMENSIONS




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|---|---|---|---|---|
| 13″ | 386 | 280 | 370 | 5 |

DD0002