SGM61060
2.9V to 6V Input, 6A Output, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM61060 is an efficient, 6A, synchronous, Buck converter with integrated power MOSFETs and wide 2.9V to 6V input range. This current mode control device is optimized for high density applications with minimal number of external components. High switching frequency, up to 2MHz, can be chosen to reduce the solution size by smaller inductor and capacitors. This device can be used as a standalone or tracking power supply. The SS/TR pin can be used to control the output voltage startup ramp or as an input for tracking.

Power supply sequencing for two or more power supplies is possible by using the enable input (EN) and the open-drain power good output (PG) signals.

The high-side (HS) MOSFET current is cycle-by-cycle limited for overload protection. The low-side (LS) MOSFET sourcing current is also limited to prevent current runaway. The low-side switch also has a sinking current limit will turn the switch off if an excessive reverse current flows through it.

Thermal shutdown protection is activated to prevent damage to the device when the junction temperature is above the shutdown threshold.

The SGM61060 is available in a Green TQFN-3×3-16CL package.

FEATURES

- **Supply Voltage Range: 2.9V to 6V**
- **Low R_{DSON} Integrated Switches (11.2mΩ/11.2mΩ)**
- **Fixed 200kHz to 2MHz Switching Frequency**
- **External Clock Synchronization**
- **Voltage Tracking Capability**
- **0.6V Internal Voltage Reference**
- **2μA (TYP) Shutdown Quiescent Current**
- **Hiccup Mode Current Limit**
- **Monotonic Startup with Pre-Biased Outputs**
- **Adjustable Soft-Start Time**
- **Power Sequencing Capability**
- **Under-Voltage/Over-Voltage Power Good Output**
- **Adjustable Input Under-Voltage Lockout (UVLO)**
- **Available in a Green TQFN-3×3-16CL Package**

APPLICATIONS

Industrial and Commercial Power Systems
Low-Voltage Distributed Power Systems
Server and Storage
Communications Equipment

TYPICAL APPLICATION

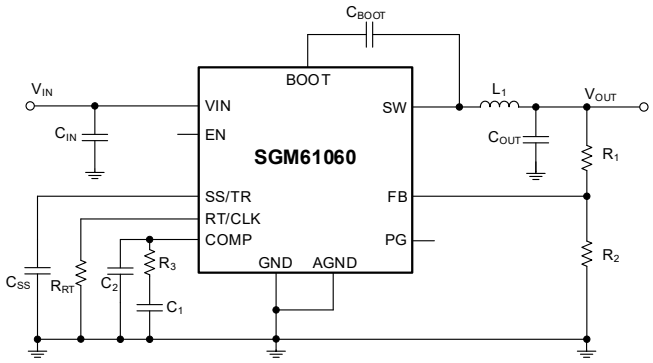
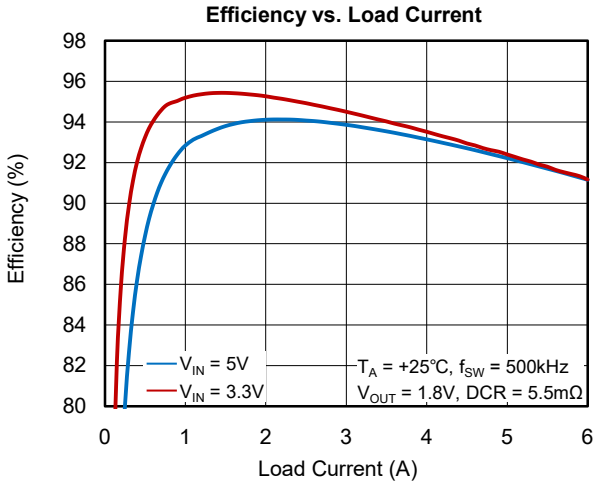


Figure 1. Typical Application Circuit

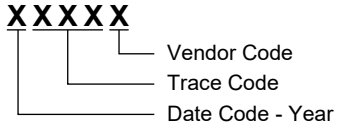


PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM61060	TQFN-3×3-16CL	-40℃ to +140℃	SGM61060XTSM16G/TR	01LSM XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Voltage
VIN, EN ..... -0.3V to 7V
RT/CLK, PG ..... -0.3V to 6V
COMP, SS/TR, FB ..... -0.3V to 3V
Output Voltage
BOOT-SW 7V
SW ..... -0.7V to 7V
SW, 20ns Transient ..... -2V to 10V
SW, 5ns Transient ..... -4V to 12V
Source Current
EN, RT/CLK 100μA
Sink Current
COMP, SS 100μA
PG 10mA
Package Thermal Resistance
TQFN-3×3-16CL, θ_{JA} ..... 42℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 2000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range ..... 2.9V to 6V
Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

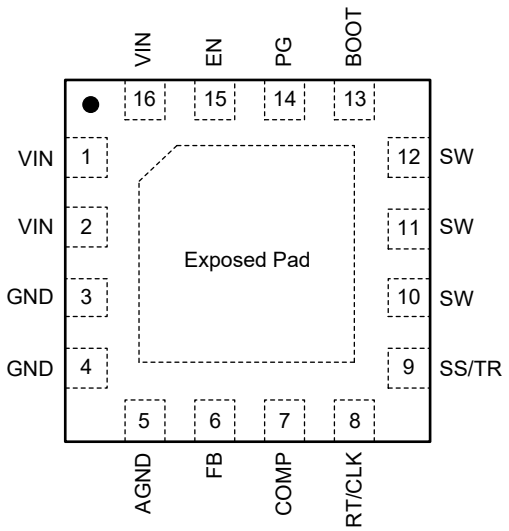
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TQFN-3×3-16CL

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1, 2, 16	VIN	I	Power Input for the Control Circuitry.
3, 4	GND	G	Control Circuit and Low-side Power MOSFET Ground Returns.
5	AGND	G	Analog Ground. Only connected to the GND pins.
6	FB	I	Inverting Input of the Transconductance Error Amplifier.
7	COMP	O	Error Amplifier Output and the Input to the High-side Switch Current Comparator. Connect the frequency compensation circuit between this pin and GND.
8	RT/CLK	I/O	An Input Pin for RT Programming Resistor or External CLK Input (auto select) for Setting the Switching Frequency. In RT mode, an external timing resistor connected between this pin and GND adjusts the switching frequency. In CLK mode, the device synchronizes to an external clock received by this pin.
9	SS/TR	I/O	Soft-Start and Tracking Input. Connect a capacitor between the SS and GND to set the rise time of the internal voltage reference. A voltage applied on this pin (TR) overrides the internal reference and the output will follow that voltage. This feature is used for tracking and sequencing functions.
10, 11, 12	SW	O	Switching Node Output of the Converter.
13	BOOT	I	Bootstrap Input to Supply the High-side Gate Driver. A bootstrap capacitor (0.1μF) is required between the BOOT and SW pins. The voltage on this capacitor supplies the gate driver of the high-side MOSFET.
14	PG	O	Power Good Open-Drain Output Pin. PG is released to go high by the external pull-up resistor if the output is in regulation. It is pulled low during soft-start, when EN is low or during fault events such as thermal shutdown, dropout and over-voltage.
15	EN	I	Enable Input Pin with Internal Pull-Up. Float this pin to enable the device or pull it down to disable it. The EN input can be used to adjust the input UVLO by a resistor divider from VIN.
—	Exposed Pad	—	Package Thermal Pad and Analog Ground. This pad must be soldered to the ground plane for proper operation and heat relief. Connect it to a PCB ground on the top layer that is only connected to the GND pins. Use it as reference for RT, COMP, SS/TR, UVLO setting and VIN bypass.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.9V to 6V, T_J = -40℃ to +150℃, all typical values are measured at V_{IN} = 5V and T_J = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (VIN Pin)							
Operating Input Voltage	V_{IN}			2.9		6	V
Shutdown Supply Current	I_{SD}	V_{EN} = 0V	T_J = +25℃		2	3	μA
			T_J = -40℃ to +150℃			15	
Operating Non-Switching Supply Current	I_Q	V_{FB} = 0.62V, V_{IN} = 5V	T_J = +25℃		930	1100	μA
			T_J = -40℃ to +150℃			1300	
Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising			2.4	2.6	V
Under-Voltage Lockout Threshold Hysteresis	V_{UVLO_HYS}	Hysteresis			105		mV
Enable and UVLO (EN Pin)							
Enable Threshold	V_{EN_R}	Rising			1.28	1.5	V
	V_{EN_F}	Falling		1.0	1.16		
Input Current	I_P	Enable threshold + 50mV			-3.8		μA
		Enable threshold - 50mV			-0.75		
Voltage Reference							
Voltage Reference	V_{REF}	V_{IN} = 2.9V to 6V	T_J = +25℃	0.595	0.6	0.605	V
			T_J = -40℃ to +150℃	0.585	0.6	0.615	
MOSFET							
High-side Switch Resistance	R_{DSON_H}	$V_{BOOT-SW}$ = 5V			11.2	22	mΩ
		$V_{BOOT-SW}$ = 2.9V			13	24	
Low-side Switch Resistance	R_{DSON_L}	V_{IN} = 5V			11.2	22	mΩ
		V_{IN} = 2.9V			13	24	
Error Amplifier							
Input Current	I_{IN}				2		nA
Error Amplifier Transconductance (gm)	gm_{EA}	-2μA < I_{COMP} < 2μA, V_{COMP} = 1V			265		μA/V
Error Amplifier Transconductance (gm) during Slow-Start		-2μA < I_{COMP} < 2μA, V_{COMP} = 1V, V_{FB} = 0.4V			102		
Error Amplifier Source/Sink Current	I_{EA}	V_{COMP} = 1V, 100mV overdrive			±23		μA
COMP to SW Current gm	gm_{ps}				19		A/V
Current Limit							
Current Limit Threshold	I_{LIMT}	f_{SW} = 500kHz, V_{IN} = 6V		10	12	14	A
		f_{SW} = 500kHz, V_{IN} = 2.9V to 6V		7	12	14.5	
Cycles before Entering Hiccup during Over-Current					512		cycles
Hiccup Cycles					16384		cycles
Low-side Sourcing Current Threshold				6	8.5	12.5	A
Low-side FET Reverse Current Protection					4.5		A
Thermal Shutdown							
Thermal Shutdown	T_{SD}				170		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}				15		℃

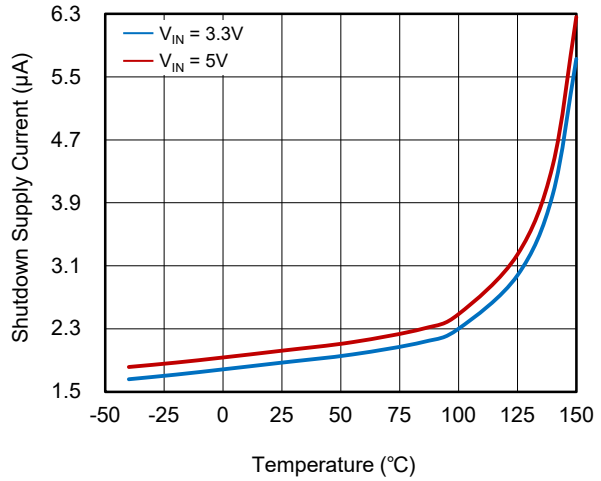
ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 2.9V to 6V, T_J = -40℃ to +150℃, all typical values are measured at V_{IN} = 5V and T_J = +25℃, unless otherwise noted.)

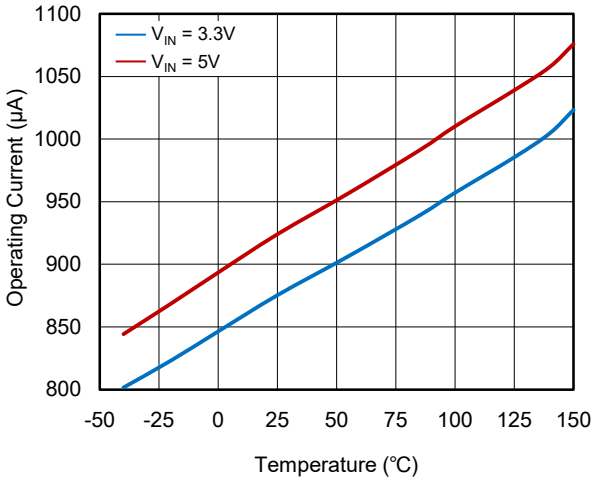
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timing Resistor and External Clock (RT/CLK Pin)						
Switching Frequency Range Using RT Mode	f_{SW}		200		2000	kHz
Switching Frequency	f_{SW}	R_{RT} = 82.5kΩ	420	500	580	kHz
Switching Frequency Range Using CLK Mode	f_{CLK}		200		2000	kHz
Minimum CLK Input Pulse Width	t_{CLK_MIN}			75		ns
RT/CLK Voltage		R_{RT} = 82.5kΩ		0.5		V
RT/CLK High Threshold				1.6	2.2	V
RT/CLK Low Threshold			0.4	1.2		V
RT/CLK Falling Edge to SW Rising Edge Delay		Measure at 500kHz with R_{RT} resistor in series		55		ns
PLL Lock-In Time	t_{LOCK_IN}	Measure at 500kHz		40		μs
SW (SW Pin)						
Minimum On-Time	t_{ON}	Measured at 50% points on SW, I_{OUT} = 3A		85		ns
Minimum Off-Time	t_{OFF}	Prior to skipping off pulses, $V_{BOOT-SW}$ = 3V, I_{OUT} = 3A		70		ns
BOOT (BOOT Pin)						
Charging Resistor		V_{IN} = 5V, $V_{BOOT-SW}$ = 5V		12		Ω
BOOT-SW UVLO		V_{IN} = 3.3V		2.2		V
Soft-Start and Tracking (SS/TR Pin)						
Charge Current	I_{SS}	$V_{SS/TR}$ < 0.15V		48		μA
		$V_{SS/TR}$ > 0.15V		2.2		
SS/TR to FB Matching	V_{SS_OFFSET}	V_{IN} = 3.3V		18	60	mV
SS/TR to Reference Crossover		98% nominal		0.68		V
SS/TR Discharge Voltage (Overload)		V_{FB} = 0V		15		mV
SS/TR Discharge to Current (Overload)		V_{FB} = 0V, $V_{SS/TR}$ = 1.5V		160		μA
SS/TR Discharge Current (UVLO, EN, Thermal Fault)		V_{IN} = 3V, $V_{SS/TR}$ = 1.5V		850		μA
Power Good (PG Pin)						
FB Threshold		V_{FB} falling (fault)		91		% V_{REF}
		V_{FB} rising (good)		94		% V_{REF}
		V_{FB} rising (fault)		106		% V_{REF}
		V_{FB} falling (good)		104		% V_{REF}
Output High Leakage		V_{FB} = V_{REF}, V_{PG} = 5.5V		2	1000	nA
On-Resistance		V_{IN} = 5V		77	120	Ω
Output Low		I_{PG} = 2.5mA, V_{IN} = 5V		0.19	0.3	V
Minimum V_{IN} for Valid Output		V_{PG} < 0.5V at 100μA		1.0	1.2	V

TYPICAL PERFORMANCE CHARACTERISTICS

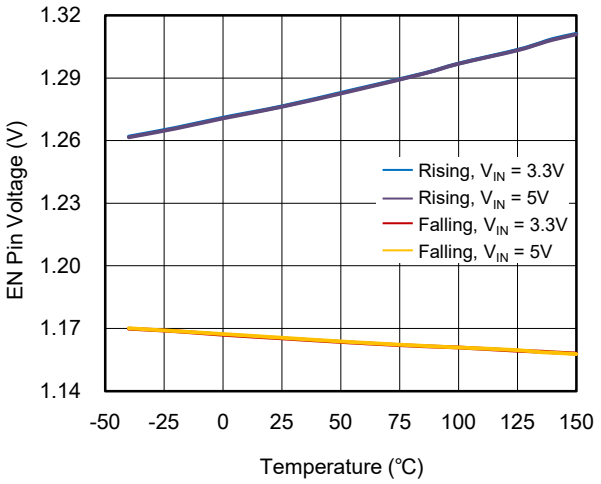
Shutdown Supply Current vs. Junction Temperature



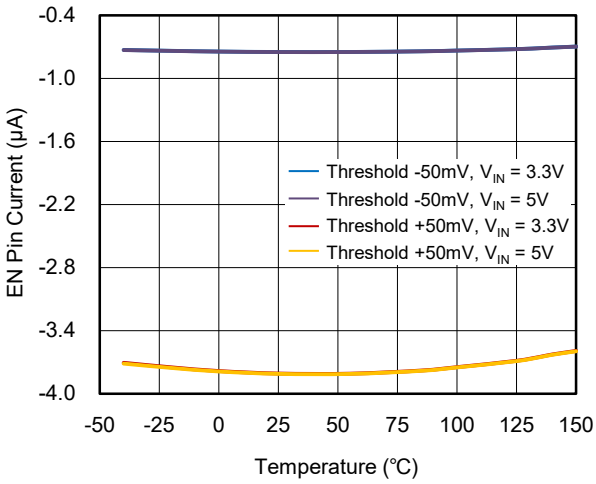
Operating Current vs. Junction Temperature



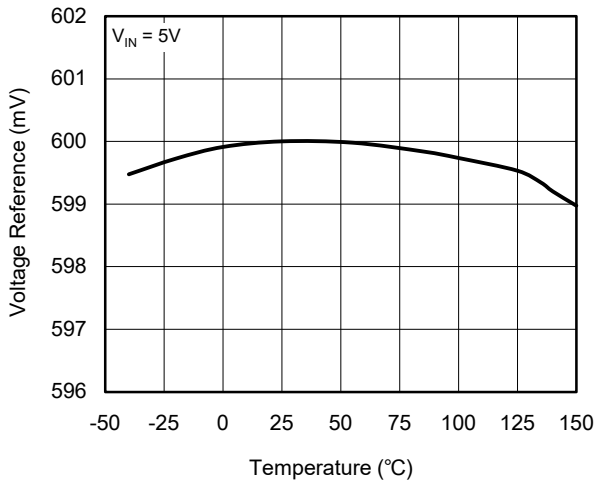
EN Pin Voltage vs. Junction Temperature



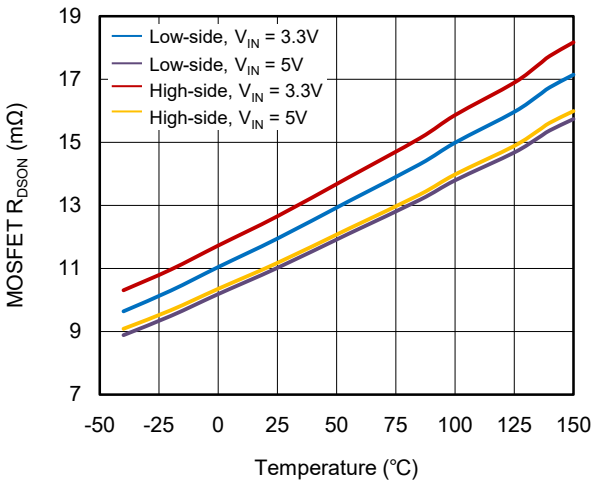
EN Pin Current vs. Junction Temperature



Voltage Reference vs. Junction Temperature

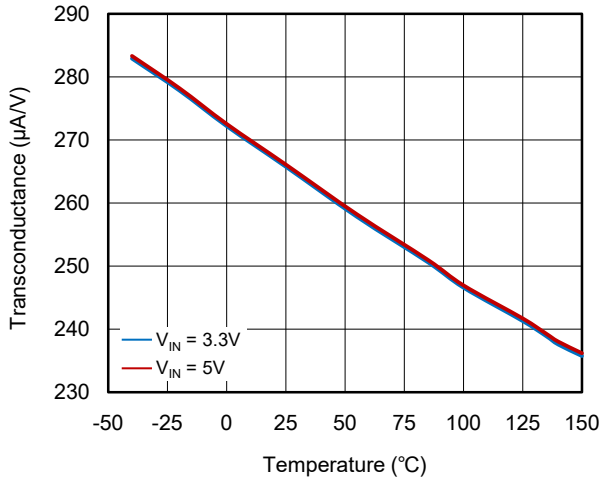


MOSFET R_{DSON} vs. Junction Temperature

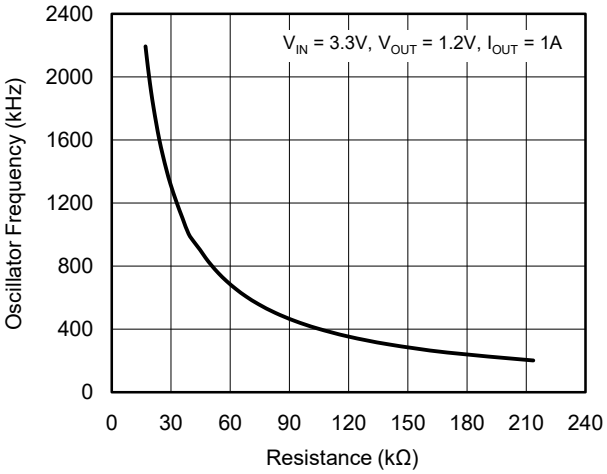


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

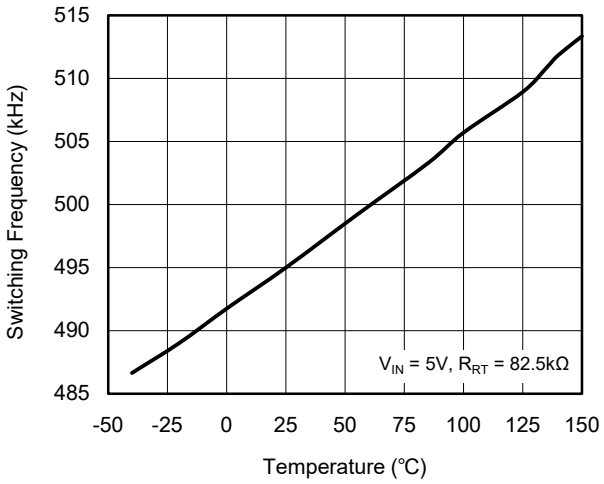
Transconductance vs. Junction Temperature



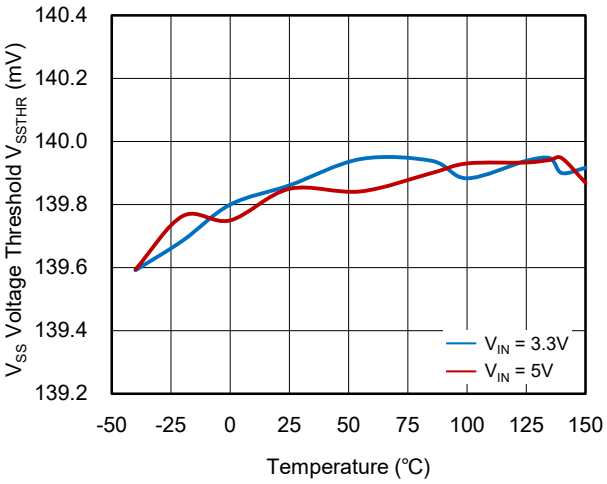
Frequency vs. Resistance



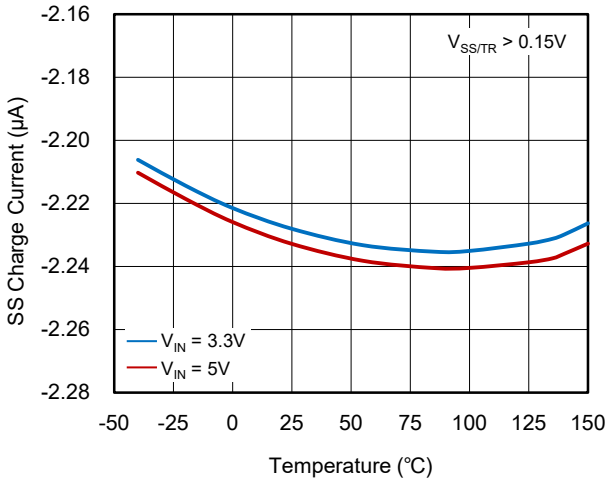
Switching Frequency vs. Junction Temperature



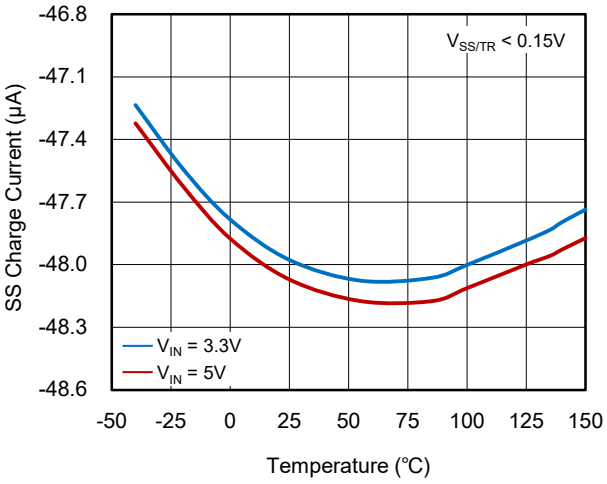
VSS Voltage Threshold vs. Junction Temperature



SS Charge Current vs. Junction Temperature

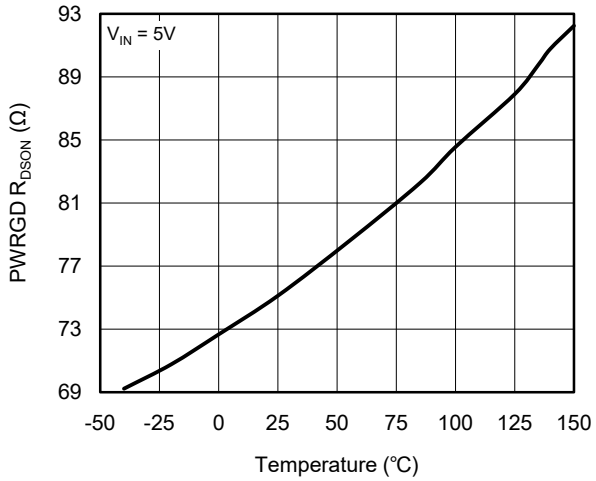


SS Charge Current vs. Junction Temperature

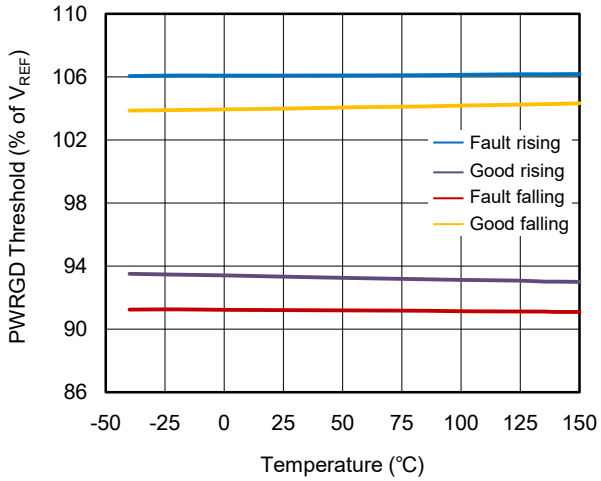


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

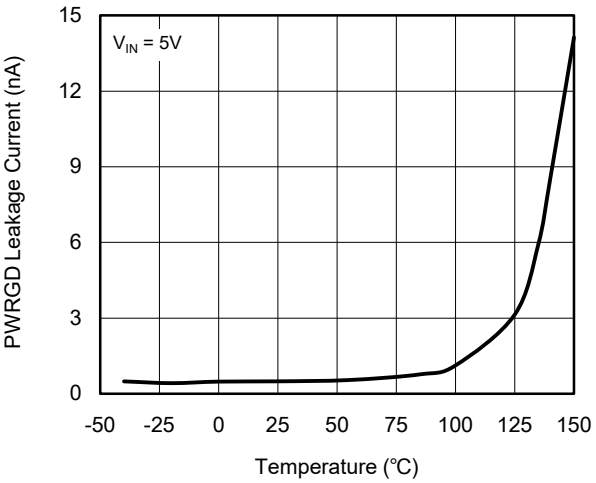
PWRGD R_{DSON} vs. Junction Temperature



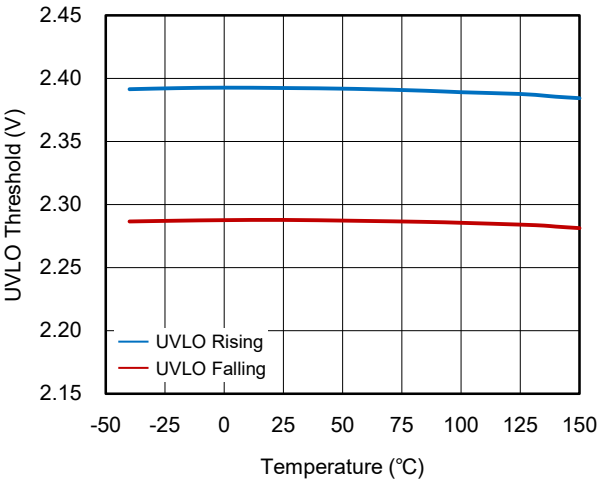
PWRGD Threshold vs. Junction Temperature



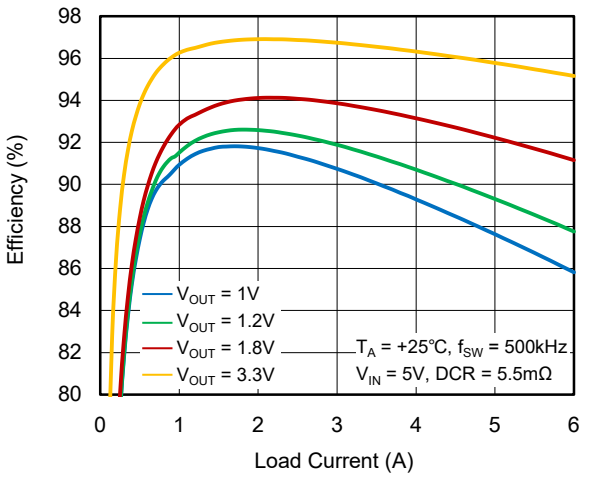
PWRGD Leakage Current vs. Junction Temperature



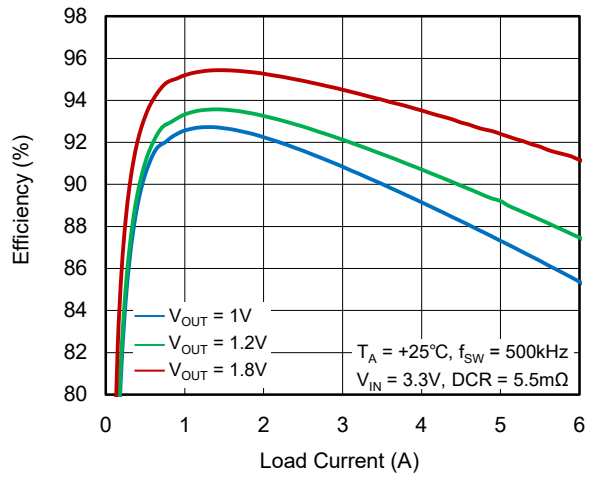
Under-Voltage Lockout Threshold vs. Junction Temperature



Efficiency vs. Load Current



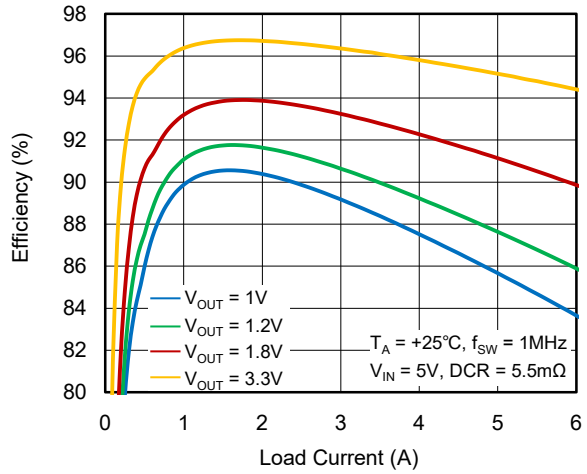
Efficiency vs. Load Current



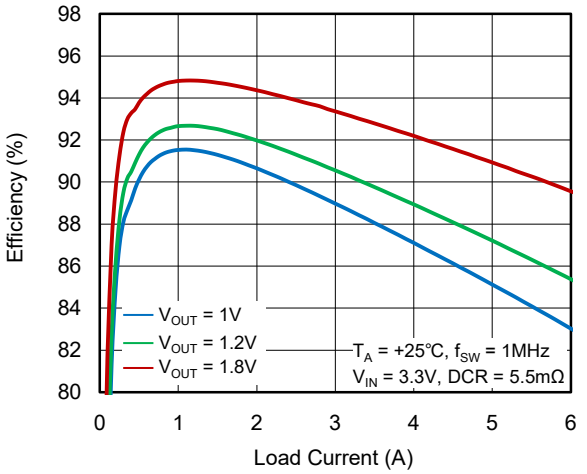
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 2.9V to 6V, V_{OUT} = 1.2V, C_{OUT} = 5 × 47μF and L = 1μH, unless otherwise noted.

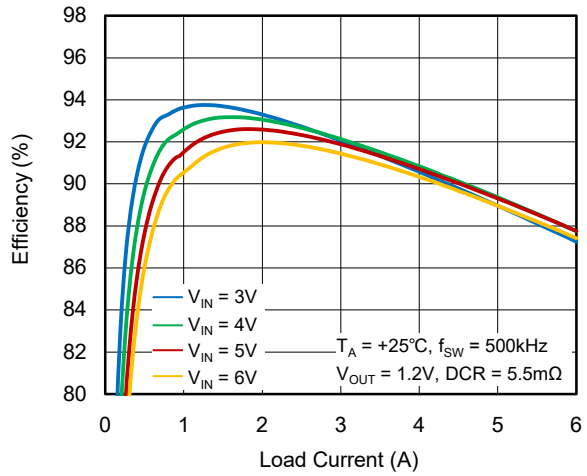
Efficiency vs. Load Current



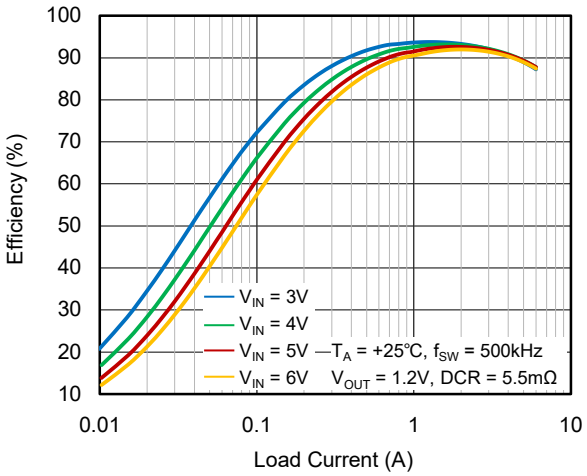
Efficiency vs. Load Current



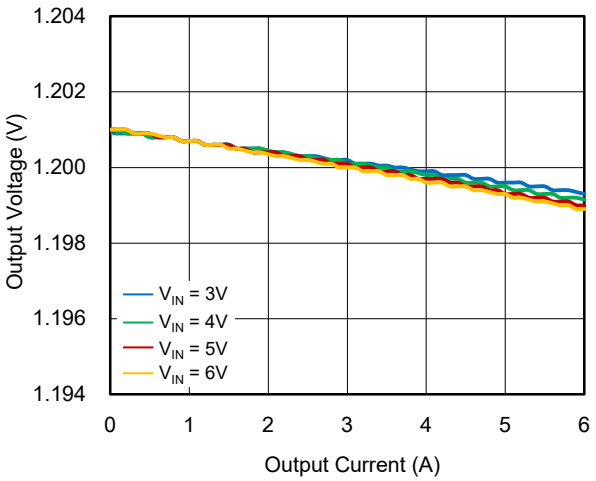
Efficiency vs. Load Current



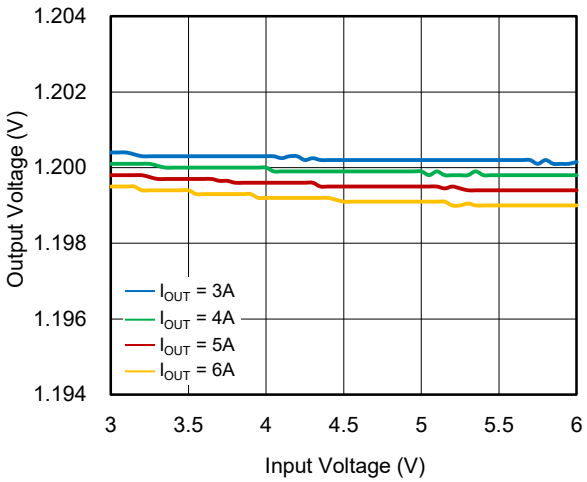
Efficiency vs. Load Current



Load Regulation



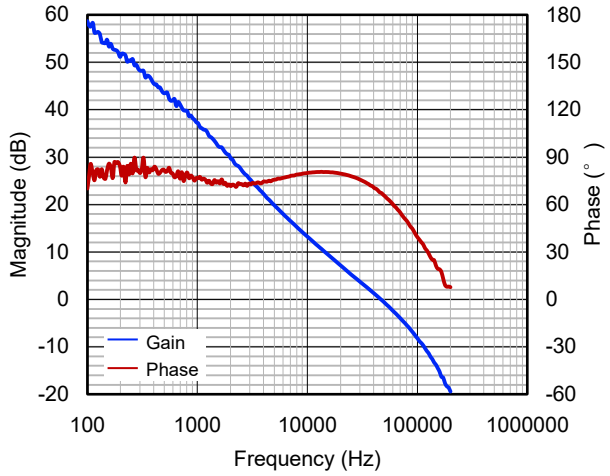
Line Regulation



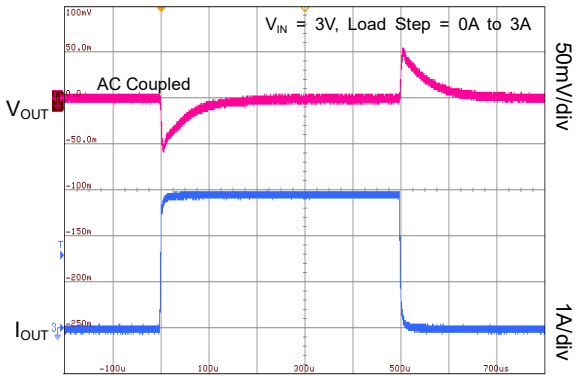
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{IN} = 2.9V to 6V, V_{OUT} = 1.2V, C_{OUT} = 5 × 47μF and L = 1μH, unless otherwise noted.

Loop Response

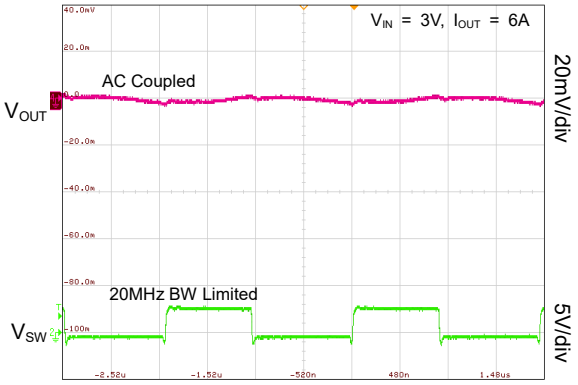


Transient Response



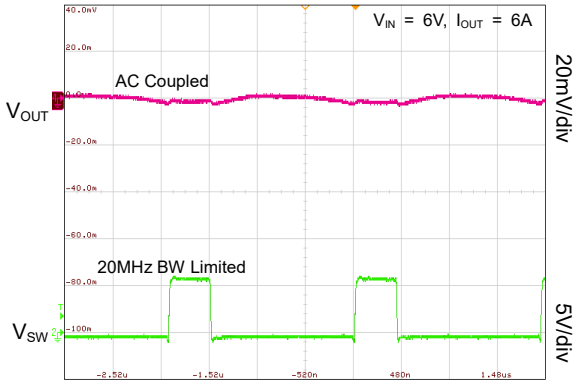
Time (100μs/div)

Output Ripple



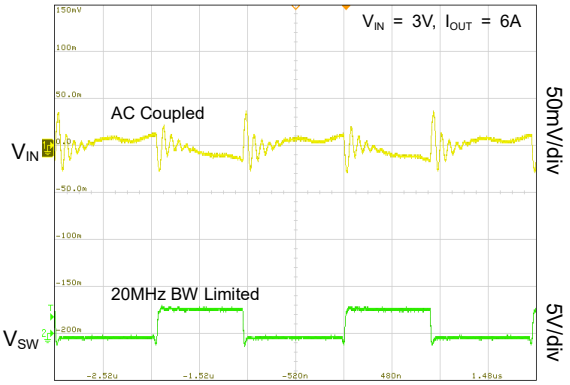
Time (500ns/div)

Output Ripple



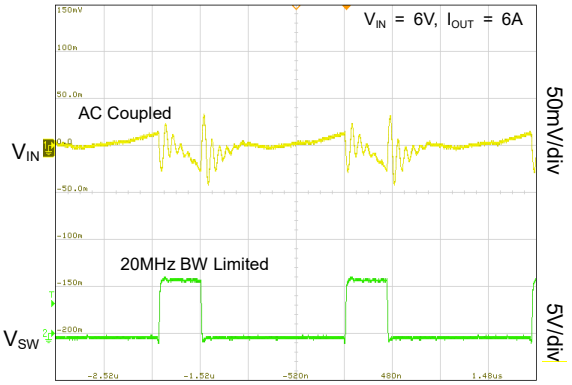
Time (500ns/div)

Input Ripple



Time (500ns/div)

Input Ripple

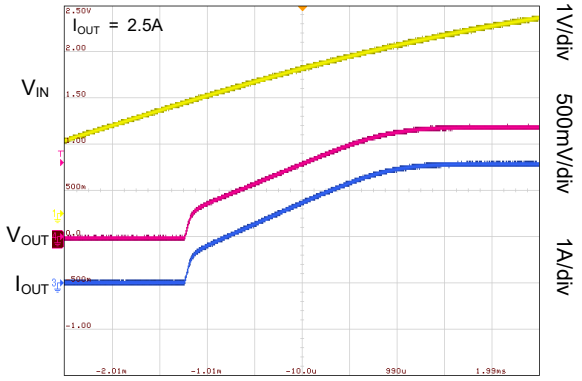


Time (500ns/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

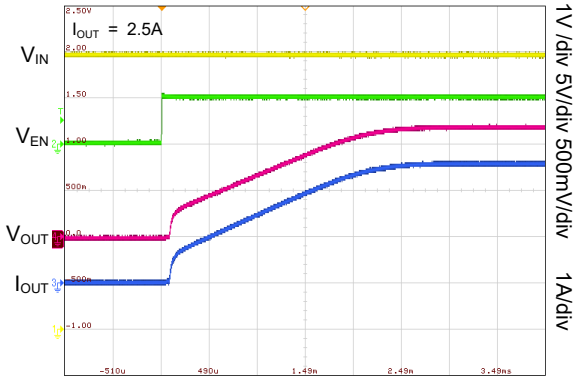
T_A = +25℃, V_{IN} = 2.9V to 6V, V_{OUT} = 1.2V, C_{OUT} = 5 × 47μF and L = 1μH, unless otherwise noted.

Startup Relative to V_{IN}



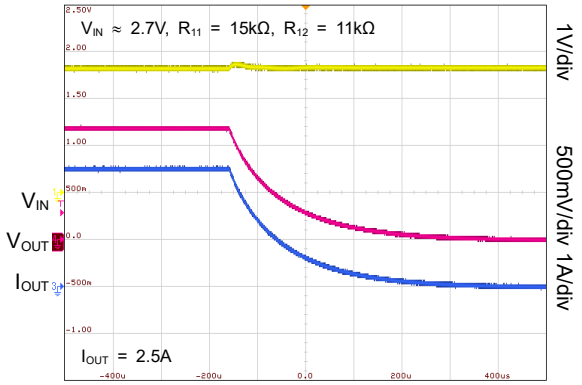
Time (500μs/div)

Startup Relative to Enable



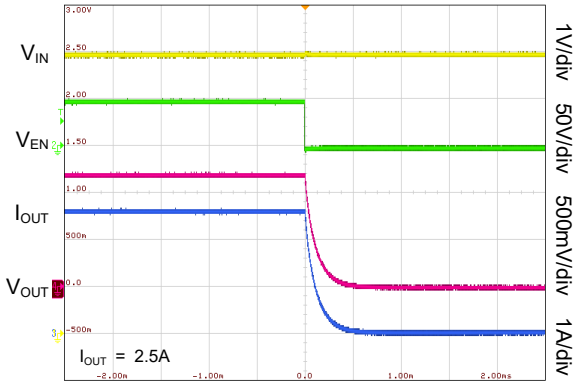
Time (500μs/div)

Shutdown Relative to V_{IN}



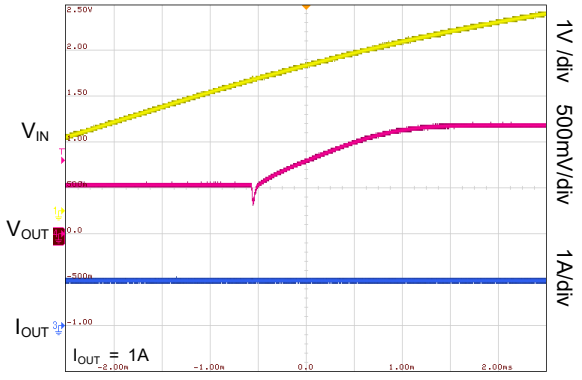
Time (100μs/div)

Shutdown Relative to Enable



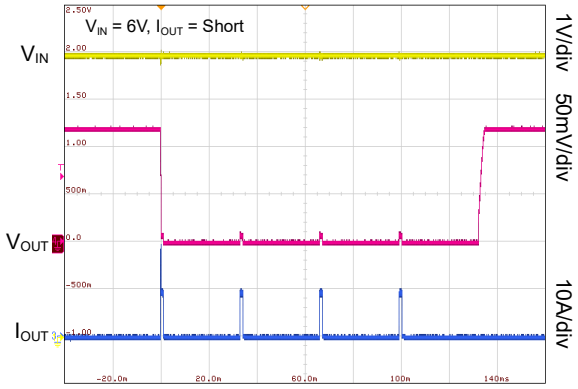
Time (500μs/div)

Startup into Prebias



Time (500μs/div)

Short Entry and Recovery



Time (20ms/div)

FUNCTIONAL BLOCK DIAGRAM

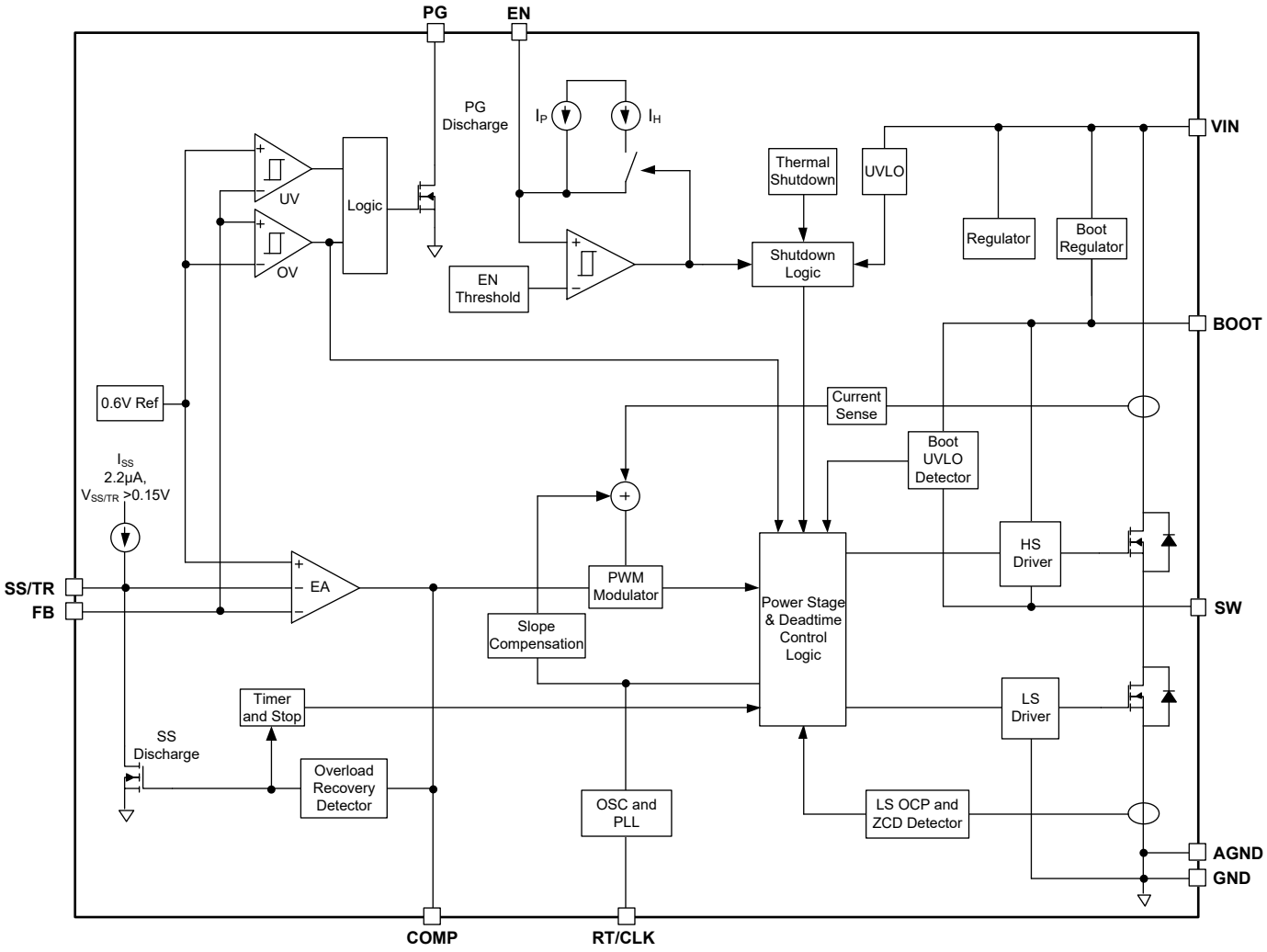


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61060 is a 2.9V to 6V, 6A, synchronous Buck converter with integrated high-side and low-side MOSFETs. The output voltage can be set as low as 0.6V, which is equal to the device internal reference voltage (V_{REF}).

As a constant frequency, peak current mode control device, SGM61060 can provide fast transient response with a simple compensation circuit. The fixed switching frequency is adjustable from 200kHz to 2000kHz to allow optimization of the efficiency and size of the converter. For adjusting the internal switching frequency, an external resistor R_{RT} is connected between the RT/CLK pin and GND. The device also accepts an external clock source on this pin to synchronize the oscillator using the internal phase locked loop (PLL).

This device has a safe and monotonic startup in output pre-biased conditions. The V_{IN} must exceed the under-voltage lockout threshold (V_{UVLO}, 2.4V TYP) for device power-up. The UVLO thresholds can be adjusted (increased) by connecting the EN pin to the tap point of a resistor divider between the VIN pin and GND. The EN internal pull-up current source and the resistor divider determine the UVLO thresholds. When the EN is floated or is pulled high, the device is enabled and the total device current (no switching) is near 880μA. Pulling the EN pin low will shut down the device with 2μA (TYP) supply current.

The integrated MOSFETs are optimized for higher efficiency at lower duty cycles. They can efficiently provide up to 6A continuous output current.

The integrated bootstrap circuit along with the external boot capacitor provides the bias voltage for the high-side MOSFET driver. The voltage of the bootstrap capacitor that is placed between the BOOT and SW pins is continuously monitored for bootstrap UVLO (BOOT-SW UVLO) detection. If the boot capacitor voltage drops below the bootstrap UVLO, the SW pin will be pulled low to recharge the boot capacitor. 100% duty cycle operation is possible as long as the boot capacitor voltage is higher than the 2.2V (TYP) threshold (preset UVLO level).

The device contains a power good (PG) pin which indicates the status of the output voltage by comparing the FB voltage and the internal reference voltage. PG pin is connected to the drain of internal MOSFET. The PG signal is high when VOUT is between 94% and 104% of its nominal (set) value and goes low if V_{OUT} drops below 91% or rises above 106% of its nominal value.

The SS/TR (soft-start/tracking) pin can be used to minimize the inrush currents (soft-start function) with a small value capacitor, or for power supply sequencing during power-up with a resistor divider from preceding voltage rail. It is the input pin for the voltage that is followed by the output when the power supply is used in the tracking mode.

The SGM61060 is protected from output over-voltage, over-current and over-heating damage. The output over-voltage transients are effectively minimized by the over-voltage comparator of the power good circuit. When an over-voltage occurs, the high-side switch is forced off and allowed to turn on again if the V_{OUT} drops below 104% of its nominal value.

High-side MOSFET is naturally protected from sourcing over-current by peak current mode control. The low-side MOSFET is also protected bi-directionally against over-current. This feature helps the control of the inductor current to avoid current runaway.

If the die temperature is too high ($T_J > T_{SD}$), the device will stop switching and go to shutdown state. It will automatically recover with a soft-start when the junction temperature drops 15℃ (TYP) below the shutdown temperature.

Note that a continued overload condition may cause a cycling thermal shutdown and recovery. It will depend on the temperature and the ventilation conditions of the system.

DETAILED DESCRIPTION (continued)

Power Input Pins

VIN pins can be tied together or separated depending on the application and minimum input voltage. The VIN pin supplies the internal circuits of the device and needs to be above 2.9V. A voltage divider connected to the EN pin from either VIN can be used to adjust the power supply UVLO.

EN Pin and UVLO Programming

The EN pin is used to turn the device on and off. The device starts operation when the EN pin voltage rises above the enable rising threshold. Pulling the EN voltage below the enable falling threshold, stops switching and reduces the device current to the very low quiescent shutdown level. Floating the EN pin enables the device due to its internal pull-up current source. This current source is used for programming the UVLO threshold. An open-drain or open-collector output connected to the EN pin can be used to control the device. An internal UVLO circuit is implemented on the VIN pin to disable the device and prevent malfunction when the supply voltage is too low. The internal V_{UVLO} hysteresis is 105mV. To program a higher UVLO threshold for the VIN that is typically needed for split-rail applications, the EN pin can be configured to Figure 3. Without external components, the internal pull-up current (I_P) sets the EN pin default state to enable. When the device is enabled, the second current source (I_H) is activated. I_P and I_H are used to set the UVLO.

The divider resistors can be calculated from Equations 1 and 2 based on the desired UVLO start and stop thresholds. A 300mV or higher hysteresis (V_{START} - V_{STOP}) is recommended for the UVLO programming.

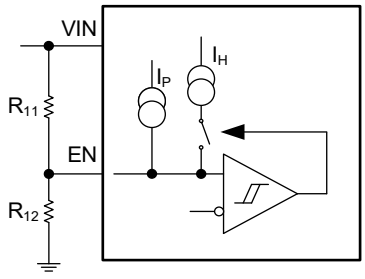


Figure 3. VIN UVLO Setting with a Resistor Divider

$$R_{11} = \frac{V_{START}\left(\frac{V_{EN\_F}}{V_{EN\_R}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{EN\_F}}{V_{EN\_R}}\right) + I_H} \quad (1)$$

$$R_{12} = \frac{R_{11} \times V_{EN\_F}}{V_{STOP} - V_{EN\_F} + R_{11}(I_P + I_H)} \quad (2)$$

where:

- I_H = 3.05μA.
- I_P = 0.75μA.
- V_{EN_R} = 1.28V.
- V_{EN_F} = 1.16V.

Soft-Start (SS/TR)

The lower voltage between the internal V_{REF} and the SS/TR pin is used as the reference to regulate the output. The soft-start capacitor is connected to the SS/TR pin and is charged by a 48μA ($V_{SS/TR}$ < 0.15V) or 2.2μA ($V_{SS/TR}$ > 0.15V) internal current source to set the soft-start time (t_{SS}).

Equation 3 can be used to calculate the soft-start time (10% to 90% rise) for a selected soft-start capacitor (C_{SS}).

$$t_{SS}\ (ms) = \frac{C_{SS}(nF)}{3} \quad (3)$$

Startup with Pre-biased Output

The low-side switch is prohibited from turning on and discharging the output if a pre-biased voltage is sensed on the output before startup. As long as the SS/TR pin voltage is below V_{FB}, the low-side switch is not allowed to sink current to have a monotonic startup with pre-bias output.

Reference Voltage (V_{REF})

A precise 0.6V reference is internally implemented by scaling the output of a temperature-stable bandgap circuit. The actual reference voltage for output setting is changed during startup or tracking.

DETAILED DESCRIPTION (continued)

Output Voltage Setting

The output voltage of the device can be adjusted by resistors R_1 and R_2 which are connected to the FB pin (see Figure 1) to set the output voltage. Use resistors with 1% tolerance or better for good output accuracy. Equation 4 can be used to calculate the R_1 and R_2 (upper and lower resistors) values based on the desired output voltage (V_{OUT}) and V_{REF}.

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_2 \quad (4)$$

where: V_{REF} = 0.6V.

For example, a 20kΩ resistor can be chosen for R_2 and then R_1 is calculated. Do not choose too large resistors to cause output errors due to the FB bias current or make the regulator susceptible to the noises coupled to the FB input.

The minimum and maximum adjustable output voltages are limited by the minimum on-time of the high-side switch and the required bootstrap voltage respectively. More details are provided in the Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle) section.

Power Good (PG)

The PG is an open-drain output. It is released if there is no fault and the FB pin voltage is in regulation. The PG is pulled low if the FB voltage is lower than 91% or above 106% of the reference voltage. When the device is disabled by EN pin or the voltage of SS/TR pin is under 1.33V, or if a fault such as UVLO or thermal shutdown occurs, PG is also pulled low.

A 10kΩ to 100kΩ pull-up resistor connected to a voltage rail less than 5.5V is recommended for PG. An option is to use the output voltage for PG pull-up. The state of PG is valid only if the V_{IN} > 1.2V. The current sinking capability of PG is limited until V_{IN} exceeds the 2.9V at which the full sinking capacity is available.

Startup Sequencing (SS/TR)

The SS/TR, EN and PG pins allow the implementation of common power supply sequencing methods. A simple sequencing approach is shown in Figure 4 in which the right side SGM61060 device is powered up after the left one. The PG of the first device is coupled to the EN pin of the second. The second power supply is enabled after the primary supply reaches regulation.

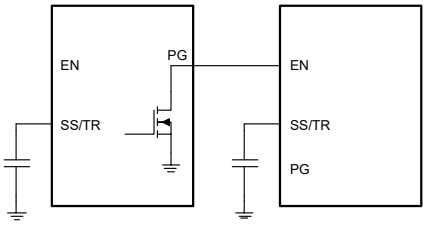


Figure 4. Sequential Startup Sequence

Frequency and Synchronization (RT/CLK)

The device can operate in two modes to adjust switching frequency.

In the RT mode, a resistor (R_{RT}) is placed between the RT/CLK and GND pins to set the free running switching frequency of the PLL.

In the CLK mode, an external clock drives the RT/CLK pin and the internal switching clock oscillator is synchronized to CLK by the PLL. The CLK mode overrides the RT mode. The device automatically detects the input clock and switches to the CLK mode.

Switching Frequency Setting (RT Mode)

Selection of the switching frequency is generally a tradeoff among the solution size, efficiency, and the minimum controllable on-time. The R_{RT} resistance can be designed from Equation 5.

$$R_{RT}\ (k\Omega) = \frac{72432}{f_{SW}(kHz)^{1.084} + 25} \quad (5)$$

Synchronization (CLK Mode)

The device uses an internal phase locked loop (PLL) to set or synchronize to an external clock signal with the 200kHz to 2000kHz range. Mode change which is from RT mode to CLK mode is allowed.

For stable synchronization, a square wave clock with 20% to 80% duty cycle must be applied to the RT/CLK pin. The logic low and high levels of the clock must be below 0.4V and above 2.2V respectively. The switching cycle starts with the falling edge of the RT/CLK signal.

If both RT and CLK modes are needed in an application, configuration shown in Figure 5 can be used. The RT mode can be overridden by CLK mode when both R_{RT} and clock are present.

DETAILED DESCRIPTION (continued)

Mode switch occurs when the RT/CLK is pulled above 2.0V for the first time. Once CLK mode is selected, the PLL is locked to external CLK and the RT/CLK pin shifts to a high-impedance state. Going back from CLK mode to RT mode is not recommended.

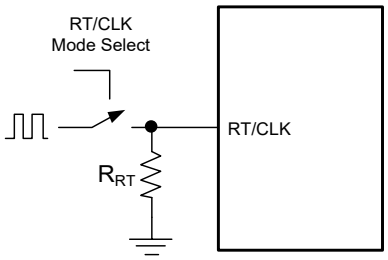


Figure 5. Using RT and CLK Modes Together

Constant Frequency PWM

The SGM61060 operates at fixed frequency that can be set by an external resistor or synchronized by external clock.

It is based on peak current control mode architecture. The high-side MOSFET is turned on until the sensing current ramp signal reaches the COMP voltage determined by the EA. If the switch current does not reach the reference value that generates from the COMP voltage at the end of a cycle, the high-side switch remains on for the next cycle until the current meets the reference value. A slope compensation block slightly reduces the sensed high-side switch current before comparison (depending on the on-time) to avoid sub-harmonic oscillations.

Continuous Current Mode Operation (CCM)

In most load conditions, the device operates in continuous conduction mode (CCM) (forced PWM). For light loads, the inductor current can be negative when the low-side switch is on. However, if the current reaches the low-side sinking current limit, the low-side switch will be forced off.

Error Amplifier

The output voltage is sensed by a resistor divider through the FB pin and is compared with the internal reference. The error amplifier generates an output current that is proportional to the voltage difference (error), and the transconductance is 265μA/V. The generated current is then fed into the external compensation network to generate the voltage on the COMP pin, which sets the reference value for the peak current that controls the on-time of the power MOSFET. COMP is pulled down to the ground when the device shuts down.

Slope Compensation

To avoid sub-harmonic oscillations that result in unstable PWM pulses, a small negative-slope compensating ramp is added to the measured switch current before it is used to generate the PWM signal. The slope compensation has no influence on the peak current limit which is maintained over full range of duty cycle.

Output Over-Voltage Protection (OVP)

The device contains an over-voltage protection circuit to avoid high overshoots of the output voltage during operation. Usually an OVP occurs after removal of an overload condition. When the output voltage is dropped due to a persisting overload, the error amplifier output reaches to its maximum and forces the converter to provide the maximum output current. Upon removal of the overload condition, the regulator output rises quickly because the high inductor current charges the output capacitor rapidly, especially if C_{OUT} is small. The error amplifier will respond and re-adjust itself but not as fast as the output filter (LC) and an overshoot occurs.

To minimize the overshoots, the device monitors the FB pin voltage and compares it to the internal OVP threshold. If the threshold is exceeded, the high-side MOSFET is turned off to stop feeding current to the output. When the FB voltage drops below the OVP threshold, the high-side MOSFET can turn on again in the next cycle.

DETAILED DESCRIPTION (continued)

Device Functional Modes

Bootstrap Voltage (BOOT) and Operation with Low Dropout (100% Duty Cycle)

An integrated bootstrap regulator is used for powering the high-side MOSFET gate driver. A small 0.1μF ceramic capacitor (X5R or X7R grade) with at least 10V rating is required between the BOOT and SW pins to supply the gate driver. It is recharged from VIN source through an internal switch every time the SW goes low. Recharge happens when the BOOT pin voltage is less than V_{IN} and the BOOT-SW voltage is below the required regulation for the high-side gate voltage.

The SGM61060 has no minimum off-time. It can operate at 100% duty cycle as long as the BOOT-SW voltage is higher than its UVLO threshold (2.2V TYP). If the BOOT-SW voltage drops below its UVLO threshold, the high-side switch turns off and the low-side switch turns on to recharge the boot capacitor. If the BOOT-SW voltage drops below its UVLO threshold, the high-side switch turns off and the low-side turns on to recharge the boot capacitor.

Over-Current Protection

Both high-side (HS) and low-side (LS) switches are protected from over-current with cycle-by-cycle current limiting as will be explained in the next two sections.

High-side Switch Over-Current Protection

Using current mode control, the pulse width (from the beginning of the cycle until HS turn-off) is determined by the compensator output voltage (V_{COMP} at COMP pin) in a cycle-by-cycle basis. In each cycle the high-side switch current is continuously compared with the current set point determined by compensator output (V_{COMP}) and when the high-side current reaches to that reference (peak current), the high-side switch is turned off.

Low-side MOSFET Over-Current Protection

The current of the low-side switch is continuously monitored while it is turned on. Normally, the low-side switch sources current from ground to the load through the inductor. Before the beginning of a new cycle, the low-side current is compared to its current limit which is normally lower than the high-side current limit. Only when the low-side source current drops below its current limit, the high-side MOSFET will turn on again for the new cycle.

In some operating conditions, the low-side switch sinks current from the load to the ground. The low-side sinking current has a typical limit of 4.5A. If this limit is exceeded, the low-side switch will immediately turn off and both switches will not turn on until the end of the cycle.

Thermal Shutdown

To protect the device from damage due to overheating, a thermal shutdown feature is implemented to disable the device when the die temperature exceeds +170℃ (TYP). A new power-up sequence is initiated automatically once the temperature falls below +155℃ (15℃ hysteresis, TYP).

Feedback Loop Small Signal Model

The equivalent small signal model of the control loop for frequency response and transient analysis is given in Figure 6.

The compensation network (R_3, C_1 and C_2) is placed in the output of the transconductance error amplifier (EA). The EA can be simplified as an ideal voltage controlled current source with 265μA/V gain. The R_{OEA} model the output resistance of the EA. Power converter is modeled with a pure 19A/V gain. The inductor dynamics are effectively removed in the cycle-by-cycle average small signal model, because with the current mode control the inductor average current is set by the compensator. The C_{OUT} and R_{ESR} model the output capacitance and its parasitic ESR.

To measure the frequency response, the loop is broken at points ‘a’ and ‘b’ to insert a small signal (e.g. 1mV) AC source. For small signal frequency response analysis, the magnitude and phase versus frequency for the output to input transfer functions of each stage is plotted. The ‘a/c’ (power stage gain), ‘c/b’ (compensation gain) and ‘a/b’ (loop gain) voltage ratios are commonly used for the analysis.

DETAILED DESCRIPTION (continued)

To simulate or test the response of the output to load steps in time domain (dynamic loop response), the load (R_L) is replaced with a stepping current source with proper amplitude, repetition rate and rate of change (A/μs) depending on the application. As a common example, stepping between 25% and 75% of the nominal load with ±1A/μs slew rate and repeating at 1kHz or 10kHz can be used for testing and comparison of the power supply transient response to rapid load changes.

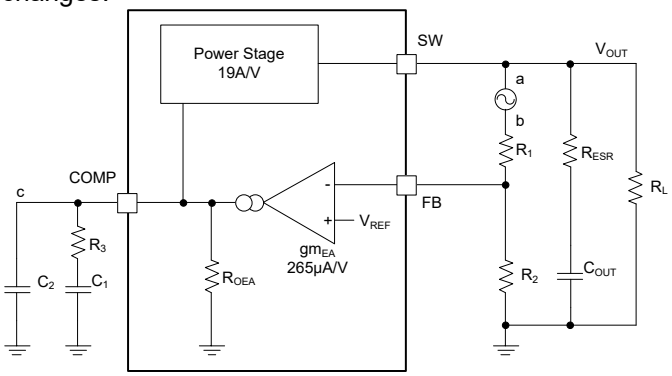


Figure 6. Small Signal Model for Loop Response

Simplified Model for Peak Current Mode

A simplified small signal model to design the frequency compensation network is given in Figure 7. The power stage and duty cycle modulator are approximated by a voltage-controlled current source (V_{CCS}) that is controlled by the error amplifier output (V_{COMP}) and provides current to the output capacitor and the load. The control-to-output transfer function (V_{OUT}/V_{COMP}) consists of a DC voltage gain (A_{DC}), a dominant pole (f_P) determined by $R_L \times C_{OUT}$ time constant, and a simple ESR-zero (f_Z) determined by $R_{ESR} \times C_{OUT}$ time constant as given in Equations 5, 6, 7 and 8. The VCCS transconductance is the ratio of the output current change to the control voltage (COMP) change. This is equivalent to the power stage transconductance (gm_{PS}) that is 19A/V for this device. As indicated in Equation 6, for resistive loads, the DC voltage gain (A_{DC}) is equal to the power stage transconductance (gm_{PS}) multiplied by the load resistance (R_L). Therefore, the DC gain drops with the reduced load resistance. This relationship can be problematic because it could move the crossover frequency of the converter in the same way.

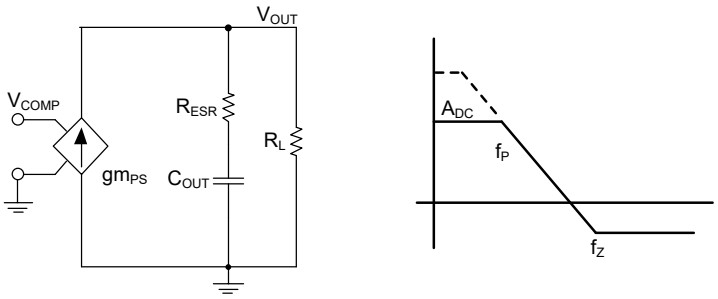


Figure 7. Simplified Model for Peak Current Mode Control and Frequency Response

$$\frac{V_{OUT}(V)}{V_{COMP}} = A_{DC} \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (6)$$

$$A_{DC} = gm_{PS} \times R_L \quad (7)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (8)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (9)$$

where:

- gm_{PS} is the gain of the power stage (19A/V).
- R_L is the load resistance.
- C_{OUT} is the output capacitance.
- R_{ESR} is the equivalent series resistance of the output capacitor.

Fortunately, the dominant pole also moves with load current as given in Equation 7. As highlighted in Figure 5, the crossover frequency (0dB gain location) is not affected by the combined effect. As the load current decreases, the gain increases and the pole frequency decreases. Having a fixed crossover frequency simplifies the design of the frequency compensation for a changing load.

DETAILED DESCRIPTION (continued)

Small Signal Model for Frequency Compensation

The SGM61060 can easily use the common Type 2 and 3 compensation circuits, as shown in Figure 6. Compared to Type 2B, the Type 2A compensation has an extra high-frequency pole (by C_2) to attenuate high-frequency noise and ensure that gain remains very low at high frequencies against the ESR-zero effect that tends to increase the gain at higher frequencies. In the Type 3 compensation, the additional C_{10} capacitor is added in parallel to the upper feedback resistor divider for phase boost at the crossover frequency. An extra resistor may be used in series with C_{10} for more control on the phase boost. The following guidelines are provided for designers who prefer to compensate by the standard loop design method. These equations are only available for those applications where the ESR-zero is higher than the control loop bandwidth (crossover frequency). This condition is usually valid when ceramic output capacitors are used. For low frequency ESR-zeros (capacitors with high ESR), see the Application Information section for a step-by-step design procedure.

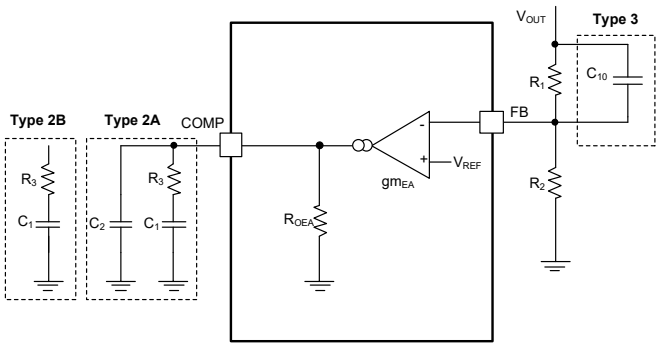


Figure 8. Types of Frequency Compensation

General Guidelines for Loop Compensation Design

1. The first step is to determine the crossover frequency, which is normally set to 1/10th of the switching frequency.

C_{OUT} is also initially chosen based on the switching frequency and ripple requirement.

2. R_3 can be determined by:

$$R_3 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{gm_{EA} \times V_{REF} \times gm_{PS}} \quad (10)$$

where:

- gm_{EA} is the gm amplifier gain (265μA/V).
- gm_{PS} is the power stage gain (19A/V).
- V_{REF} is the reference voltage (0.6V).

3. A compensating zero should be placed at the dominated pole of the device, which is at $f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi}$. C_1 can be determined by:

$$C_1 = \frac{R_L \times C_{OUT}}{R_3} \quad (11)$$

4. C_2 is optional and adds a high frequency pole to cancel the zero created by the output capacitor ESR.

$$C_2 = \frac{R_{ESR} \times C_{OUT}}{R_3} \quad (12)$$

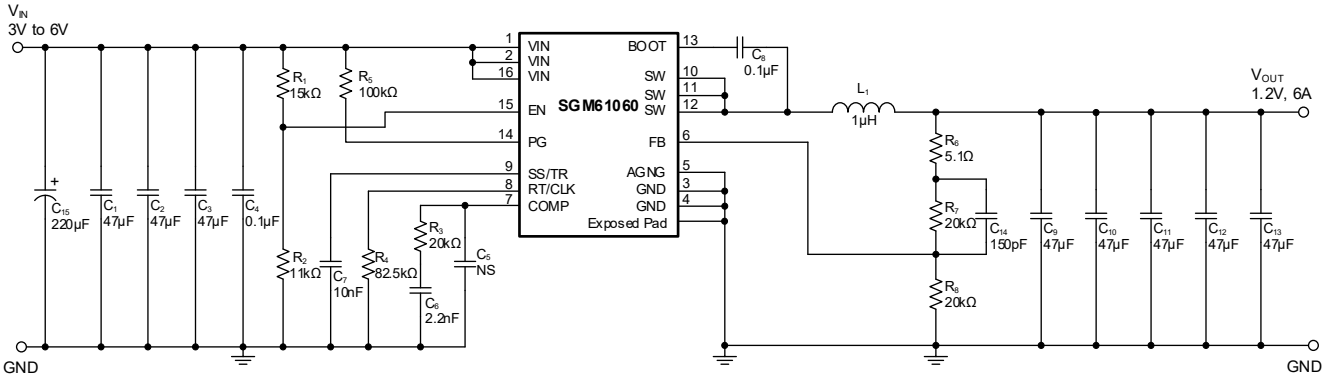
5. C_{10} can be added for Type 3 compensation that allows a slightly higher bandwidth and better phase margin. If C_{10} is needed, use Equation 12.

$$C_{10} = \frac{1}{2\pi \times R_1 \times f_C \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (13)$$

APPLICATION INFORMATION

Typical Application

The schematic of a typical application circuit that is used for SGM61060 evaluation module is given in Figure 9.



NOTE: C_{15} is optional. If the input voltage is more than 200mm far from the VIN of SGM61060, or the input voltage is on/off by air-break switch, C_{15} should be installed. Otherwise, the spike voltage over 7V at the input side is caused, which will damage SGM61060.

Figure 9. SGM61060 Typical Application Circuit

Design Requirements

In this example, a high frequency regulator with ceramic output capacitors will be designed using SGM61060 and the details will be reviewed. The design requirements are typically determined at the system level. In this example, the known parameters are summarized in Table 1.

Table 1. Design Parameters

Design Parameter	Example Value
Output Voltage	1.2V
Maximum Output Current	6A
Transient Response to 3A Load Step	ΔV_{OUT} = 5%
Input Voltage Range	5V nominal, 3V to 6V
Maximum Output Voltage Ripple	30mV_{P-P}
Switching Frequency (f_{SW})	500kHz

Operating Frequency

Usually the first parameter to design is the switching frequency (f_{SW}). Higher switching frequencies allow smaller solution size, smaller filter inductors and capacitors. The bandwidth of the converter can be increased for faster response. It is also easier to filter noises because they also shift to higher frequencies. The drawbacks are increased switching and gate driving losses that result in lower efficiency and tighter thermal limits. Also the duty cycle range and Buck ratio will be limited due to the minimum on-time and/or off-time limits of the converter. In this design, f_{SW} = 500kHz is chosen as a tradeoff. From Equation 13, the nearest standard resistor for this frequency is R_4 = 82.5kΩ.

APPLICATION INFORMATION (continued)

Inductor Design

Equation 14 is conventionally used to calculate the output inductance of a Buck converter. Generally, a smaller inductor is preferred to allow larger bandwidth and smaller size. The ratio of inductor current ripple (ΔI_L) to the maximum output current (I_{OUT}) is represented as K_{IND} factor ($\Delta I_L/I_{OUT}$). The inductor ripple current is bypassed and filtered by the output capacitor and the inductor DC current is passed to the output. Inductor ripple is selected based on a few considerations. The peak inductor current (I_{OUT} + $\Delta I_L/2$) must have a safe margin from the saturation current of the inductor in the worst-case conditions, especially if a hard-saturation core type inductor (such as ferrite) is chosen. During power-up with large output capacitor, over-current, output shorted or load transient conditions, the actual peak current of inductor can be greater than I_{L_PEAK} calculated in Equation 17. For peak current mode converter, selecting an inductor with saturation current above the switch current limit is sufficient. The ripple current also affects the selection of the output capacitor. C_{OUT} RMS current rating must be higher than the inductor RMS ripple. Typically, a 10% to 30% ripple is selected (K_{IND} = 0.1 ~ 0.3). Choosing a higher K_{IND} value reduces the selected inductance.

$$L_1 = \frac{V_{INMAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (14)$$

In this example, K_{IND} = 0.3 is chosen and the inductance is calculated to be 1.067μH. The nearest standard value is 1μH. The ripple, RMS and peak inductors current calculations are summarized in Equations 19, 20 and 21 respectively.

$$I_{RIPPLE} = \frac{V_{INMAX} - V_{OUT}}{L_1} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (15)$$

$$IL_{RMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} \times \left[\frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times L_1 \times f_{SW}} \right]^2} \quad (16)$$

$$IL_{PEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (17)$$

For this example, the ripple, RMS, and peak inductor current are calculated as 1.92A, 6.03A and 6.96A respectively.

Output Capacitor Design

Three primary criteria must be considered for design of the output capacitor (C_{OUT}): (1) the converter pole location, (2) the output voltage ripple, (3) the transient response to a large change in load current. The selected value must satisfy all of them. The desired transient response is usually expressed as maximum overshoot, maximum undershoot, or maximum recovery time of V_{OUT} in response to a large load step. Transient response is usually the more stringent criteria in low output voltage applications. The output capacitor must provide the increased load current or absorb the excess inductor current (when the load current steps down) until the control loop can re-adjust the current of the inductor to the new load level. Typically, it requires two or more cycles for the loop to detect the output change and respond (change the duty cycle). Another requirement may also be expressed as desired hold-up time in which the output capacitor must hold the output voltage above a certain level for a specified period if the input power is removed. It may also be expressed as the maximum output voltage drop or rise when the full load is connected or disconnected (100% load step). Equation 18 can be used to calculate the minimum output capacitance that is needed to supply energy until the control loop responds to the load change with a maximum allowed output transient of ΔV_{OUT} (overshoot or undershoot).

$$E_L = 1/2 \times L \times I^2 = 1/2 \times 1 \times 3^2 = 4.5\mu J$$

$$E_{L\_INITIAL} = 1/2 \times C_{OUT} \times V^2 = 1/2 \times C_{OUT} \times 1.2^2$$

$$E_{L\_FINAL} = 1/2 \times C_{OUT} \times (V + \Delta V_{OUT})^2$$

$$= 1/2 \times C_{OUT} \times (1.2 + 0.06)^2$$

$$E_{L\_FINAL} = E_{L\_INITIAL} + E_L \quad (18)$$

For example, if the acceptable transient to a 3A load step is 5%, by inserting ΔV_{OUT} = 0.05 × 1.2V = 0.06V and ΔI_{OUT} = 3.0A, the minimum required capacitance will be 60.98μF. Generally, the ESR of ceramic capacitors is small enough. The impact of output capacitor ESR on the transient is not taken into account in Equation 18.

APPLICATION INFORMATION (continued)

Equation 19 can be used for the output ripple criteria and finding the needed minimum output capacitance. $V_{ORIPPLE}$ is the maximum acceptable ripple. In this example, the allowed ripple is 30mV that results in minimum capacitance of 16μF.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\frac{V_{ORIPPLE}}{I_{RIPPLE}}} \quad (19)$$

where

• V_{RIPPLE} is the maximum allowable output voltage ripple.

• I_{RIPPLE} is the inductor ripple current.

Note that the impact of output capacitor ESR on the ripple is not considered in Equation 19. Use Equation 20 to calculate the maximum acceptable ESR of the output capacitor to meet the output voltage ripple requirement. In this example, the ESR must be less than 30mV/1.92A = 15.6mΩ.

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} \quad (20)$$

Higher nominal capacitance value must be chosen due to aging, temperature, and DC bias derating of the output capacitors. In this example, a 47μF/10V X5R ceramic capacitor with 3mΩ of ESR is used. The amount of ripple current that a capacitor can handle without damage or overheating is limited. The inductor ripple is bypassed through the output capacitor. Equation 21 calculates the RMS current that the output capacitor must support. In this example, it is 554.3mA.

$$I_{CORMS} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{\sqrt{12} \times V_{INMAX} \times L_1 \times f_{SW}} \quad (21)$$

Input Capacitor Design

A high-quality ceramic capacitor (X5R or X7R or better dielectric grade) must be used for input decoupling of the SGM61060. At least 4.7μF of effective capacitance (after deratings) is needed on the VIN input. The input ripple current can be calculated from Equation 22. For this example, the input ripple RMS current is 2.94A.

$$I_{CIRMS} = I_{OUT} \times \sqrt{\frac{V_{OUT} \times (V_{INMIN} - V_{OUT})}{V_{INMIN} \times V_{INMIN}}} \quad (22)$$

For this design, a ceramic capacitor with at least 10V voltage rating is required to support the maximum input voltage. So, three 47μF/10V and a 0.1μF/10V capacitors are selected for VIN to cover all DC bias, thermal and aging deratings.

The input capacitance determines the regulator input voltage ripple. This ripple can be calculated from Equation 23. In this example, the input voltage ripple is 21.3mV.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times 0.25}{C_{IN} \times f_{SW}} \quad (23)$$

Soft-Start Capacitor

The soft-start capacitor programs the ramp-up time of the output voltage during power-up. The ramp is needed in many applications due to limited voltage slew rate required by the load or limited available input current to avoid input voltage sag during startup (UVLO) or to avoid over-current protection that can occur during output capacitor charging. Soft-start will solve all these issues by limiting the output voltage slew rate.

Equation 24 can be used to calculate the soft-start capacitor for a required soft-start time (t_{SS}). In this example, the output capacitor value is 5 × 47μF and the soft-start time is not critical because it does not require too much charge for 1.2V output voltage. However, it is better to set a small arbitrary value, like C_{SS} = 10nF that results in 3.33ms startup time.

$$t_{SS}\ (ms) = \frac{C_{SS}(nF)}{3} \quad (24)$$

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor with 10V or higher voltage rating must be connected between the BOOT-SW pins. X5R or better dielectric types are recommended.

Feedback Resistors

Choosing a 20kΩ value for the upper resistor (R_7), the lower resistor (R_8) can be calculated from Equation 25. R_2 is also calculated as 20kΩ. For higher output accuracy, choose resistors with better tolerance (1% or better).

$$R_8 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_7 \quad (25)$$

APPLICATION INFORMATION (continued)

Minimum Output Voltage

There is a minimum output voltage limit for any given input voltage due to the limited minimum switching on-time of the device. Above the 0.6V minimum possible output, the lowest achievable voltage is given by Equation 26.

$$V_{OUTMIN} = t_{ONMIN} \times f_{SWMAX} (V_{INMAX} + I_{OUTMIN} (R_{DSON\_HMIN} - R_{DSON\_LMIN})) - I_{OUTMIN} (R_L + R_{DSON\_HMIN}) \quad (26)$$

where

• V_{OUTMIN} = Minimum achievable output voltage.
• t_{ONMIN} = Minimum controllable on-time (85ns MAX).
• f_{SWMAX} = Maximum f_{SW} (including tolerance).
• V_{INMAX} = Maximum input voltage.
• I_{OUTMIN} = Minimum load current.
• R_{DSON_HMIN} = Minimum high-side switch R_{DSON} (11.2mΩ to 13mΩ TYP).
• R_{DSON_LMIN} = Minimum low-side switch R_{DSON} (11.2mΩ to 13mΩ TYP).
• DCR = Inductor series resistance.
• R_L = Output Inductor series resistance.

Loop Compensation Design

Several techniques are used by engineers to compensate a DC/DC regulator. The method presented here uses simple calculations and generally results in high phase margins. For current mode control, Type 2 compensation is usually chosen. However, due to the more slope compensation, which brings some phase attenuation, Type 3 compensation is adopted.

For the SGM61060, 50kHz is selected as the crossover frequency. From the Figure 10, the gain at 50kHz is -9.816dB and the phase is -125.663 degrees. The error amplifier gain set by R_3 is required to compensate power stage for +11.35dB at f_C, and the value can be calculated from Equation 27.

$$R_3 = \frac{10^{\left(\frac{-G_{PowerStage}}{20}\right)}}{gm_{EA}} \times \sqrt{\frac{V_{OUT}}{V_{REF}}} \quad (27)$$

It can be seen from Figure 10 that DC gain is 19dB and -3dB is at 2.295kHz. C_6 sets the location of the compensation zero along with R_3. To place this zero on the converter pole, use Equation 28.

$$C_6 = \frac{1}{2\pi \times R_3 \times f_{PowerStagePole}} \quad (28)$$

C_5 and R_3 can add a high-frequency pole (not used in this design), C_5 can be calculated from Equation 29.

$$C_5 = \frac{1}{2\pi \times R_3 \times f_{Pole}} \quad (29)$$

For the feed-forward capacitor C_{14} can be calculated from Equation 30.

$$C_{14} = \frac{1}{2\pi \times R_7 \times f_C \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (30)$$

Table 2. Compensation Parameter Selection

	Calculated Value	Chosen Value
R_3	16.39kΩ	20kΩ
C_6	4.23nF	2.2nF
C_{14}	225pF	150pF

Layout Guidelines

• Layout is a critical portion of good power supply design. See Figure 10 and Figure 11 for a PCB layout example.

• The top layer contains the main power traces for VIN, VOUT, and FB. Also, on the top layer, there are connections for the remaining pins of the SGM61060 and a large top-side area filled with ground.

• The top layer ground area must be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the SGM61060 device to provide a thermal path from the exposed thermal pad land to ground.

• The GND pin must be tied directly to the power pad under the IC and the power pad.

• For operation at full rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipating area.

• There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

• Take care to minimize the loop area formed by the bypass capacitor connections, the AGND pins, and the ground connections.

• The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric.

APPLICATION INFORMATION (continued)

• Since the SW connection is the switching node, the output inductor must be placed close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.

•Try to minimize this conductor length while maintaining adequate width.

• The small signal components must be grounded to the analog ground path as shown.

• All sensitive analog traces and components such as FB, RT/CLK and COMP must be placed away from high-voltage switching nodes such as SW, BOOT and the output inductor to avoid noise coupling.

• The output voltage sense trace must be connected to the positive terminal of one output capacitor in the design with the best high frequency characteristics. The output voltage will be most tightly regulated at the voltage sense point.

• The RT/CLK pin is sensitive to noise, so the RT resistor must be placed as close as possible to the IC and routed with minimal lengths of trace.

• The additional external components can be placed approximately as shown.

• It may be possible to obtain acceptable performance with alternate PCB layouts. However, this layout has been shown to produce good results and is meant as a guideline.

• Land pattern and stencil information is provided in the datasheet addendum.

• The dimension and outline information is for the standard TQFN-3×3-16CL package.

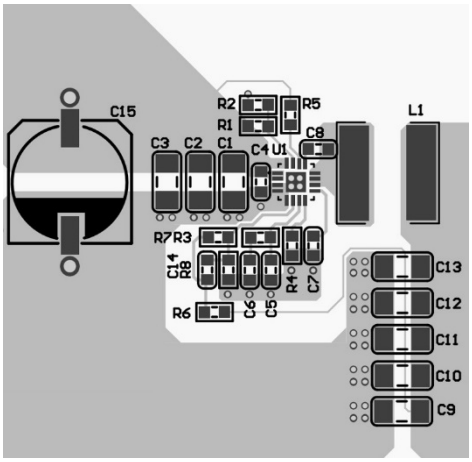


Figure 10. Top Layer

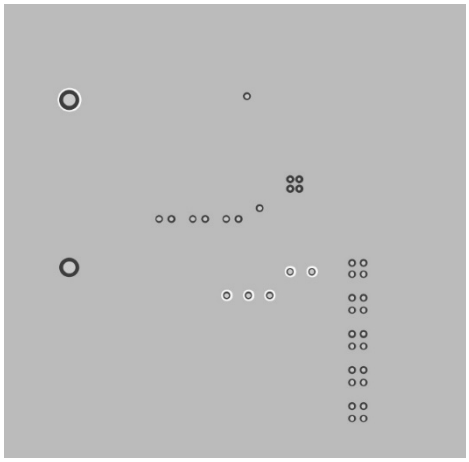


Figure 11. Bottom Layer

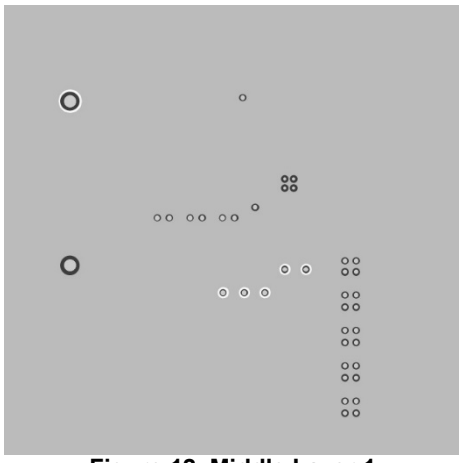


Figure 12. Middle Layer 1

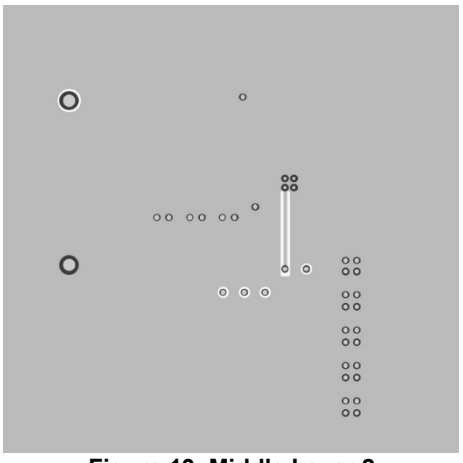


Figure 13. Middle Layer 2

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

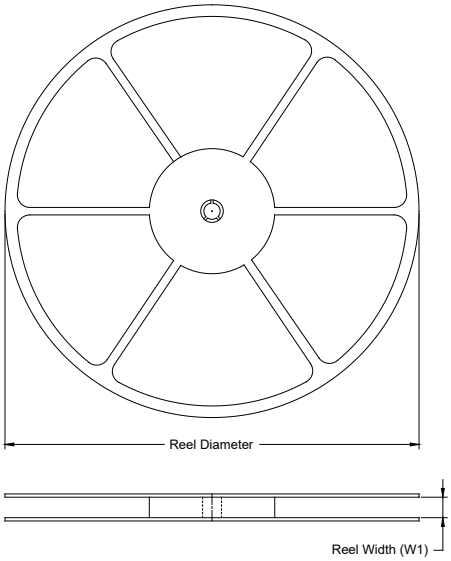
JANUARY 2024 – REV.A.1 to REV.A.2	Page
Updated load regulation, line regulation and PCB layout figures	9, 24

APRIL 2023 – REV.A to REV.A.1	Page
Updated electrical characteristics and typical performance characteristics	4, 5, 6

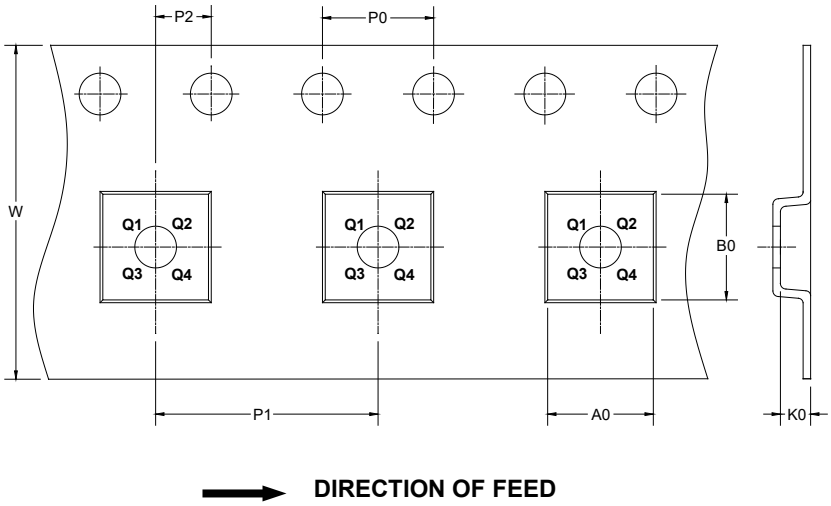
Changes from Original (APRIL 2023) to REV.A	Page
Changed from product preview to production data	All

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

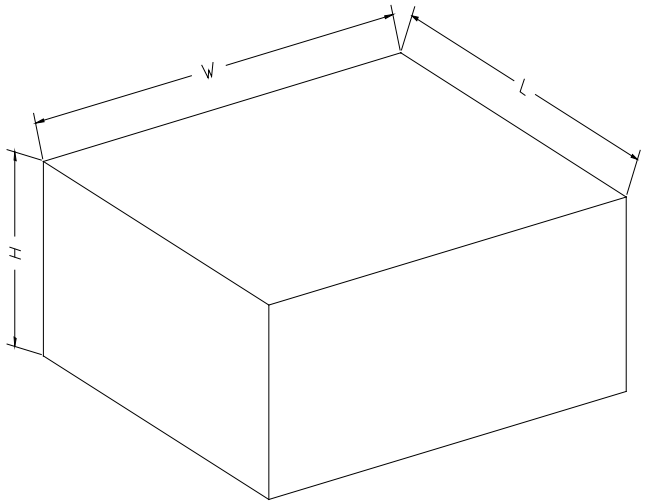
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TQFN-3×3-16EL	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002