SGM6035
2.3V to 5.5V Input, 2.6MHz, Synchronous Buck Converter

GENERAL DESCRIPTION

The SGM6035 is a synchronous Buck converter with 2.3V to 5.5V input voltage range. It operates at a 2.6MHz (TYP) fixed switching frequency, which makes the device to achieve a total solution size of 5.24mm^2. The device has an excellent load transient response even with such a low 40μA (TYP) quiescent current.

The SGM6035 has a 0.6V to 3.3V programmable output voltage and it also implements an I^{2}C to program the output voltage in 25mV steps to further enhance the device's flexibility and ease of use. With a proprietary architecture with synchronous rectification, the SGM6035 is able to achieve 97% (TYP) peak efficiency and 1300mA (TYP) output current capability.

The device implements auto PFM mode operation to maximize the efficiency at moderate and light load condition. At heavy load, the device automatically switches to fixed-frequency control with 2.6MHz (TYP) switching frequency. When the device is powered off, the supply current will decrease below 0.2μA, which reduces the power consumption.

The SGM6035 is available in a Green WLCSP-0.89×1.23-6B package.

FEATURES

- **2.3V to 5.5V Input Voltage Range**
- **40μA (TYP) Quiescent Current**
- **2.6MHz (TYP) Fixed Switching Frequency**
- **1300mA (MAX) Output Current Capability**
- **0.6V to 3.3V Programmable Output Voltage (25mV Steps) via I^{2}C Functionality**
- **455mA to 2045mA Programmable Current Limit (106mA Steps) via I^{2}C Functionality**
- **Excellent Load Transient Response**
- **Internal Soft-Start Function to Avoid Brown-out Scenarios**
- **5.24mm^2 Total Solution Size**
- **Over-Current Protection (OCP)**
- **Under-Voltage Lockout (UVLO) Protection**
- **Overload Protection**
- **Thermal Shutdown Protection**
- **Available in a Green WLCSP-0.89×1.23-6B Package**

APPLICATIONS

Smart Phones and Watches
Health Monitoring Devices
Wearable Devices
Energy Harvesting and Sensor Drive
Utility and Safety Modules
RF Modules

TYPICAL APPLICATION

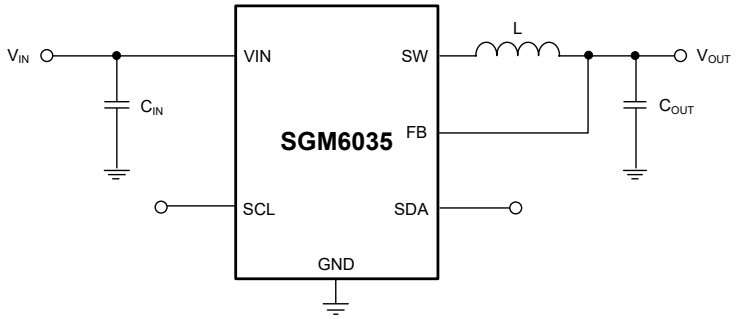


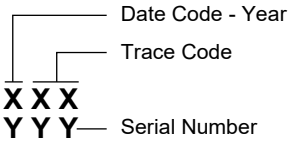
Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM6035	WLCSP-0.89×1.23-6B	-40℃ to +85℃	SGM6035YG/TR	XXX 0OA	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXX = Date Code and Trace Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN Voltage ..... -0.3V to 6.0V
SW Voltage ..... -0.3V to V_{IN} + 0.3V
CTRL Voltages
SDA ..... -0.3V to V_{IN} + 0.3V (1)
SCL, FB ..... -0.3V to V_{IN} + 0.3V (1)
Package Thermal Resistance
WLCSP-0.89×1.23-6B, θ_{JA} ..... 196.1℃/W
WLCSP-0.89×1.23-6B, θ_{JB} ..... 64.0℃/W
WLCSP-0.89×1.23-6B, θ_{JC} ..... 56.5℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (2) (3)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. Lesser of 6V or V_{IN} + 0.3V.

2. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

3. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

RECOMMENDED OPERATING CONDITIONS

Input Supply Voltage Range, V_{IN} ..... 2.3V to 5.5V
Output Current Range, I_{OUT} ..... 1300mA (TYP)
Input Capacitor, C_{IN} ..... 4.7μF (TYP)
Output Capacitor, C_{OUT} ..... 10μF (TYP)
Inductor, L ..... 0.47μH (TYP)
Operating Ambient Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

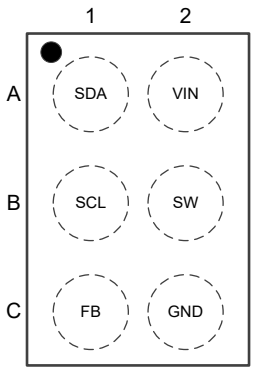
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-0.89×1.23-6B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	SDA	I	I^2C Bus Data Signal. Do not leave it floating.
A2	VIN	P	Power Supply Input. Connect a ceramic capacitor (C_{IN}) close to this pin and GND.
B1	SCL	I	I^2C Bus Clock Signal. Do not leave it floating.
B2	SW	O	Switching Node Pin.
C1	FB	O	Feedback Pin.
C2	GND	G	Ground Pin. Power and device ground. All signals refer to this pin.

NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +85℃, V_{IN} = 3.8V, all typical values are measured at T_J = +25℃, V_{IN} = 3.8V and V_{OUT} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PFM Quiescent Current	I_{Q_PFM}	ENABLE bit = 1, PFM mode, no load, non-switching		40	85	μA
Shutdown Supply Current	I_{SD}	ENABLE bit = 0, no load		0.2	1	μA
Under-Voltage Lockout Threshold	V_{UVLO_R}	V_{IN} rising	2.05	2.15	2.25	V
	V_{UVLO_F}	V_{IN} falling	1.94	2.04	2.15	
UVLO Hysteresis	V_{UVLO_HYS}			110		mV
Switching Frequency	f_{SW}	PWM, no load	2.20	2.60	3.00	MHz
Output Voltage Accuracy	V_{OUT_ACC}	V_{OUT} = 0.6V to 2.6V, I_{OUT} = 0A	-40		40	mV
		V_{OUT} = 2.625V to 3.3V, I_{OUT} = 0A	-1.5		1.5	%
Peak Inductor Current Limit Accuracy	I_{LIM_ACC}	Programmed to 1833mA current limit setting	1460	1833	2215	mA
Programmable Peak Inductor Current Limit Range	I_{LIM_PRG}		455		2045	mA
Negative Current Limit	I_{LIM_NEG}			-950		mA
PMOS Resistance	R_{DSON}	V_{IN} = V_{GS} = 3.8V		115	160	mΩ
NMOS Resistance	R_{DSON}	V_{IN} = V_{GS} = 3.8V		45	80	mΩ
Thermal Shutdown	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{SD_HYS}			15		℃

SYSTEM CHARACTERISTICS

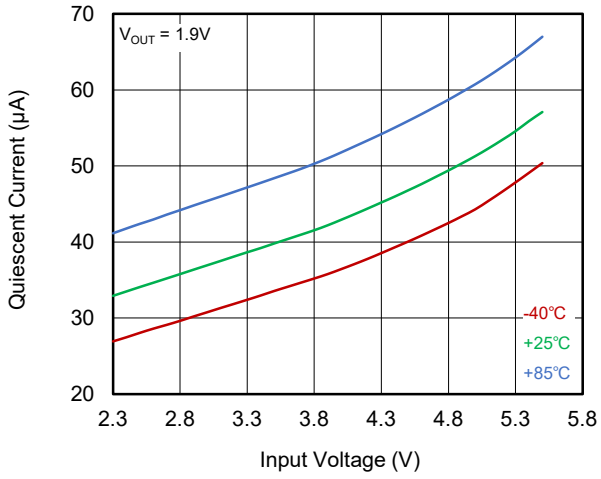
(T_J = −40℃ to +85℃, V_{IN} = 2.3V to 5.5V and V_{OUT} = 3.3V, all typical values are measured at T_J = +25℃, V_{IN} = 3.6V and V_{OUT} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Efficiency	Eff	I_{OUT} = 1mA		85		%
		I_{OUT} = 100mA		94		
		I_{OUT} = 300mA		97		
		I_{OUT} = 500mA		96		
		I_{OUT} = 700mA		96		
I_{OUT} MAX	I_{OUT}			1300		mA
Load Regulation	$LOAD_{REG}$	0mA < I_{OUT} < 1200mA, V_{IN} = 3.8V		11		mV/A
Line Regulation	$LINE_{REG}$	3.8V < V_{IN} < 4.35V, I_{OUT} = 300mA, PWM Mode		0.68		mV/V
Load Transient	V_{TRRP}	I_{OUT} = 10mA - 150mA, T_R = T_F = 1μs, Auto Mode, V_{IN} = 3.8V		±44		mV
		I_{OUT} = 100mA - 1200mA, T_R = T_F = 5μs, Auto Mode, V_{IN} = 3.8V		±100		
Ripple Voltage	V_{OUT_RIPPLE}	I_{OUT} = 40mA, PFM Mode		22		mV
		I_{OUT} = 200mA, PWM Mode		25.2		

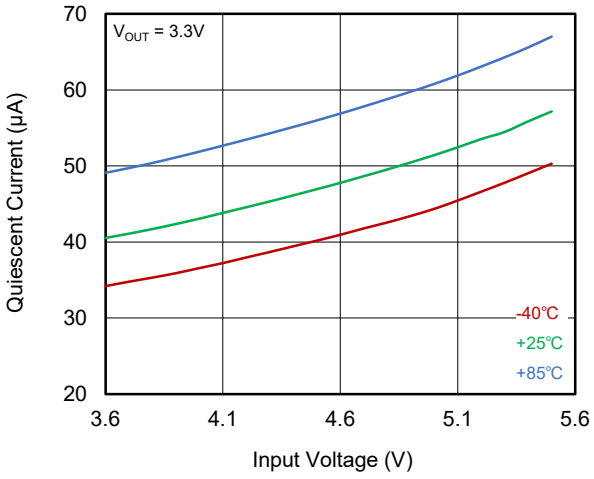
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{IN} = 3.8V, V_{OUT} = 3.3V, unless otherwise noted.

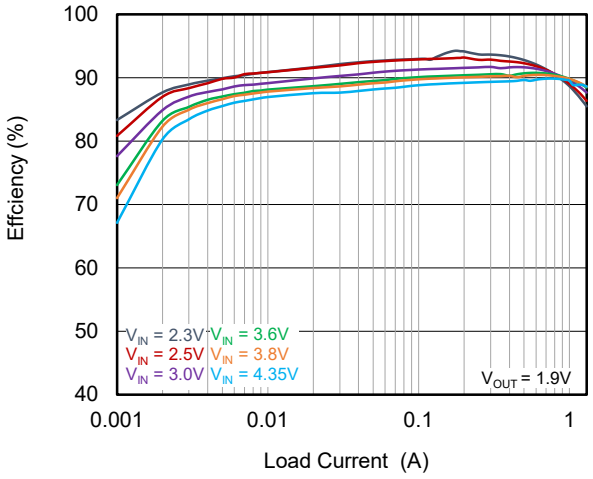
Quiescent Current vs. Input Voltage



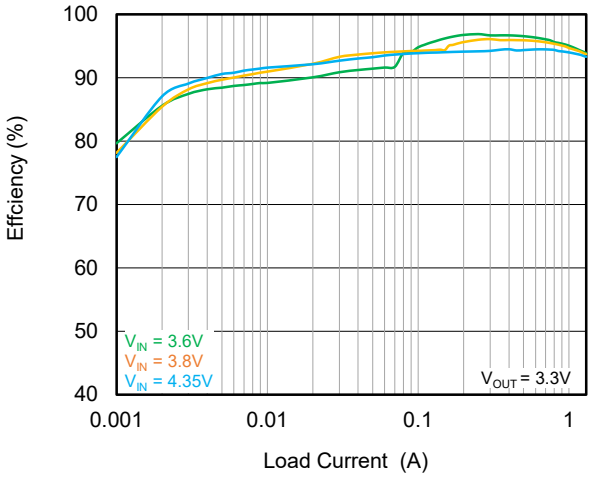
Quiescent Current vs. Input Voltage



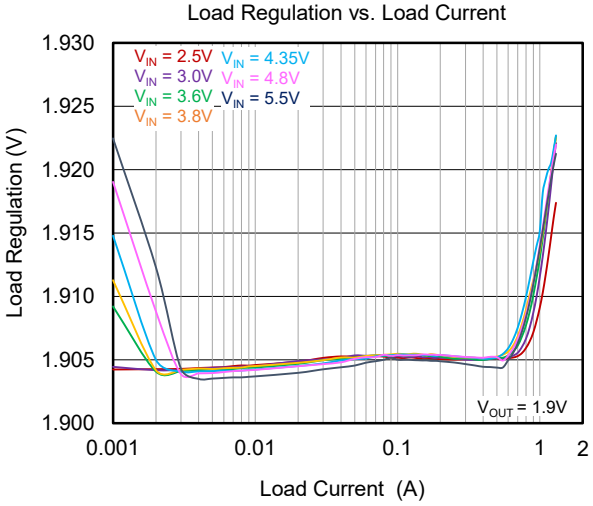
Efficiency vs. Load Current



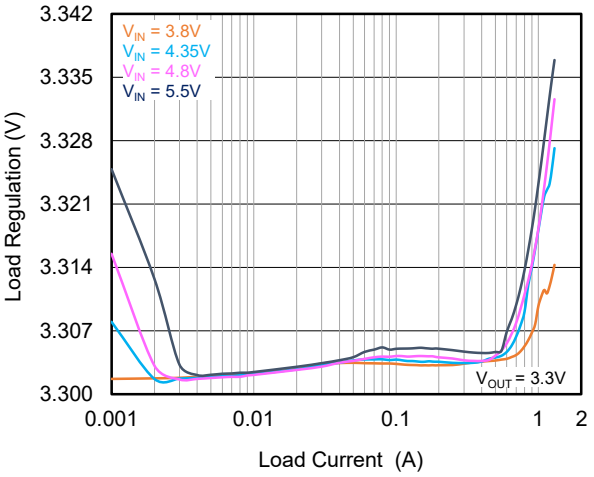
Efficiency vs. Load Current



Load Regulation vs. Load Current



Load Regulation vs. Load Current



FUNCTIONAL BLOCK DIAGRAM

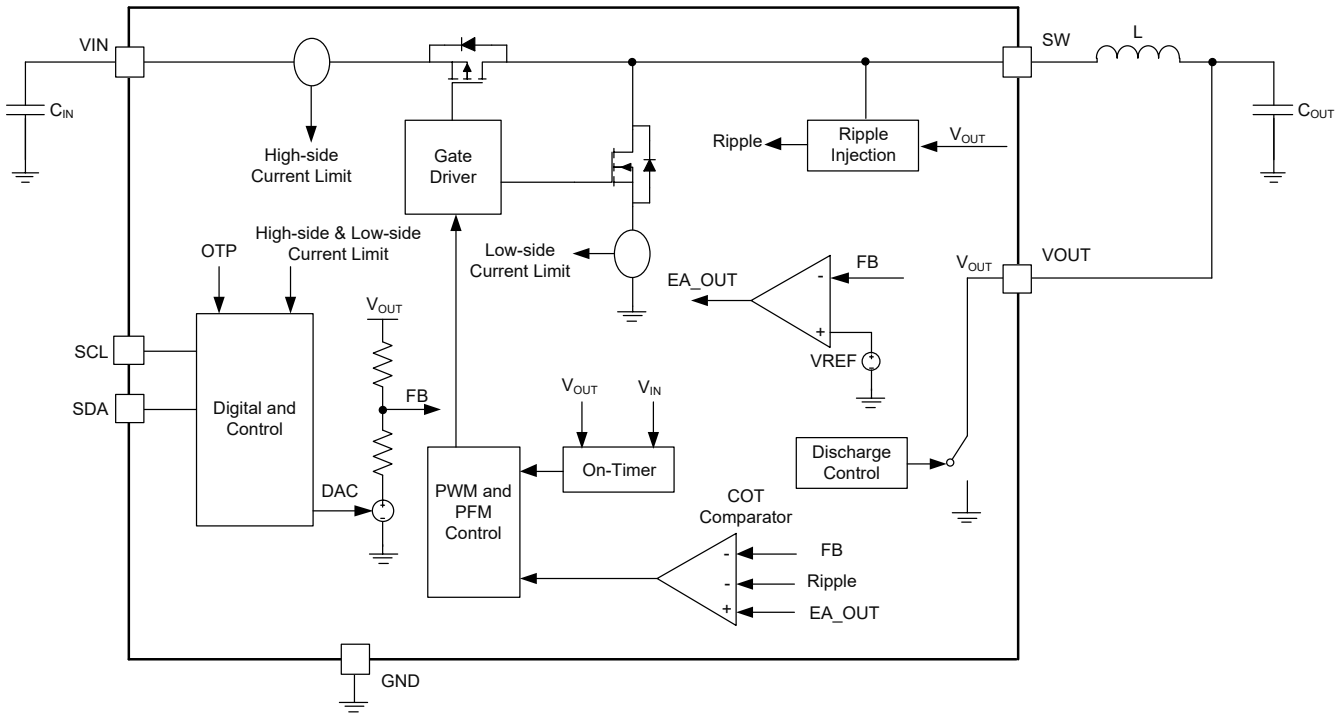


Figure 2. Block Diagram

DETAILED DESCRIPTION

Overview

SGM6035 is a 2.6MHz synchronous Buck converter with an operating voltage range of 2.3V to 5.5V. The synchronous rectification architecture enables the device to provide a peak efficiency of up to 97%. The device provides a fixed switching frequency of 2.6MHz, so only 0.47μH output inductance and 10μF output capacitance are recommended to achieve the normal operation of the device.

The SGM6035 is capable of delivering up to 1300mA continuous output current and supports the output voltage range from 0.6V to 3.3V by stepping in 25mV via I^2C.

Modes of Operations

PFM Mode

When the load current is below 150mA (TYP) in auto mode, the converter enters PFM mode to ensure lower switching frequency and higher efficiency under light load.

PWM Mode

The device can operate in PWM mode to achieve a fixed switching frequency of 2.6MHz and supports the use of small external components. The SGM6035 can enter forced PWM mode by inserting 1 into the register bit via I^2C

Protection Features

Start-up Description

When the input voltage is fully established, the ENABLE bit is set to 1 via I^2C, and the SGM6035 adjusts the output voltage to start through the internal soft-start circuit. If the output voltage is less than 200mV during start-up, the current limit will be reduced by 50%. If the output voltage is able to rise above 200mV, the current limit will be released to 100% to ramp the output voltage towards the programmed value.

If the output voltage does not reach 95% of the target value within 12ms, a start-up fault is declared and the device attempts to restart after 33ms.

For start-up into short-circuit case or output short case, the current limit will be clamped at 50% of the programmed threshold.

Programmable Output Voltage

The SGM6035 output voltage of ranges from 0.6V to 3.3V, and the voltage can be adjusted by I^2C with a step of 25mV. The conversion process of the output voltage from low to high voltage, the internal reference voltage of the SGM6035 is converted in a single step and the load current and output capacitance determine the rise time.

VOUT Fault

When the output start time exceeds 12ms and the output voltage does not reach 95% of the set value, the device will declare a VOUT fault. In the fault state, the SGM6035 will restart every 33ms. Once the output voltage is established normally, the VOUT fault will be cleared.

Under-Voltage Lockout (UVLO)

The SGM6035 offers input under-voltage lockout to prevent false triggering with unstable input source. The device's UVLO rising voltage is 2.15V (TYP) and falling threshold is 2.04V (TYP), the device stops operation as soon as the input voltage drops below the falling threshold.

Over-Current Protection (OCP)

The device implements over-current protection when the inductor current exceeds the set peak current to prevent excessive currents from passing through the input. In the event of heavy load or output short-circuit, the peak inductor current exceeding the set value, the device turns off the high-side power MOSFETs immediately to prevent damage to the device. The peak current limit ranges from 455mA to 2045mA with a step of 106mA, which can be programmed via I^2C.

DETAILED DESCRIPTION (continued)

Negative Current Limit

In PWM mode, when the output voltage is higher than the set target voltage, the current flowing through the inductor will be negative. In order to prevent large negative currents from damaging the device, when the negative current exceeds -950mA, the SGM6035 will directly turn off the power MOSFETs and enter tri-state until the input or output voltage is restored, and the device resumes switching.

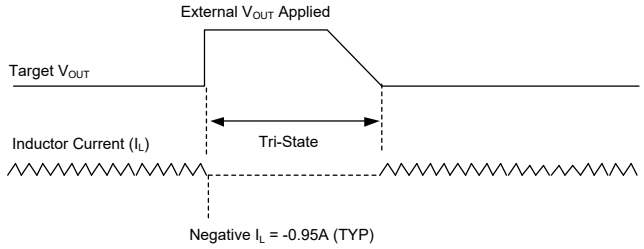


Figure 3. Negative Current Limit

The SGM6035 has an internal zero crossing detection (ZCD) in PFM mode, when the load is light or the output voltage is higher than the set value, the ZCD detects a negative current and immediately turns off the low-side FET to prevent any negative current from flowing through the inductor.

It should be noted that once the output voltage is higher than the input voltage, the current will flow through the body diode of the high-side FET.

Thermal Shutdown Protection (TSP)

The SGM6035 implements the thermal shutdown function to prevent device from overheating damage. When the junction temperature of the device rises and exceeds +150 ℃ , the device enters the thermal shutdown and stops switching. The device has a 15℃ thermal shutdown hysteresis to allow internal soft-start for automatic restart.

Shutdown

To disable the SGM6035, the ENABLE bit must be configured to code 0. When part is disabled, output voltage will tri-state and discharge via load or pull-down resistor.

Active Pull-Down

The device implements I^2C programmable output voltage discharge function. The SGM6035 can set the active pull-down function through the PULLDOWN register (**REG0x06**), and the device provides four options based on the PULL_DOWN_SEL configuration: OPEN, 50Ω, 100Ω and 200Ω.

DETAILED DESCRIPTION (continued)

I²C

I²C Serial Interface and Data Communication

Standard I²C interface is used to program SGM6035 parameters and get status reports. I²C is the well-known 2-wire serial communication interface that can connect one (or more) master device(s) to some slave devices for two-way communication. The bus lines are named serial data (SDA) and serial clock (SCL). The device that initiates a data transfer is a master. A master generates the SCL signal. Slave devices have unique addresses to identify. A master is typically a micro controller or a digital signal processor.

The SGM6035 operates as a slave device that address is 0x52. It has eight 8-bit registers, numbered from REG0x00 to REG0x07.

The interface of SGM6035 supports four communication modes defined in the I²C specification: standard mode (100kbps), fast mode (400kbps), fast mode plus mode (1Mbps) and high-speed mode (3.4Mbps). The data transfer protocols for the standard, fast and fast plus modes are the same, while the protocol for high-speed is different.

I²C Data Communication for Standard, Fast and Fast Plus Modes

START and STOP Conditions

A transaction is started by taking control of the bus by master if the bus is free. The START condition is defined when SCL is high and a high to low transition on the SDA is generated by master. Similarly, a STOP is defined when SCL is high and SDA goes from low to high. START and STOP are always generated by a master. After a START and before a STOP, the bus is considered busy.

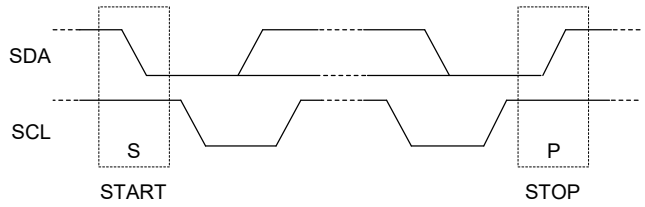


Figure 4. I²C Bus in START and STOP Conditions

Data Bit Transmission and Validity

The data bit (high or low) must remain stable during clock high period. The state of SDA can only change when SCL is low. For each data bit transmission, one clock pulse is generated by master. Bit transfer in I²C is shown in Figure 5.

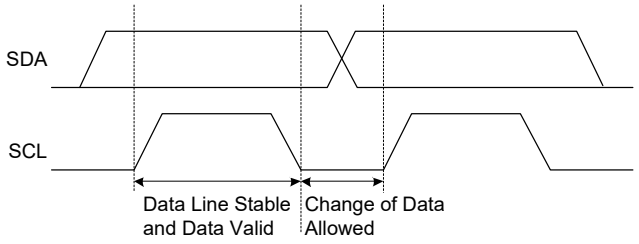


Figure 5. I²C Bus Bit Transfer

Byte Format

Data is transmitted in 8-bit packets (one byte at a time). The number of bytes in one transaction is not limited. In each packet, the 8 bits are sent successively with the Most Significant Bit (MSB) first. An acknowledge (or not-acknowledge) bit must come after the 8 data bits. This bit informs the transmitter whether the receiver is ready to proceed for the next byte or not. If the slave is busy and cannot transfer another byte of data, it can hold the SCL line low and keep the master in a wait state (called clock stretching). When the slave is ready for another byte of data, it releases the clock line and data transfer can continue with clocks generated by master. Figure 6 shows the byte transfer process with I²C interface.

DETAILED DESCRIPTION (continued)

Acknowledge (ACK) and Not Acknowledge (NCK)

After transmission of each byte by transmitter, an acknowledge bit is replied by the receiver as the ninth bit. With the acknowledge bit, the receiver informs the transmitter that the byte is received, and another byte is expected or can be sent (ACK) or it is not expected (NCK = not ACK). Clock (SCL) is always generated by master, including the acknowledge clock pulse, no matter who is acting as transmitter or receiver. SDA line is released for receiver control during the acknowledge clock pulse. And the receiver can pull the SDA line low as ACK (reply a 0 bit) or let it be high as NCK during the SCL high pulse. After that, the master can either apply a STOP (P) condition to end the transaction or send a new START (S) condition to start a new transfer (called repeated start). For example, when master wants to read a register in slave, one start is needed to send the slave address and register address, and then, without a STOP condition, another start is sent by master to initiate the receiving transaction from slave. Master then sends the STOP condition and releases the bus.

Data Direction Bit and Addressing Slaves

The first byte sent by master after the START is always the target slave address (7 bits) and an eighth data-direction bit (R/$\overline{W}$). R/$\overline{W}$ bit is 0 for a WRITE transaction and 1 for READ (when master is asking for data). Data direction is the same for all next bytes of the transaction. To reverse it, a new START or repeated START condition must be sent by master (STOP will end the transaction). Usually the second byte is a WRITE sending the register address that is supposed to be accessed in the next byte(s). The data transfer transaction is shown in Figure 7.

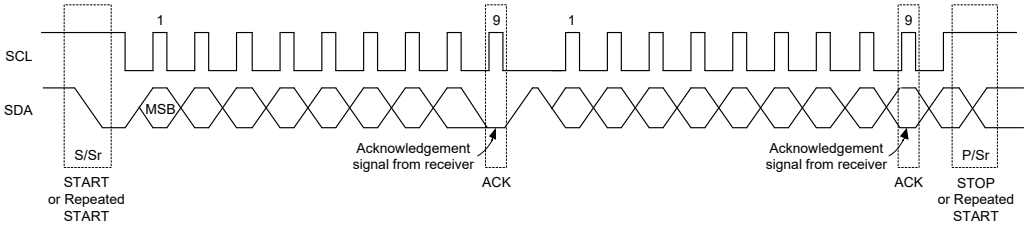


Figure 6. Byte Transfer Process

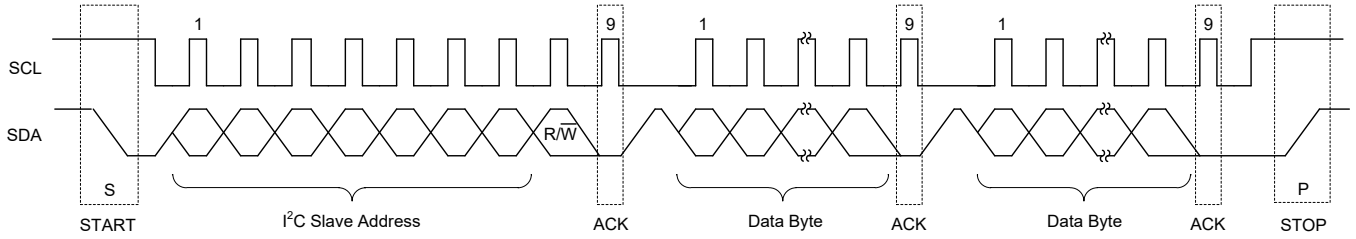


Figure 7. Data Transfer Transaction in Standard, Fast and Fast Plus Modes

DETAILED DESCRIPTION (continued)

WRITE: If the master wants to write in the register, the third byte can be written directly as shown in Figure 8 for a single write data transfer. After receiving the ACK, master may issue a STOP condition to end the transaction or send the next register data, which will be written to the next address in a slave as multi-write. A STOP is needed after sending the last data.

READ: If the master wants to read a single register (Figure 9), it sends a new START condition along with device address with R/$\overline{W}$ bit = 1. After ACK is received, master reads the SDA line to receive the content of the register. Master replies with NCK to inform slave that no more data is needed (single read) or it can send an ACK to request for sending the next register content (multi-read). This can continue until an NCK is sent by master. A STOP must be sent by master in any case to end the transaction.

High-Speed (HS) Mode

The protocol for High-Speed Mode is different from Standard, Fast and Fast Plus Modes. The High-Speed Mode is entered after the master sends the HS master code 00001XXX after a start condition. The HS master code is sent at Standard, Fast or Fast Plus mode with rate less than 1Mbps. The slave device is not allowed to acknowledge the HS master code, while they need to recognize and shift the interface to HS Mode. Then, the master sends a repeated start condition. After that, the transaction in HS Mode begins where the protocol is the same as Standard, Fast and Fast Plus Mode except that the transmission rate is increased to 3.4 Mbps. The master sends a stop condition to stop the HS Mode. Instead, repeated start condition is necessary to maintain transmission in HS Mode.

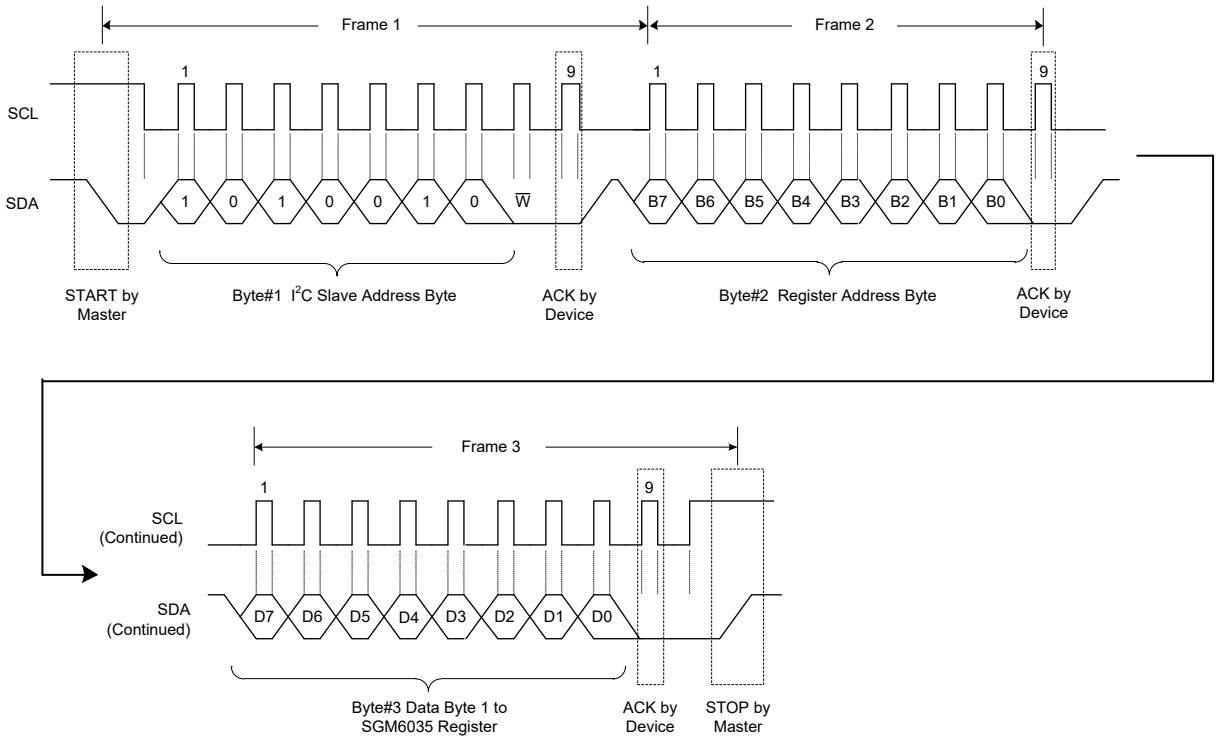


Figure 8. A Single Write Transaction in Standard, Fast and Fast Plus Modes

DETAILED DESCRIPTION (continued)

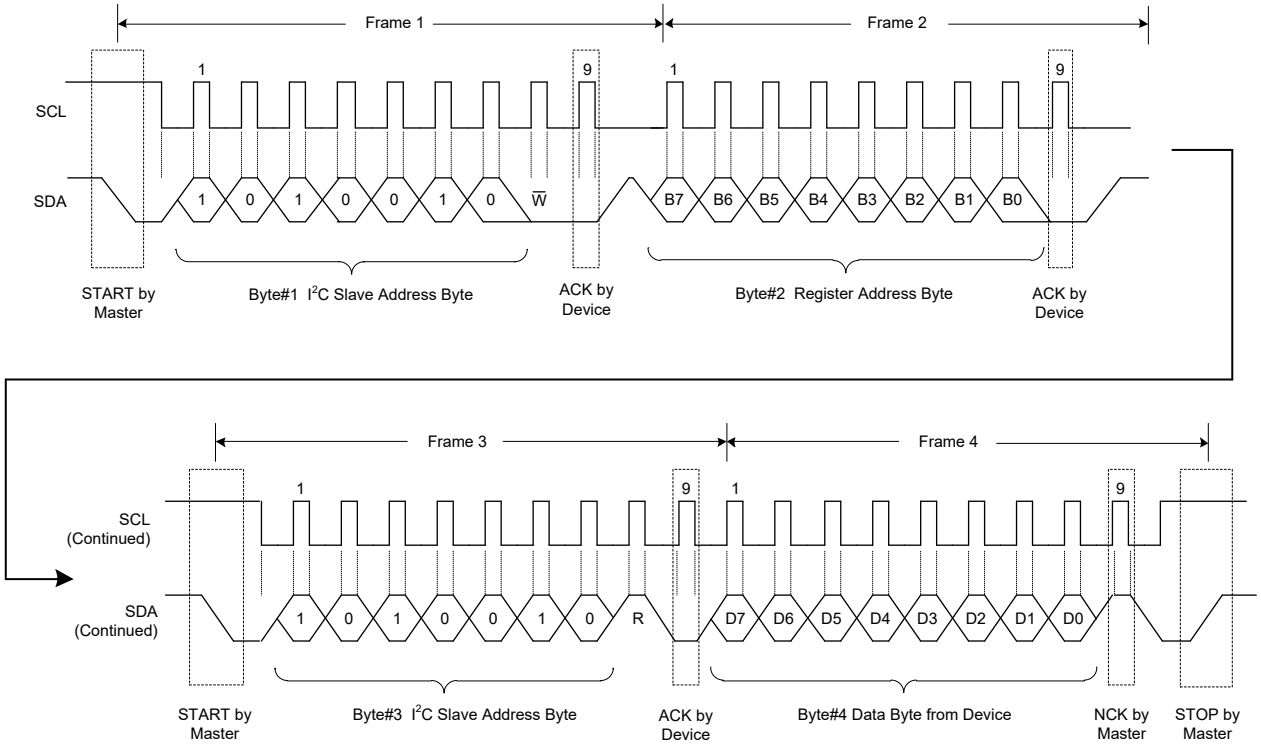


Figure 9. A Single Read Transaction in Standard, Fast and Fast Plus Modes

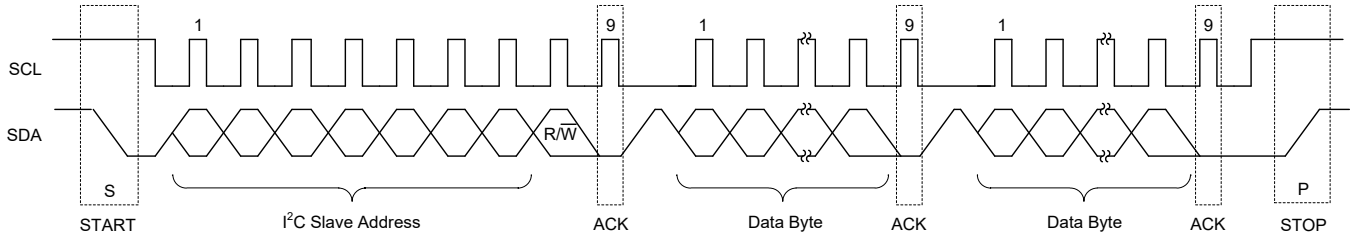


Figure 10. Data Transfer Transaction in High-Speed Mode

REGISTER MAPS

All registers are 8-bit and individual bits are named from D[0] (LSB) to D[7] (MSB).

I²C Slave Address of SGM6035: 0xXX (1010010 + R/W)

ADDRESS	REGISTER NAME	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
0x00	Product ID_REV	PRODUCT_ID[7:4]				SILICON_REV[3:0]			
0x01	Fault Flag Status	Reserved		POR	UVLO_FAULT	TSD_FAULT	CURRENT_LIM_FAULT	START-UP_TIMEOUT_FAULT	VOUT_SHORT_FAULT
0x02	Fault Live Status	Reserved			UVLO	TSD	CURRENT_LIM	START-UP_TIME	VOUT_SHORT
0x03	MODE	Reserved						ENABLE	FORCED_PWM
0x04	VSEL	Reserved	BUCK_VOUT[6:0]						
0x05	Current Limit	Reserved				ILIM[3:0]			
0x06	Pull-down	Reserved					PULL_DOWN	PULL_DOWN_SEL[1:0]	
0x07	Reset	SOFT_RESET[7:0]							

Bit Types:

R: Read only

R/W: Read/Write

R/C: Read clears the bit.

REGISTER MAPS (continued)

REG0x00: Product ID Register [Reset = 0x10]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	PRODUCT_ID	0001	R	Capture product configuration to allow customers to identify a device (if they have access to I^2C) and allow read−back of desired configuration in the event of a customer return 0000 = None 0001 = SGM6035 (default) 0010 = Reserved 0011 = Reserved 0100 = Reserved 0101 = Reserved 0110 = Reserved 0111 = Reserved 1000 = Reserved 1001 = Reserved 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
D[3:0]	SILICON_REV	0000	R	To allow identification of silicon revision through ATE test. Customer visible when there is I^2C bus that the customer has access to. 000 = Initial Silicon 001 = Increment register with each iteration 010 011 100 101 110 111

REG0x01: Fault Flag Status Register [Reset = 0x20]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	Reserved	00	R/C	Reserved
D[5]	POR	1	R/C	Indicate a POR fault. The indication is latched until it is cleared after being read. 0 = Default 1 = POR fault (default)
D[4]	UVLO_FAULT	0	R/C	Indicate an UVLO fault. The indication is latched until it is cleared after being read. 0 = No UVLO fault (default) 1 = UVLO fault
D[3]	TSD_FAULT	0	R/C	Indicate a thermal shutdown fault. The indication is latched until it is cleared after being read. 0 = No TSD fault (default) 1 = TSD fault
D[2]	CURRENT_LIM_FAULT	0	R/C	Indicate a current limiting fault. The indication is latched until it is cleared after being read. 0 = No current limit fault (default) 1 = Current limit fault
D[1]	START-UP_TIMEOUT_FAULT	0	R/C	Indicate a startup timeout fault. The indication is latched until it is cleared after being read. 0 = No start-up timeout fault (default) 1 = Start-up timeout fault
D[0]	VOUT_SHORT_FAULT	0	R/C	Indicate output short-circuit fault. The indication is latched until it is cleared after being read. 0 = No V_{OUT} short fault (default) 1 = V_{OUT} short fault

REGISTER MAPS (continued)

REG0x02: Fault Live Status Register [Reset = 0x18]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	Reserved	000		Reserved
D[4]	UVLO	1	R	Indicate an under-voltage lockout fault 0 = No UVLO fault 1 = UVLO fault(default)
D[3]	TSD	1	R	Indicate an over-temperature fault. 0 = No TSD fault 1 = TSD fault(default)
D[2]	CURRENT_LIM	0	R	Indicate a current limiting fault. 0 = No current limit fault(default) 1 = Current limit fault
D[1]	START-UP_TIME	0	R	Indicate a start-up timeout fault. 0 = No start-up timeout fault(default) 1 = Start-up timeout fault
D[0]	VOUT_SHORT	0	R	Indicate output short-circuit fault. 0 = No V_{OUT} short fault(default) 1 = V_{OUT} short fault

REG0x03: MODE Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:2]	Reserved	00000		Reserved
D[1]	ENABLE	0	R/W	Software Enable Device. 0 = Regulation Disabled(default) 1 = Regulation Enabled
D[0]	FORCED_PWM	0	R/W	Enable PWM Mode. 0 = Auto (PFM/PWM depending on load current) (default) 1 = PWM

REG0x04: VSEL Register [Reset = 0x7B]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7]	Reserved	0		Reserved
D[6:0]	BUCK_VOUT	111 1011	R/W	Set Buck converter target output voltage. 00 = Reserved …. = …. 0E = Reserved 0F = 600mV 10 = 625mV …. = …. 44 = 1.925V …. = …. 7A = 3.275V 7B = 3.300V 7C = Reserved …. = …. 7F = Reserved

REG0x05: ILIMIT Register [Reset = 0x0F]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	Reserved	0000		Reserved
D[3:0]	ILIM	1111	R/W	Set the current limiting value. The range is from 455mA to 2045mA in 106mA steps. 0000 = 455mA (open loop) 0010 = 667mA (open loop) 0011 = 773mA (open loop) 0100 = 879mA (open loop) 1000 = 1303mA (open loop) 1111 = 2045mA (open loop) (default)

REGISTER MAPS (continued)

REG0x06: PULLDOWN Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:3]	Reserved	00000		Reserved
D[2]	PULL_DOWN	0	R/W	Enable the internal pull-down resistor. 0 = Pull-down not used (Off) (default) 1 = Pull-down active during transition
D[1:0]	PULL_DOWN_SEL	00	R/W	Enable the value of the pull-down resistor. 00 = Open (default) 01 = 200Ω 10 = 100Ω 11 = 50Ω

REG0x07: RESET Register [Reset = 0x00]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:0]	SOFT_RESET	0000 0000	W	When 0x60h is written, the software reset register restores all I^2C settings to POR defaults.

APPLICATION INFORMATION

Typical Application

Figure 11 below shows a typical schematic.

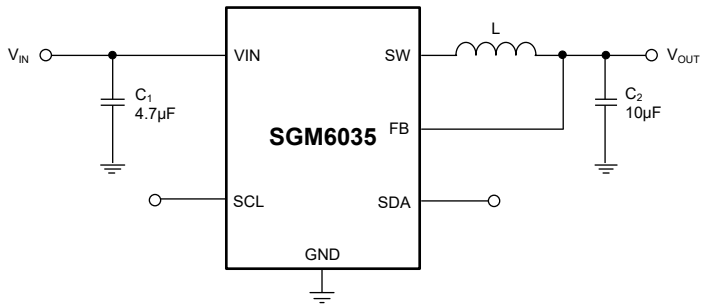


Figure 11. Typical Application Circuit

Inductor Selection

The inductance of the output filter (L) determines the peak-to-peak ripple current and indirectly affects the converter efficiency and output voltage ripple. It also determines the current at which the PWM to PFM transition occurs (CCM to DCM). The ripple current (ΔI_L) can be estimated from Equation 1. It shows that ΔI_L decreases with larger inductance values and increases at higher voltage levels (V_{IN} or V_{OUT}).

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (1)$$

In steady state, the maximum inductor current can be calculated from Equation 2.

$$I_{L\_MAX} = I_{OUT\_MAX} + \frac{\Delta I_L}{2} \quad (2)$$

Where, f_{SW} is switching frequency, L is inductance value, ΔI_L is the inductor peak-to-peak ripple current and I_{L_MAX} is the peak inductor current. The maximum current should never reach the inductor saturation level. This situation can happen after a large load step. A common conservative option is to choose an inductor with a saturation current equal to or higher than the high-side switch current limit.

Input Capacitor

A low ESR ceramic capacitor must be connected close to the VIN and GND pins to provide the pulsating input current of the converter and minimize switching noise and ringing. A 4.7μF ceramic capacitor is satisfactory for most applications, however, if a high impedance source such as a coin cell-battery is used, larger input capacitance (C_1 ≥ 10μF) is preferred to prevent voltage drops during start-up or load steps. There is no high limit for the input capacitance, however, note that the higher leakage current of a large input capacitor will increase the total quiescent current of the power supply.

Output Capacitor

The architecture of SGM6035 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR) to achieve low output voltage ripple. X5R or X7R dielectrics are recommended. For SGM6035, one 10μF X5R, 6.3V ceramic capacitor is recommended.

Layout Guidelines

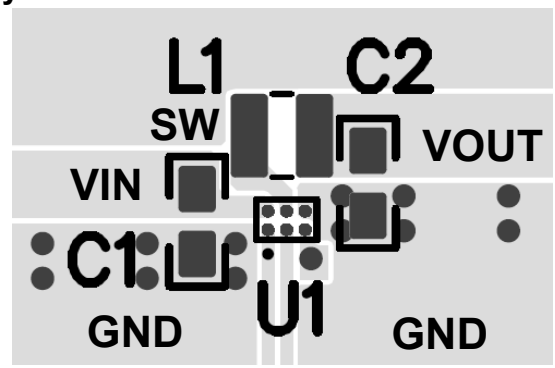


Figure 12. PCB Layout Example

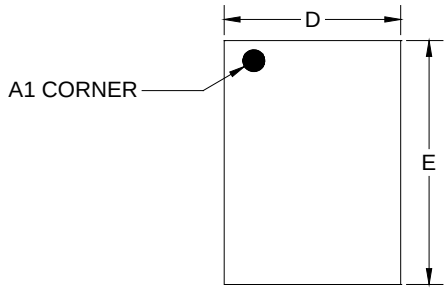
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

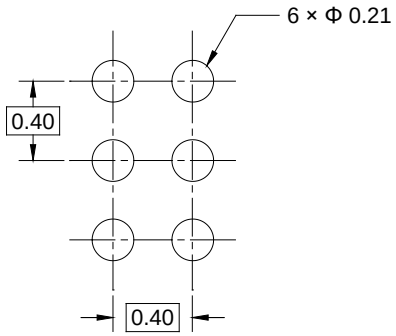
Changes from Original (DECEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

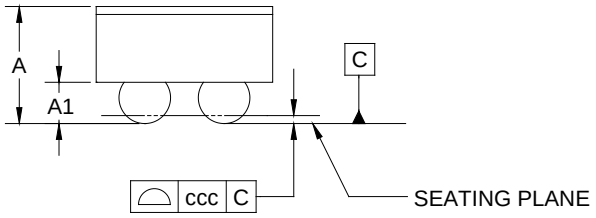
WLCSP-0.89×1.23-6B



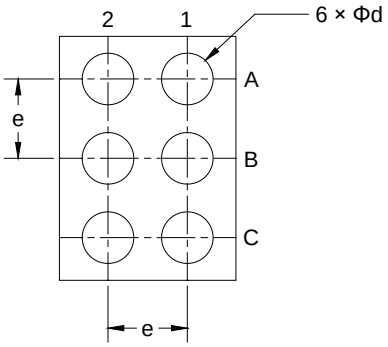
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



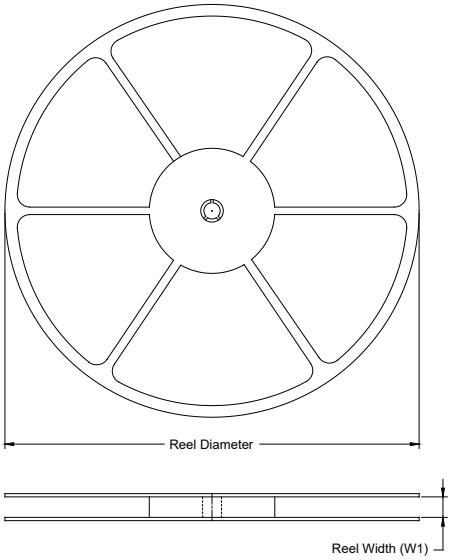
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.625
A1	0.188	-	0.228
D	0.860	-	0.920
E	1.200	-	1.260
d	0.230	-	0.290
e	0.400 BSC		
ccc	0.050		

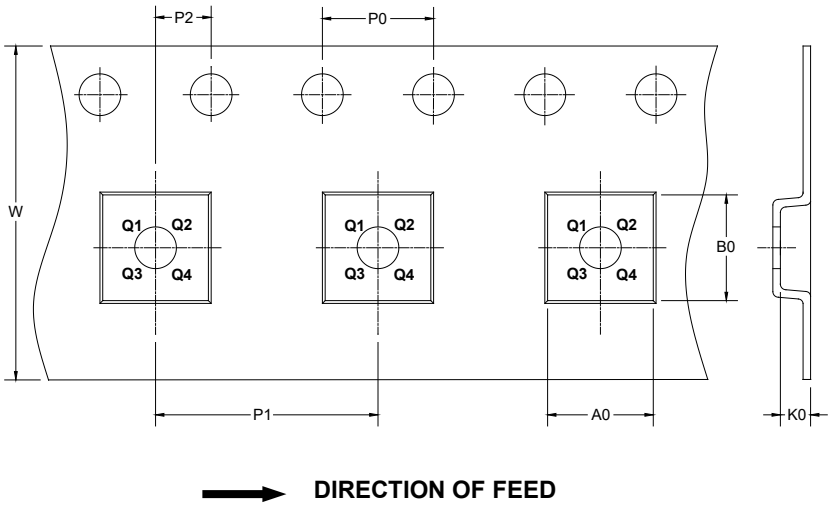
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



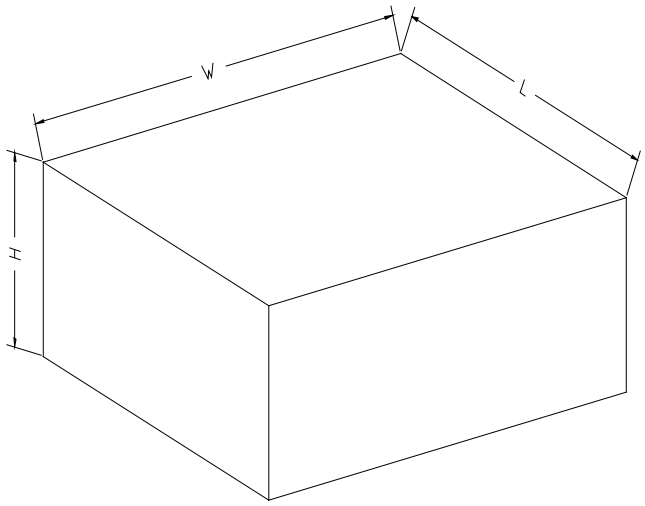
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-0.89×1.23-6B	7"	9.5	1.00	1.34	0.78	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002