SGM58201
4-Channel, 2kSPS, Low-Power, 24-Bit ADC with Integrated PGA and Reference

GENERAL DESCRIPTION

The SGM58201 is a precise 24-bit analog-to-digital converter (ADC) designed to minimize system costs and component count in applications involving the measurement of small sensor signals. It features four single-ended inputs or two differential inputs through a versatile input multiplexer (MUX), a low-noise programmable gain amplifier (PGA), two programmable excitation current sources, a voltage reference, an oscillator, a low-side switch, and a detailed temperature sensor.

The SGM58201 is capable of achieving conversions at data rates up to 2000 samples per second (SPS) with single-cycle settling. The device's digital filter operates at 20SPS, effectively rejecting 50Hz and 60Hz frequencies in noisy industrial environments. The internal PGA provides amplification levels up to 128V/V, making the SGM58201 suitable for measuring delicate sensor signals such as resistance temperature detectors (RTDs), thermocouples, thermistors, and resistive bridge sensors. The SGM58201 supports the measurement of pseudo-differential or fully-differential signals when the PGA is used. Alternatively, it can be configured to bypass the internal PGA while still offering high input impedance and amplification levels up to 4V/V, facilitating single-ended measurements.

In duty-cycle mode with the PGA deactivated, the power consumption drops to a minimal 175μA.

The SGM58201 is available in Green TSSOP-16 and TQFN-3.5×3.5-16L packages, and it is suitable for an extended temperature range from -40℃ to +125℃.

FEATURES

- **Wide Supply Voltage Range: 2.3V to 5.5V**
- **4 Single-Ended or 2 Differential Inputs**
- **Programmable Gain: 1V/V to 128V/V**
- **Programmable Data Rates: Up to 2kSPS**
- **Low Current Consumption:**
  As Low as 175μA (TYP) in Duty-Cycle Mode
- **Effective Resolution: Up to 22 Bits**
- **Simultaneous 50Hz and 60Hz Rejection at 20SPS with Single-Cycle Settling Digital Filter**
- **Dual Matched Programmable Current Sources: 10μA to 1.5mA**
- **SPI-Compatible Interface (Mode 1)**
- **Internal 2.048V Reference Drift: 5ppm/℃ (TYP)**
- **Internal ±0.15% (TYP) Accurate Oscillator**
- **Internal Temperature Sensor Accuracy: ±0.9℃ (TYP)**
- **Available in Green TSSOP-16 and TQFN-3.5×3.5-16L Packages**

APPLICATIONS

Acquisitions for Temperature Sensor
- Thermistors
- Thermocouples
- Resistance Temperature Detectors (RTDs)

Acquisitions for Resistive Bridge Sensors
- Weigh Scales Sensors
- Pressure Sensors
- Strain Gauges Sensors

Factory Automation

Process Control

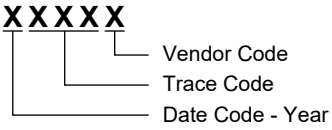
Portable Devices

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM58201	TSSOP-16	-40℃ to +125℃	SGM58201XTS16G/TR	SGM58201 XTS16 XXXXX	Tape and Reel, 4000
			SGM58201XTS16SG/TR	SGM58201 XTS16 XXXXX	Tape and Reel, 500
	TQFN-3.5×3.5-16L	-40℃ to +125℃	SGM58201XTVI16G/TR	58201 XTVI16 XXXXX	Tape and Reel, 4000
			SGM58201XTVI16SG/TR	58201 XTVI16 XXXXX	Tape and Reel, 500

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage Range
AVDD to AVSS ..... -0.3V to 7V
DVDD to DGND ..... -0.3V to 7V
AVSS to DGND ..... -2.8V to 0.3V
Analog Input Voltage Range (AIN0/REFP1, AIN1, AIN2, AIN3/REFN1, REFP0, REFN0)
..... (AVSS - 0.3V) to (AVDD + 0.3V)
Digital Input Voltage Range (nCS, SCLK, DIN, DOUT/nDRDY, nDRDY, CLK) ..... (DGND - 0.3V) to (DVDD + 0.3V)
Input Current Range (Continuous, Any Pin except Power Supply Pins)..... -10mA to 10mA
Package Thermal Resistance
TSSOP-16, θ_{JA} ..... 107℃/W
TSSOP-16, θ_{JB} ..... 68.9℃/W
TSSOP-16, θ_{JC} ..... 35.2℃/W
TQFN-3.5×3.5-16L, θ_{JA} ..... 39.1℃/W
TQFN-3.5×3.5-16L, θ_{JB} ..... 14.3℃/W
TQFN-3.5×3.5-16L, $\theta_{JC\ (TOP)}$ ..... 33.3℃/W
TQFN-3.5×3.5-16L, $\theta_{JC\ (BOT)}$ ..... 2.3℃/W
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility (1) (2)
HBM ..... ±4000V
CDM ..... ±1000V

NOTES:

1. For human body model (HBM), all pins comply with ANSI/ESDA/JEDEC JS-001 specifications.

2. For charged device model (CDM), all pins comply with ANSI/ESDA/JEDEC JS-002 specifications.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

RECOMMENDED OPERATING CONDITIONS

Unipolar Analog Power Supply Range
AVDD to AVSS ..... 2.3V to 5.5V
AVSS to DGND ..... -0.1V to 0.1V
Bipolar Analog Power Supply Range
AVDD to DGND ..... 2.3V to 2.75V, 2.5V (TYP)
AVSS to DGND ..... -2.75V to -2.3V, -2.5V (TYP)
Digital Power Supply Range
DVDD to DGND ..... 2.3V to 5.5V
Differential Input Voltage Range, V_{IN}, ($V_{IN} = V_{AINP} - V_{AINN}$) (3) (4)
..... $-V_{REF}$/Gain to V_{REF}/Gain
Absolute Input Voltage Range, V_{AINx}
PGA Disabled, Gain = 1 to 4
..... (AVSS - 0.1V) to (AVDD + 0.1V)
PGA Enabled, Gain = 1 to 128
..... See the Low-Noise PGA Section
Common Mode Input Voltage Range
PGA Disabled, Gain = 1 to 4
..... (AVSS - 0.1V) to (AVDD + 0.1V)
PGA Enabled, Gain = 1 to 128
..... See the Low-Noise PGA Section
Differential Reference Input Voltage Range (5), V_{REF}, ($V_{REF} = V_{REFPx} - V_{REFNx}$) ..... 0.75V to AVDD, 2.5V (TYP)
Absolute Negative Reference Voltage Range (5), V_{REFNx}
..... (AVSS - 0.1V) to (V_{REFPx} - 0.75V)
Absolute Positive Reference Voltage Range (5), V_{REFPx}
..... (V_{REFNx} + 0.75V) to (AVDD + 0.1V)
External Clock Frequency, f_{CLK}
..... 0.5MHz to 4.5MHz, 4.096MHz (TYP)
Duty-Cycle ..... 40% to 60%
Input Voltage Range ..... DGND to DVDD
Operating Temperature Range ..... -40℃ to +125℃

NOTES:

3. The AIN_P and AIN_N represent the positive and negative inputs of the PGA. The AIN_x refers to one of the four available analog inputs. When the PGA is disabled, it means that the low-noise PGA is powered down and bypassed. However, gains of 1, 2, and 4 are still possible in this case. Refer to the Bypassing the PGA section for more details.

4. Except for the effects of gain and offset error, the measurement range is limited to ±[(AVDD - AVSS) - 0.4V]/Gain when the PGA is enabled.

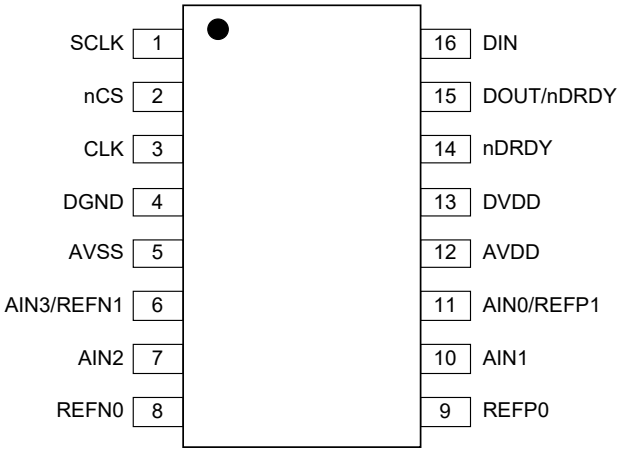
5. The REFPx and REFNx refer to one of the two available differential reference input pairs.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

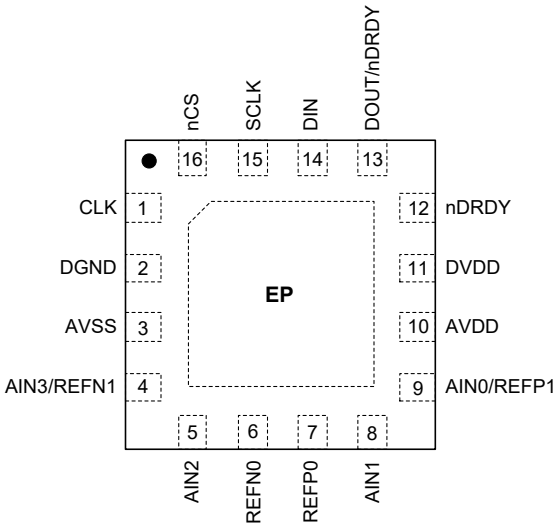
PIN CONFIGURATIONS

(TOP VIEW)



TSSOP-16

(TOP VIEW)



TQFN-3.5×3.5-16L

PIN DESCRIPTION

PIN		NAME	TYPE	FUNCTION
TSSOP-16	TQFN-3.5×3.5-16L			
1	15	SCLK	DI	Serial Clock Input Pin.
2	16	nCS	DI	Chip Select Pin. Active low. Connect to DGND when not in use.
3	1	CLK	DI	External Cock Source Pin. Connect to DGND when not in use.
4	2	DGND	G	Digital Ground.
5	3	AVSS	P	Negative Analog Power Supply.
6	4	AIN3/REFN1	AI	Analog Input 3/Negative Reference Input 1. The internal low-side power switch is connected between AIN3/REFN1 and AVSS.
7	5	AIN2	AI	Analog Input 2.
8	6	REFN0	AI	Negative Reference Input 0.
9	7	REFP0	AI	Positive Reference Input 0.
10	8	AIN1	AI	Analog Input 1.
11	9	AIN0/REFP1	AI	Analog Input 0/Positive Reference Input 1.
12	10	AVDD	P	Positive Analog Power Supply.
13	11	DVDD	P	Positive Digital Power Supply.
14	12	nDRDY	DO	Data Ready Pin. Active low. Keep floating or tie to DVDD with a weak pull-up resistor if unused.
15	13	DOUT/nDRDY	DO	Serial Data Output Combined with Data Ready. Active low.
16	14	DIN	DI	Serial Data Input Pin.
—	Exposed Pad	EP	—	Exposed Pad. It should be connected to AVSS.

NOTE: DI = digital input, DO = digital output, AI = analog input, P = power, G = ground.

ELECTRICAL CHARACTERISTICS

(T_A = -40℃ to +125℃, AVDD = 3.3V, AVSS = 0V, DVDD = 3.3V, PGA enabled, DR = 20SPS, and external V_{REF} = 2.5V, typical values are at T_A = +25℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Inputs						
Absolute Input Current			See the Typical Performance Characteristics section			
Differential Input Current			See the Typical Performance Characteristics section			
System Performance						
Resolution (No Missing Codes)				24		Bits
Data Rate	DR	Normal mode	20, 40, 75, 150, 300, 600, 1000			SPS
		Duty-cycle mode	5, 10, 18.75, 37.5, 75, 150, 250			
		Turbo mode	40, 80, 150, 300, 600, 1200, 2000			
Noise (Input-Referred)			See the Noise Performance section			
Integral Nonlinearity	INL	Gain = 1 to 128, V_{CM} = 0.5 AVDD, best fit (2)	-15	±4.5	15	ppmFSR
Input Offset Voltage	V_{IO}	PGA disabled, Gain = 1 to 4, differential inputs		±70		μV
		Gain = 1, differential inputs, T_A = +25℃	-35	±5	35	
		Gain = 2 to 128, differential inputs		±5		
Offset Drift		PGA disabled, Gain = 1 to 4		0.15		μV/℃
		Gain = 1 to 128, T_A = -40℃ to +85℃ (2)		0.15	0.35	
		Gain = 1 to 128		0.15		
Offset Match		Match between any two inputs		±5		μV
Gain Error	E_G	PGA disabled, Gain = 1 to 4		±0.015		%
		Gain = 1 to 64, T_A = +25℃	-0.07	±0.015	0.07	
		Gain = 128, T_A = +25℃	-0.25	±0.04	0.25	
Gain Drift		PGA disabled, Gain = 1 to 4		1		ppm/℃
		Gain = 1 to 128 (2)		1.5	4	
Normal Mode Rejection Ratio (2)	NMRR	DR = 20SPS, external CLK, 50Hz ± 3%, 50/60[1:0] bits = 10		100		dB
		DR = 20SPS, external CLK, 60Hz ± 3%, 50/60[1:0] bits = 11		100		
		DR = 20SPS, external CLK, 50Hz or 60Hz ± 3%, 50/60[1:0] bits = 01		85		
Common Mode Rejection Ratio	CMRR	At DC, Gain = 1		95		dB
		f_{CM} = 50Hz, DR = 2000SPS (2)		101		
		f_{CM} = 60Hz, DR = 2000SPS (2)		101		
Power Supply Rejection Ratio	PSRR	AVDD at DC, V_{CM} = 0.5 AVDD, Gain = 1	80	95		dB
		DVDD at DC, V_{CM} = 0.5 AVDD, Gain = 1 (2)	98	120		
Internal Voltage Reference						
Initial Accuracy		T_A = +25℃		2.048		V
Reference Drift (2)				5	10	ppm/℃
Long-Term Drift		1000 hours		80		ppm

NOTES:

1. PGA disabled stands for the low-noise PGA is bypassed, while the gains are still available for 1, 2, and 4. Refer to the Bypassing the PGA section for more information.

2. Design and characterization data guarantee the establishment of the minimum and maximum values.

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, AVDD = 3.3V, AVSS = 0V, DVDD = 3.3V, PGA enabled, DR = 20SPS, and external V_{REF} = 2.5V, typical values are at T_A = +25℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Reference Inputs						
Reference Input Current		REFP0 = V_{REF}, REFN0 = AVSS		±25		nA
Internal Oscillator						
Internal Oscillator Accuracy		Normal mode	-2.2	±0.15	2.2	%
Excitation Current Sources (IDACs)						
Current Settings			10, 50, 100, 250, 500, 1000, 1500			μA
Compliance Voltage		All current settings			AVDD - 0.9	V
Accuracy		1500μA, 1000μA current settings		±0.2		%
		500μA, 50μA current settings		±0.4		
		250μA current setting		±0.8		
		100μA current setting		±1.1		
		10μA current setting		±5.5		
Current Match		Between IDACs (not valid for 10μA setting)		±0.7		%
		Between IDACs (not valid for 10μA,100μA setting)		±0.02		
Temperature Drift		1500μA, 1000μA, 500μA, 50μA current settings		17.5	47	ppm/℃
		250μA current setting		26	65	
		100μA current setting		44	101	
Temperature Drift Matching		Between IDACs, 1500μA current setting		1.1	3	ppm/℃
		Between IDACs, 1000μA current setting		1.7	4.5	
		Between IDACs, 500μA current setting		3.0	7.5	
		Between IDACs, 250μA current setting		3.5	11	
		Between IDACs, 100μA current setting		32	65	
		Between IDACs, 50μA current setting		7.5	26	
Temperature Sensor						
Conversion Resolution				14		Bits
Temperature Resolution				0.03125		℃
Accuracy		T_A = 0℃ to +75℃	-1.5	±0.5	1.5	℃
		T_A = -40℃ to +125℃	-3	±0.9	3	
Accuracy vs. Analog Supply Voltage				0.18	1.1	℃/V
Low-side Power Switch						
On-Resistance	R_{ON}			4.5	14	Ω
Current through Switch					30	mA
Digital Inputs/Outputs						
High-Level Input Voltage	V_{IH}		0.7 × DVDD		DVDD	V
Low-Level Input Voltage	V_{IL}		DGND		0.3 × DVDD	V
High-Level Output Voltage	V_{OH}	I_{OH} = 3mA	0.8 × DVDD			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 3mA			0.2 × DVDD	V
Input High Leakage Current	I_{IH}	V_{IH} = 5.5V	-1		1	μA
Input Low Leakage Current	I_{IL}	V_{IL} = DGND	-1		1	μA

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40℃ to +125℃, AVDD = 3.3V, AVSS = 0V, DVDD = 3.3V, PGA enabled, DR = 20SPS, and external V_{REF} = 2.5V, typical values are at T_A = +25℃, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
Analog Supply Current (3)	I_{AVDD}	Power-down mode			0.45	2.5	μA
		Duty-cycle mode	PGA disabled		175		
			Gain = 1 to 16		206		
			Gain = 32		211		
			Gain = 64, 128		216		
		Normal mode	PGA disabled		480		
			Gain = 1 to 16		615	750	
			Gain = 32		655		
			Gain = 64, 128		706		
		Turbo mode	PGA disabled		752		
			Gain = 1 to 16		950		
			Gain = 32		996		
			Gain = 64, 128		1027		
Digital Supply Current (3)	I_{DVDD}	Power-down mode			0.45	3	μA
		Duty-cycle mode			48		
		Normal mode			120	200	
		Turbo mode			246		
Power Dissipation (3)	P_D	Duty-cycle mode, PGA disabled			0.8		mW
		Normal mode, Gain = 1 to 16			2.5		
		Turbo mode, Gain = 1 to 16			4		

NOTE:

3. With the internal voltage reference engaged, the internal oscillator activated, IDACs in the deactivated state, and continuous conversion mode, the analog supply current experiences a fall of 70μA on average (typical) in both normal mode and turbo mode when transitioning to an external reference. In cases where the IDACs are enabled (excluding the current flowing through the IDACs themselves), the analog supply current undergoes a typical elevation of 200μA.

SPI TIMING REQUIREMENTS

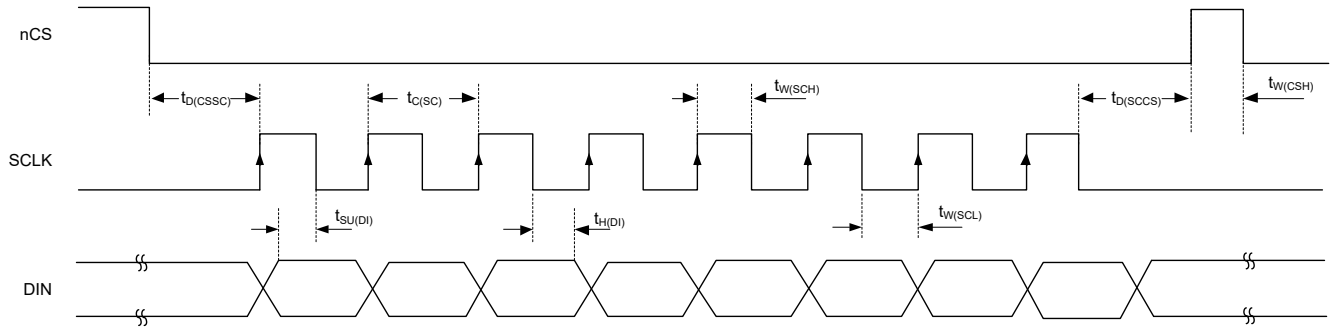
(T_A = -40℃ to +125℃, DVDD = 2.3V to 5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay Time, nCS Falling Edge to First SCLK Rising Edge (1)	$t_{D(CSSC)}$		50			ns
Delay Time, Final SCLK Falling Edge to nCS Rising Edge	$t_{D(SCCS)}$		25			ns
Pulse Duration, nCS High	$t_{W(CSH)}$		50			ns
SCLK Period	$t_{C(SC)}$		150			ns
Pulse Duration, SCLK High	$t_{W(SCH)}$		60			ns
Pulse Duration, SCLK Low	$t_{W(SCL)}$		60			ns
Setup Time, DIN Valid before SCLK Falling Edge	$t_{SU(DI)}$		50			ns
Hold Time, DIN Valid after SCLK Falling Edge	$t_{H(DI)}$		25			ns
SPI Timeout (2)		Normal mode, duty-cycle mode			13955	t_{MOD}
		Turbo mode			27910	t_{MOD}

NOTES:

1. nCS can be kept low without sharing SPI bus with the other devices.

2. Using the internal oscillator or an external 4.096MHz clock. $t_{MOD} = 1/f_{MOD}$. The modulator frequency f_{MOD} is 256kHz for normal and duty-cycle modes and 512kHz for turbo mode.



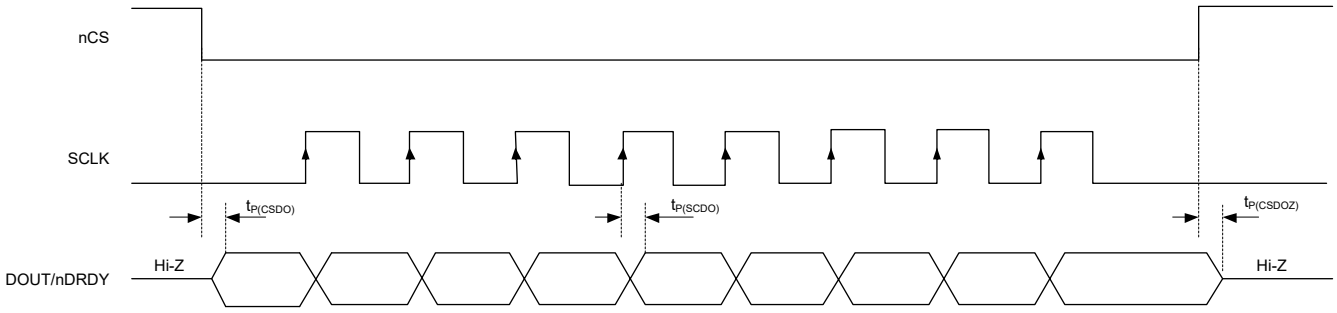
NOTE:
Shown as the single-byte communication, the actual communication may be multiple bytes.

Figure 1. Serial Interface Timing Diagram

SPI SWITCHING CHARACTERISTICS

(T_A = -40℃ to +125℃, DVDD = 2.3V to 5.5V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time, nCS Falling Edge to DOUT Driven	$t_{P(CSDO)}$	DOUT load = 20pF || 10kΩ to DGND			50	ns
Propagation Delay Time, SCLK Rising Edge to Valid New DOUT	$t_{P(SCDO)}$	DOUT load = 20pF || 10kΩ to DGND	0		50	ns
Propagation Delay Time, nCS Rising Edge to DOUT High Impedance	$t_{P(CSDOZ)}$	DOUT load = 20pF || 10kΩ to DGND			50	ns



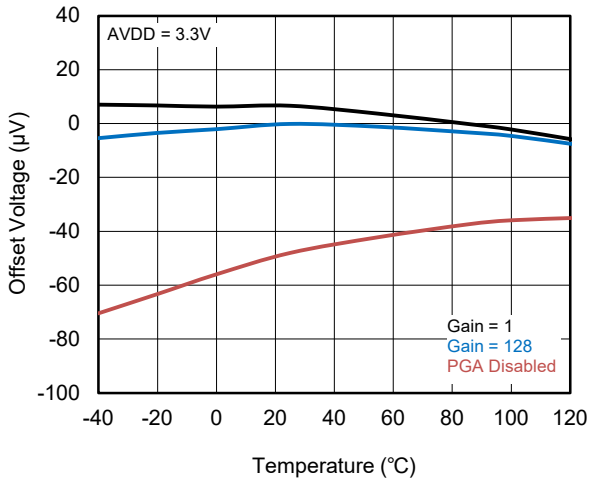
NOTE:
Shown as the single-byte communication, the actual communication may be multiple bytes.

Figure 2. Serial Interface Switching Characteristics

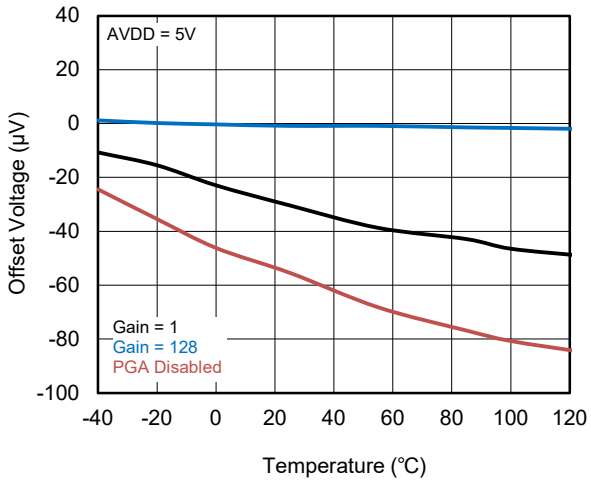
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, AVDD = 3.3V, AVSS = 0V, and PGA enabled using external V_{REF} = 2.5V, unless otherwise noted.

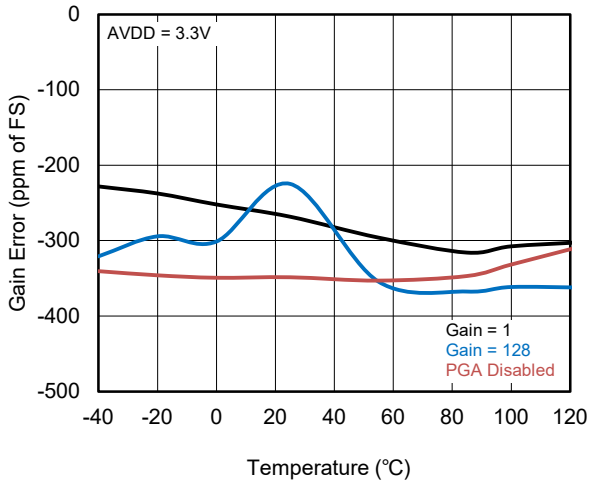
Input-Referred Offset Voltage vs. Temperature



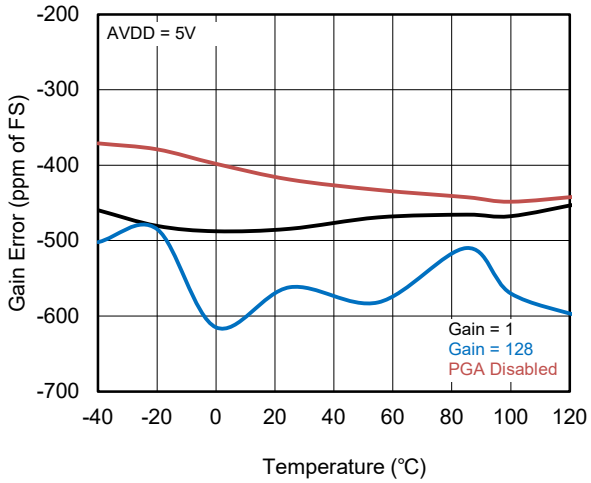
Input-Referred Offset Voltage vs. Temperature



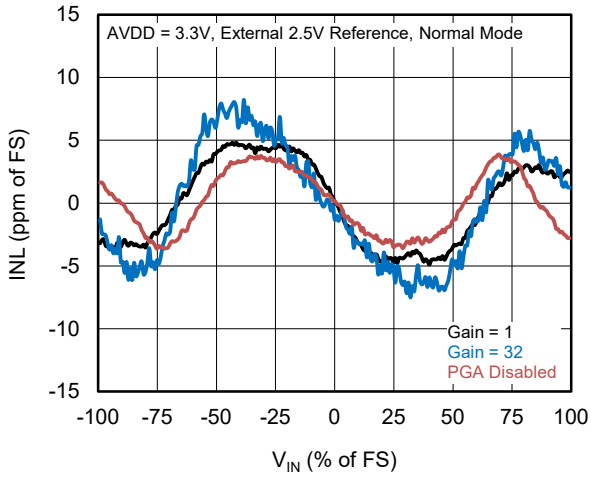
Gain Error vs. Temperature



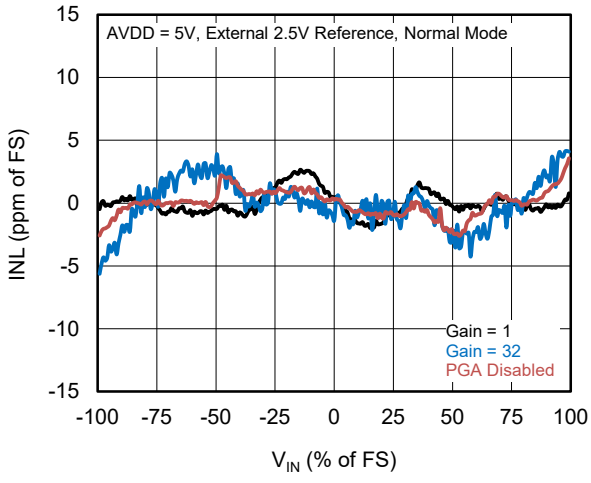
Gain Error vs. Temperature



Integral Nonlinearity vs. Differential Input Signal



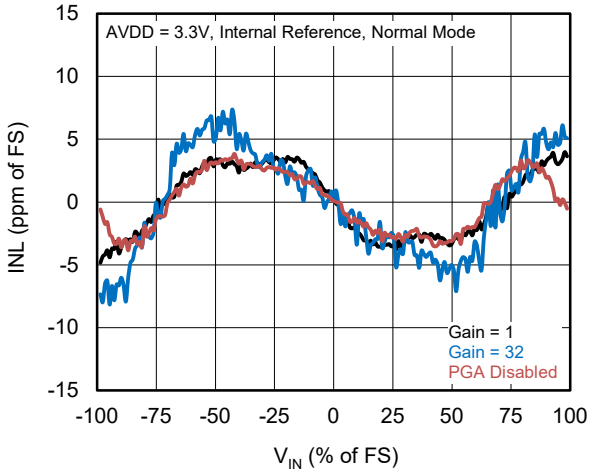
Integral Nonlinearity vs. Differential Input Signal



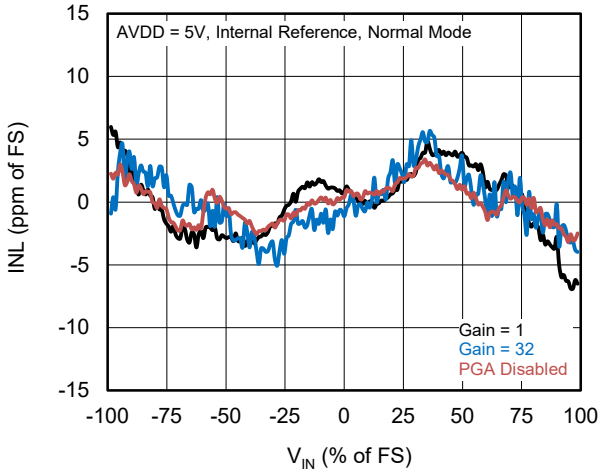
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3.3V, AVSS = 0V, and PGA enabled using external V_{REF} = 2.5V, unless otherwise noted.

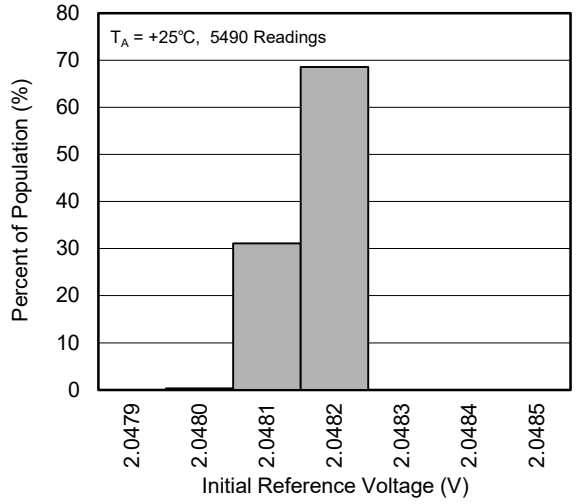
Integral Nonlinearity vs. Differential Input Signal



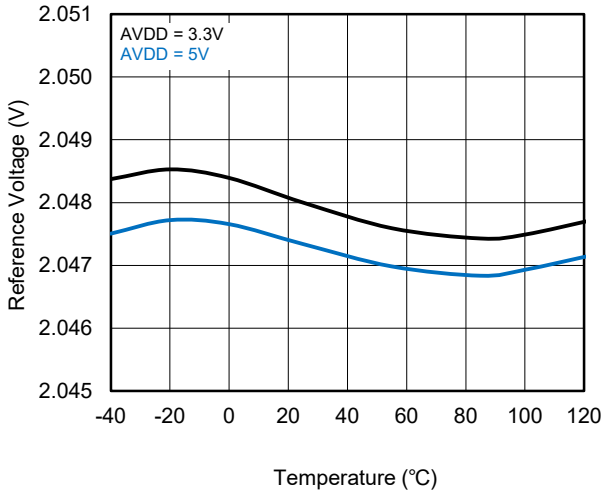
Integral Nonlinearity vs. Differential Input Signal



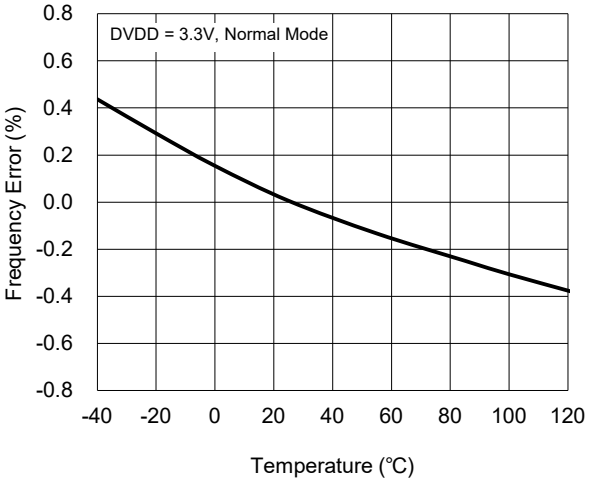
Internal Reference Voltage Histogram



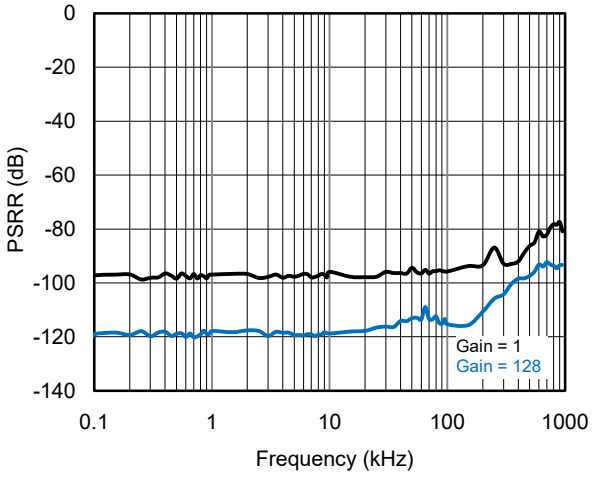
Internal Reference Voltage Error vs. Temperature



Internal Oscillator Accuracy vs. Temperature



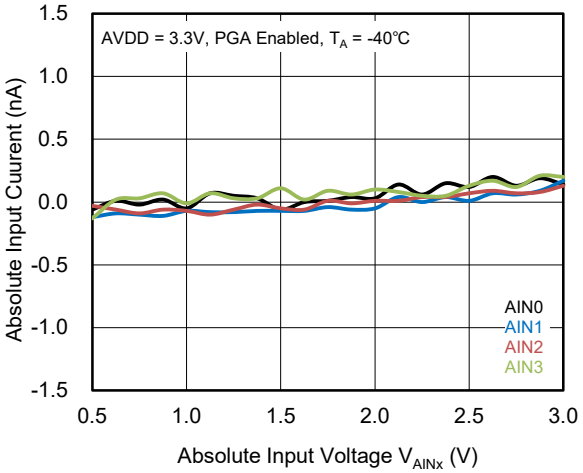
AVDD Power-Supply Rejection Ratio vs. Frequency



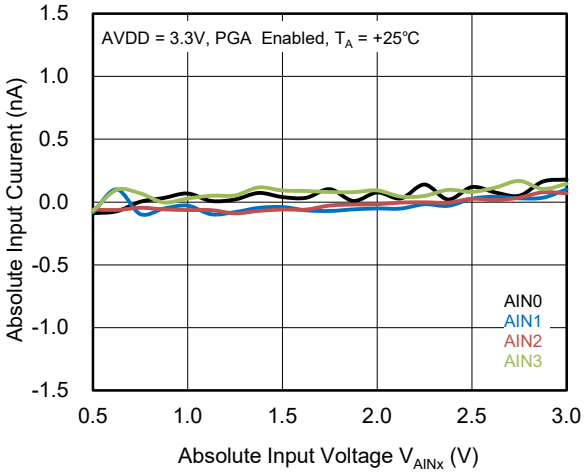
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3.3V, AVSS = 0V, and PGA enabled using external V_{REF} = 2.5V, unless otherwise noted.

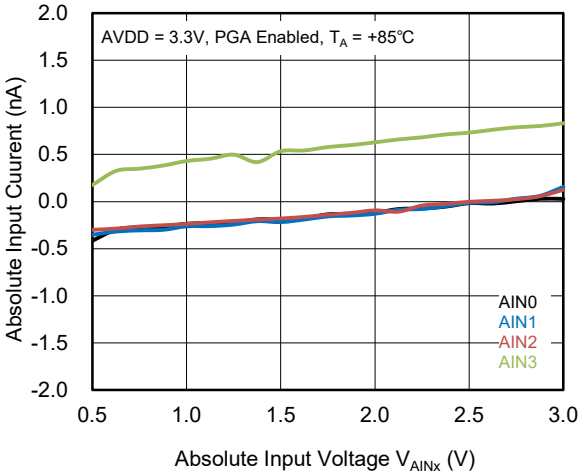
Absolute Input Current vs. Absolute Input Voltage



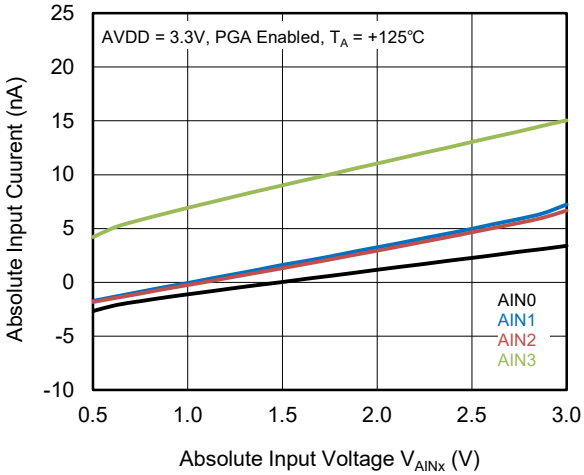
Absolute Input Current vs. Absolute Input Voltage



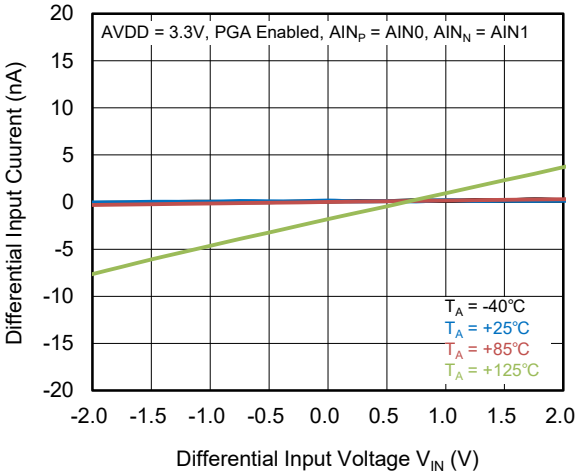
Absolute Input Current vs. Absolute Input Voltage



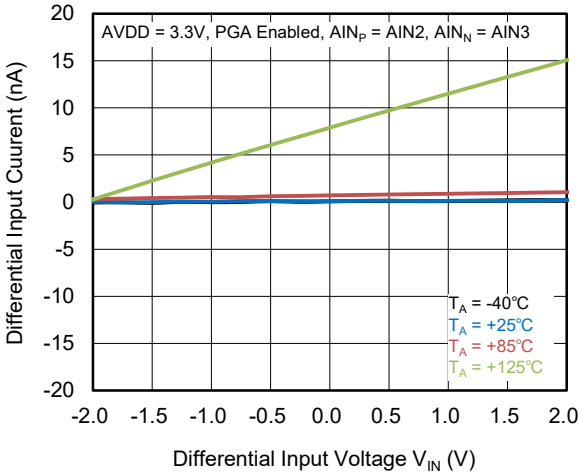
Absolute Input Current vs. Absolute Input Voltage



Differential Input Current vs. Differential Input Voltage



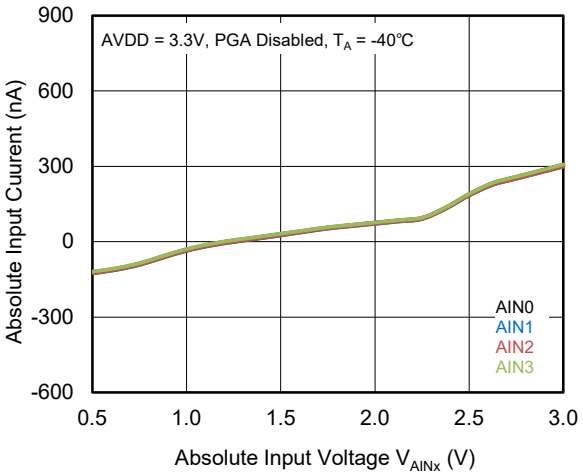
Differential Input Current vs. Differential Input Voltage



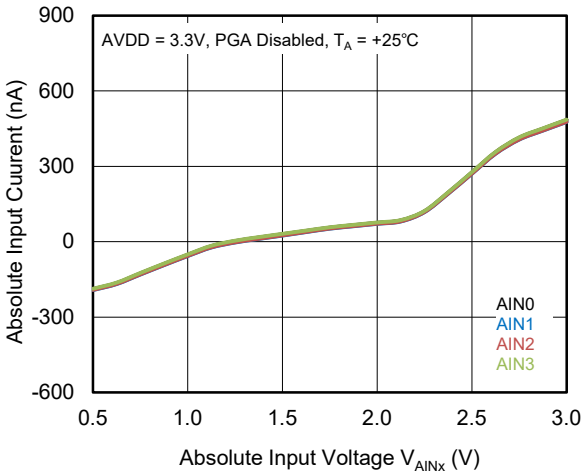
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3.3V, AVSS = 0V, and PGA enabled using external V_{REF} = 2.5V, unless otherwise noted.

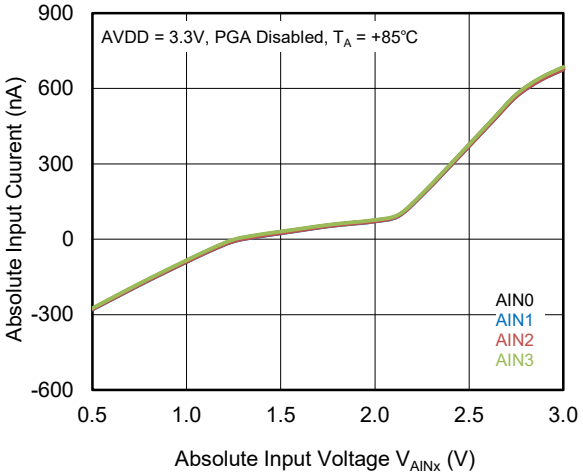
Absolute Input Current vs. Absolute Input Voltage



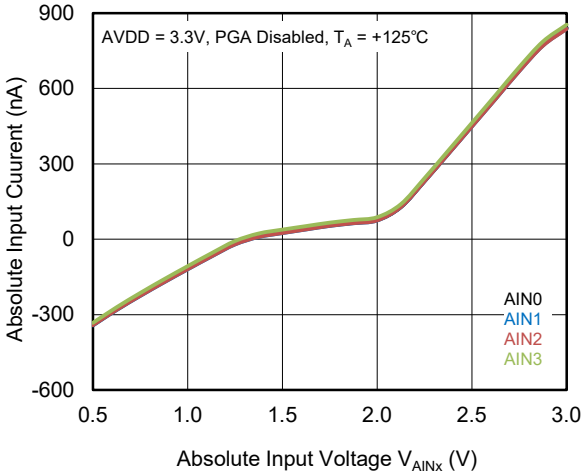
Absolute Input Current vs. Absolute Input Voltage



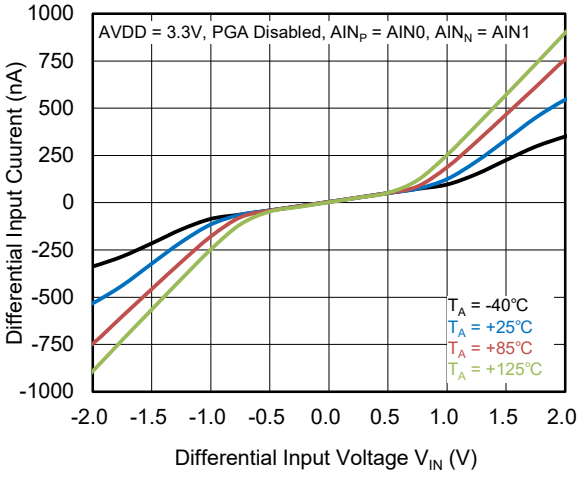
Absolute Input Current vs. Absolute Input Voltage



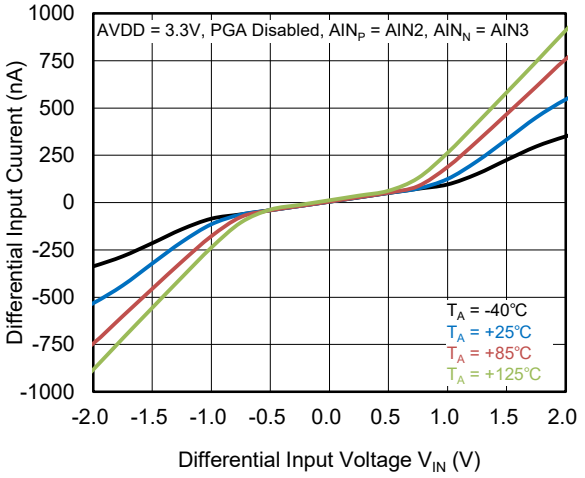
Absolute Input Current vs. Absolute Input Voltage



Differential Input Current vs. Differential Input Voltage



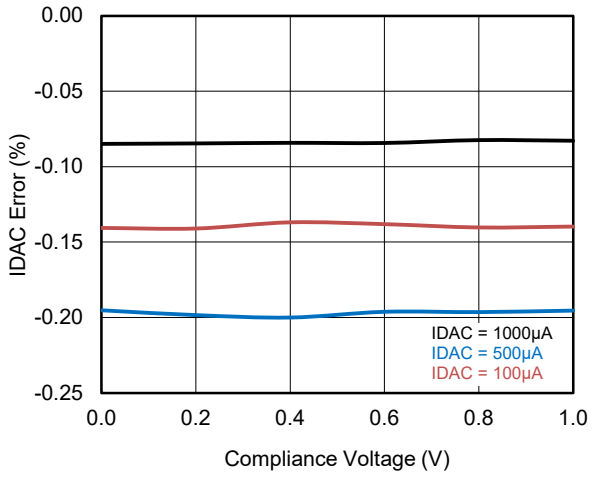
Differential Input Current vs. Differential Input Voltage



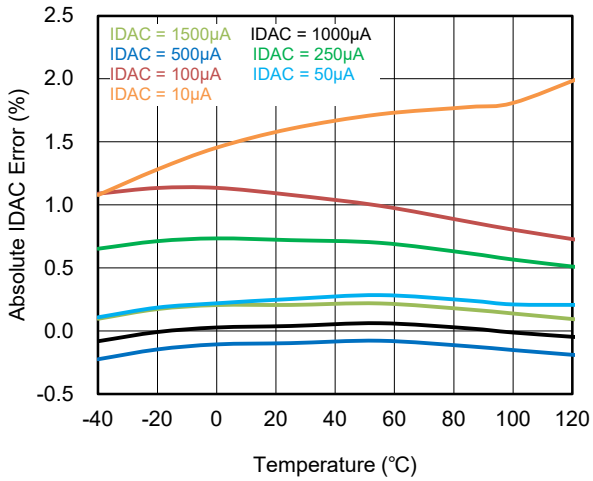
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3.3V, AVSS = 0V, and PGA enabled using external V_{REF} = 2.5V, unless otherwise noted.

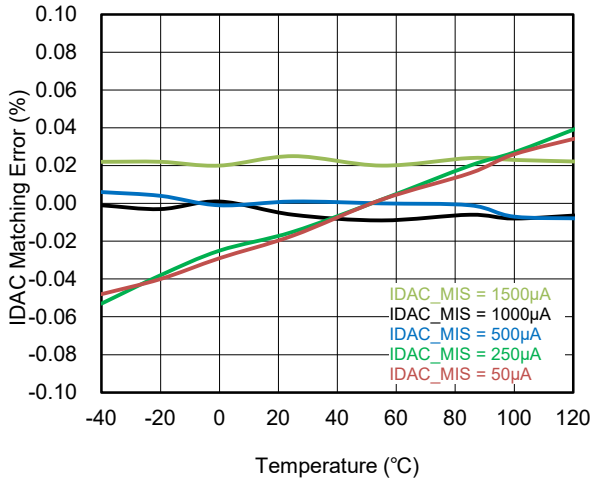
IDAC Accuracy vs. Compliance Voltage



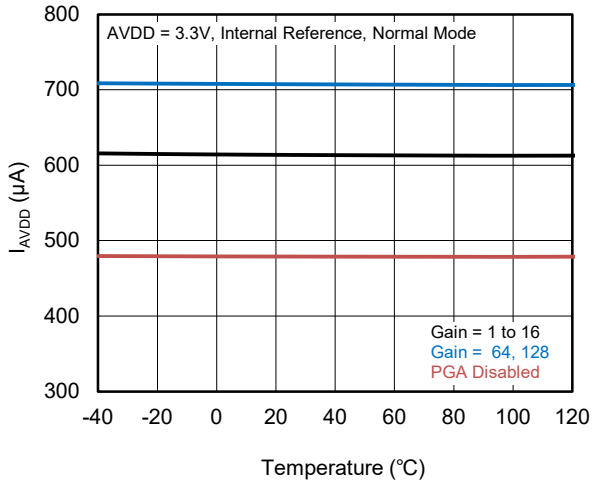
IDAC Accuracy vs. Temperature



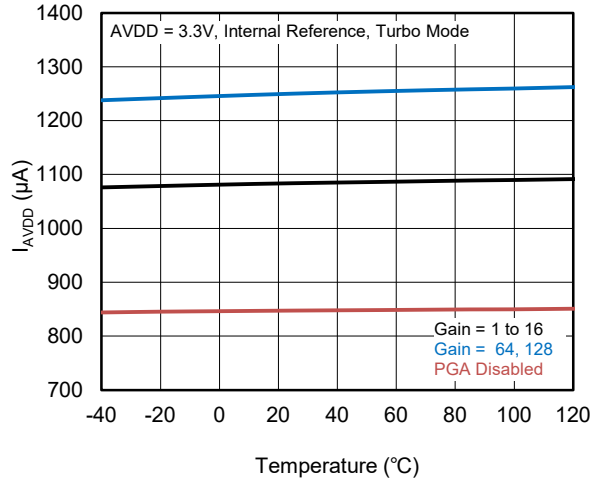
IDAC Matching Error vs. Temperature



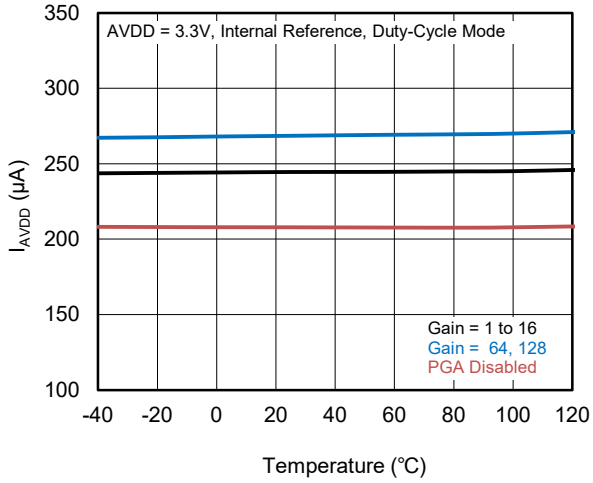
I_{AVDD} vs. Temperature



I_{AVDD} vs. Temperature



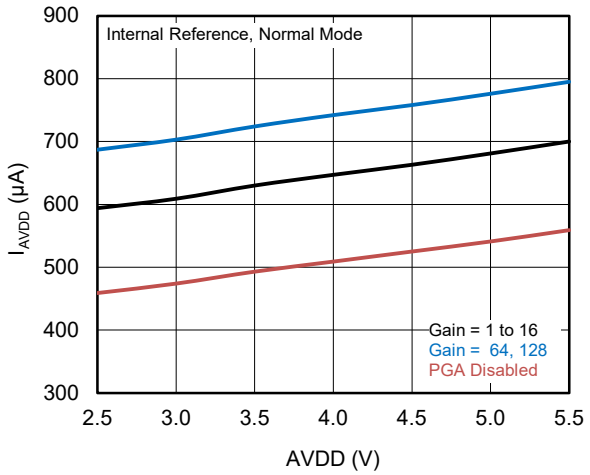
I_{AVDD} vs. Temperature



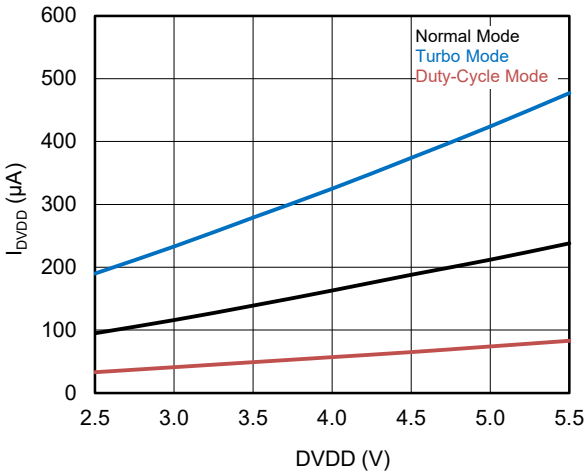
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, AVDD = 3.3V, AVSS = 0V, and PGA enabled using external V_{REF} = 2.5V, unless otherwise noted.

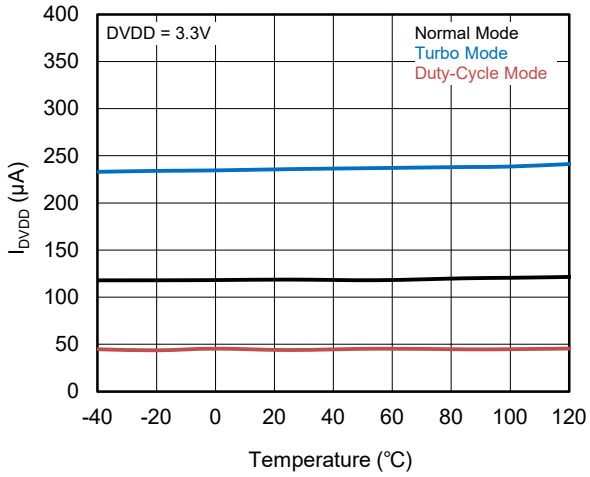
I_{AVDD} vs. AVDD



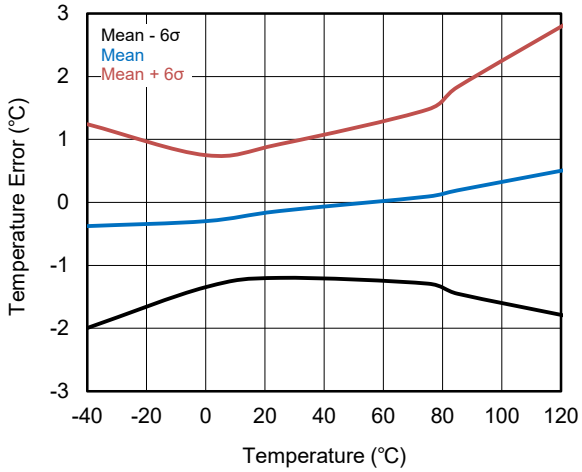
I_{DVDD} vs. DVDD



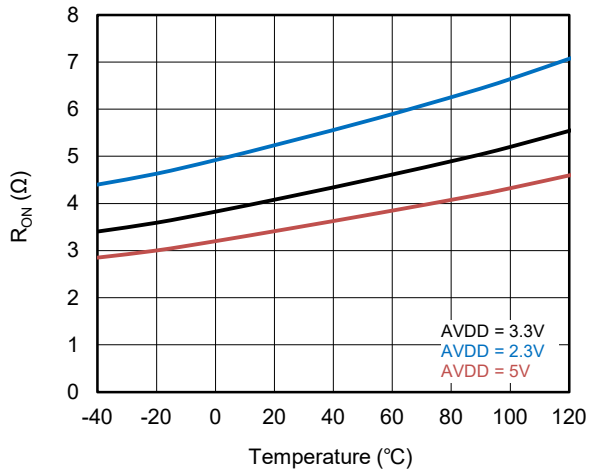
I_{DVDD} vs. Temperature



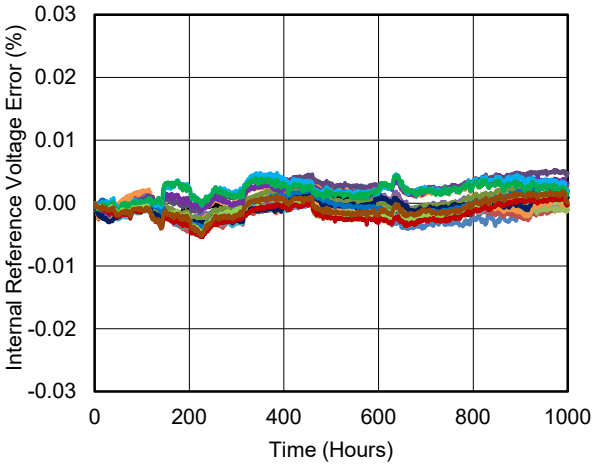
Internal Temperature Sensor Accuracy vs. Temperature



Low-side Power Switch R_{ON} vs. Temperature



Internal Reference Voltage vs. Time



PARAMETER MEASUREMENT INFORMATION

Noise Performance

The sigma-delta (Σ-Δ) analog-to-digital converters (ADCs) operate on the oversampling principle. In this technique, the input signal of a Σ-Δ ADC is sampled at a high frequency called the modulator frequency. Subsequently, the sampled data undergoes digital filtering and decimation, resulting in a conversion outcome at the desired output data rate. The relationship between the modulator frequency and the output data rate is termed the oversampling ratio (OSR). Improve the OSR to reduce the output data rate, and optimize the ADC's noise performance. Lowering the output data rate reduces input-related noise, as more modulator samples are averaged for each conversion outcome. Increasing the gain further decreases the input-referred noise, which is especially beneficial for precise measurement of weak signals.

The noise performance details are presented in Table 1 through Table 8. These tables showcase the typical noise performance results at +25℃ using the internal 2.048V reference. The data represents average readings from a single device over approximately 0.75 seconds, with the inputs shorted together internally. For the given conditions, Table 1, Table 3, Table 5, and Table 7 report input-referred noise in μV_{RMS} units (with corresponding values in μV_{PP} shown in parentheses). Meanwhile, Table 2, Table 4, Table 6, and Table 8 present the corresponding information in terms of effective number of bits (ENOB), derived from μV_{RMS} values using Equation 1. Additionally, the noise-free bits, determined from peak-to-peak noise values through Equation 2, are indicated in parentheses.

It is noteworthy that the input-referred noise (Table 1, Table 3, Table 5, and Table 7) experiences only minor fluctuations when an external low-noise reference is used. When dealing with reference voltages other than 2.048V, ENOB values and noise-free bits can be calculated by using Equation 1 through Equation 3.

$$ENOB = \ln(\text{Full-Scale Range}/V_{RMS\text{-}Noise})/\ln(2) \quad (1)$$

$$\text{Noise-Free Bits} = \ln(\text{Full-Scale Range}/V_{PP\text{-}Noise})/\ln(2) \quad (2)$$

$$\text{Full-Scale Range} = 2 \cdot V_{REF}/\text{Gain} \quad (3)$$

Table 1. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3V, AVSS = 0V, Normal Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
20	0.9 (3.61)	0.46 (1.81)	0.23 (0.83)	0.15 (0.59)	0.1 (0.44)	0.1 (0.34)	0.07 (0.27)	0.08 (0.31)
40	1.29 (5.62)	0.72 (3.42)	0.35 (1.5)	0.19 (0.9)	0.16 (0.72)	0.12 (0.54)	0.11 (0.5)	0.11 (0.48)
75	1.76 (8.64)	0.9 (4.61)	0.48 (2.38)	0.29 (1.39)	0.21 (1.05)	0.17 (0.86)	0.16 (0.8)	0.17 (0.78)
150	2.59 (13.53)	1.33 (7.1)	0.67 (3.81)	0.42 (2.4)	0.3 (1.59)	0.27 (1.42)	0.24 (1.23)	0.24 (1.24)
300	3.59 (20.46)	1.75 (9.72)	0.94 (5.44)	0.58 (3.28)	0.44 (2.53)	0.38 (2.09)	0.35 (1.99)	0.34 (2.0)
600	4.91 (29.15)	2.4 (14.5)	1.33 (8.36)	0.76 (4.71)	0.58 (3.58)	0.5 (3.01)	0.46 (2.66)	0.46 (2.74)
1000	8.43 (61.67)	4.26 (32.71)	2.21 (16.86)	1.2 (9.28)	0.81 (5.64)	0.64 (4.01)	0.58 (3.77)	0.57 (3.62)

Table 2. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise) at AVDD = 3.3V, AVSS = 0V, Normal Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
20	22.12 (20.11)	22.1 (20.11)	22.07 (20.23)	21.73 (19.72)	21.22 (19.14)	20.29 (18.51)	19.72 (17.85)	18.69 (16.65)
40	21.6 (19.48)	21.43 (19.19)	21.48 (19.38)	21.34 (19.12)	20.64 (18.43)	20.02 (17.86)	19.2 (16.98)	18.16 (16.02)
75	21.15 (18.85)	21.11 (18.76)	21.02 (18.71)	20.77 (18.49)	20.23 (17.9)	19.48 (17.18)	18.65 (16.29)	17.54 (15.32)
150	20.59 (18.21)	20.56 (18.14)	20.55 (18.04)	20.22 (17.7)	19.68 (17.3)	18.88 (16.46)	18.0 (15.67)	17.03 (14.66)
300	20.12 (17.61)	20.16 (17.69)	20.05 (17.52)	19.75 (17.25)	19.14 (16.63)	18.36 (15.9)	17.48 (14.97)	16.52 (13.96)
600	19.67 (17.1)	19.7 (17.11)	19.56 (16.9)	19.37 (16.73)	18.75 (16.12)	17.97 (15.38)	17.08 (14.55)	16.1 (13.51)
1000	18.89 (16.02)	18.88 (15.93)	18.82 (15.89)	18.71 (15.75)	18.27 (15.47)	17.61 (14.96)	16.75 (14.05)	15.79 (13.11)

PARAMETER MEASUREMENT INFORMATION (continued)

Table 3. Noise in μV_{RMS} (μV_{PP}) with PGA Disabled at AVDD = 3.3V, AVSS = 0V, Normal Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Disabled)		
	1	2	4
20	0.7 (2.78)	0.63 (2.49)	0.41 (1.64)
40	1.13 (5.18)	0.91 (4.49)	0.51 (2.47)
75	1.49 (7.52)	1.22 (5.79)	0.73 (3.43)
150	2.14 (11.28)	1.71 (9.28)	1.11 (5.52)
300	2.89 (16.89)	2.4 (13.7)	1.46 (8.41)
600	3.95 (23.63)	3.36 (20.61)	2.04 (13.24)
1000	7.85 (62.6)	5.11 (36.69)	3.02 (20.18)

Table 4. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise) with PGA Disabled at AVDD = 3.3V, AVSS = 0V, Normal Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Disabled)		
	1	2	4
20	22.47 (20.49)	21.64 (19.65)	21.26 (19.26)
40	21.8 (19.59)	21.1 (18.8)	20.93 (18.66)
75	21.39 (19.06)	20.67 (18.43)	20.42 (18.19)
150	20.87 (18.47)	20.19 (17.75)	19.82 (17.5)
300	20.43 (17.89)	19.7 (17.19)	19.42 (16.89)
600	19.98 (17.4)	19.22 (16.6)	18.94 (16.24)
1000	18.99 (16.0)	18.61 (15.77)	18.37 (15.63)

Table 5. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3V, AVSS = 0V, Turbo Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
40	0.92 (4.1)	0.47 (1.95)	0.24 (1.11)	0.17 (0.72)	0.14 (0.64)	0.11 (0.5)	0.1 (0.48)	0.1 (0.42)
80	1.33 (6.45)	0.66 (3.15)	0.37 (1.97)	0.23 (1.26)	0.18 (0.9)	0.16 (0.86)	0.15 (0.71)	0.14 (0.66)
150	1.88 (10.45)	0.95 (5.08)	0.5 (3.05)	0.32 (1.68)	0.26 (1.35)	0.23 (1.21)	0.22 (1.15)	0.22 (1.19)
300	2.64 (14.89)	1.3 (7.28)	0.67 (3.75)	0.45 (2.51)	0.36 (2.12)	0.32 (1.85)	0.3 (1.72)	0.31 (1.84)
600	3.56 (22.31)	1.76 (10.91)	0.95 (6.31)	0.63 (3.94)	0.49 (3.15)	0.44 (2.8)	0.4 (2.56)	0.4 (2.41)
1200	4.94 (31.3)	2.43 (16.36)	1.3 (8.44)	0.83 (5.39)	0.63 (4.04)	0.56 (3.54)	0.52 (3.53)	0.51 (3.24)
2000	8.57 (66.8)	4.32 (35.33)	2.22 (17.36)	1.27 (9.99)	0.87 (6.17)	0.71 (4.71)	0.63 (4.37)	0.62 (4.07)

Table 6. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise) at AVDD = 3.3V, AVSS = 0V, Turbo Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Enabled)							
	1	2	4	8	16	32	64	128
40	22.09 (19.93)	22.05 (20.0)	22.0 (19.81)	21.56 (19.44)	20.81 (18.61)	20.11 (17.97)	19.3 (17.02)	18.33 (16.21)
80	21.55 (19.28)	21.56 (19.31)	21.39 (18.99)	21.08 (18.64)	20.46 (18.12)	19.58 (17.19)	18.72 (16.47)	17.82 (15.57)
150	21.06 (18.58)	21.05 (18.62)	20.96 (18.36)	20.6 (18.21)	19.89 (17.53)	19.1 (16.69)	18.15 (15.76)	17.14 (14.71)
300	20.56 (18.07)	20.59 (18.1)	20.54 (18.06)	20.12 (17.64)	19.43 (16.88)	18.62 (16.08)	17.71 (15.18)	16.67 (14.08)
600	20.13 (17.49)	20.15 (17.52)	20.04 (17.31)	19.64 (16.99)	18.99 (16.31)	18.16 (15.48)	17.28 (14.61)	16.27 (13.7)
1200	19.66 (17.0)	19.68 (16.93)	19.59 (16.89)	19.24 (16.54)	18.63 (15.95)	17.81 (15.14)	16.91 (14.15)	15.93 (13.27)
2000	18.87 (15.9)	18.85 (15.82)	18.82 (15.85)	18.62 (15.65)	18.17 (15.34)	17.47 (14.73)	16.63 (13.84)	15.65 (12.94)

PARAMETER MEASUREMENT INFORMATION (continued)

Table 7. Noise in μV_{RMS} (μV_{PP}) with PGA Disabled at AVDD = 3.3V, AVSS = 0V, Turbo Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Disabled)		
	1	2	4
40	0.77 (3.22)	0.62 (2.66)	0.38 (1.62)
80	1.05 (4.93)	0.91 (4.15)	0.55 (2.93)
150	1.43 (8.06)	1.23 (6.59)	0.78 (4.09)
300	2.05 (12.21)	1.74 (10.5)	1.08 (6.51)
600	2.89 (17.92)	2.44 (14.87)	1.52 (9.06)
1200	4.11 (28.12)	3.26 (21.61)	2.07 (13.49)
2000	7.77 (64.36)	5.2 (38.4)	2.97 (21.67)

Table 8. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise) with PGA Disabled at AVDD = 3.3V, AVSS = 0V, Turbo Mode, and Internal Reference = 2.048V

Data Rate (SPS)	Gain (PGA Disabled)		
	1	2	4
40	22.34 (20.28)	21.66 (19.55)	21.37 (19.27)
80	21.89 (19.66)	21.11 (18.91)	20.83 (18.42)
150	21.45 (18.96)	20.67 (18.25)	20.33 (17.93)
300	20.93 (18.36)	20.16 (17.57)	19.85 (17.26)
600	20.43 (17.8)	19.68 (17.07)	19.37 (16.79)
1200	19.93 (17.15)	19.26 (16.53)	18.92 (16.21)
2000	19.01 (15.96)	18.59 (15.7)	18.4 (15.53)

TYPICAL APPLICATION CIRCUIT

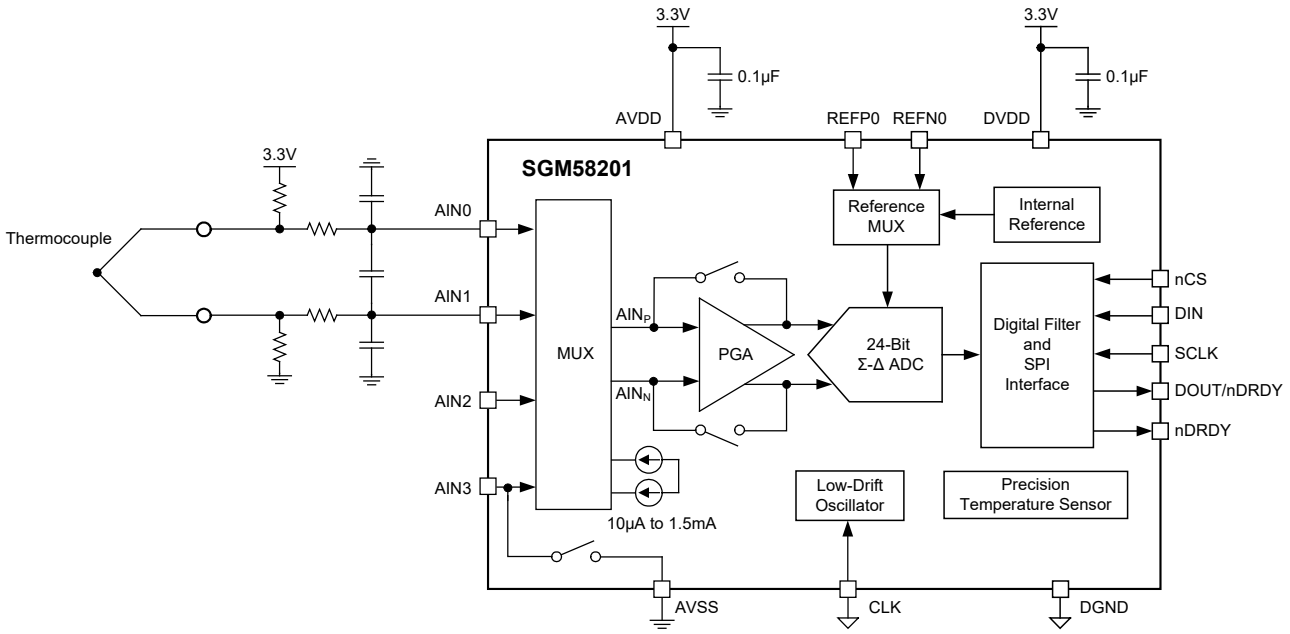


Figure 3. K-Type Thermocouple Measurement

FUNCTIONAL BLOCK DIAGRAM

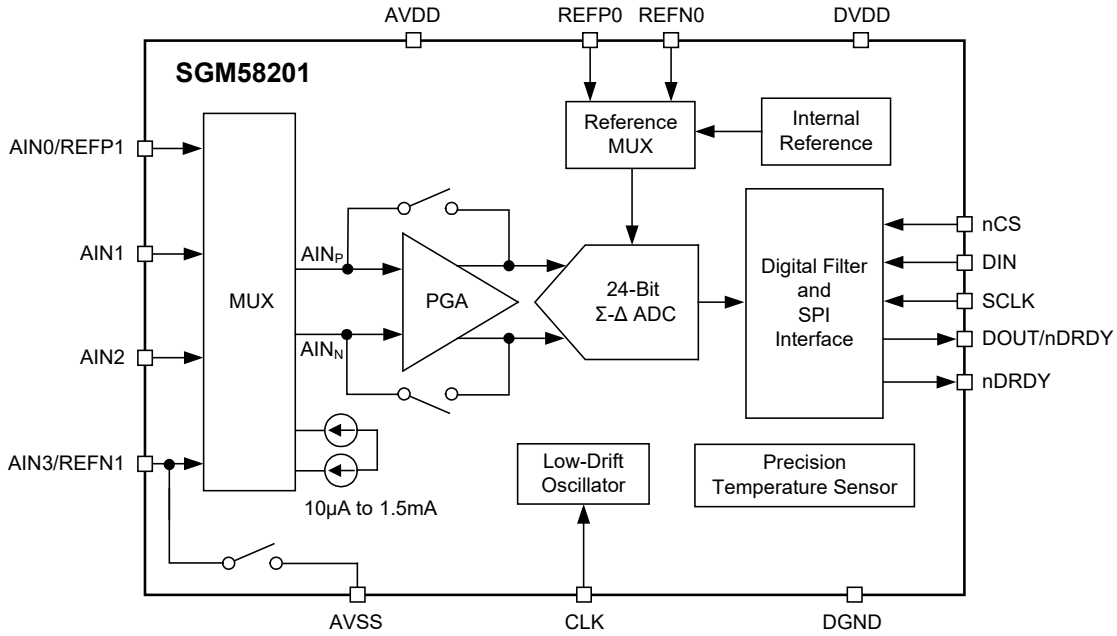


Figure 4. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM58201 is a compact and energy-efficient 24-bit Σ-Δ ADC designed for applications that require precise measurement of delicate sensor signals. Its small size and low power consumption make it an ideal choice for efficient systems.

Featuring a Σ-Δ ADC core, a single-cycle settling digital filter, a low-noise, high input impedance programmable gain amplifier (PGA), an internal voltage reference, and a clock oscillator, the SGM58201 offers a comprehensive set of functionalities. The inclusion of a highly linear and accurate temperature sensor, along with two precisely matched programmable current sources (IDACs) for sensor excitation, enhances the device's versatility.

The ADC accurately measures a differential signal (V_{IN}), which represents the voltage difference between AIN_P and AIN_N nodes. Its core comprises a differential switched-capacitor Σ-Δ modulator followed by a digital filter. This architecture effectively attenuates the common mode signals, contributing to improve the signal fidelity.

The SGM58201 provides two conversion modes: single-shot and continuous conversion. In single-shot mode, the ADC performs a single conversion upon request, stores the result in an internal data buffer and enters a low-power state for energy efficiency. Continuous conversion mode initiates a new conversion immediately after the completion of the previous one, providing freshly generated data at the programmed data rate for a consistent flow of information.

Multiplexer

The SGM58201 features a highly versatile input multiplexer, as shown in Figure 5. This multiplexer setup provides the flexibility to measure either four single-ended signals, two differential signals, or a combination of two single-ended and one differential signal. The multiplexer configuration is controlled by four bits labeled MUX[3:0] within the configuration register. When dealing with single-ended signals, a switch within the multiplexer allows the internal connection of the negative ADC input (AIN_N) to AVSS. For system monitoring purposes, the ADC offers the option to select either (AVDD - AVSS)/4 or the currently chosen external reference voltage (VREFPx - VREFNx)/4 as inputs.

In addition, the multiplexer allows routing of the two programmable current sources to any analog input (AIN_x) or to dedicated reference pins (REFP0, REFN0), providing enhanced application flexibility. The device incorporates electrostatic discharge (ESD) diodes to protect AVDD and AVSS integrity. To keep these ESD diodes inactive, it is crucial to ensure that the absolute voltage applied to any input falls within the specified range as defined by Equation 4.

$$AVSS - 0.3V < V_{AINx} < AVDD + 0.3V \quad (4)$$

In cases where the voltages applied to the input pins have the potential to exceed the specified conditions, it may be necessary to consider incorporating the external Schottky clamp diodes or series resistors to limit the input current within safe parameters (for detailed guidance, refer to the ABSOLUTE MAXIMUM RATINGS section). It is important to note that if an unused input is subjected to overdriving, it could potentially impact ongoing conversions on other input pins. In situations where the risk of overdrive on idle inputs exists, it is recommended to use external Schottky diodes to clamp the signal and prevent adverse effects.

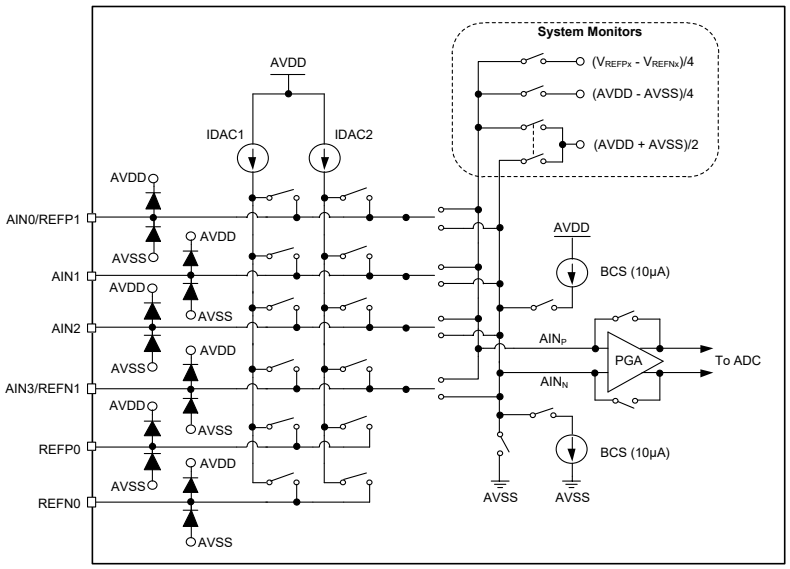


Figure 5. Analog Input Multiplexer

DETAILED DESCRIPTION (continued)

Low-Noise PGA

The SGM58201 features a programmable gain amplifier (PGA) known for its low-noise, minimal drift and high input impedance characteristics. This versatile PGA allows easy adjustment to achieve gains of 1, 2, 4, 8, 16, 32, 64, or 128, providing significant flexibility. The input of the PGA is strengthened with an electromagnetic interference (EMI) filter, enhancing signal integrity.

The range of the differential full-scale input voltage (FSR) for the programmable gain amplifier (PGA) is determined by the combination of the selected gain setting and the reference voltage used. This relationship is expressed by Equation 5.

$$FSR = \pm V_{REF}/Gain \quad (5)$$

Table 9 provides an overview of the associated full-scale ranges applicable when utilizing the internal 2.048V reference.

Table 9. PGA Full-Scale Range

Gain Setting	FSR
1	±2.048V
2	±1.024V
4	±0.512V
8	±0.256V
16	±0.128V
32	±0.064V
64	±0.032V
128	±0.016V

PGA Common Mode Voltage Requirements

To ensure that the programmable gain amplifier (PGA) operates within its linear range, the specific conditions must be met by the input signals, as explained in this section.

In Figure 6, it is crucial to understand that the outputs of both amplifiers (A1 and A2), labeled as OUT_P and OUT_N, should not approach the supply rails (AVSS and AVDD) closer than a threshold of 200mV. When these output voltages come within 200mV of the supply rails, the amplifiers go into saturation, leading to nonlinearity. To prevent this nonlinear state, the output voltage levels must meet the criterion shown in Equation 6:

$$AVSS + 0.2V \le V_{OUTN}, V_{OUTP} \le AVDD - 0.2V \quad (6)$$

Translating the conditions specified by Equation 6 into requirements for the inputs of the programmable gain amplifier (PGA), specifically AIN_P and AIN_N, is beneficial as direct access to the PGA outputs is not available. Considering the symmetrical nature of the PGA, it is reasonable to assume that the common mode voltage at the PGA output reflects that of the common mode voltage in the input signal. This symmetry is depicted in Figure 6.

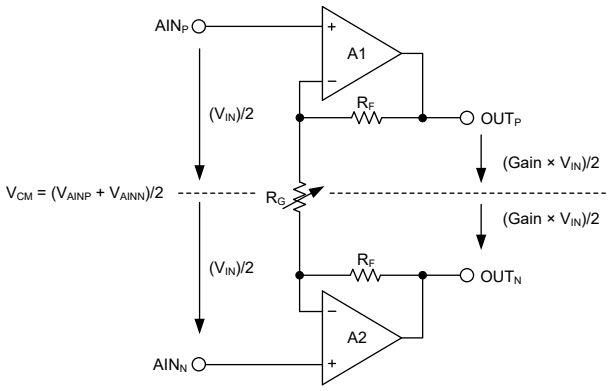


Figure 6. PGA Common Mode Voltage

The determination of the common mode voltage is achieved through the utilization of Equation 7:

$$V_{CM} = (V_{AINP} + V_{AINN})/2 = (V_{OUTP} + V_{OUTN})/2 \quad (7)$$

The voltages present at the inputs of the programmable gain amplifier (PGA), named AIN_P and AIN_N, can be formulated by using Equation 8 and Equation 9:

$$V_{AINP} = V_{CM} + V_{IN}/2 \quad (8)$$

$$V_{AINN} = V_{CM} - V_{IN}/2 \quad (9)$$

Consequently, the output voltages (V_{OUTP} and V_{OUTN}) can be calculated according to Equation 10 and Equation 11:

$$V_{OUTP} = V_{CM} + Gain \times V_{IN}/2 \quad (10)$$

$$V_{OUTN} = V_{CM} - Gain \times V_{IN}/2 \quad (11)$$

The conditions governing the output voltages of the amplifiers A1 and A2 (as shown in Equation 6) can now be transformed into prerequisites for the input common mode voltage range, employing Equation 10 and Equation 11. This translation leads to the expression of these requirements in the form of Equation 12 and Equation 13:

$$V_{CM\,(MIN)} \ge AVSS + 0.2V + Gain \times V_{IN\,(MAX)}/2 \quad (12)$$

$$V_{CM\,(MAX)} \le AVDD - 0.2V - Gain \times V_{IN\,(MAX)}/2 \quad (13)$$

DETAILED DESCRIPTION (continued)

To establish the upper and lower boundaries of the common mode voltage, it is imperative to employ the maximum differential input voltage ($V_{IN(MAX)}$) that emerges within the application. It is important to note that $V_{IN(MAX)}$ may be less than the theoretically achievable full-scale (FS) value.

Furthermore, apart from adhering to Equation 12, the minimum value of the common mode voltage (V_{CM}) must also satisfy Equation 14 due to the distinct design characteristics of the programmable gain amplifier (PGA).

$$V_{CM\ (MIN)} \geq AVSS + (AVDD - AVSS)/4 \quad (14)$$

Graphical depictions of the common mode voltage limits are elucidated in Figure 7 and Figure 8. These illustrations are predicated on the conditions of AVDD = 3.3V and AVSS = 0V, considering two distinct scenarios: Gain = 1 and Gain = 16.

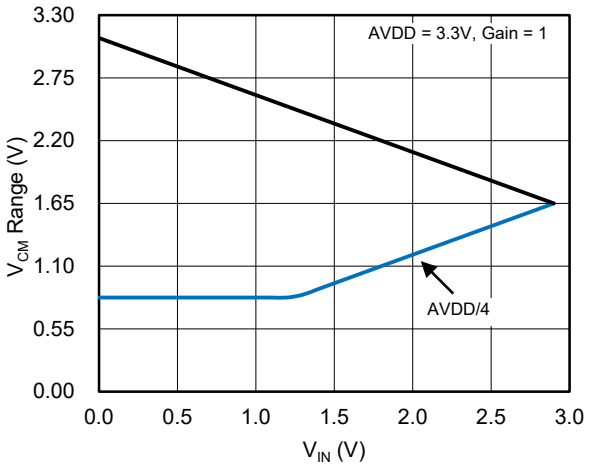


Figure 7. Common Mode Voltage Limits (Gain = 1)

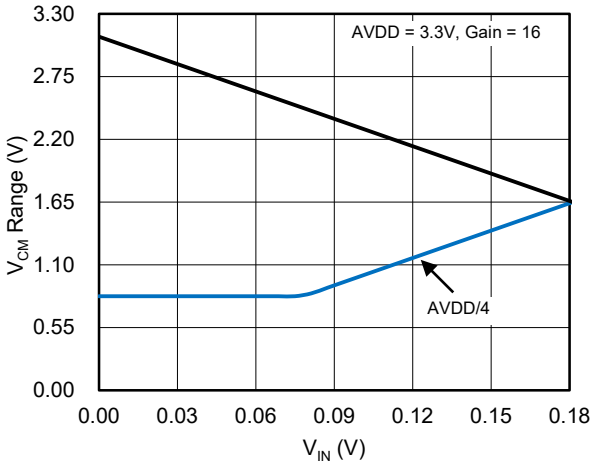


Figure 8. Common Mode Voltage Limits (Gain = 16)

The example of the fully-differential input signal is shown in Figure 9, and the example of the pseudo-differential input signal is shown in Figure 10.

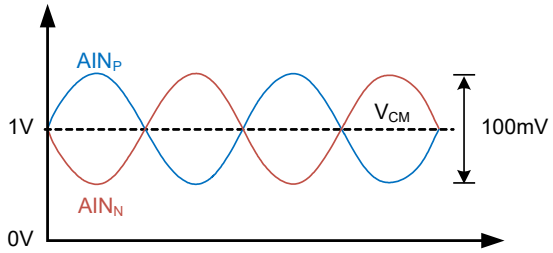


Figure 9. Fully-Differential Input Signal

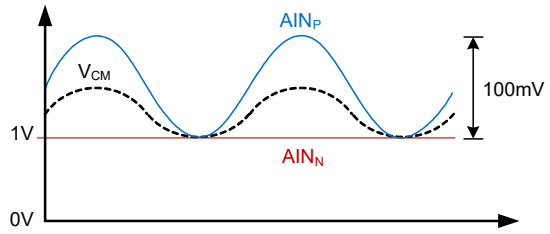


Figure 10. Pseudo-Differential Input Signal

Bypassing the PGA

For gain settings of 1, 2, and 4, the device provides an option to turn off and bypass the low-noise PGA by toggling the PGA_BYPASS bit in the configuration register. Disabling the PGA offers a dual advantage of reducing overall power consumption and relaxing the constraints outlined in Equations 12 to 14 related to the common mode input voltage range (V_{CM}). With the PGA turned off, the valid range for both absolute and common mode input voltage is (AVSS - 0.1V ≤ V_{AINx}, V_{CM} ≤ AVDD + 0.1V).

When measuring single-ended signals referenced to AVSS (where AIN_P = V_{IN} and AIN_N = AVSS), bypassing the PGA is necessary. The device allows the configuration of single-ended measurements either by externally connecting one of the analog inputs to AVSS or by utilizing the internal AVSS connection provided by the multiplexer (achieved through MUX[3:0] settings 1000 to 1011). It is important to note that when the internal multiplexer is set to configurations where AIN_N = AVSS (specifically, MUX[3:0] = 1000 to 1011), the PGA is automatically bypassed and disabled, irrespective of the PGA_BYPASS setting. Additionally, when the gain is set to values greater than 4, the device limits the gain to a maximum of 4.

DETAILED DESCRIPTION (continued)

Modulator

Within the SGM58201, a sophisticated Σ-Δ modulator is employed to convert the analog input voltage into a pulse code modulated (PCM) data stream. The modulator operates at a clock frequency called f_{MOD}, which is set to $f_{CLK}/16$ in both normal and duty-cycle modes. In turbo mode, the clock frequency increases to $f_{MOD} = f_{CLK}/8$. The modulator's clock source, f_{CLK}, can be derived from either the internal oscillator or an external clock input. Table 10 provides a detailed breakdown of modulator frequencies for each operational mode, depending on whether the internal oscillator or an external clock source with a frequency of 4.096MHz is used.

Table 10. Modulator Clock Frequency for Different Operating Modes (1)

Operating Mode	f_{MOD}
Duty-cycle mode	256kHz
Normal mode	256kHz
Turbo mode	512kHz

NOTE:

1. Using the internal oscillator or an external 4.096MHz clock.

Digital Filter

The SGM58201 features a finite impulse response (FIR) digital filter with linear-phase characteristics. This filter serves a dual purpose, filtering and decimating the incoming digital data stream from the modulator. Notably, the digital filter automatically adapts to different data rates, ensuring a settling process within a single-cycle. Operating at data rates of 5SPS and 20SPS, the filter configuration provides flexibility to reject either 50Hz or 60Hz line frequencies, or both simultaneously. Two bits (50/60[1:0]) in the configuration register enable easy customization of the filter's behavior. The frequency responses of the digital filter across various output data rates are thoroughly detailed for scenarios involving the internal oscillator or an external 4.096MHz clock, as shown in Figure 11 to Figure 24.

The notching characteristics of the filter and the scaling of output data rates are directly proportional to the clock frequency. For example, a notch that appears at 20Hz with a 4.096MHz clock will shift to 10Hz with a 2.048MHz clock. It is important to note that the internal oscillator is subject to temperature-induced variations, detailed in the ELECTRICAL CHARACTERISTICS table. As a result, the data rate and conversion time vary with these oscillation fluctuations. For applications that require stricter tolerance for a digital filter notch at a specific frequency, considering an external precision clock source is advisable.

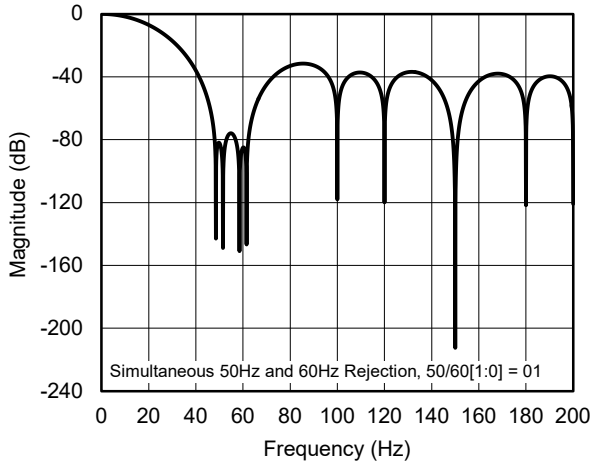


Figure 11. Filter Response (DR = 20SPS)

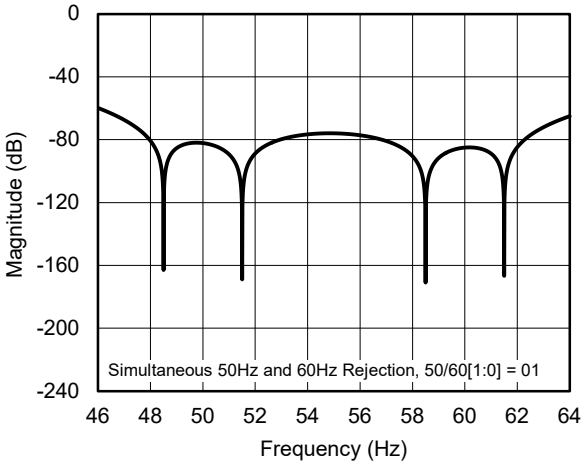


Figure 12. Detailed View of Filter Response (DR = 20SPS)

DETAILED DESCRIPTION (continued)

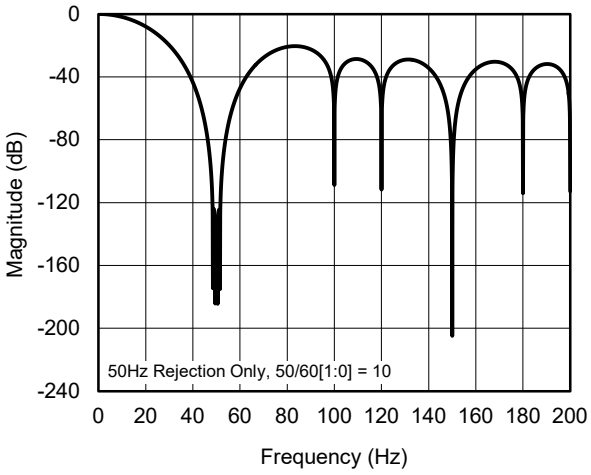


Figure 13. Filter Response (DR = 20SPS)

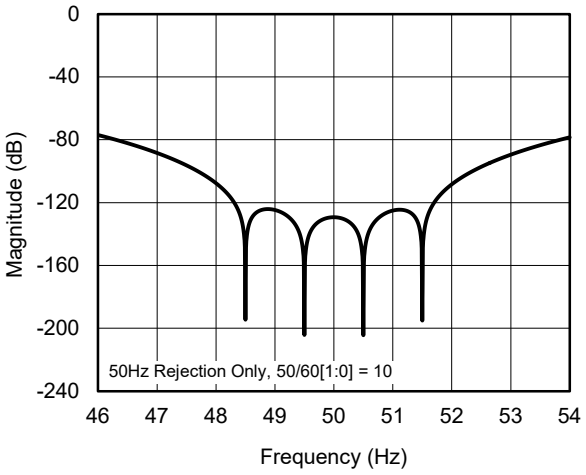


Figure 14. Detailed View of Filter Response (DR = 20SPS)

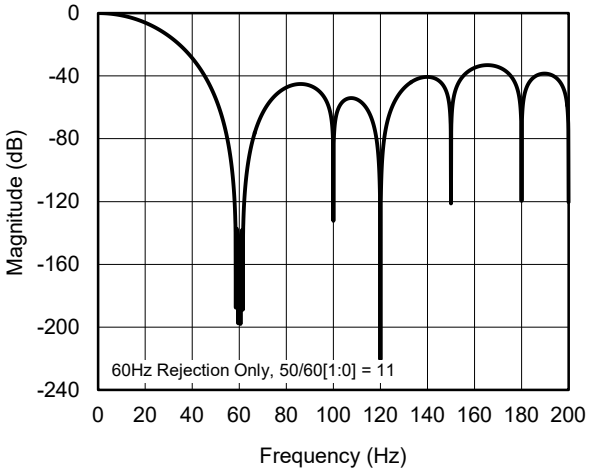


Figure 15. Filter Response (DR = 20SPS)

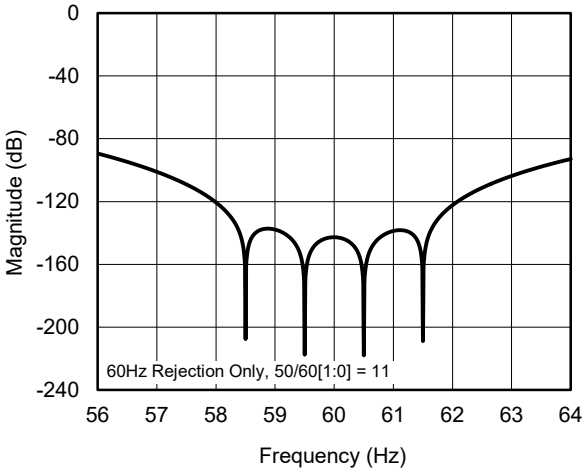


Figure 16. Detailed View of Filter Response (DR = 20SPS)

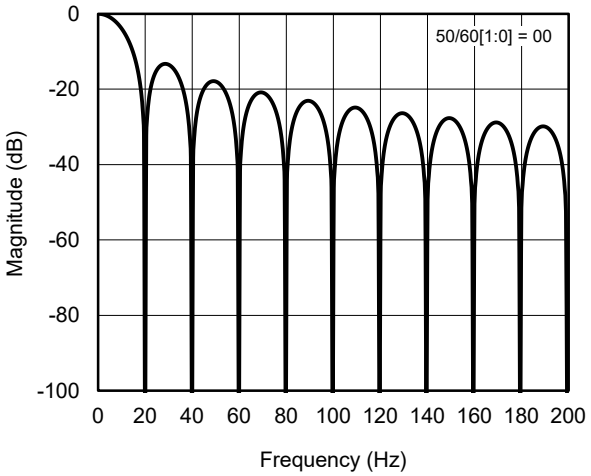


Figure 17. Filter Response (DR = 20SPS)

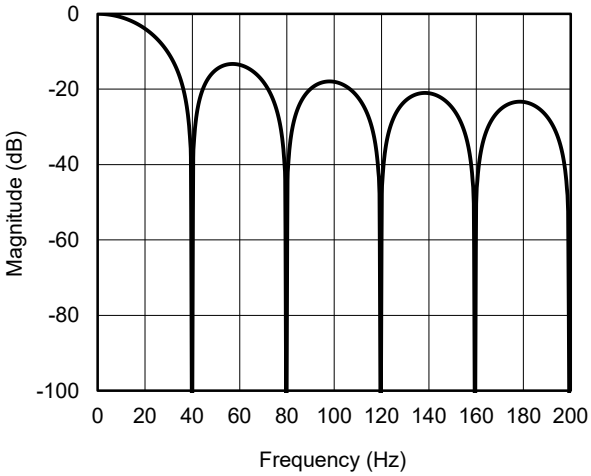


Figure 18. Filter Response (DR = 40SPS)

DETAILED DESCRIPTION (continued)

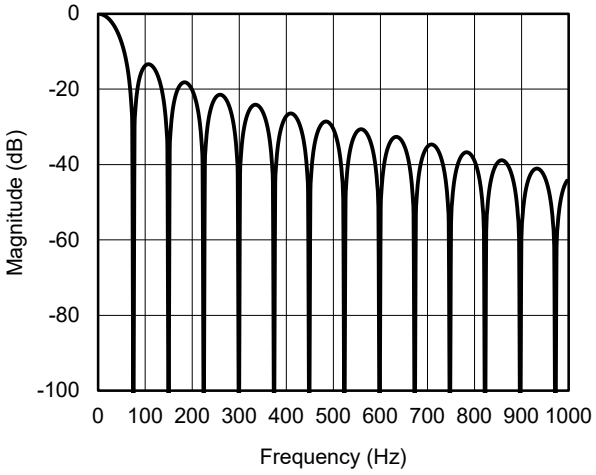


Figure 19. Filter Response (DR = 75SPS)

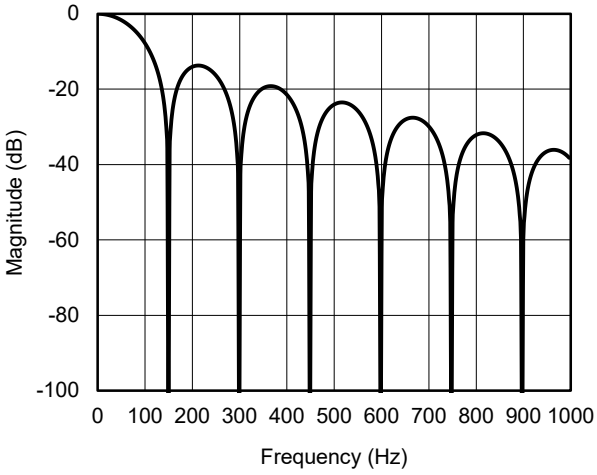


Figure 20. Filter Response (DR = 150SPS)

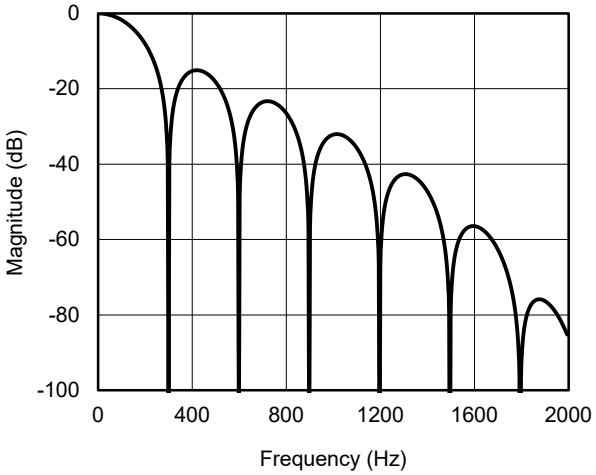


Figure 21. Filter Response (DR = 300SPS)

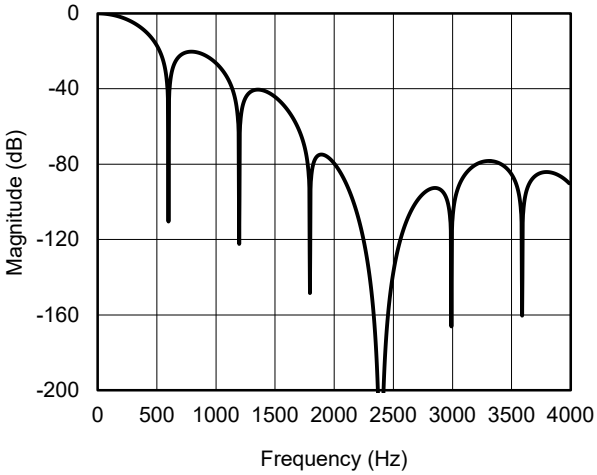


Figure 22. Filter Response (DR = 600SPS)

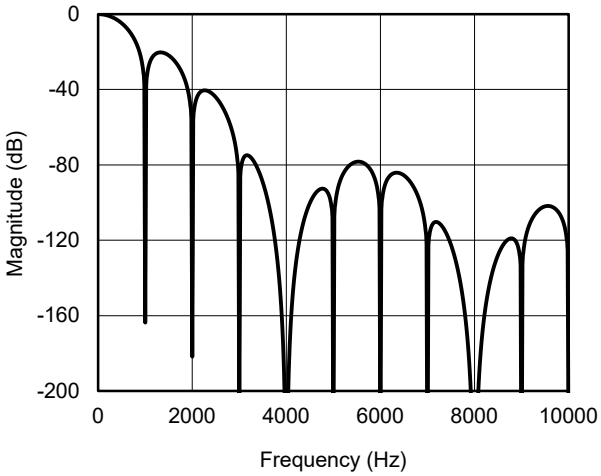


Figure 23. Filter Response (DR = 1kSPS)

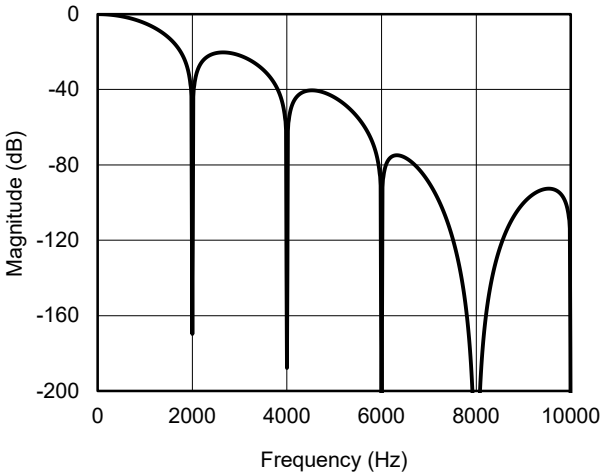


Figure 24. Filter Response (DR = 2kSPS)

DETAILED DESCRIPTION (continued)

Output Data Rate

The effective conversion times for each specified data rate configuration are shown in Table 11, expressed in terms of t_{CLK} cycles, assuming an external clock with a frequency of f_{CLK} = 4.096MHz.

In continuous conversion mode, the data rate sequence is measured from one falling edge of nDRDY to the next nDRDY falling edge. The first conversion begins either 210 • t_{CLK} cycles (normal mode, duty-cycle mode) or 114 • t_{CLK} cycles (turbo mode) after the final SCLK falling edge of the START/SYNC command.

For single-shot mode, the data rate sequence is measured from the last SCLK falling edge of the START/SYNC command to the upcoming nDRDY falling edge, rounded up to the next t_{CLK} cycle. If the internal oscillator is in use, an additional time is needed to accommodate the oscillator's wake-up period, which can be up to 50μs (normal mode, duty-cycle mode) or 25μs (turbo mode) in single-shot mode. The wake-up process of the internal oscillator starts with the initial SCLK rising edge of the START/SYNC command. If the SCLK frequency exceeds 160kHz (normal mode, duty-cycle mode) or 320kHz (turbo mode), there is a chance that the internal oscillator may not be fully operational by the end of the START/SYNC command. In such cases, the ADC waits for the internal oscillator to fully power up before initiating a conversion.

It is important to note that while the conversion time for the 20SPS setting is not precisely equal to 1/20Hz = 50ms, this deviation does not apply any influence on the specified 50Hz or 60Hz rejection performance. For the accomplishment of the specified 50Hz and 60Hz rejection levels listed in the Electrical Characteristics table, a requisite condition necessitates the external clock frequency to be set at 4.096MHz. Conversely, in scenarios where the internal oscillator is utilized, the conversion time and filter notching characteristics exhibit variations corresponding to the figures detailed in the Electrical Characteristics table, accounting for oscillator accuracy considerations.

Table 11. Conversion Times

Nominal Data Rate (SPS)	-3dB Bandwidth (Hz)	Actual Conversion Time (t_{CLK})	
		Continuous Conversion Mode	Single-Shot Mode
Normal Mode			
20	8.8	205439	206262
40	17.6	102719	103543
75	33	54784	55607
150	66	27390	28217
300	130	13693	14516
600	240	6824	7696
1000	400	4071	4944
Duty-Cycle Mode			
5	8.8	819597	206262
10	17.6	409887	103543
18.75	33	218735	55607
37.5	66	109519	28213
75	130	54895	14520
150	240	27591	7696
250	400	16663	4944
Turbo Mode			
40	17.6	102719	103166
80	35.2	51360	51806
150	66	27390	27841
300	132	13693	14143
600	260	6849	7295
1200	480	3412	3883
2000	800	2036	2507

DETAILED DESCRIPTION (continued)

Voltage Reference

The SGM58201 incorporates a built-in 2.048V reference with excellent stability over time. However, for scenarios requiring alternative reference voltage values or an approach centered on ratiometric measurements, the device introduces two sets of differential reference inputs—REFP0, REFN0, and REFP1, REFN1. Furthermore, the analog supply (AVDD) serves as an additional option for reference.

The mechanism for reference selection involves two essential bits (VREF[1:0]) in the configuration register, where the internal reference is the default. Quickly settling within 25μs post-power-up, exit from power-down mode, or transition from an external reference source to the internal reference is smoothly facilitated.

The availability of differential reference inputs introduces a novel layer of flexibility in terms of the reference's common mode voltage. REFP0 and REFN0 are especially dedicated reference inputs, while REFP1 and REFN1 serve a dual purpose by being concurrently associated with inputs AIN0 and AIN3, respectively. These reference inputs undergo internal buffering, bolstering their input impedance. This essentially alleviates the necessity for supplementary reference buffers when an external reference is employed. In scenarios characterized by ratiometric applications, the reference inputs manifest negligible load on the external circuitry. It is prudent to acknowledge that when employing an external reference, there is a corresponding uptick in the analog supply current owing to the activation of reference buffers.

In most cases, the conversion outcome stands in direct correlation with the steadiness exhibited by the chosen reference source. Any fluctuations in noise or drift within the voltage reference are aptly mirrored in the final conversion result.

Clock Source

For the fundamental timekeeping, an internal low-drift oscillator stands ready, ever reliable. Alternatively, an external clock source can take on this role, entering through the CLK input. Before initiating power or reset, the CLK pin should be connected to DGND to keep internal oscillator active. If it is decided that an external clock with the CLK pin is to be used, note that the internal oscillator will smoothly transition down after detecting two consecutive rising edges. From that moment, the device synchronizes with the external clock. To restore the internal oscillator's operation, either cycle the power supply or issue a RESET command.

Excitation Current Sources

Embedded in this device are two highly adaptable excitation current sources (IDACs), meticulously designed for RTD applications. These sources can be precisely adjusted to produce currents of 10μA, 50μA, 100μA, 250μA, 500μA, 1000μA, or 1500μA. The intricate dance of these currents is controlled by manipulating specific bits (IDAC[2:0]) in the configuration register. This precision dance enables effortless connection of each current source to either analog inputs (AIN_x) or the esteemed reference inputs (REFP0 and REFN0), with the possibility of using a shared pin for both sources. The path of the current is skillfully guided by a sophisticated routing configuration, orchestrated by bits (I1MUX[2:0], I2MUX[2:0]) within the configuration register.

A vigilant guardian is crucial to prevent exceeding the compliance voltage of these IDACs. If the voltage on the selected path exceeds ≤ (AVDD - 0.9V), the revered accuracy of the IDAC current diminishes. This strategic safeguard finds its purpose in 3-wire RTD scenarios, where the synchronized collaboration of these paired current sources mitigates the impact of sensor lead resistance. This harmonious interplay is demonstrated in the 3-wire RTD measurement segment, revealing a symphony in action.

At the beginning, the IDACs need a brief 200μs to wake up gracefully after their designated currents are set using the IDAC[2:0] bits. If configuring registers 2 and 3 separately with the WREG command, it is advised to start the process by setting the IDAC current using IDAC[2:0] before selecting the routing options, delicately defined through I1MUX[2:0] and I2MUX[2:0] choices.

In single-shot operating mode, the IDACs remains active between successive conversions, as long as the IDAC[2:0] configuration bits are set to a value other than 000. They deactivate when the POWERDOWN command is executed.

It is essential to note that enabling the IDACs (especially by setting IDAC[2:0] bits to a non-000 value) increases the analog supply current. This bias current is necessary for the IDAC circuitry to work, even if the IDACs are not connected to any external pins (both I1MUX[2:0] and I2MUX[2:0] are set to 000). Additionally, the chosen output current is drawn from the analog supply when I1MUX[2:0] or I2MUX[2:0] are configured to a value other than 000.

DETAILED DESCRIPTION (continued)

Low-side Power Switch

The SGM58201 features a low-side power switch with minimal on-resistance to connect analog input AIN3/REFN1 to AVSS.

This built-in power switch plays a crucial role in reducing overall system power consumption, especially in bridge sensor applications. It achieves this by allowing the bridge circuit to power down between conversions. Activation of the power switch is controlled by the dedicated PSW bit in the configuration register. Enabling this bit causes the power switch to automatically engage with the START/SYNC command and disengage with the POWERDOWN command.

In the single-shot operational mode, setting the PSW bit to 1 keeps the power switch closed throughout conversion cycles. To interrupt this, the power switch can be opened at any point by resetting the PSW bit to 0. It is important to note that the power switch defaults to the open position.

Sensor Detection

To aid in identifying potential sensor issues, the device includes internal burn-out current sources, each providing 10μA. These sources are activated by the dedicated bit (BCS) in the configuration register and help detect faults. One source directs current to the selected positive analog input (AIN_P), while the other draws current from the chosen negative analog input (AIN_N).

With an open sensor circuit, these burn-out current sources pull the positive input toward AVDD and the negative input toward AVSS, resulting in a full-scale reading. However, note that a full-scale reading may indicate sensor overload or a lack of reference voltage. Conversely, a reading near zero may suggest a shorted sensor. The ±10% variation in the magnitude of burn-out current sources and a small series resistance introduced by the internal multiplexer add complexity. This makes distinguishing between a shorted sensor and a normal reading challenging, especially with input RC filters. Even if the sensor is shorted, the voltage drops across the external filter resistance, combined with the remaining multiplexer resistance, yields an output higher than zero.

It is crucial to recognize that enabling burn-out current sources may corrupt ADC readings from a functioning sensor. Therefore, it is recommended to deactivate these sources during precision measurements. They should be exclusively enabled for assessing potential sensor faults.

System Monitor

The device includes features for monitoring both the analog power supply and an external voltage reference. To specify the observed voltage, set the internal multiplexer (MUX[3:0]) accordingly in the configuration register. When using the monitoring feature, the device bypasses the programmable gain amplifier (PGA) and automatically sets the gain to 1, overriding other settings in the configuration register. However, it is crucial to note that the system monitoring function is intended for rough measurements and should not be relied upon for precise readings.

When the analog power supply is measured (MUX[3:0] bits are set to 1101), the conversion result is approximately (AVDD - AVSS)/4. Notably, for this measurement, the device uses the internal 2.048V reference, regardless of the chosen reference source in the configuration register (VREF[1:0]).

Alternatively, when monitoring an external reference voltage source (MUX[3:0] bits are set to 1100), the outcome is roughly (REFPx - REFNx)/4, where REFPx and REFNx are the pair of external reference inputs designated in the configuration register (VREF[1:0]). For this measurement, the device automatically utilizes the internal reference.

It is crucial to emphasize that these monitoring functions provide only approximate results, and their primary purpose is not to deliver high-precision measurements.

Offset Calibration

The internal multiplexer allows connecting both inputs of the programmable gain amplifier (PGA), AIN_P and AIN_N, to the mid-supply voltage point, (AVDD + AVSS)/2. This setup is beneficial for measuring and calibrating the device's offset voltage. To achieve this, record the voltage reading from the shorted inputs with a microcontroller, enabling subsequent correction of readings. It is recommended to take multiple readings with the shorted inputs and calculate the average to effectively minimize the influence of ambient noise on the readings.

DETAILED DESCRIPTION (continued)

Temperature Sensor

The SGM58201 features a highly precise integrated temperature sensor. To activate the temperature sensor mode, set TS bit to 1 in the configuration register. Once in this mode, changes to configuration register 0 have no effect. Regardless of the chosen voltage reference source, the device uses its internal reference for measurements. The process for obtaining temperature readings is similar to that of analog inputs, involving the initiation of conversions and extraction of results.

The temperature data is presented as a 14-bit output, occupying the higher-order positions within the 24-bit conversion outcome. The data stream starts with the most significant byte (MSB). In the three data bytes, the initial 14 bits contain the temperature measurement outcome. Each least significant bit (LSB) within the 14 bits corresponds to a temperature increment of 0.03125℃. Following the binary two's complement format, negative values are represented, as detailed in Table 12.

Table 12. 14-Bit Temperature Data Format

Temperature (℃)	Digital Output (Binary)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
-0.25	11 1111 1111 1000	3FF8
-25	11 1100 1110 0000	3CE0
-40	11 1011 0000 0000	3B00

Converting from Temperature to Digital Codes

For Positive Temperatures (for Example, 50℃):

For positive numbers, there is no need for the application of two's complement. The process involves a direct conversion to binary code in a 14-bit, left-justified format. Positivity is indicated by setting the most significant bit (MSB) to 0.

Example: 50℃/(0.03125℃ per count) = 1600 = 0640h = 00 0110 0100 0000.

For Negative Temperatures (for Example, -25℃):

To represent a negative number with two's complement, invert the absolute binary value and add 1. After this operation, denote the negative nature of the number by setting the most significant bit (MSB) to 1.

Example: |-25℃|/(0.03125℃ per count) = 800 = 0320h = 00 0011 0010 0000.
Two's complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000.

Converting from Digital Codes to Temperature

When translating digital codes into temperature values, the initial step involves examining the most significant bit (MSB) to determine if it is 0 or 1. If the MSB is 0, the process straightforwardly multiplies the decimal code by 0.03125℃, providing the temperature result directly. On the other hand, if the MSB is 1, a more complex protocol is initiated. Begin by subtracting 1 from the numerical outcome and then perform a bit-wise complement across all bits. This prepares for the final step: multiplying the resulting value by -0.03125℃, ultimately providing the accurate temperature measurement.

Example: The device reads back 0960h: 0960h has an MSB = 0.
0960h · 0.03125℃ = 2400 · 0.03125℃ = 75℃

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.
Subtract 1 and complement the result: 3CE0h → 0320h
0320h · (-0.03125℃) = 800 · (-0.03125℃) = -25℃

Device Functional Modes

Power-Up and Reset

Upon device initialization, an automatic reset sequence begins, completing in approximately 50 microseconds. After this power-up reset, all internal circuit components, including the voltage reference, stabilize, setting the stage for smooth device communication. A vital part of this reset mechanism is resetting all bits in the configuration registers to their default values.

Out of the box, the device is configured in single-shot mode as the default setting. After power-up, the device performs an individual conversion cycle based on the default register values. Afterward, it enters a state of low-power operation. When the conversion process finishes, the nDRDY pin transitions from a high logic level to a low logic level, indicating that the SGM58201 is ready for operation.

The orchestrated behavior during power-up is carefully designed to prevent scenarios with strict power-supply requirements from experiencing undesirable current surges upon power initialization.

DETAILED DESCRIPTION (continued)

Conversion Modes

In terms of operational options, the device offers a split into two distinct conversion modes, accessible by adjusting the CM bit in the configuration register. These modes are single-shot and continuous conversion modes, each presenting a unique operational approach.

Single-Shot Mode

In single-shot mode, the device exclusively engages in conversion activities when prompted by a START/SYNC command. As a result, a single conversion operation occurs, followed by an automatic transition into a low-power operational state. In this energy-efficient state, the internal oscillator, and the entire analog circuitry (excluding the excitation current sources) enter a quiescent state. The device remains in this low-power mode, ready for the initiation of the next conversion event.

Furthermore, any write operation directed at a configuration register can be served as the start of a new conversion cycle. While a conversion is in progress, performing a write action on any configuration register is analogous to initiating a new START/SYNC command. This action effectively stops the ongoing conversion process and triggers the start of a new single conversion sequence.

Each conversion cycle, naturally synchronized with the input signal's final stabilization before conversion initiation, is equipped with full settling attributes. This rapid settling behavior is attributed to the device's digital filter, which achieves stability within a single-cycle, ensuring accurate and precise conversions.

Continuous Conversion Mode

In continuous conversion mode, the device engages in an uninterrupted series of conversion operations. After completing a conversion cycle, the device promptly places the resulting output into the designated buffer and seamlessly initiates another conversion sequence.

The start of continuous conversion mode follows a systematic procedure: it begins by setting the CM bit to 1, followed immediately by issuing a START/SYNC command. This orchestrated process acts as the trigger, propelling the device into a continuous series of conversions. The first conversion in this mode starts 210 • t_{CLK} units of time after the final falling edge of the START/SYNC command, where t_{CLK} represents the clock period. In normal mode or duty-cycle mode, this interval extends to 210 • t_{CLK}, while in turbo mode, a more accelerated timeframe of 114 • t_{CLK} is used.

It is crucial to emphasize that writing to any configuration register while an ongoing conversion is in progress instantly restarts the current conversion sequence. To ensure optimal performance, it is highly recommended to promptly issue a START/SYNC command immediately after setting the CM bit to 1, a practice endorsed to streamline operational efficiency.

Operating Modes

In addition to the different conversion modes, the device provides a range of operating modes to strike a balance between power consumption, noise performance, and output data rate. These operating modes include: normal mode, duty-cycle mode, turbo mode, and power-down mode.

Normal Mode

The default operational state upon power-up is known as "normal mode." In this mode, the internal modulator of the Σ-Δ ADC operates at a modulator clock frequency, denoted as $f_{MOD} = f_{CLK}/16$, where the system clock (f_{CLK}) can come from either the internal oscillator or an external clock input. When using the internal oscillator, the modulator frequency is set at 256kHz. In the context of the internal oscillator, normal mode offers a range of output data rate choices from 20SPS to 1kSPS, determined by the configuration register's DR[2:0] bits.

In cases where an external clock with a frequency different from 4.096MHz is employed, the data rates undergo proportional adjustments. For instance, using an external clock of f_{CLK} = 2.048MHz results in data rate options ranging from 10SPS to 500SPS.

Duty-Cycle Mode

When the output data rate is decreased, the noise characteristics of a Σ-Δ ADC show improvement because a greater number of samples from the internal modulator can be averaged to produce a single conversion outcome. However, in situations where power consumption is crucial and heightened noise performance at lower data rates is not necessary, the device introduces an automated duty-cycle mode. This mode conserves power by cyclically transitioning into a low-power state between conversions.

Fundamentally, the device operates in normal mode with a designated duty-cycle of 25%. This means that the device performs a conversion sequence similar to its normal mode operation, followed by an automatic entry into a low-power state for three consecutive conversion cycles. As a result, the noise performance in duty-cycle mode is equivalent to the noise performance in normal mode at four times the data rate. The achievable data rates in duty-cycle mode range from 5SPS to 250SPS when using the internal oscillator.

DETAILED DESCRIPTION (continued)

Turbo Mode

For applications requiring high data rates of up to 2kSPS, the device provides the option to operate in turbo mode. In this mode, the internal modulator operates at an increased frequency, denoted as $f_{MOD} = f_{CLK}/8$. When using either the internal oscillator or an external clock set at 4.096MHz, f_{MOD} is equal to 512kHz. It is essential to note that activating turbo mode results in higher device power consumption due to the elevated modulator frequency. When the SGM58201 is used in turbo mode, the output data rate is comparable to that in normal mode, resulting in superior noise performance. For example, at a data rate of 90SPS, the input-referred noise in turbo mode is lower than the input-referred noise at the same data rate in normal mode.

Power-Down Mode

When the POWERDOWN command is initiated, the device smoothly transitions into power-down mode after completing the ongoing conversion process. In this mode, all analog circuitry, including the voltage reference and both IDACs, is effectively deactivated. Additionally, the low-side power switch is disengaged, resulting in a mere 400nA of average current consumption. While in power-down mode, the device retains the established configuration register settings and remains responsive to commands. However, it refrains from executing any data conversion procedures.

Activating a START/SYNC command wakes the device from its low-power state. Depending on the conversion mode designated by the CM bit, this command either initializes a single conversion or initiates continuous conversion mode. Importantly, any modification to a configuration register not only awakens the device but also triggers a single conversion event, regardless of the chosen conversion mode (CM).

Programming

Serial Interface

The SGM58201 features an SPI-compatible serial interface with versatile functions such as retrieving conversion data, adjusting device configuration, and managing device operations. This interface operates exclusively in SPI mode 1 (CPOL = 0, CPHA = 1) and includes five control lines (nCS, SCLK, DIN, DOUT/nDRDY, and nDRDY). However, efficient operation is possible with just four or even three control signals. The dedicated nDRDY signal, indicating data readiness, can be shared with DOUT/nDRDY. When the serial bus is exclusively dedicated to this device, connecting nCS to low permanently reduces the essential signals to just three: SCLK, DIN, and DOUT/nDRDY, simplifying communication with the device.

Chip Select (nCS)

The chip select (nCS) feature acts as an active-low input, serving as a key entry point for initiating SPI communication in situations where multiple devices share the serial bus. It is essential to keep the nCS signal low throughout the entire SPI communication process. Transitioning nCS to a high state triggers a reset mechanism, causing SCLK to be ignored and putting DOUT/nDRDY in a high-impedance state. This results in the loss of DOUT/nDRDY's ability to signal data availability. In cases where multiple devices share the bus, the dedicated nDRDY pin ensures consistent monitoring of conversion status. If the serial bus is exclusively dedicated to this peripheral, keeping nCS perpetually low simplifies communication requirements.

Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input mechanism and plays a crucial role in coordinating the flow of data through the DIN and DOUT/nDRDY pins. The input incorporates hysteresis, but it is essential to ensure a clean SCLK signal to prevent unintended data shifts caused by glitches. It is recommended to keep SCLK low during periods of inactivity in the serial interface.

Data Ready (nDRDY)

The nDRDY signal indicates the availability of recently converted data for retrieval. When nDRDY goes low, it signals the readiness of new conversion data. It returns to a high state with the rising edge of the SCLK signal. In continuous conversion mode, when no data retrieval occurs, nDRDY stays low. However, it briefly goes high for a duration of $2 \cdot t_{MOD}$ before descending again. Importantly, the nDRDY pin remains actively driven even when nCS is high.

Data Input (DIN)

The data input pin (DIN) works with SCLK to send data to the device, including commands and register data. The device captures data from DIN on the falling edge of SCLK. Importantly, the device remains passive with respect to the DIN pin and does not actively affect its signal state.

DETAILED DESCRIPTION (continued)

Data Output and Data Ready (DOUT/nDRDY)

The DOUT/nDRDY pin serves a dual function. Paired with SCLK, it aids in retrieving both conversion and register data from the device, with data shifting out during the rising edge of SCLK. The state of DOUT/nDRDY turns to high-impedance when nCS is set to high.

Moreover, by setting the DRDYM bit to high in the configuration register, the DOUT/nDRDY pin can act as a data-ready indicator. Consequently, DOUT/nDRDY goes low simultaneously with nDRDY, signaling the availability of fresh conversion data. Both signals can be used to detect data readiness. However, since DOUT/nDRDY becomes inactive when nCS is high, the recommended approach for monitoring conversion completion, especially in scenarios with multiple devices on the SPI bus, is to use the dedicated nDRDY pin.

SPI Timeout

The SGM58201 introduces an SPI timeout feature, which effectively re-establishes communication after a disruption in the serial interface transmission. This feature is particularly useful when nCS is consistently low and not used as a communication framing signal. If a complete command is not sent within a time window of 13955 • t_{MOD} (in normal or duty-cycle mode) or 27910 • t_{MOD} (in turbo mode), the serial interface resets, and a new communication cycle starts with the subsequent SCLK pulse. Detailed information about the modulator frequency (f_{MOD} = 1/t_{MOD}) in different operational modes is available in the Modulator section. It is important to note that for RREG and WREG commands, a complete command includes the command byte and the register bytes being read or written.

Data Format

The device provides a 24-bit data output arranged in binary two's complement format. The calculation of the size of a single code, specifically the least significant bit (LSB), can be determined using Equation 15:

$$1LSB = (2 \cdot V_{REF}/Gain)/2^{24} = +FS/2^{23} \quad (15)$$

For a positive full-scale input [$V_{IN} \geq$ (+FS - 1LSB) = (V_{REF}/Gain - 1LSB)], the resulting output code is 7FFFFFh. In contrast, a negative full-scale input ($V_{IN} \leq$ -FS = -V_{REF}/Gain) corresponds to an output code of 800000h. These output codes act as clipping points for signals exceeding the full-scale range.

Table 13 provides a complete compilation of the expected output codes for various input signals.

Table 13. Ideal Output Code versus Input Signal

Input Signal, V_{IN} (AIN_P - AIN_N)	Ideal Output Code (1)
≥ FS (2^{23} - 1)/2^{23}	7FFFFFh
FS/2^{23}	000001h
0	000000h
-FS/2^{23}	FFFFFFh
≤ -FS	800000h

NOTE:

1. Except for the effects of noise, INL, offset, and gain errors.

Illustration of the correlation between the analog input signal and the resultant output codes is visually depicted in Figure 25.

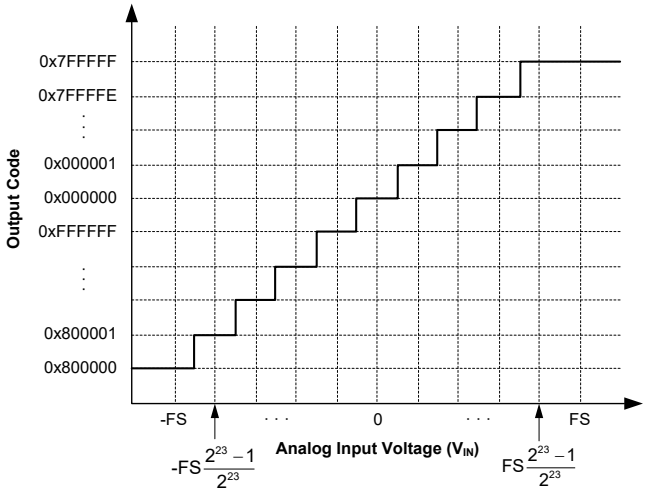


Figure 25. Code Transition Diagram

DETAILED DESCRIPTION (continued)

Commands

The device offers six carefully crafted commands to control its operational functions, detailed in Table 14. Among these, four commands act independently (RESET, START/SYNC, POWERDOWN, and RDATA). In contrast, commands for retrieving (RREG) and modifying (WREG) configuration register data require additional information to be included in the instruction.

RESET (0000 011x)

Triggers a complete restoration of the device to its predefined default settings. It is crucial to wait for a minimum period of (50μs + 32 • t_{CLK}) after sending the RESET command before transmitting any further commands.

START/SYNC (0000 100x)

In single-shot mode, activating the START/SYNC command has a dual purpose. It either initiates a single conversion or, if sent during an ongoing conversion, resets the digital filter, which subsequently triggers the start of a new individual conversion. In continuous conversion mode, a single issuance of the START/SYNC command is necessary to begin an uninterrupted stream of consecutive conversions. If the START/SYNC command is transmitted while the device is in continuous conversion mode, it triggers a dual action: first, resetting the digital filter, and then restarting the ongoing cycle of continuous conversions.

POWERDOWN (0000 001x)

Executing the POWERDOWN command initiates the transition of the device into a power-down mode. This command shuts down all internal analog components, disconnects the low-side switch, and deactivates both IDACs. Meanwhile, all register values are retained. If the POWERDOWN command is executed while a conversion is in progress, the conversion completes before the device enters the power-down sequence. After sending a START/SYNC command, the analog components swiftly return to their previous operational states.

RDATA (0001 xxxx)

The RDATA command loads the output shift register with the latest conversion result. This instruction is useful when the indicators DOUT/nDRDY or nDRDY are not being monitored to signal the availability of a newly obtained conversion result. In cases where a conversion completes during the transmission of the RDATA command byte, the status of the nDRDY pin at the end of the read operation determines whether the previous or the current result is loaded. If the former result is loaded, the nDRDY signal stays low, indicating that the recent result is unprocessed. Conversely, the new conversion result is loaded when nDRDY goes high.

RREG (0010 rrnn)

The RREG command is used to retrieve a specified number of bytes, indicated by nn (where nn + 1 represents the total number of bytes to be read), from the device configuration register. This retrieval operation starts from the register address rr. The command execution completes when nn + 1 bytes are successfully clocked out after transmitting the RREG command byte. For example, requesting three bytes of data (with nn = 10) from configuration register 1 (with rr = 01) corresponds to the command sequence 0010 0110.

WREG (0100 rrnn)

The WREG command is used to write a specified number of bytes, indicated by nn (where nn + 1 represents the total number of bytes to be written), into the device configuration register. This writing process begins from the register address rr. The completion of this command occurs when nn + 1 bytes are successfully clocked in after transmitting the WREG command byte. For example, the instruction to write two bytes of data (where nn = 01) starting from configuration register 0 (where rr = 00) corresponds to the command sequence 0100 0001. Importantly, updates to the configuration registers occur on the final falling edge of the SCLK signal.

Table 14. Command Definitions

Command	Description	Command Byte (1)
RESET	Reset the device	0000 011x
START/SYNC	Start or restart conversions	0000 100x
POWERDOWN	Enter power-down mode	0000 001x
RDATA	Read data by command	0001 xxxx
RREG	Read nn registers starting at address rr	0010 rrnn
WREG	Write nn registers starting at address rr	0100 rrnn

NOTE:

1. x = don't care, rr = configuration register (00 to 11), nn = number of bytes - 1 (00 to 11).

DETAILED DESCRIPTION (continued)

Reading Data

When the new data is ready for retrieval, the nDRDY and DOUT/nDRDY output pins transition to a low state. This change signals the availability of new conversion data, which is then carefully written into an internal data buffer. Direct access to this buffer's contents is possible through DOUT/nDRDY when nDRDY is low, avoiding concerns about compromising data integrity. In this context, sending an RDATA command is unnecessary. Data transmission occurs during the rising edges of the SCLK signal, starting with the most significant bit (MSB) and covering three bytes of data.

For a detailed representation of the chronological sequences involved in reading conversion data in both continuous conversion mode and single-shot mode, especially when the RDATA command is not used, refer to Figure 26 through Figure 28.

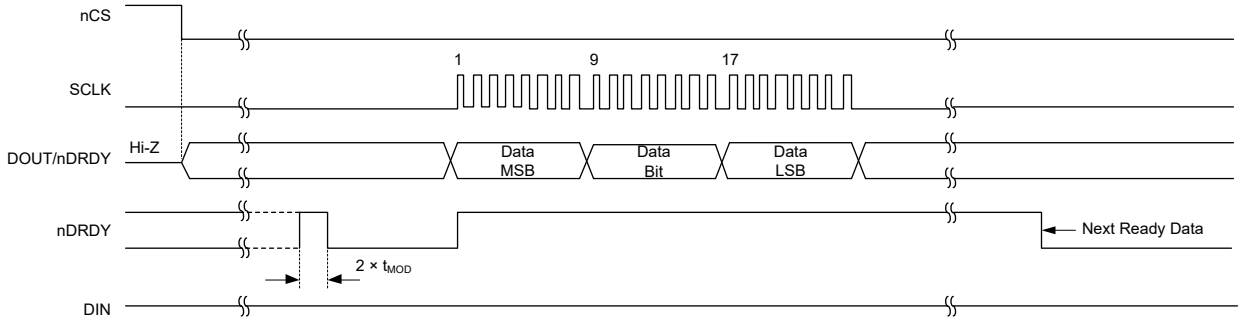


Figure 26. Continuous Conversion Mode (DRDYM = 0)

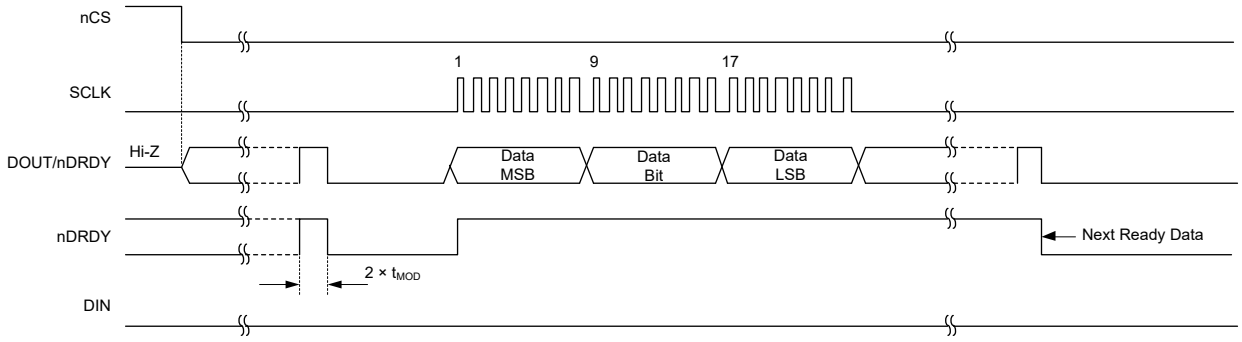


Figure 27. Continuous Conversion Mode (DRDYM = 1)

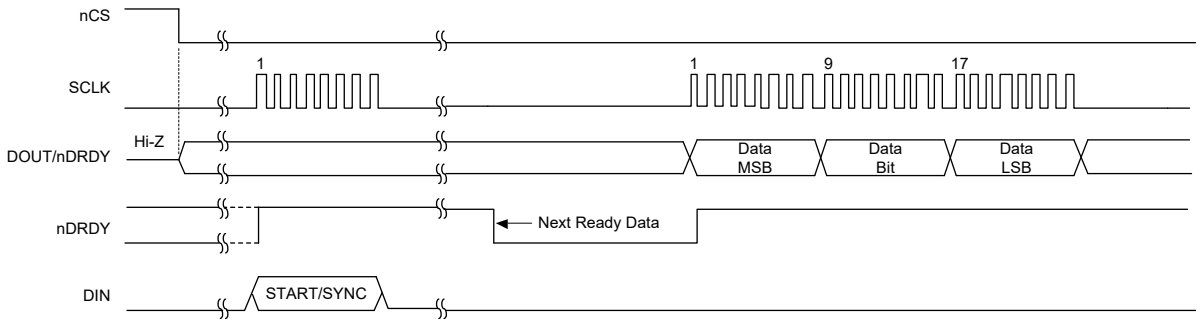


Figure 28. Single-Shot Mode (DRDYM = 0)

DETAILED DESCRIPTION (continued)

Moreover, the process of retrieving data is not limited to synchronization with the nDRDY signal. The use of the RDATA command allows data extraction at any point in time. Upon issuing an RDATA command, the current conversion result in the data buffer undergoes a transmission sequence, effectively being shifted out via DOUT/nDRDY during subsequent rising edges of the SCLK signal. Utilizing the RDATA command enables smooth and continuous data extraction, offering a practical alternative to monitoring nDRDY or DOUT/nDRDY.

The nDRDY pin can be polled after clocking out the least significant bit (LSB) to determine whether a new conversion result has been loaded. In situations where a new conversion concludes while a read operation is ongoing, but data from a previous conversion is being extracted, nDRDY remains low. Conversely, if the most recent result is being retrieved, nDRDY goes high. These two scenarios are clearly explained in Figure 29 and Figure 30.

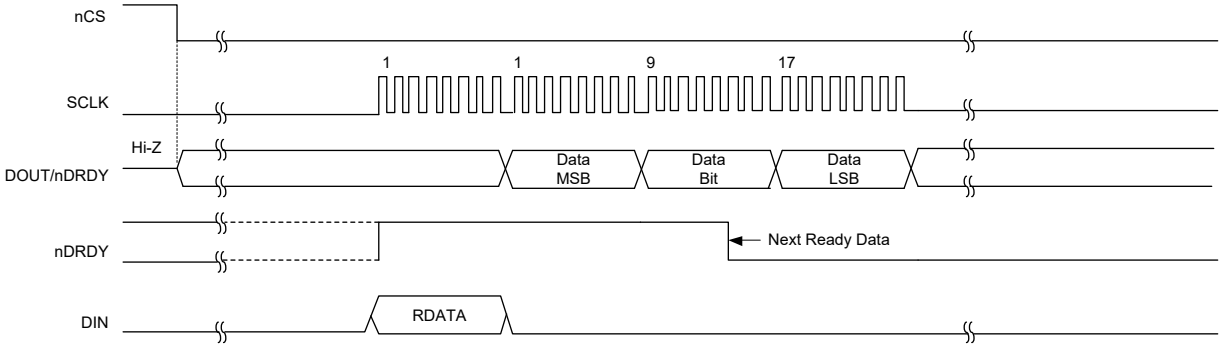


Figure 29. State of nDRDY when a New Conversion Finishes during an RDATA Command

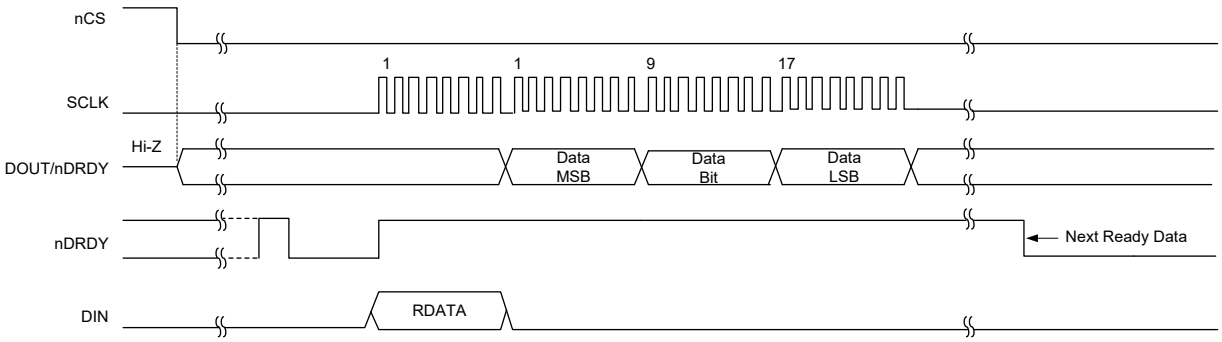


Figure 30. State of nDRDY when the Most Recent Conversion Result is Read during an RDATA Command

DETAILED DESCRIPTION (continued)

Sending Commands

The device's serial interface is designed to support full-duplex operation when reading conversion data, especially when the RDATA command is not used. This means that commands can be decoded simultaneously with the extraction of conversion data. Commands can be sent at any point aligned with an 8-bit data boundary during an ongoing data read operation.

However, a crucial consideration arises when dealing with RREG or RDATA commands. If either of these commands is recognized, the ongoing data read operation is immediately terminated, posing a risk of data corruption. This issue can be avoided if the command is sent precisely when the final byte of the conversion result is being fetched. The device initiates the output of data onto DOUT/nDRDY at the first rising edge of the SCLK signal after the command byte is transmitted. To ensure uninterrupted data reading, it is recommended to keep the DIN signal low while data is being clocked out.

On the other hand, the transmission of a WREG command can be carried out without disrupting an ongoing read operation. An example of this concept is illustrated in Figure 31, showing the concurrent execution of a WREG command to modify two configuration registers while simultaneously reading conversion data in continuous conversion mode. After successfully clocking in the command (following the 32nd falling edge of the SCLK signal), the device resets the digital filter and starts a new conversion cycle using the updated register settings. The WREG command can be dispatched at any of the 8-bit boundaries within the operation.

It is crucial to note that while executing an RDATA or RREG command, the serial interface does not process additional commands. Essentially, after issuing an RDATA command, all 24 bits of the conversion result must be read before initiating another command. Similarly, after transmitting an RREG command, all the requested registers must be read entirely before starting a new command.

Interfacing with Multiple Devices

When connecting multiple SGM58201 devices through a shared SPI bus, a prudent approach is to use a dedicated chip-select (nCS) line for each device, allowing shared use of SCLK, DIN, and DOUT/nDRDY. When nCS transitions to a high state for a specific device, the DOUT/nDRDY line enters a 3-state mode. As a result, DOUT/nDRDY stops indicating new data availability if nCS is held high, regardless of the DRDYM bit configuration. In this case, the reliable indicator of new data availability is the dedicated nDRDY pin, which remains active even when nCS is high.

However, there may be situations where connecting the nDRDY pin to the microcontroller is impractical. This can occur when the microcontroller lacks the necessary GPIO channels or when galvanic isolation in the serial interface limits available channels. In such cases, checking for new conversions can be done by periodically lowering nCS to the relevant device and then polling the status of the DOUT/nDRDY pin. When nCS drops, DOUT/nDRDY immediately goes high or low, depending on the DRDYM bit configuration set to 1. A low state of DOUT/nDRDY when nCS drops indicates fresh data availability, while a high state indicates no new data. For this approach to work effectively, it is crucial to ensure that DOUT/nDRDY is driven high after reading each conversion result and before raising nCS. To achieve this, send 8 extra SCLKs with DIN held low after each data read operation. During this phase, DOUT/nDRDY assumes a high state, as shown in Figure 32. Alternatively, the RDATA command can be used to retrieve valid data from the device at any time without concerns about data integrity.

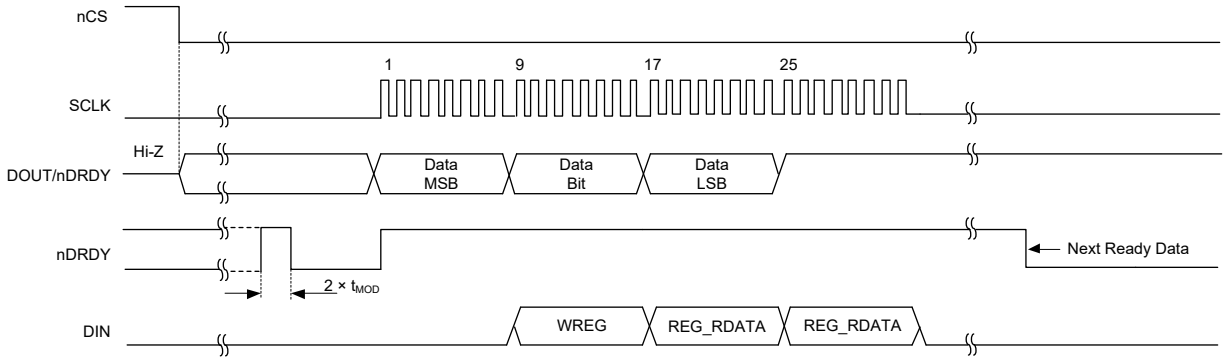


Figure 31. Example for Reading Data while Simultaneously Sending a WREG Command

DETAILED DESCRIPTION (continued)

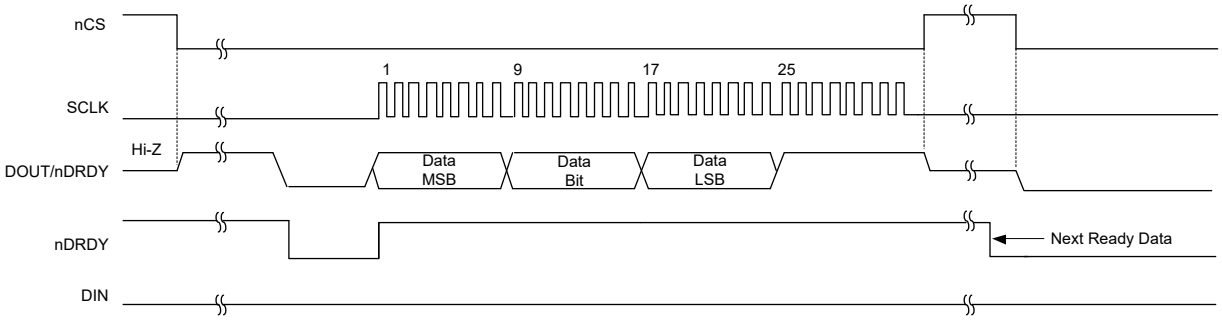


Figure 32. Example for Taking DOUT/nDRDY High after Reading a Conversion Result

REGISTER MAPS

Configuration Registers

The device includes four 8-bit configuration registers, accessible through the serial interface using the RREG and WREG commands. These configuration registers control the operational behavior of the device and can be modified dynamically without causing any data corruption. After power-up or a reset, all registers are automatically restored to predetermined values, and each register is initialized to zero. Importantly, these register values persist even during power-down mode. A detailed breakdown of the configuration registers and their corresponding mapping is carefully presented in Table 15.

Table 15. Configuration Register Maps

Register (Hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	MUX[3:0]				GAIN[2:0]			PGA_BYPASS
0x01	DR[2:0]			MODE[1:0]		CM	TS	BCS
0x02	VREF[1:0]		50/60[1:0]		PSW	IDAC[2:0]		
0x03	I1MUX[2:0]			I2MUX[2:0]			DRDYM	0

REGISTER MAPS (continued)

Bit Types:

R: Read only

R/W: Read/Write

REG0x00: Configuration Register 0 [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:4]	MUX[3:0]	0000	R/W	Input Multiplexer Configuration These bits assume the role of configuring the input multiplexer functionality. In scenarios where the AIN_N setting aligns with AVSS, it becomes imperative to deactivate the programmable gain amplifier (PGA) (PGA_BYPASS = 1). Furthermore, within such settings, only the gain values of 1, 2, and 4 are permissible for utilization. 0000 = AIN_P = AIN0, AIN_N = AIN1 (default) 0001 = AIN_P = AIN0, AIN_N = AIN2 0010 = AIN_P = AIN0, AIN_N = AIN3 0011 = AIN_P = AIN1, AIN_N = AIN2 0100 = AIN_P = AIN1, AIN_N = AIN3 0101 = AIN_P = AIN2, AIN_N = AIN3 0110 = AIN_P = AIN1, AIN_N = AIN0 0111 = AIN_P = AIN3, AIN_N = AIN2 1000 = AIN_P = AIN0, AIN_N = AVSS 1001 = AIN_P = AIN1, AIN_N = AVSS 1010 = AIN_P = AIN2, AIN_N = AVSS 1011 = AIN_P = AIN3, AIN_N = AVSS 1100 = (V_{REFPx} - V_{REFNx})/4 monitor (PGA bypassed) 1101 = (AVDD - AVSS)/4 monitor (PGA bypassed) 1110 = AIN_P and AIN_N shorted to (AVDD + AVSS)/2 1111 = Reserved
D[3:1]	GAIN[2:0]	000	R/W	Gain Configuration These particular bits are dedicated to the customization of the device's amplification factor. Gains of 1, 2, and 4 can be seamlessly implemented in the absence of the programmable gain amplifier (PGA). In this context, the acquisition of gain is achieved through the utilization of a switched-capacitor arrangement. 000 = Gain = 1 (default) 001 = Gain = 2 010 = Gain = 4 011 = Gain = 8 100 = Gain = 16 101 = Gain = 32 110 = Gain = 64 111 = Gain = 128
D[0]	PGA_BYPASS	0	R/W	Deactivation and Bypass of the Internal Low-Noise Programmable Gain Amplifier (PGA) Deactivating the PGA leads to a reduction in power consumption and permits an extended common mode voltage range (V_{CM}) spanning from AVSS - 0.1V to AVDD + 0.1V. The PGA deactivation is feasible solely for gain settings of 1, 2, and 4. For gain settings ranging from 8 to 128, the PGA remains perpetually enabled, irrespective of the PGA_BYPASS configuration. 0 = PGA enabled (default) 1 = PGA disabled and bypassed

REGISTER MAPS (continued)

REG0x01: Configuration Register 1 [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	DR[2:0]	000	R/W	Data Rate These specific bits exert authority over the data rate configuration, contingent upon the chosen operational mode. For a comprehensive overview of the bit configurations tailored to normal, duty-cycle, and turbo modes, please consult Table 16.
D[4:3]	MODE[1:0]	00	R/W	Operating Mode These bits indicate the operational mode in which the device functions. 00 = Normal mode (256kHz modulator clock) (default) 01 = Duty-cycle mode (internal duty-cycle of 1:4) 10 = Turbo mode (512kHz modulator clock) 11 = Reserved
D[2]	CM	0	R/W	Conversion Mode This particular bit establishes the conversion mode employed by the device. 0 = Single-shot mode (default) 1 = Continuous conversion mode
D[1]	TS	0	R/W	Temperature Sensor Mode Activating this bit initiates the operation of the internal temperature sensor, concurrently transitioning the device into the temperature sensor mode. During the duration of temperature sensor mode, the parameters configured in configuration register 0 exhibits no influence. Instead, the device seamlessly resorts to employing the internal reference for temperature measurements. 0 = Disable temperature sensor (default) 1 = Enable temperature sensor
D[0]	BCS	0	R/W	Burn-Out Current Sources This particular bit governs the operation of the 10μA burn-out current sources. These burn-out current sources are instrumental in detecting sensor malfunctions, including instances of wire breaks and sensor short-circuits. 0 = Current sources off (default) 1 = Current sources on

Table 16. DR Bit Settings (1)

Normal Mode	Duty-Cycle Mode	Turbo Mode
000 = 20SPS	000 = 5SPS	000 = 40SPS
001 = 40SPS	001 = 10SPS	001 = 80SPS
010 = 75SPS	010 = 18.75SPS	010 = 150SPS
011 = 150SPS	011 = 37.5SPS	011 = 300SPS
100 = 300SPS	100 = 75SPS	100 = 600SPS
101 = 600SPS	101 = 150SPS	101 = 1200SPS
110 = 1000SPS	110 = 250SPS	110 = 2000SPS
111 = Reserved	111 = Reserved	111 = Reserved

NOTE:

1. The available data rates are computed based on the utilization of either the internal oscillator or an external 4.096MHz clock source. In the event that an external clock frequency divergent from 4.096MHz is employed, the data rates adapt in direct correlation to the amplitude of the external clock frequency.

REGISTER MAPS (continued)

REG0x02: Configuration Register 2 [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:6]	VREF[1:0]	00	R/W	Voltage Reference Selection These bits serve the purpose of selecting the source for the voltage reference utilized during the conversion process. 00 = Internal 2.048V reference selected (default) 01 = External reference selected using dedicated REFP0 and REFN0 inputs 10 = External reference selected using AIN0/REFP1 and AIN3/REFN1 inputs 11 = Analog supply (AVDD - AVSS) used as reference
D[5:4]	50/60[1:0]	00	R/W	FIR Filter Configuration These specific bits are designated for the customization of filter coefficients dedicated to the internal Finite Impulse Response (FIR) filter. Kindly employ these bits in conjunction with the 20SPS configuration in normal mode and the 5SPS configuration in duty-cycle mode. For all other data rates, ensure these bits are set to 00. 00 = No 50Hz or 60Hz rejection (default) 01 = Simultaneous 50Hz and 60Hz rejection 10 = 50Hz rejection only 11 = 60Hz rejection only
D[3]	PSW	0	R/W	Low-side Power Switch Configuration This specific bit determines the operational characteristics of the low-side switch, which establishes a connection between AIN3/REFN1 and AVSS. 0 = The switch is always open (default) 1 = The switch is automatically turned off when the START/SYNC command is sent, and turned on when the POWERDOWN command is sent
D[2:0]	IDAC[2:0]	000	R/W	IDAC Current Setting These bits establish the excitation current magnitude for both IDAC1 and IDAC2 current sources. 000 = Off (default) 001 = 10μA 010 = 50μA 011 = 100μA 100 = 250μA 101 = 500μA 110 = 1000μA 111 = 1500μA

REGISTER MAPS (continued)

REG0x03: Configuration Register 3 [Reset = 00h]

BITS	BIT NAME	DEFAULT	TYPE	DESCRIPTION
D[7:5]	I1MUX[2:0]	000	R/W	IDAC1 Routing Configuration These bits determine the channel to which IDAC1 is routed. 000 = IDAC1 disabled (default) 001 = IDAC1 is connected to AIN0/REFP1 010 = IDAC1 is connected to AIN1 011 = IDAC1 is connected to AIN2 100 = IDAC1 is connected to AIN3/REFN1 101 = IDAC1 is connected to REFP0 110 = IDAC1 is connected to REFN0 111 = Reserved
D[4:2]	I2MUX[2:0]	000	R/W	IDAC2 Routing Configuration These bits determine the channel to which IDAC2 is routed. 000 = IDAC2 disabled (default) 001 = IDAC2 is connected to AIN0/REFP1 010 = IDAC2 is connected to AIN1 011 = IDAC2 is connected to AIN2 100 = IDAC2 is connected to AIN3/REFN1 101 = IDAC2 is connected to REFP0 110 = IDAC2 is connected to REFN0 111 = Reserved
D[1]	DRDYM	0	R/W	nDRDY Mode This specific bit governs the functionality of the DOUT/nDRDY pin when the fresh data is available. 0 = Only the dedicated nDRDY pin is utilized to indicate when data is ready (default) 1 = Indication of data readiness occurs simultaneously on both DOUT/nDRDY and nDRDY
D[0]	Reserved	0	R/W	Reserved. Always write 0.

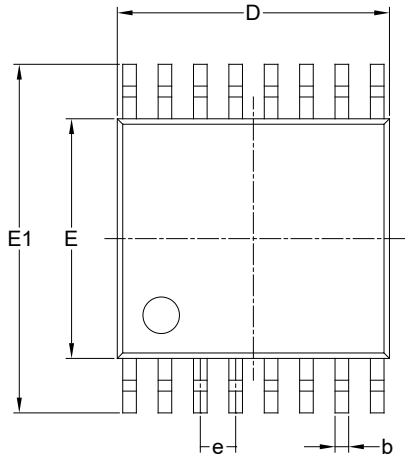
REVISION HISTORY

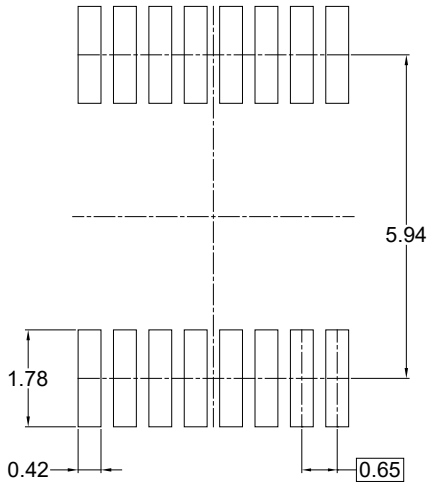
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (NOVEMBER 2024) to REV.A	Page
Changed from product preview to production data	All

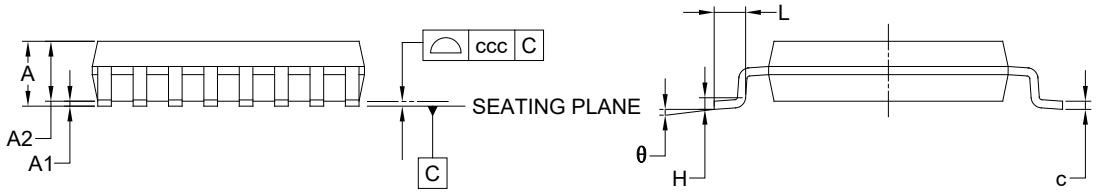
PACKAGE OUTLINE DIMENSIONS

TSSOP-16





RECOMMENDED LAND PATTERN (Unit: mm)

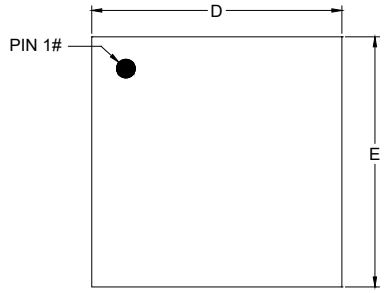


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

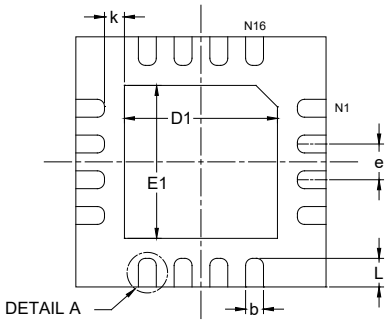
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

PACKAGE OUTLINE DIMENSIONS

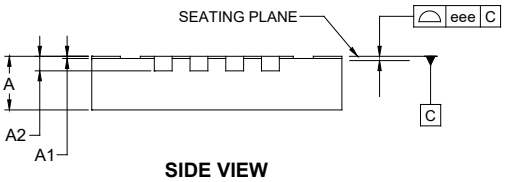
TQFN-3.5×3.5-16L



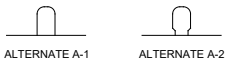
TOP VIEW



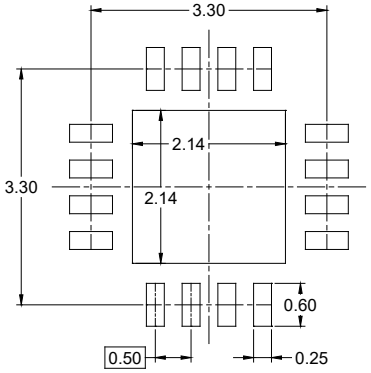
BOTTOM VIEW



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTION



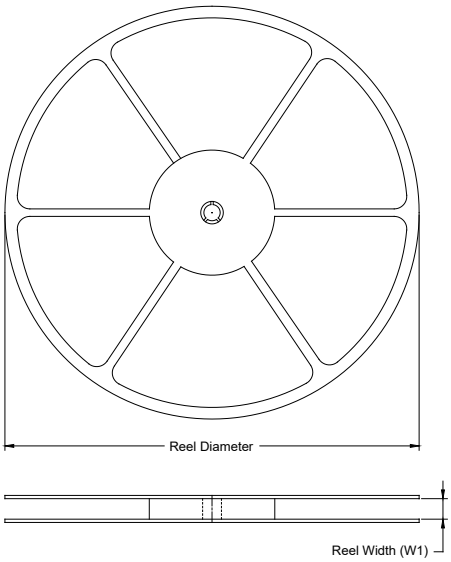
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.700	-	0.800
A1	0.000	-	0.050
A2		0.203 REF	
b	0.200	-	0.300
D	3.400	-	3.600
E	3.400	-	3.600
D1	2.040	-	2.240
E1	2.040	-	2.240
e		0.500 BSC	
k		0.280 REF	
L	0.300	-	0.500
eee		0.080	

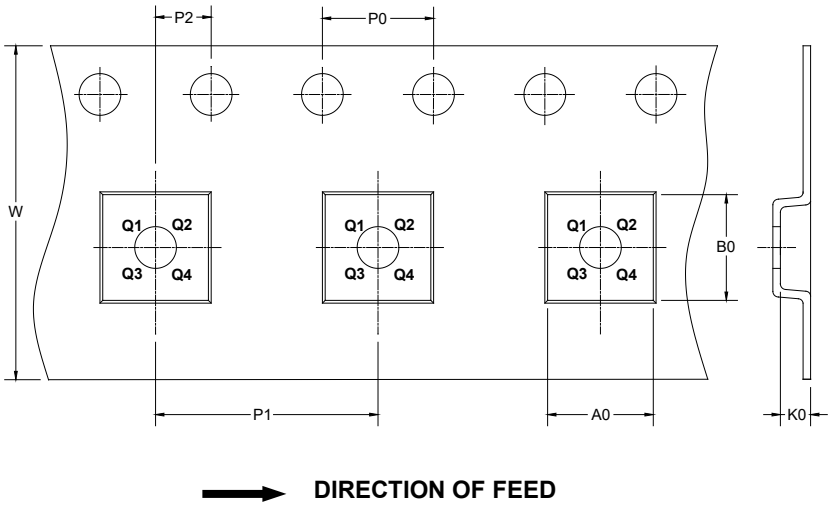
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



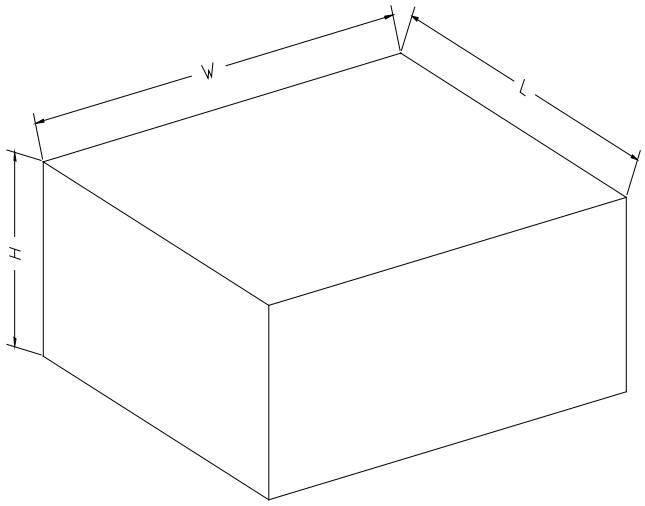
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-16	13″	12.4	6.80	5.40	1.50	4.0	8.0	2.0	12.0	Q1
TQFN-3.5×3.5-16L	13″	12.4	3.80	3.80	1.00	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002