74LVC74
Dual D-Type Positive Edge-Triggered Flip-Flop with Set and Reset

GENERAL DESCRIPTION

The 74LVC74 is a dual D-type flip-flop positive edge-triggered with set and reset. This device accepts a wide supply voltage range from 1.2V to 3.6V. nD are individual data inputs, nCP are clock inputs, $n\overline{SD}$ and $n\overline{RD}$ are set inputs, nQ and $n\overline{Q}$ are complementary outputs.

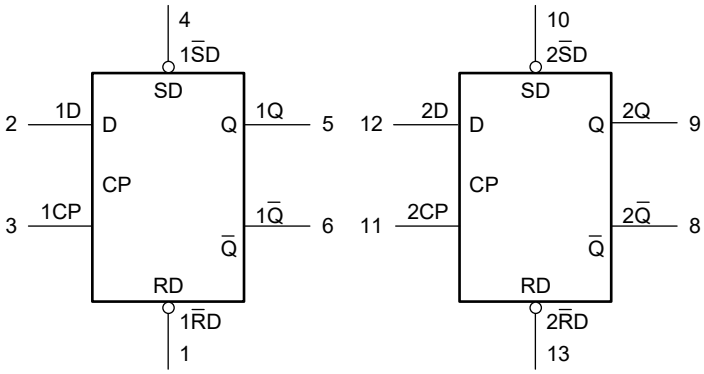
The set and reset are non-synchronous inputs (active low) and clock inputs can be operated independently. When clock pulse is in the transition of low-to-high, data at the nD inputs will be transmitted to the nQ outputs. For predictable outputs performance, prior set-up time must be required necessarily by nD inputs to the low-to-high clock transition.

Schmitt trigger action features the high tolerance of over-voltage for inputs/outputs data and control inputs and slower input rise and fall times. This device is suitable for down-translation in a mixed-voltage environment.

FEATURES

- **Wide Supply Voltage Range: 1.2V to 3.6V**
- **Inputs Accept Voltages up to 5V**
- **CMOS Low Power Consumption**
- **Direct Interface with TTL Levels**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in a Green TSSOP-14 Package**

LOGIC SYMBOL



FUNCTION TABLE

CONTROL INPUT			INPUT	OUTPUT	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$
L	H	*X*	*X*	H	L
H	L	*X*	*X*	L	H
L	L	*X*	*X*	H	H

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

CONTROL INPUT			INPUT	OUTPUT	
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ_{n+1}	$n\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

H = High Voltage Level

L = Low Voltage Level

↑ = Low-to-High Clock Transition

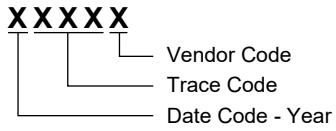
Q_{n+1} = State after the Next Low-to-High CP Transition

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74LVC74	TSSOP-14	-40℃ to +125℃	74LVC74XTS14G/TR	74LVC74 XTS14 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If yo ave additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage, V_{CC} ..... -0.5V to 6.5V
Input Voltage, V_I (2) ..... -0.5V to 6.5V
Output Voltage, V_O (2) .....-0.5V to V_{CC} + 0.5V
Input Clamping Current, I_{IK} (V_I < 0V).....-50mA
Output Clamping Current, I_{OK} (V_O > V_{CC} or V_O < 0V)
.....±50mA
Output Current, I_O (V_O = 0V to V_{CC}) .....±50mA
Supply Current, I_{CC} 100mA
Ground Current, I_{GND}.....-100mA
Junction Temperature (3) .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD Susceptibility
HBM.....6000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} .....1.65V to 3.6V
Data Retention Only, V_{CC}.....1.2V to 3.6V
Input Voltage, V_I.....0V to 5.5V
Output Voltage, V_O..... 0V to V_{CC}
Input Transition Rise and Fall Rate, Δt/ΔV
V_{CC} = 1.65V to 2.7V ..... 20ns/V (MAX)
V_{CC} = 2.7V to 3.6V ..... 10ns/V (MAX)
Operating Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

ESD SENSITIVITY CAUTION

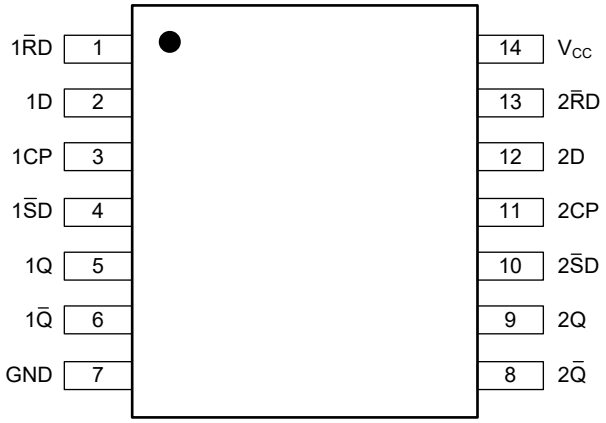
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



TSSOP-14

PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 13	1$\overline{R}$D, 2$\overline{R}$D	Non-synchronous Reset-Direct Inputs (Active Low).
2, 12	1D, 2D	Data Inputs.
3, 11	1CP, 2CP	Clock Inputs (Low-to-High, Edge-Triggered).
4, 10	1$\overline{S}$D, 2$\overline{S}$D	Non-synchronous Set-Direct Inputs (Active Low).
5, 9	1Q, 2Q	True Outputs.
6, 8	1$\overline{Q}$, 2$\overline{Q}$	Complement Outputs.
7	GND	Ground.
14	V_{CC}	Power Supply.

ELECTRICAL CHARACTERISTICS

(Full = -40℃ to +125℃, all typical values are measured at V_{CC} = 3.3V and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V_{IH}	V_{CC} = 1.2V		Full	1.2			V
		V_{CC} = 2.7V to 3.6V		Full	2			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.2V		Full			0.1	V
		V_{CC} = 2.7V to 3.6V		Full			0.8	
High-Level Output Voltage	V_{OH}	V_I = V_{IH} or V_{IL}	V_{CC} = 2.7V to 3.6V, I_O = -100μA	Full	V_{CC} - 0.05	V_{CC} - 0.005		V
			V_{CC} = 2.7V, I_O = -12mA	Full	2.35	2.57		
			V_{CC} = 3.0V, I_O = -18mA	Full	2.55	2.82		
			V_{CC} = 3.0V, I_O = -24mA	Full	2.45	2.75		
Low-Level Output Voltage	V_{OL}	V_I = V_{IH} or V_{IL}	V_{CC} = 2.7V to 3.6V, I_O = 100μA	Full		0.005	0.05	V
			V_{CC} = 2.7V, I_O = 12mA	Full		0.12	0.30	
			V_{CC} = 3.0V, I_O = 24mA	Full		0.23	0.55	
Input Leakage Current	I_I	V_{CC} = 3.6V, V_I = 5.5V or GND		Full		±0.05	±10	μA
Supply Current	I_{CC}	V_{CC} = 3.6V, V_I = V_{CC} or GND, I_O = 0A		Full		0.05	20	μA
Additional Supply Current	ΔI_{CC}	Per input pin, V_{CC} = 2.7V to 3.6V, V_I = V_{CC} - 0.6V, I_O = 0A		Full		0.1	4000	μA
Input Capacitance	C_I	V_{CC} = 0V to 3.6V, V_I = GND to V_{CC}		+25℃		6		pF

DYNAMIC CHARACTERISTICS

(For test circuit, see Figure 1. All typical values are measured at T_A = +25℃. For V_{CC} = 3.0V to 3.6V range, typical values are measured at 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Propagation Delay (1)	t_{PD}	nCP to nQ, n$\overline{Q}$, see Figure 2	V_{CC} = 1.2V	+25℃		15		ns
			V_{CC} = 2.7V	+25℃		5		
			V_{CC} = 3.0V to 3.6V	+25℃		4		
		n$\overline{S}$D to nQ, n$\overline{Q}$, see Figure 3	V_{CC} = 1.2V	+25℃		16		
			V_{CC} = 2.7V	+25℃		4		
			V_{CC} = 3.0V to 3.6V	+25℃		3.5		
		n$\overline{R}$D to nQ, n$\overline{Q}$, see Figure 3	V_{CC} = 1.2V	+25℃		17		
			V_{CC} = 2.7V	+25℃		4		
			V_{CC} = 3.0V to 3.6V	+25℃		3.5		
Pulse Width	t_W	Clock high or low, see Figure 2	V_{CC} = 2.7V	+25℃	5			ns
			V_{CC} = 3.0V to 3.6V	+25℃		2.5		
		Set or reset low, see Figure 3	V_{CC} = 2.7V	+25℃	5			
			V_{CC} = 3.0V to 3.6V	+25℃		2.5		
Recovery Time	t_{REC}	Set or reset, see Figure 3	V_{CC} = 2.7V	+25℃	2.5			ns
			V_{CC} = 3.0V to 3.6V	+25℃	2			
Set-Up Time	t_{SU}	nD to nCP, see Figure 2	V_{CC} = 2.7V	+25℃	3			ns
			V_{CC} = 3.0V to 3.6V	+25℃	2.5			
Hold Time	t_H	nD to nCP, see Figure 2	V_{CC} = 2.7V	+25℃	2			ns
			V_{CC} = 3.0V to 3.6V	+25℃	2			
Maximum Frequency	f_{MAX}	nCP, see Figure 2	V_{CC} = 2.7V	+25℃		170		MHz
			V_{CC} = 3.0V to 3.6V	+25℃		250		
Output Skew Time	$t_{SK(O)}$	V_{CC} = 3.0V to 3.6V		+25℃		0.5		ns
Power Dissipation Capacitance (2)	C_{PD}	Per flip-flop, V_I = GND to V_{CC}, V_{CC} = 3.0V to 3.6V		+25℃		15		pF

NOTES:

1. t_{PD} is the same as t_{PLH} and t_{PHL}.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$

   where:

   f_i = input frequency in MHz.

   f_o = output frequency in MHz.

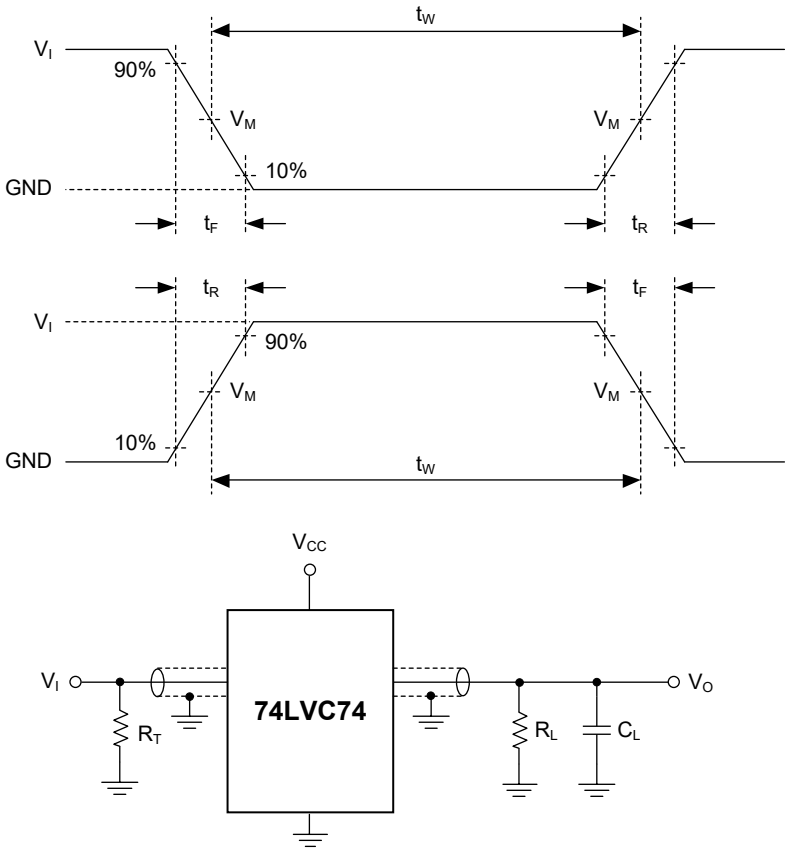
   C_L = output load capacitance in pF.

   V_{CC} = supply voltage in Volts.

   N = number of inputs switching.

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L: Load resistance.

C_L: Load capacitance (including jig and probe).

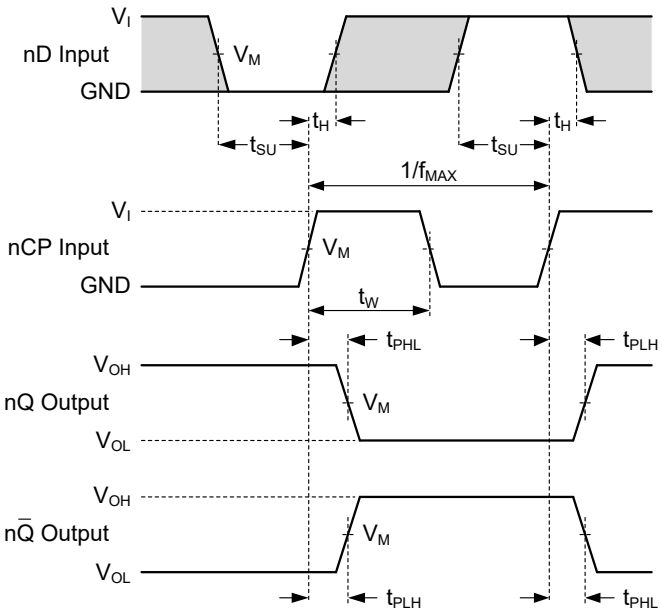
R_T: Termination resistance (equal to output impedance Z_O of the pulse generator).

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD	
V_{CC}	V_I	t_R, t_F	C_L	R_L
2.7V	2.7V	≤ 2.5ns	50pF	500Ω
3.0V to 3.6V	2.7V	≤ 2.5ns	50pF	500Ω

WAVEFORMS



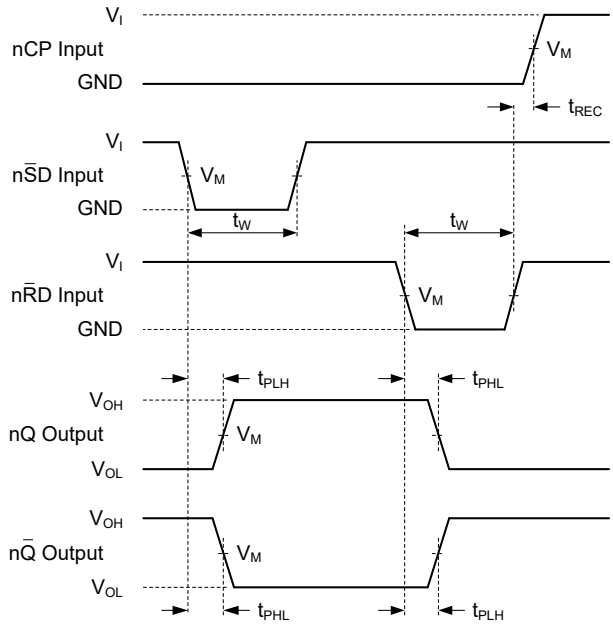
Test conditions are given in Table 1.

Test conditions are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 2. The Clock Input (nCP) to Output (nQ, nQ̄) Propagation Delays, the Clock Pulse Width, the nD to nCP Set-Up, the nCP to nD Hold Times, and the Maximum Frequency



Test conditions are given in Table 1.

Test conditions are given in Table 2.

Logic levels: V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 3. The Set (nS̄D) and Reset (nR̄D) Input to Output (nQ, nQ̄) Propagation Delays, the Set and Reset Pulse Widths, and the nR̄D to nCP Recovery Time

WAVEFORMS (continued)

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	V_M (1)	V_M
V_{CC} ≥ 2.7V	1.5V	1.5V
V_{CC} < 2.7V	0.5 × V_{CC}	0.5 × V_{CC}

NOTE:
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 2.5ns.

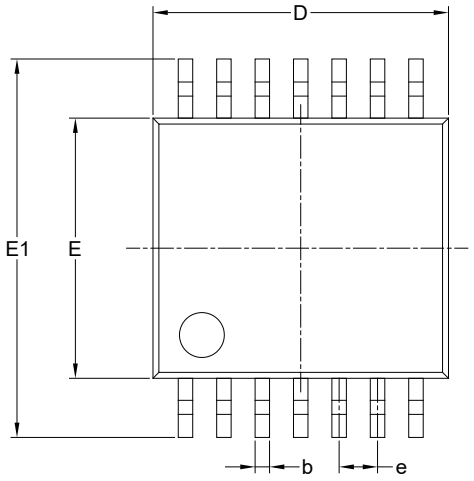
REVISION HISTORY

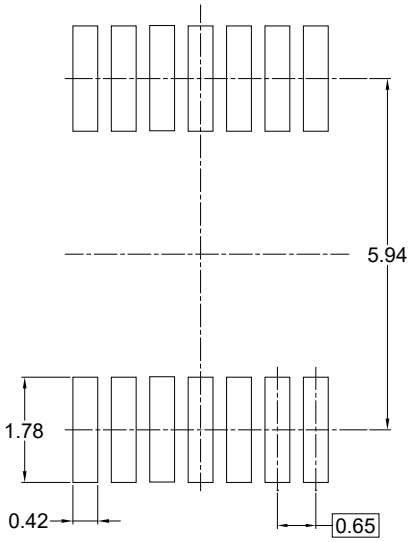
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (APRIL 2021) to REV.A	Page
Changed from product preview to production data	All

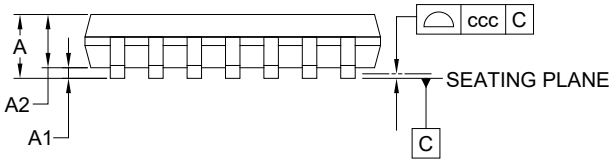
PACKAGE OUTLINE DIMENSIONS

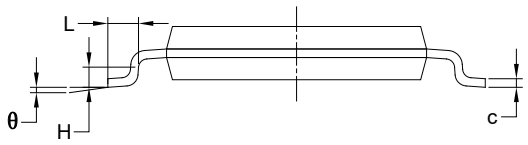
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)



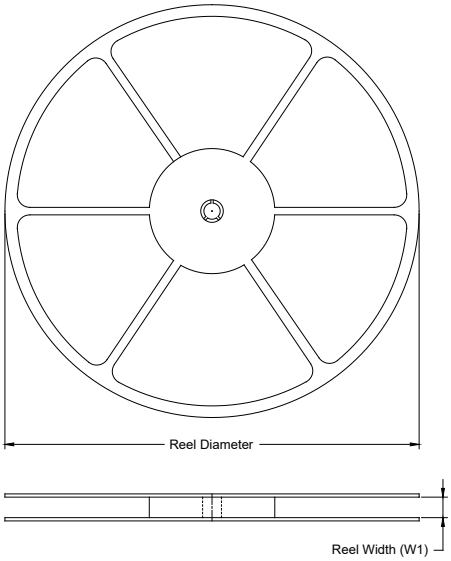


Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

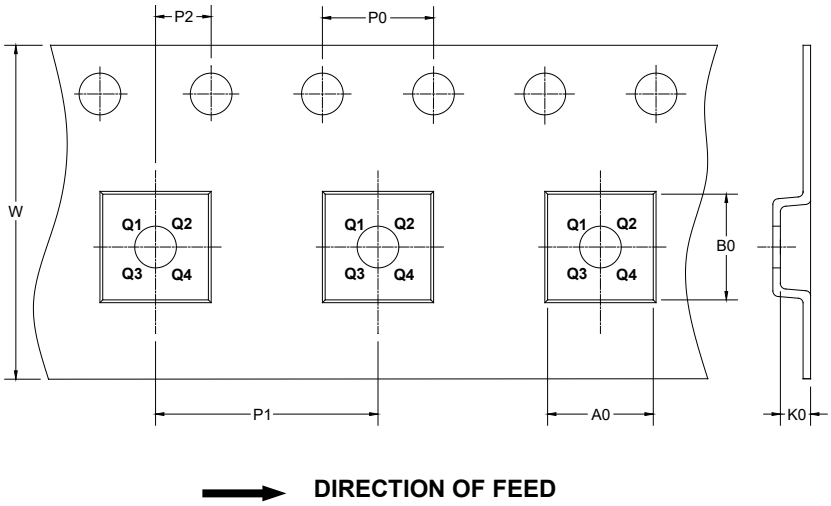
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

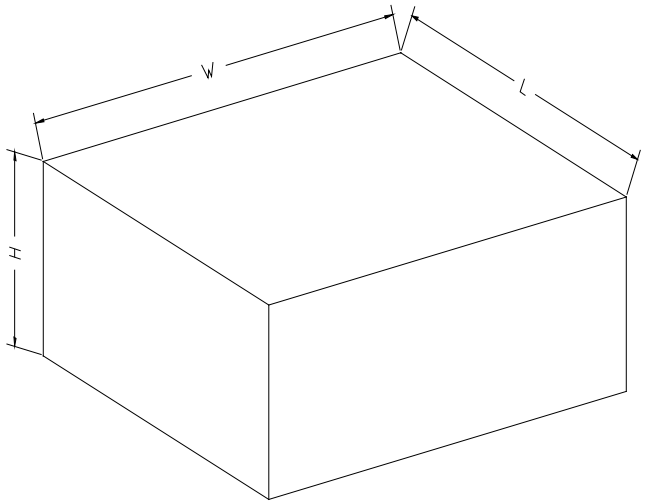
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002